中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

上海科技大学
ShanghaiTech University

Prototype Characterization of a Charge-integrating Pixel Detector Readout Chip with In-pixel A/D Conversion

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Outline

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- The Chip Design
  - The Pixel Architecture
  - Calibration Block
  - In-Pixel ADC
- Measurement results
  - Analog Outputs
  - Dynamic range
  - Gain and noise
  - Non-Linearity
- Conclusion

SHINE

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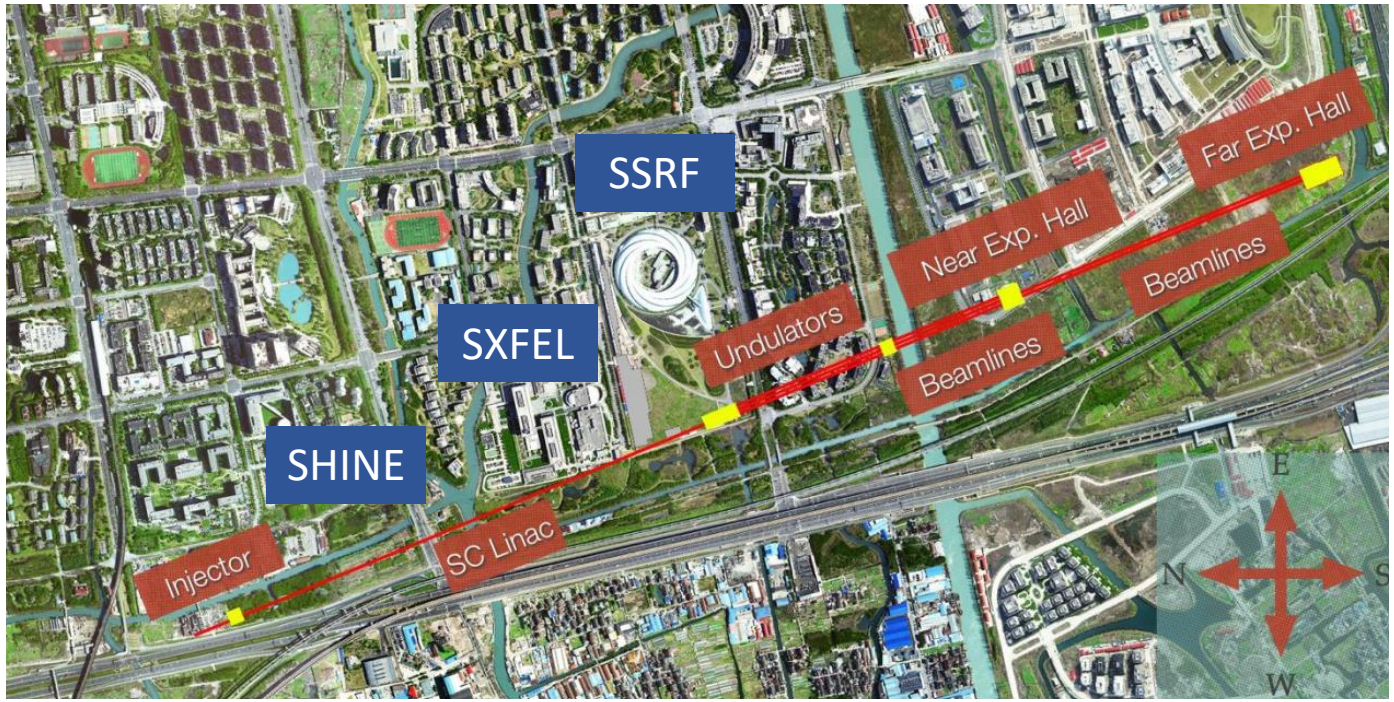
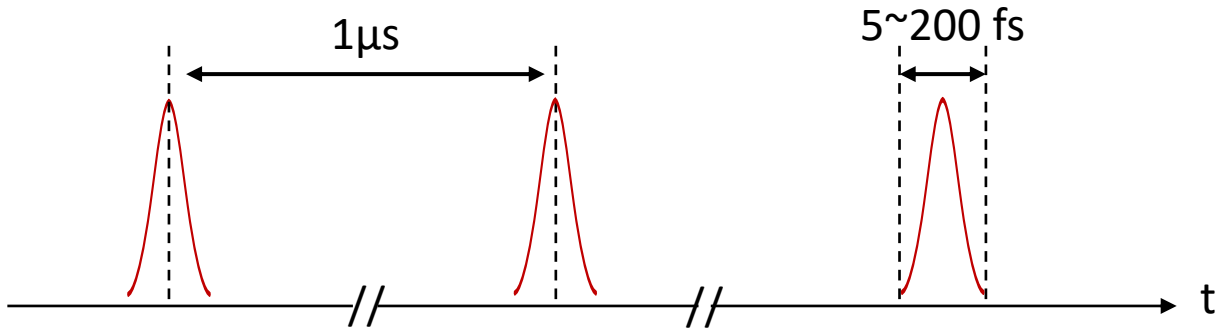
Shanghai **HI**gh repetition rate
XFEL a**N**d **E**xtreme light facility

- 3 FEL beamlines: FEL-I, FEL-II, FEL-III
- Photon Energy: 0.4~25 keV
  - FEL-I: 3~15 keV
  - FEL-II: 0.4~3 keV
  - FEL-III: 10~25 keV
- Pulse Duration: 20~50 fs (5~200 fs)
- Repetition Frequency: 10kHz (1MHz)
- Peak Brightness: 10^{32} ~10^{33} photons/μm²/rad²/s/0.1%BW

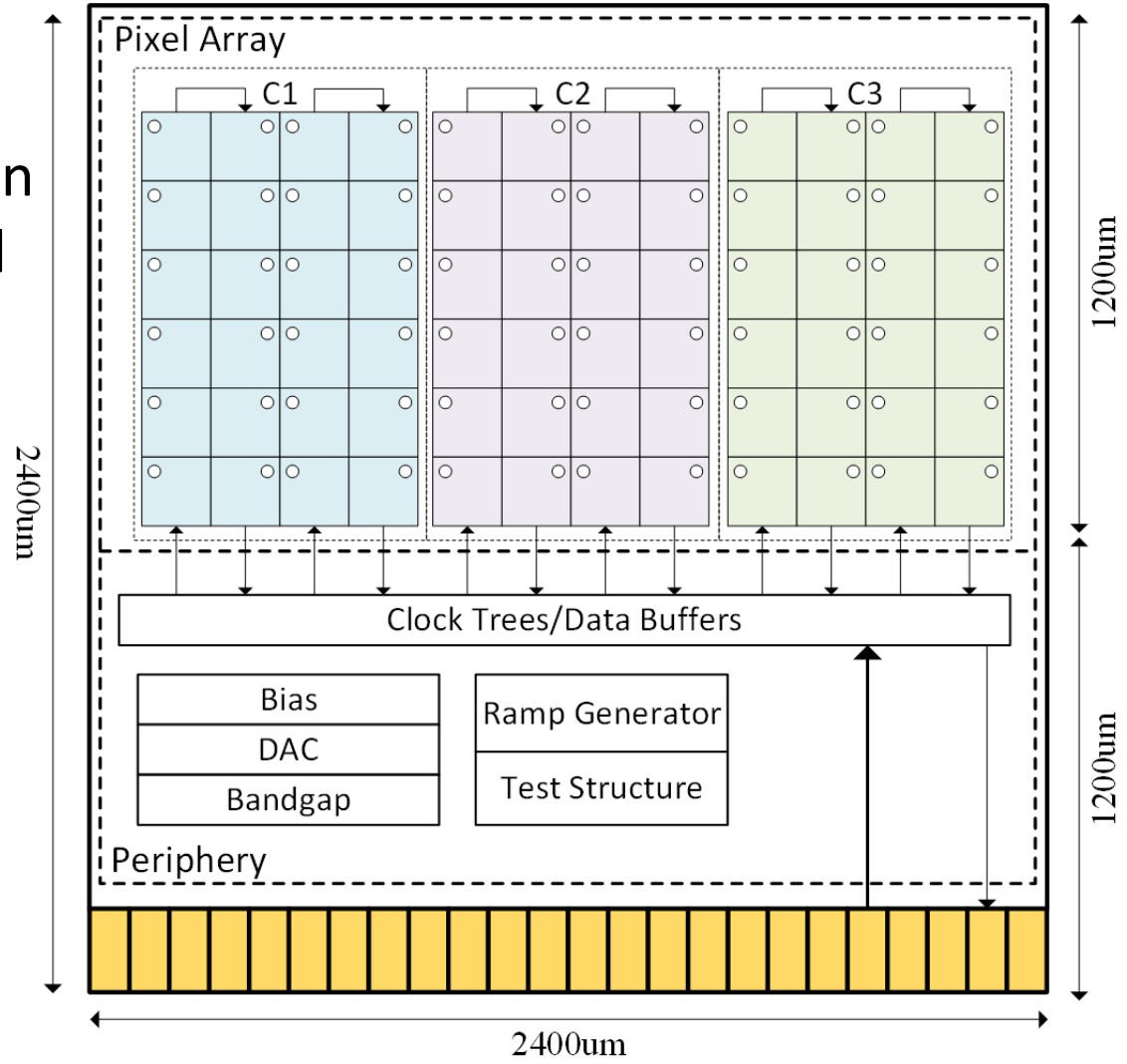




HYLITE

HYLITE (High dYmamic range free electron Laser Imaging deTEctor) is a charge-integration pixel detector readout chip, which is designed for SHINE and other advanced light sources.

- Technology: 130 nm 1P8M CMOS
- Pixel Pitch: 200 μm (100 μm)
- Frame Rate: 10 kHz (continuously read out)
- Dynamic Range: 1~10000 photons @12 keV
- HYLITE 0.1: the first verification chip
  - Chip Size: 2400 μm * 2400 μm
  - Array Size: 6*12



Pixel Architecture of HYLITE

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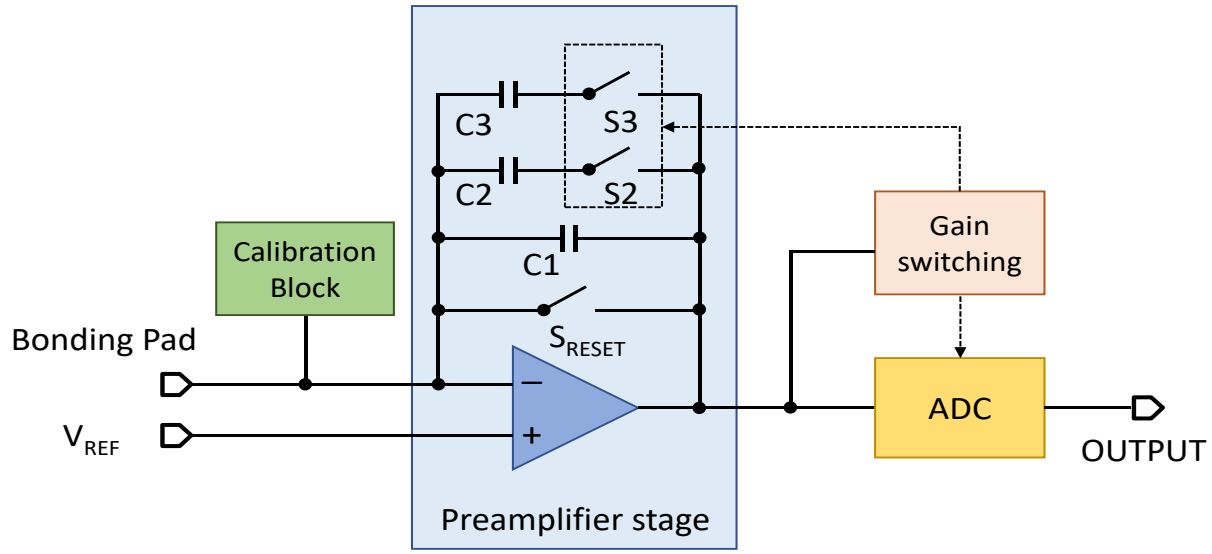

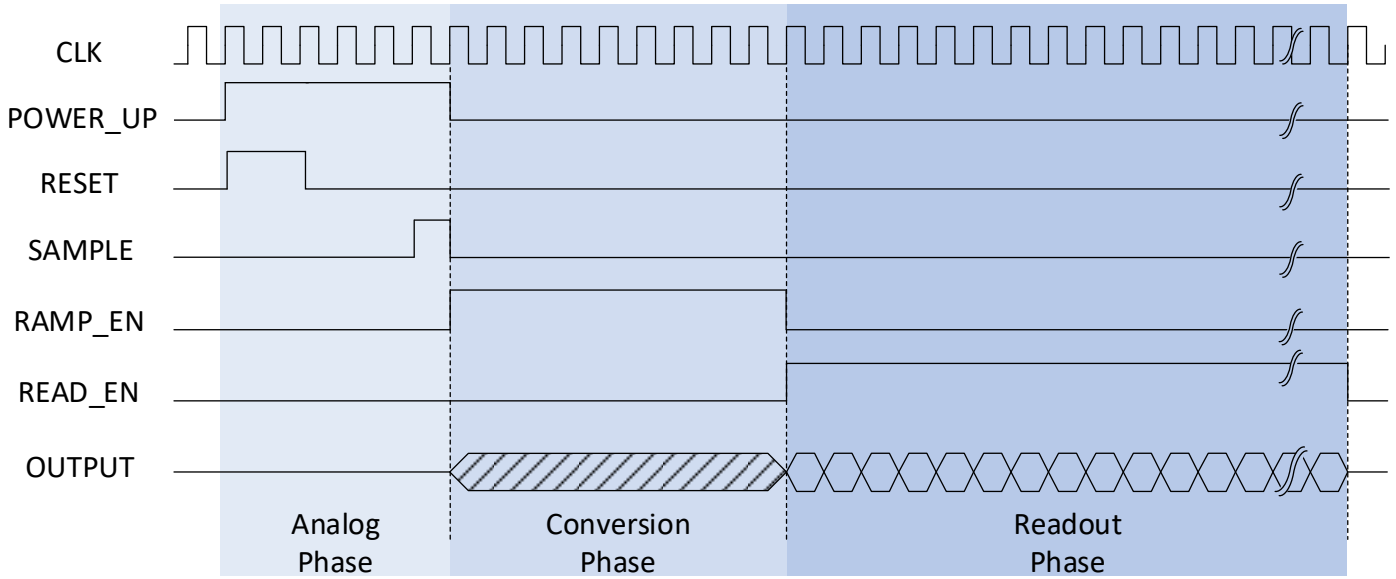

- Three Gains
  - Auto Gain Switching
- Three Working Phases
  - Analog Phase (less than 1 µs)
  - Conversion Phase (20 µs)
  - Readout Phase (~70 µs in full size chip)
- Three Schemes of capacitors
  - MIM
  - MIM with bias
  - MOS capacitors(*)
- Total Power: 34 µW/pixel

Calibration Block

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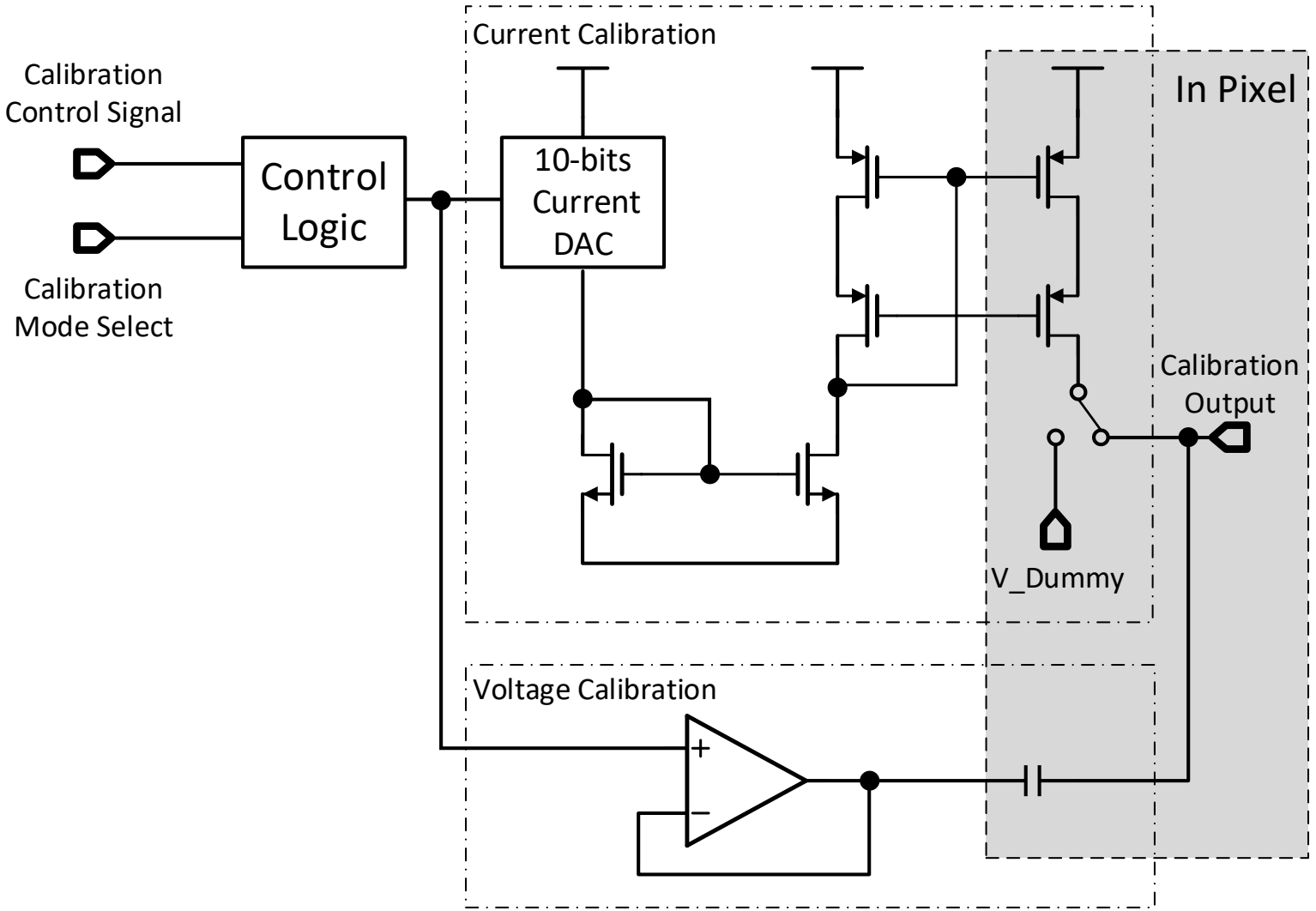
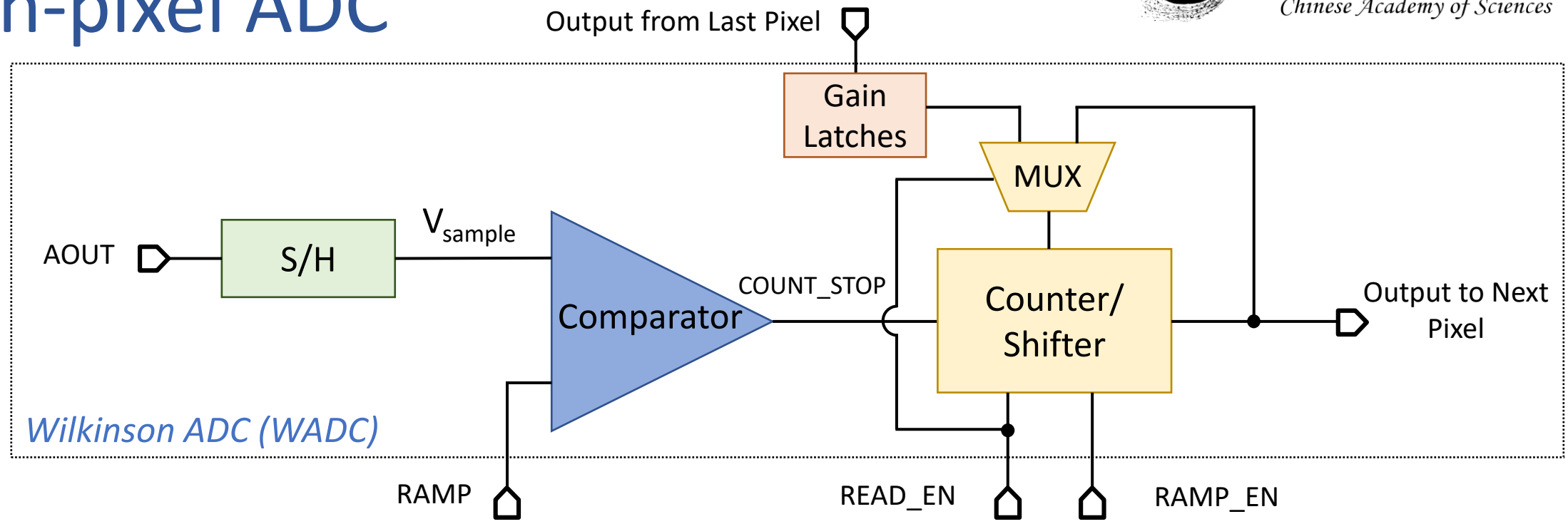


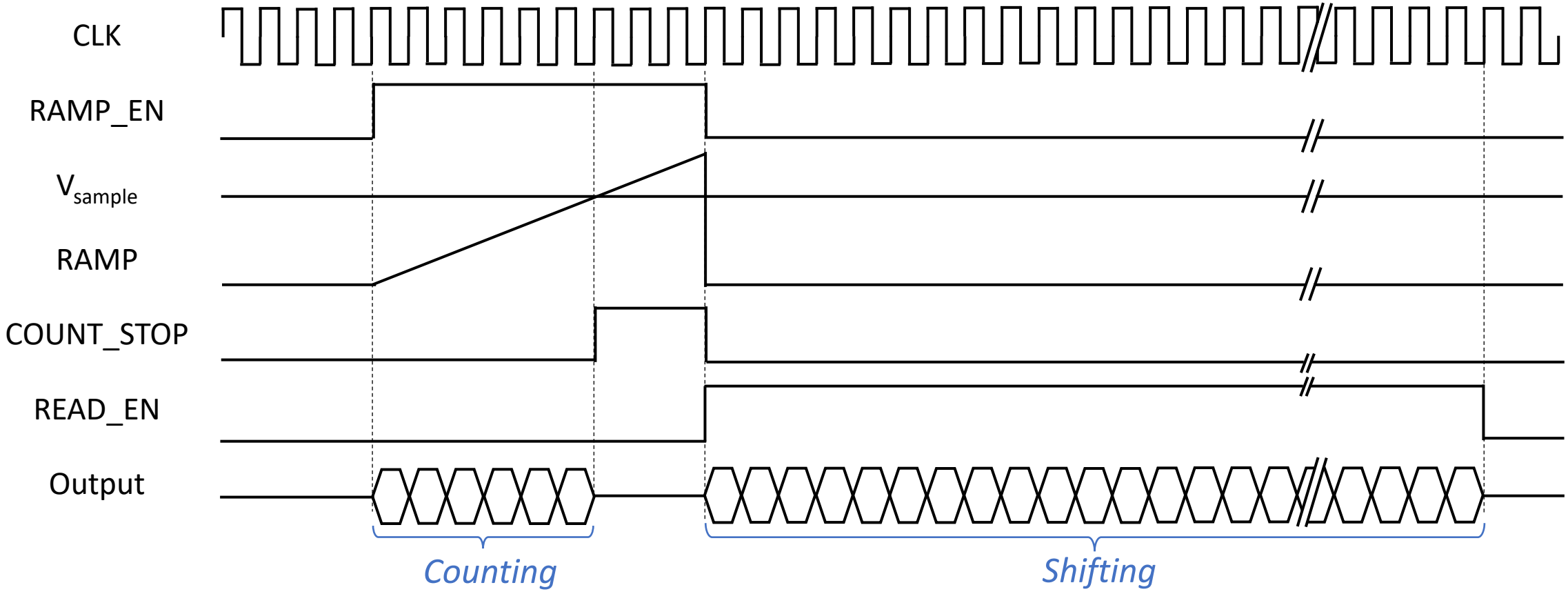
- Covers Full Dynamic Range of 10000 photons @12 keV
- Voltage Mode
  - High Linearity
  - Small Input Range
  - 8 mV amplitude voltage pulse -> a 12 keV Photon (“equivalent photons” by calculating input charges)
- Current Mode
  - Large Input Range
  - Worse Linearity
  - DAC Code=1, 150 ns width digital pulse -> 10 12 keV Photons

In-pixel ADC

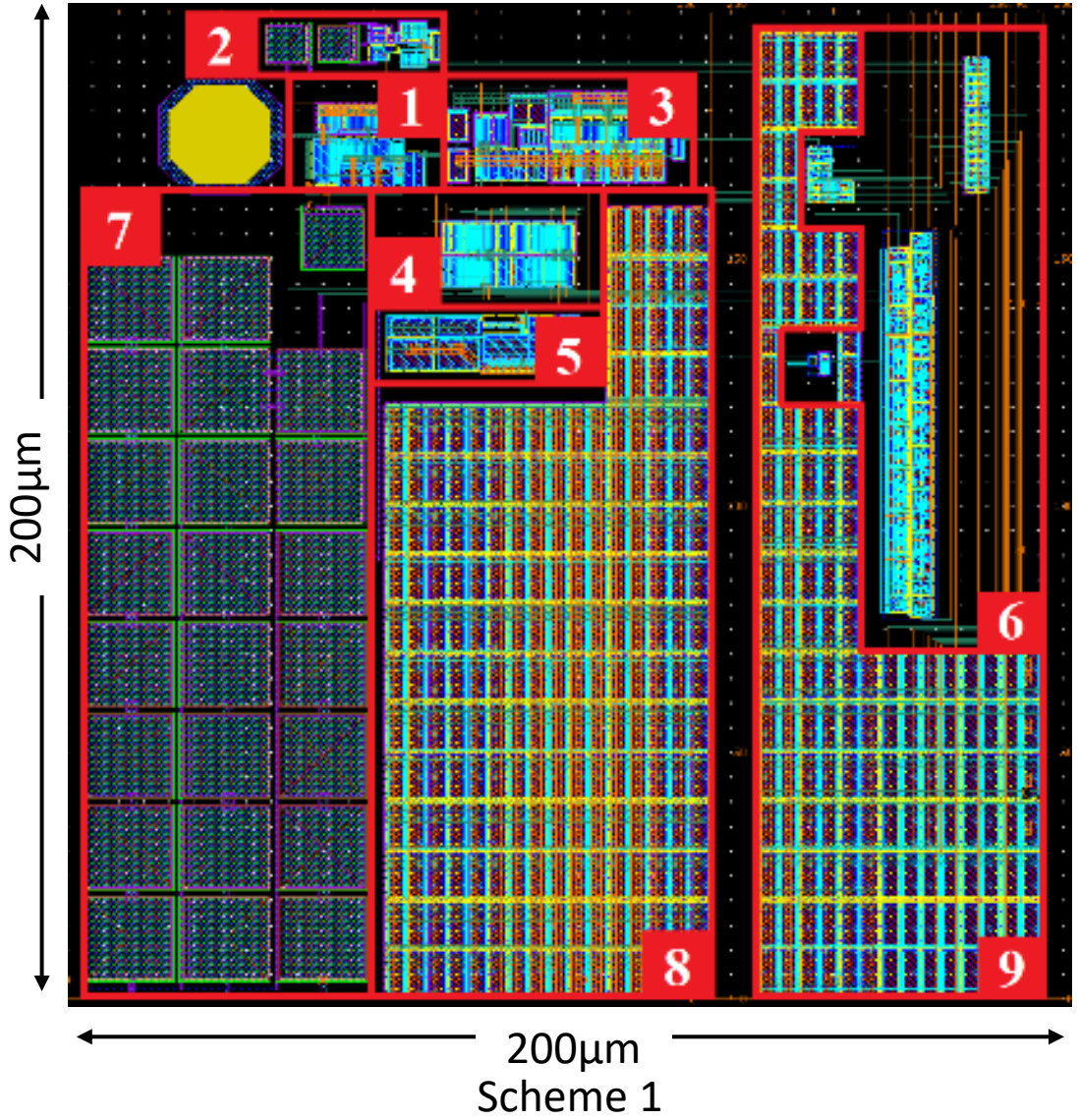


- S/H: Sample and Hold Circuit
- Comparator: Generates the stop signal of counting
- Counter/Shifter: Based on a 10-bit Linear Feedback Shift Register (LFSR), working frequency: 50 MHz
- MUX: Switches modes between counting and shifting
- Gain Latches: 2-bits registers latches gain, located in gain-switching circuits
- Power Consumption: 7.5 µW

Timing of WADC

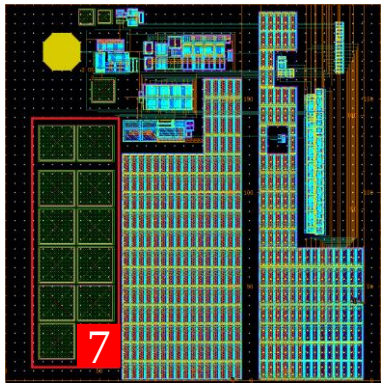


HYLITE 0.1 Layout

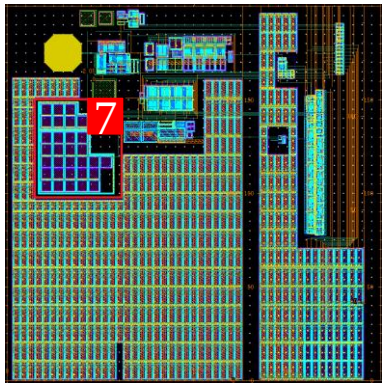


Scheme 1

- 1: Preamplifier
- 2: Calibration Block
- 3: Gain Switching Circuits
- 4: Switches
- 5: Comparator of WADC
- 6: Digital Logic
- 7: Integrating Capacitors
- 8: Decoupling Capacitors of Analog Power
- 9: Decoupling Capacitors of Digital Power

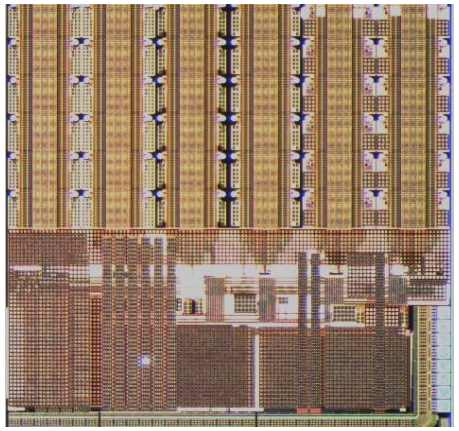


Scheme 2



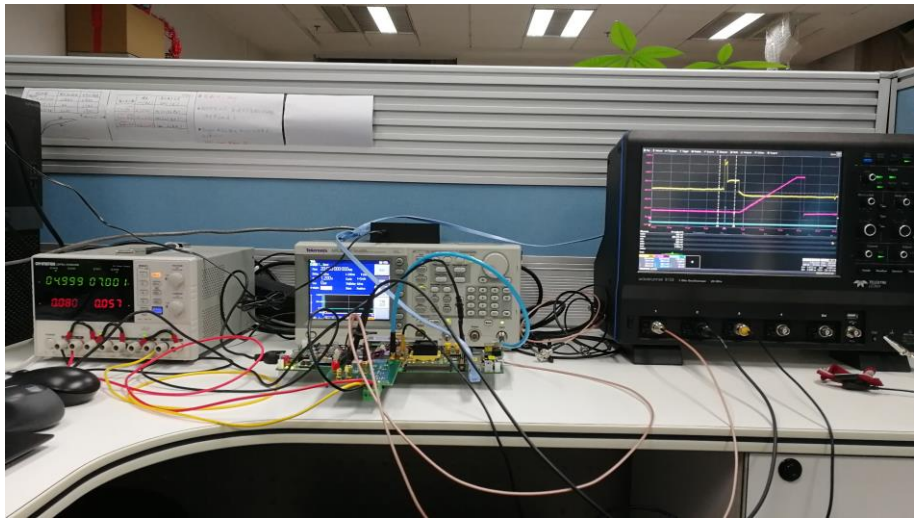
Scheme 3

Measurement System

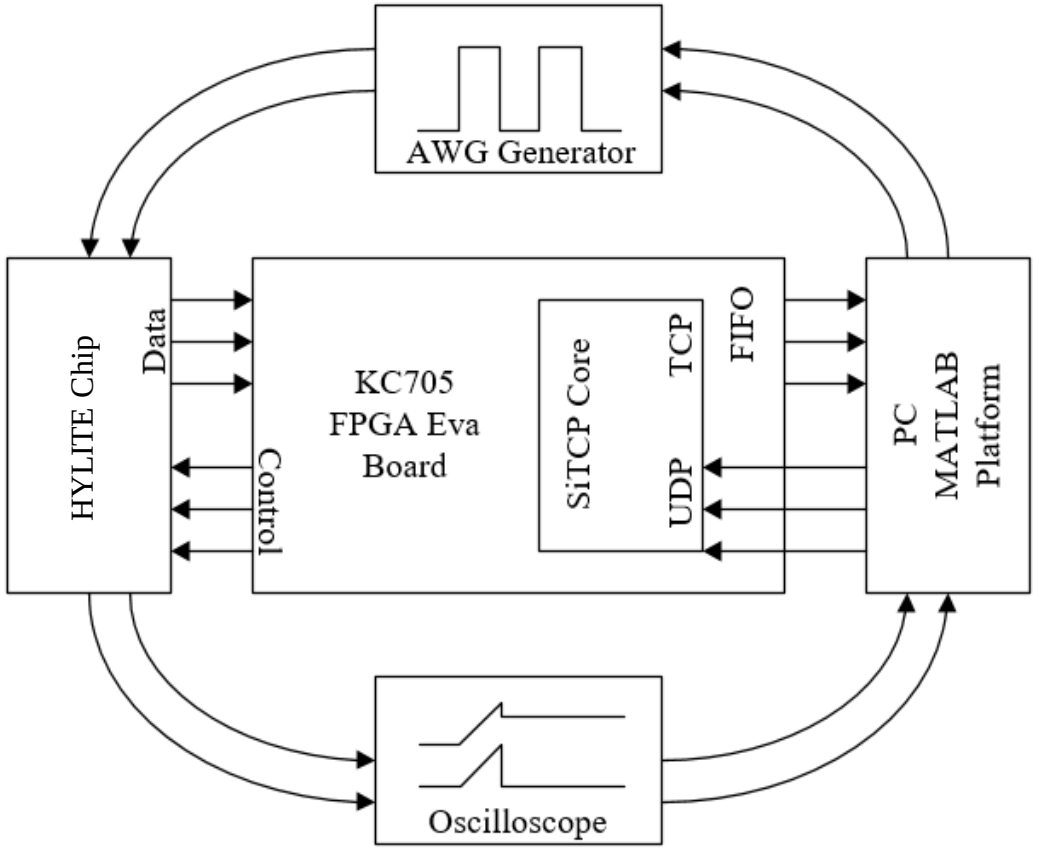


HYLITE0.1 Die

Chip Test PCB

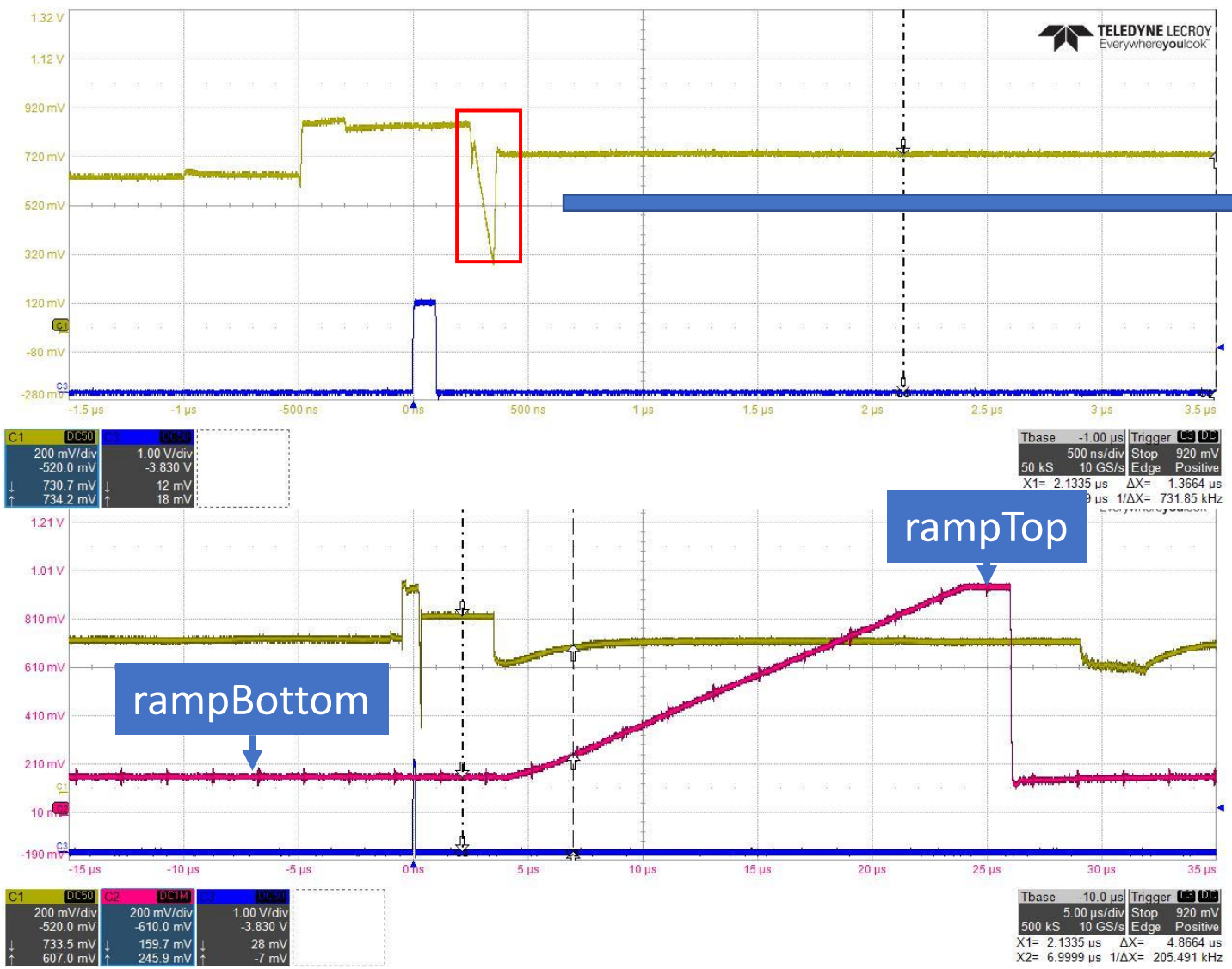


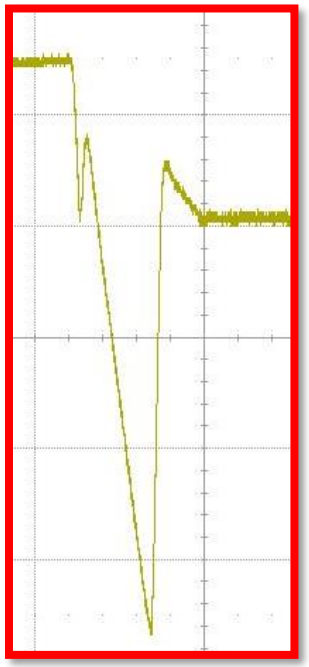
Measurement Environment



Block Diagram of Measurement System

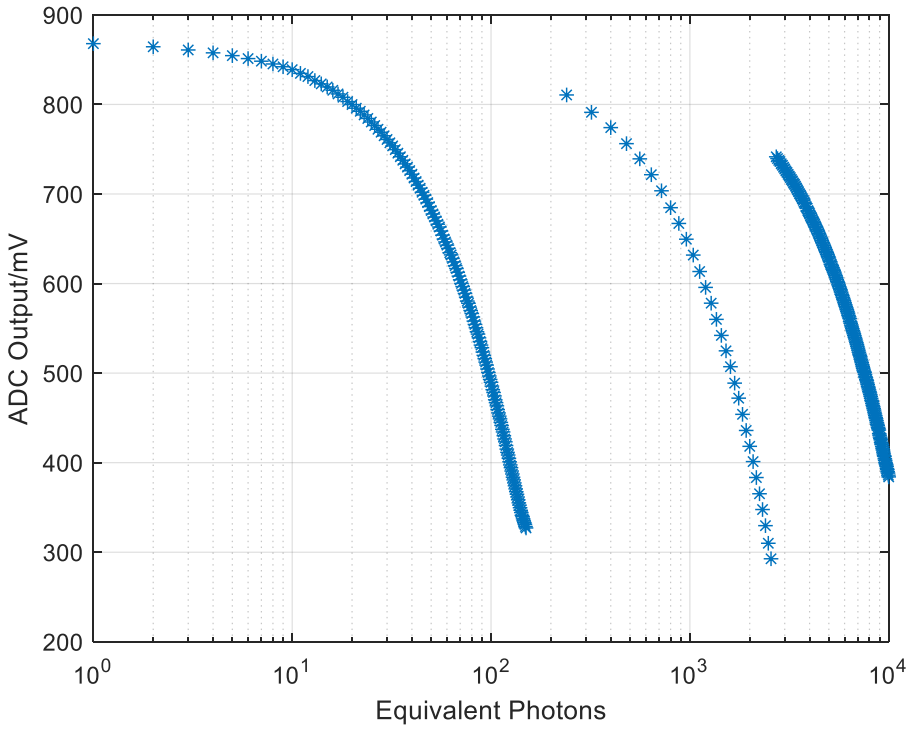
Analog Output

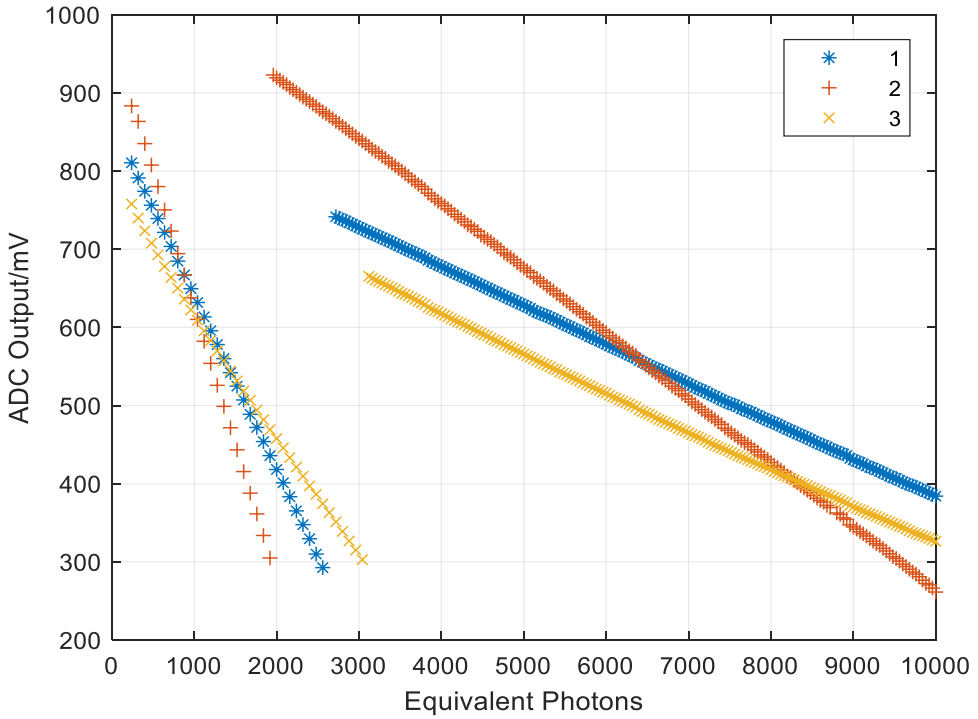




- Gain-switching is correct.
- Ramp Generator in the chip works well.
- mVolts=ADU*(rampTop-rampBottom)/1000+rampBottom

Dynamic Range

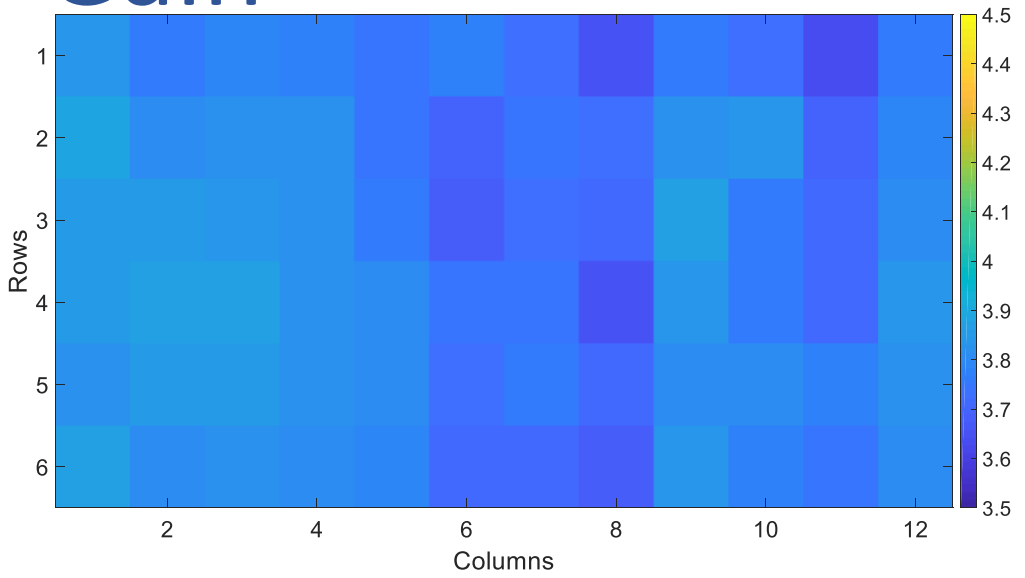




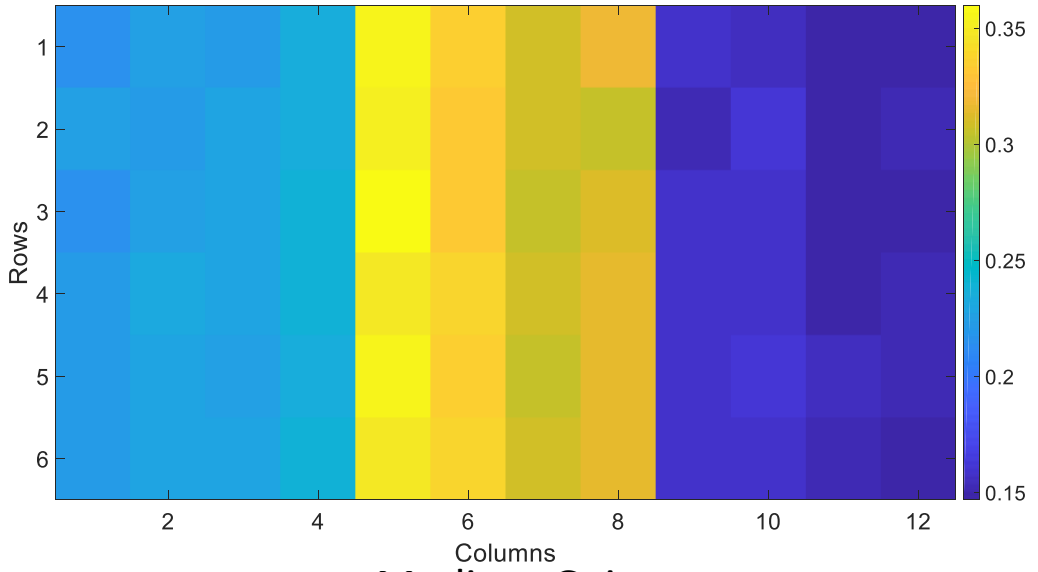
- A dynamic range of 10^4 photons is achieved.
- Different capacitor schemes have different performances.

Scheme	High Gain /12keV photons	Med Gain /12keV photons	Low Gain /12keV photons
1	1~160	160~2600	2600~10000
2		160~2000	2000~10000
3		160~3100	3100~10000

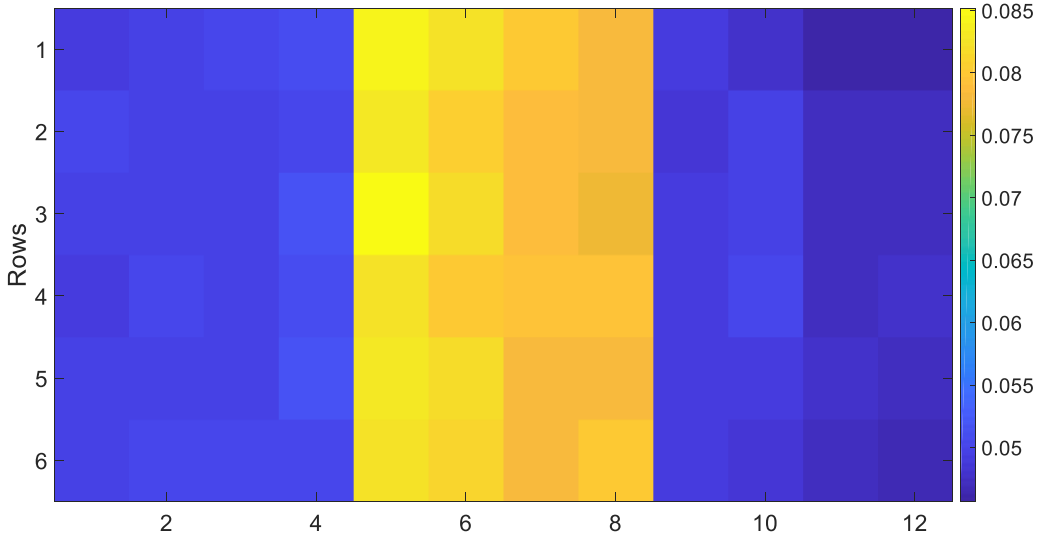
Gain



High Gain



Medium Gain

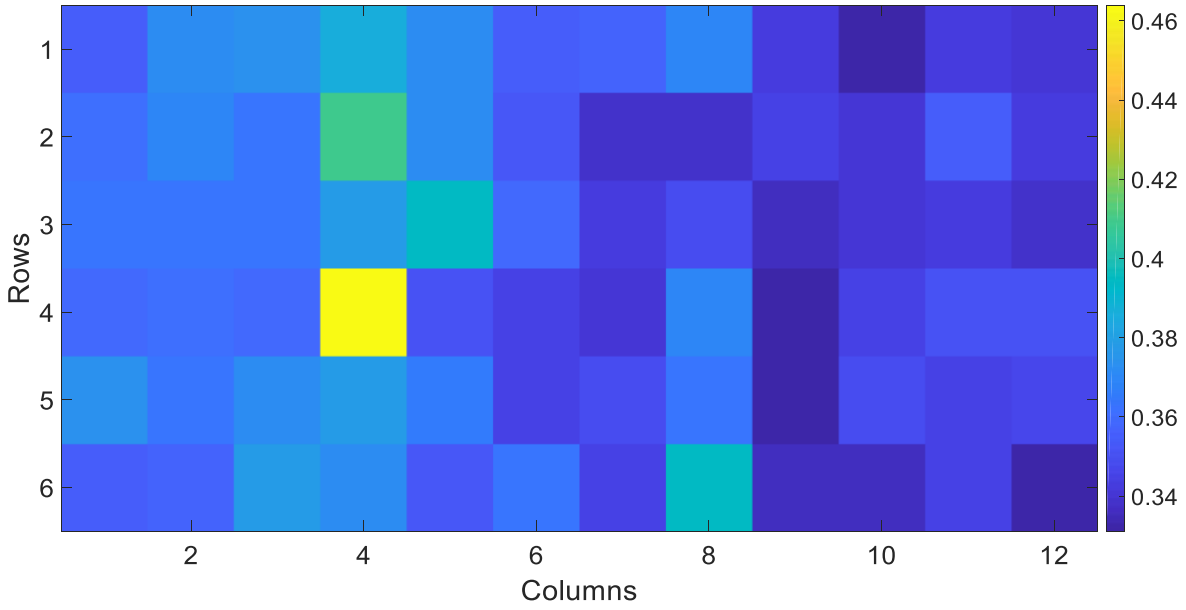


Low Gain

Scheme	High Gain /(mV/Photon)	Med Gain /(mV/Photon)	Low Gain /(mV/Photon)
1	3.82	0.23	0.050
2	3.71	0.31	0.079
3	3.76	0.15	0.047

- High Gain: G_{MIN}/G_{MAX}=93.6%

Noise



Scheme	High Gain /12keV γs	Med Gain /12keV γs	Low Gain /12keV γs
1	0.38	5.1 (12.6)	12.7 (60.0)
2	0.35	2.8 (12.6)	9.3 (44.7)
3	0.34	4.8 (12.6)	12.6 (55.7)

- The equivalent input noise is calculated on the number of 12keV photons.
- The noise performance in high gain mode can be improved further by increasing gain.
- Noise in medium and low gain mode is much lower than the minimum Poisson fluctuation in corresponding range.

Non-Linearity

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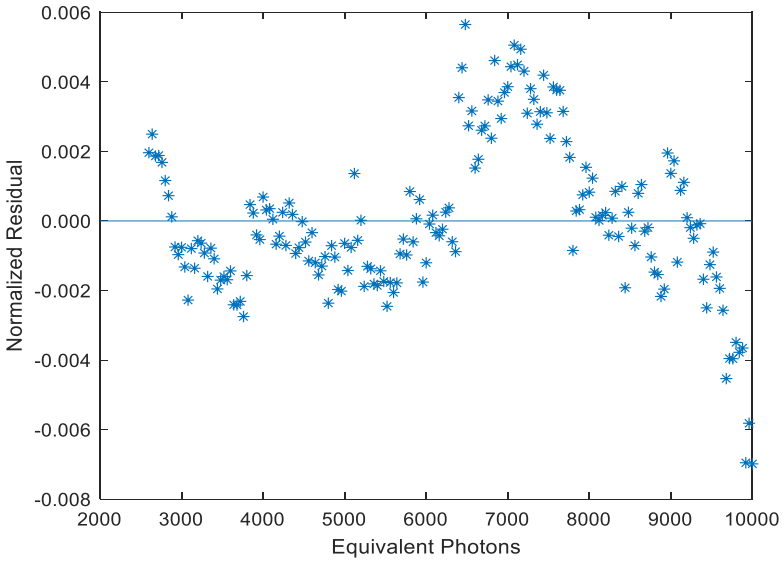

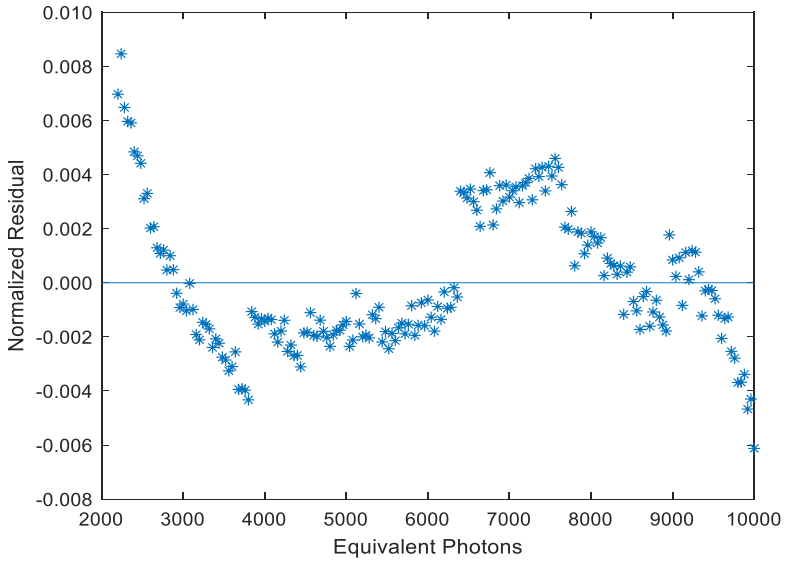

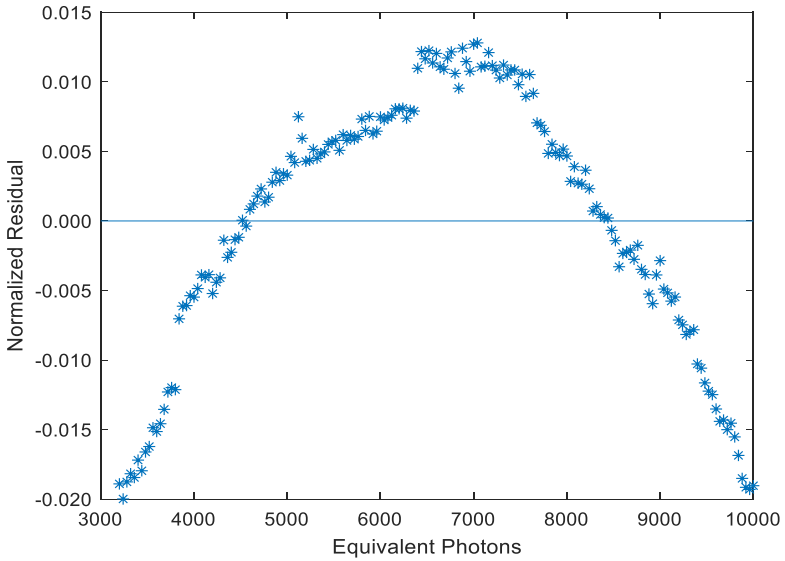

Scheme	High Gain	Med Gain	Low Gain
1	0.75%	0.21%	0.70%
2		0.35%	0.84%
3		4.0%	1.9%

- Non-Linearity of scheme 1&2 is less than 1%.
- Performance of scheme 3 in med gain is relatively high.

Conclusion

- Measurement results show that the pixel works correctly.
- The In-pixel ADC scheme is proved.
- Noise performance could be improved further.
- In our next tape out, HYLITE 0.2, a pixel pitch of 100μm was achieved. It is under testing.

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