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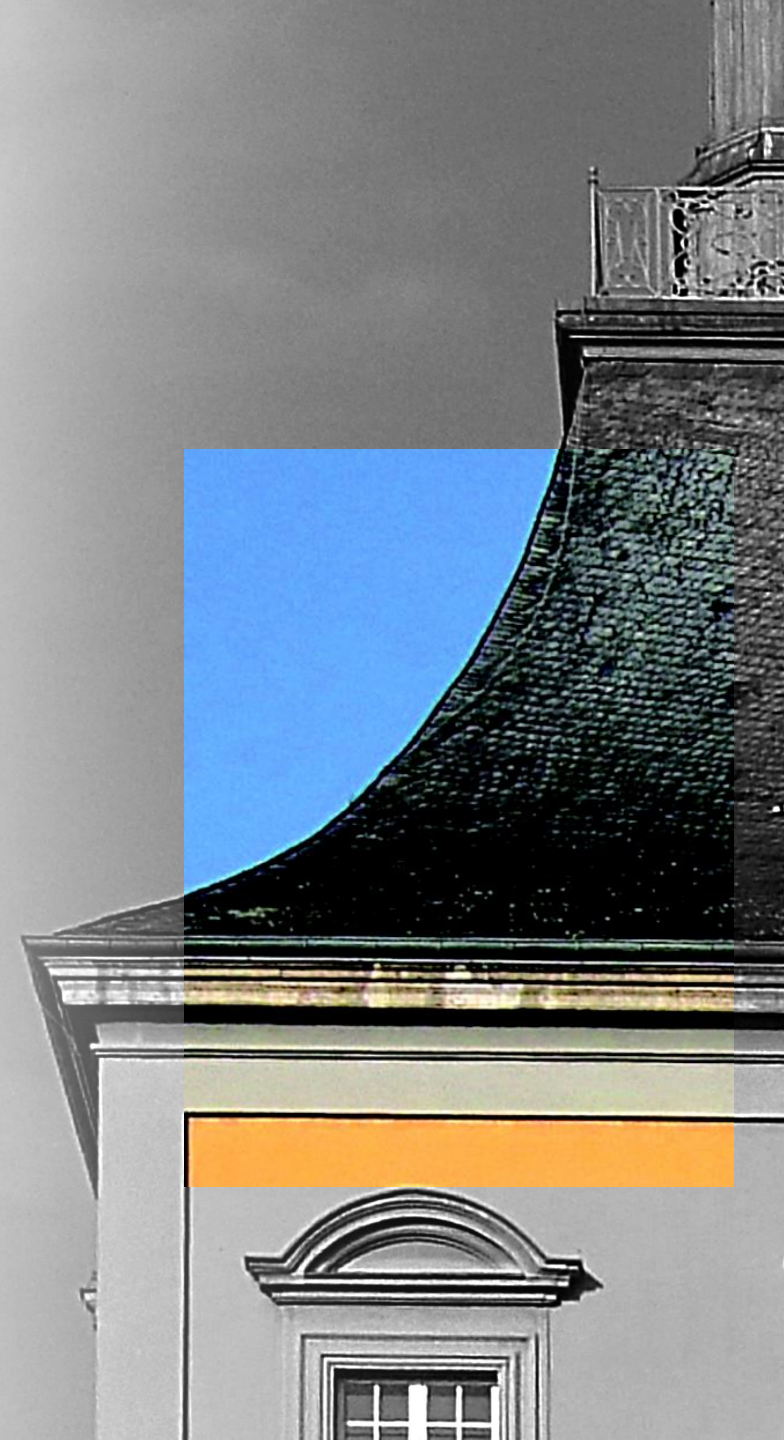
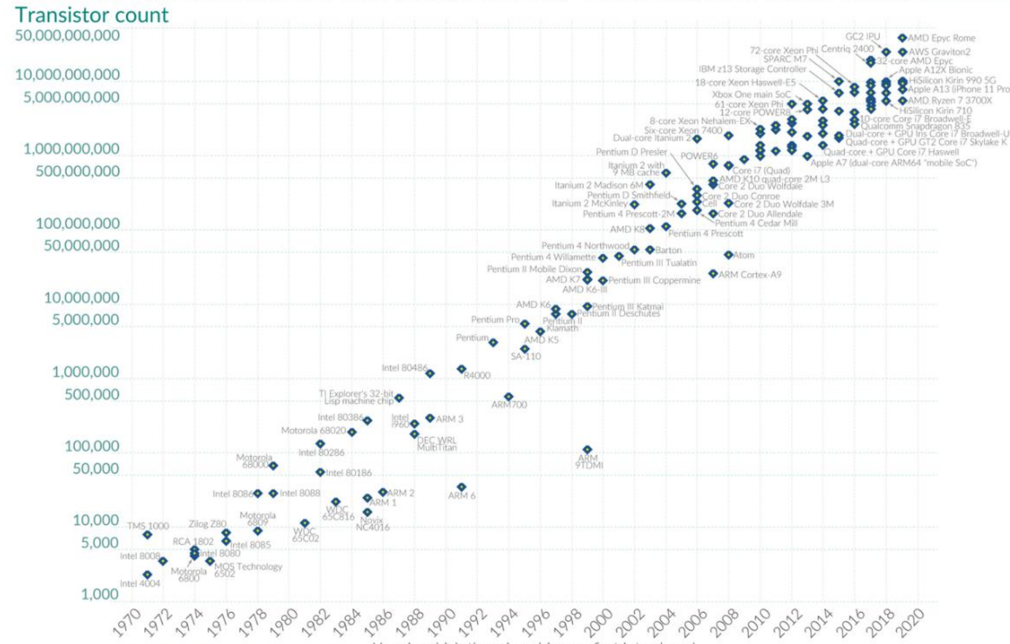
ADVANCES IN PIXEL DETECTORS

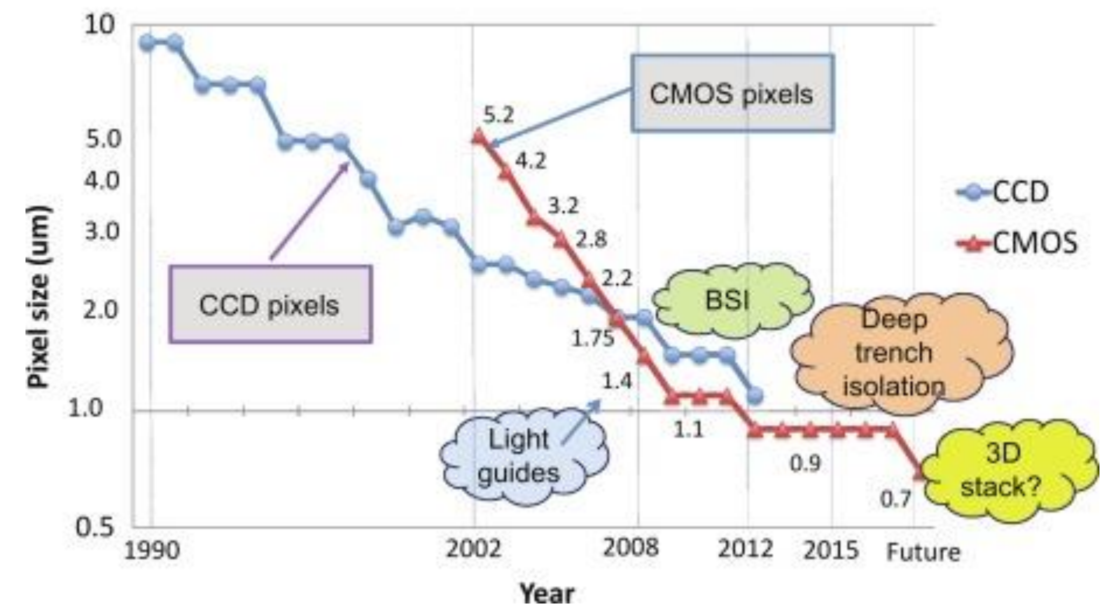
Tomasz Hemperek

hemperek@uni-bonn.de



Progress in semiconductor technology





https://doi.org/10.1016/B978-0-08-102434-8.00007-6

Name	D-OMEGA Ion	LHC1	FE-I3	FE-I4	RD53-ATLAS	?
Year	1991	~1996	~2005	~2011	2020	202?
Technology Node	3 µm	1µ	0.25 µm	0.13 µm	65 nm	28nm
Chip size [mm^2]	8.3x6.6	8x6.35	10.8x7.6	10.2x19	20x21	?
Pixel size [μm^2]	75x500	50x500	50x400	50x250	50x50	25x50
Pixel array	16x63	16x127	18x160	80x336	400x384	?
Transistor count	???	800k	3.5M	80M	600M	>1G

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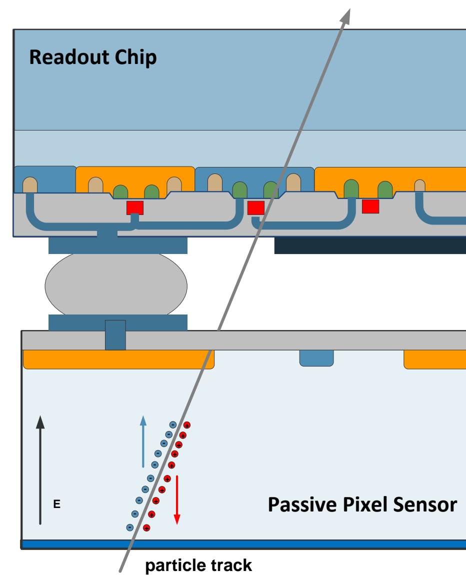
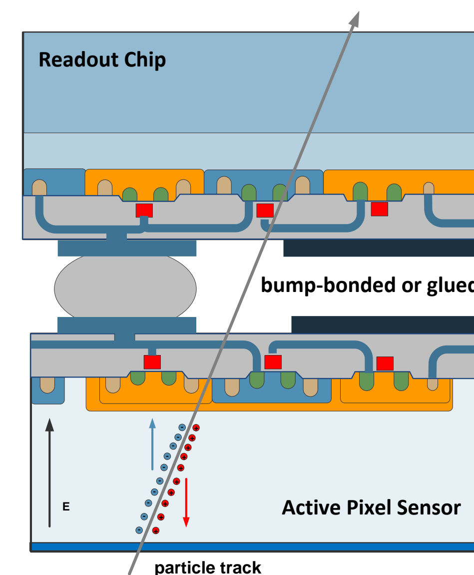
Pixel Detectors

- **Readout ASICs**
- **Monolithic detectors**
- **Monolithic modules**
- **Interconnection**
- **Timing detectors**

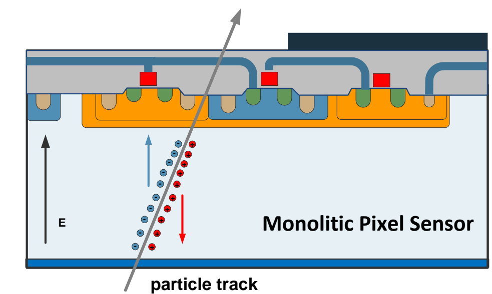
Standard Hybrid



CMOS Active Hybrid

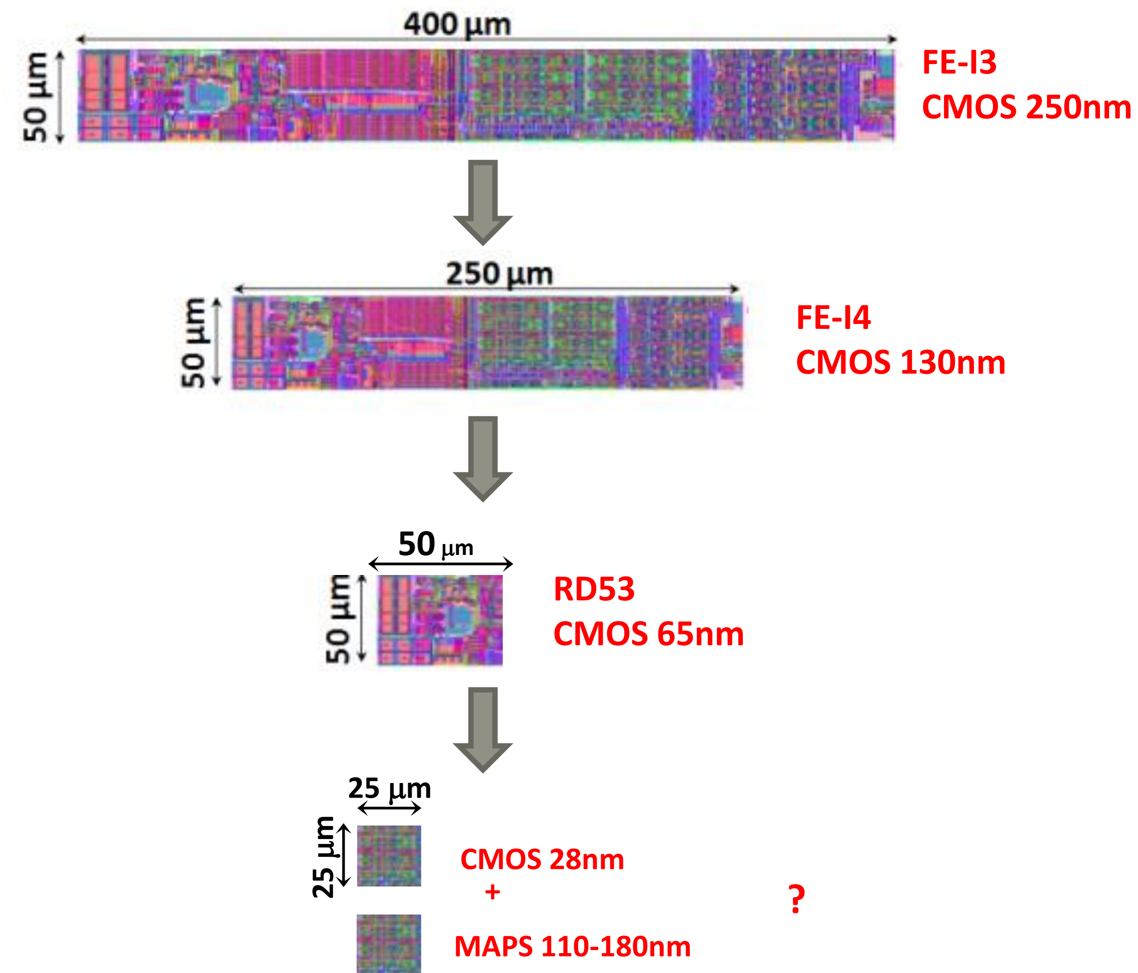


Depleted Monolithic



Pixel Detector Readout

Miniaturization in HEP



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ATLAS/CMS - RD53

Technology	**65nm CMOS**
Pixel size	**50 µm x 50 µm**
Array size	384 (336) / 400 (432)
Min. threshold	<600 e-
Noise hits	< 10^{-6}
Hit rate	**< 3 GHz/cm² (75 kHz avg. pixel hit rate)**
Trigger rate	≤ 4 MHz (trigger only, without readout)
Readout data rate	1-4 links @ 1.28Gbits/s = max **5.12 Gbits/s**
Radiation tolerance	**≥ 500 Mrad, 1 10^{16} 1Mev n.eq/cm² (-15°C)**
SEU	< 0.05 /hr/chip at 1.5GHz/cm² particle flux
Power consumption	< 1W/cm²
Temperature range	-40°C ÷ 40°C

RD53B
RD53B SCC
Rev 1.3

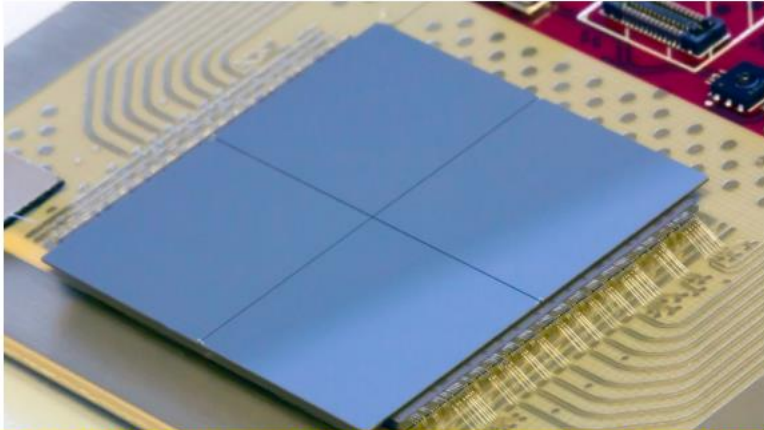
Row
100
200
300
100
200
300
400
Column

RD53C-ATLAS: Q1 2022
RD53C-CMS: Q2-Q3 2022

future

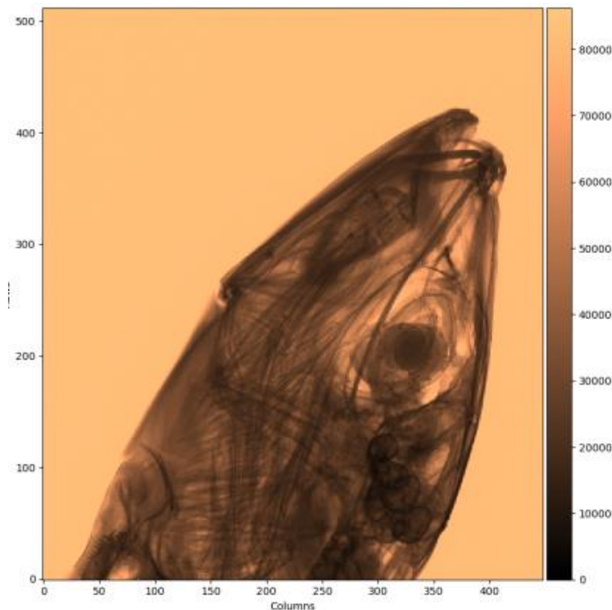
28nm + FPGA ?

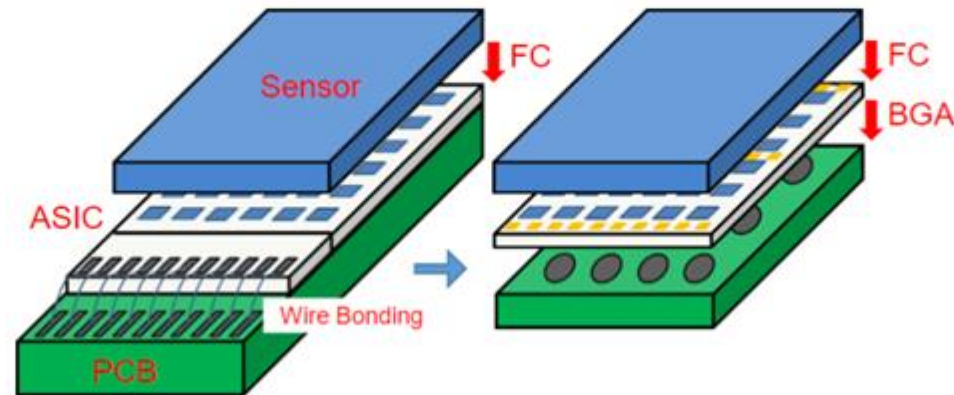
TimePix4


Timepix4 with 4x300 µm (256x256) edgeless Si sensor (August 2020)

Technology	65nm CMOS
Pixel size	55 µm x 55 µm
Array size	512x448 (4-side abuttable)
Min. threshold	< 500 e-
Timing resolution	~200ps
Max Count rate	~800 Ghits/cm²/s
Readout data rate	163 Gbps (16 x 10.24 Gbps)

→ **FPGA**





X. Llopart. iWoRiD 2021

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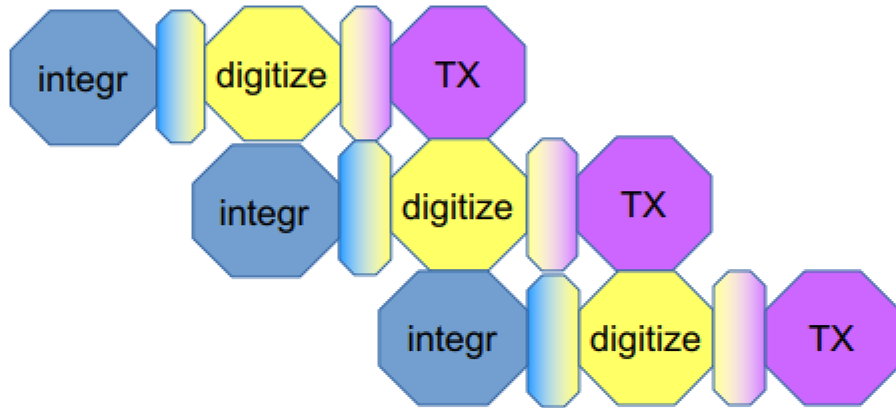
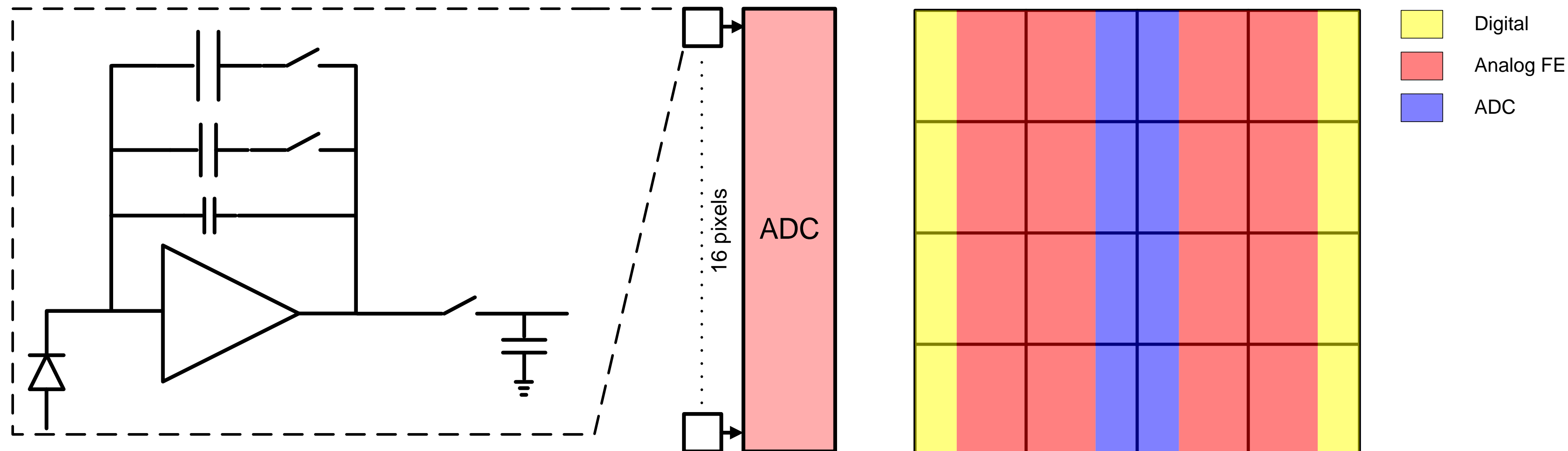
Cordia - Continous Readout Digitizing Imager Array



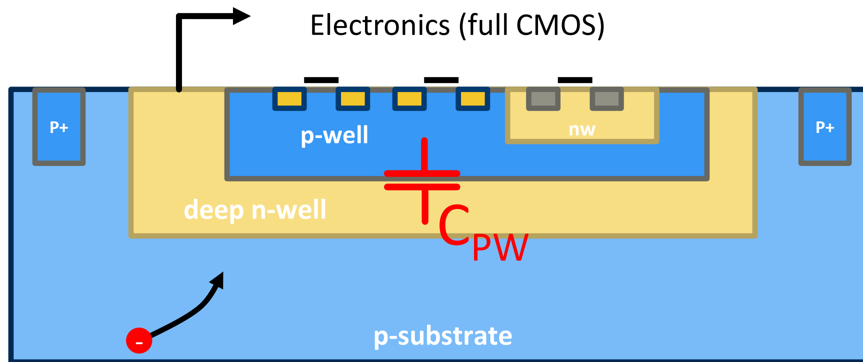
Technology	**65nm CMOS**
Pixel size	100 µm x 100 µm
Frame Rate	**≥ 100 kHz**
Dynamic range	**2+12bit - 10^4** photons (12keV) - single photos sensitive
Sensors	**Si, LGAD, CZT, DMAPS, …**
Readout data rate	**~200 Gbps**

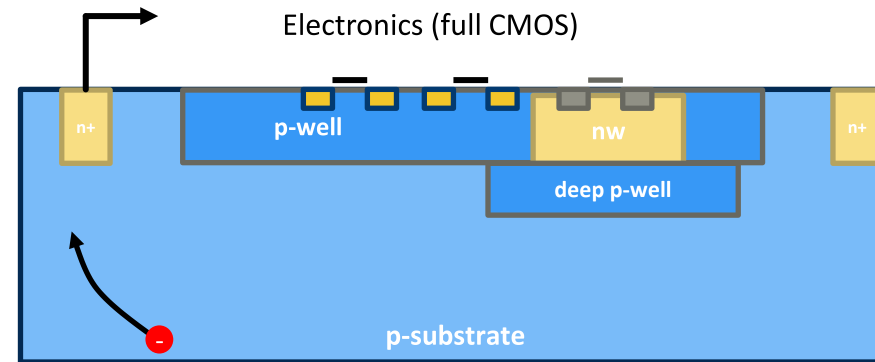


H. Graafsma, PSD 2021

Monolithic

Monolithic - Fundamental process options





Electronics **inside** charge collection well

- Collection node with **large fill factor** → rad. hard
- Large sensor capacitance (DNW/PW junction!) → x-talk, noise & speed (power) penalties
- Full CMOS with isolation between NW and DNW

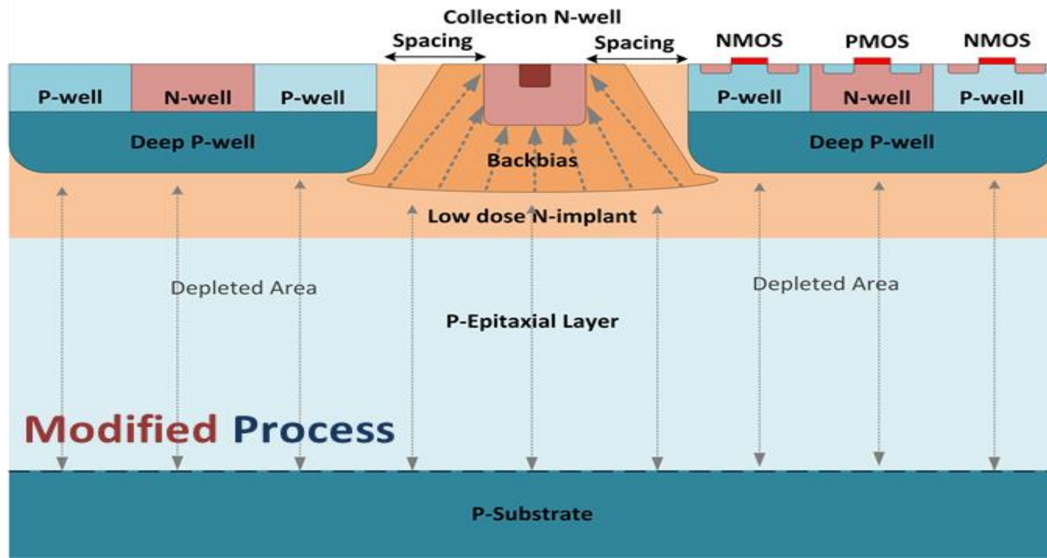
Electronics **outside** charge collection well

- Very **small sensor capacitance** → low power
- Potentially less rad. hard (longer drift lengths)
- Full CMOS with additional deep-p implant
- **Smaller pitch**

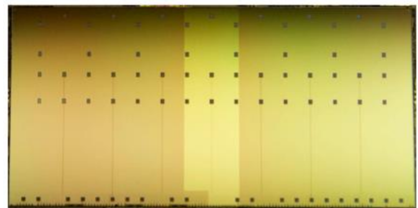
input capacitance vs **electric filed**

power VS radiation hardness

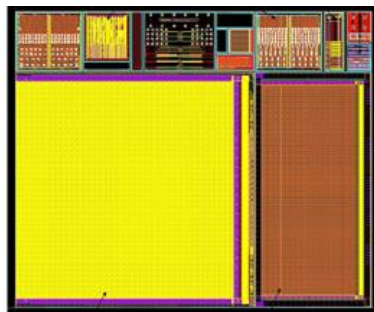
Small electrode



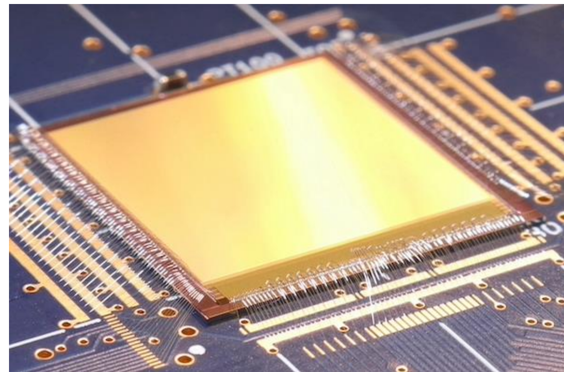
- **TowerJazz** 180 nm CMOS CIS
- Deep Pwell allows full CMOS in pixel
- Gate oxide 3 nm good for TID
- Thickness: 18 – 40 µm
- High resistivity: 1 – 8 k Ohm-cm
- Reverse substrate bias
- **Modified process** to improve lateral depletion
- Derived from ALICE development (CERN)



ALPIDE [ALICE ITS]
(x - 2016)



TJ-MonoPix/Malta
(2018)

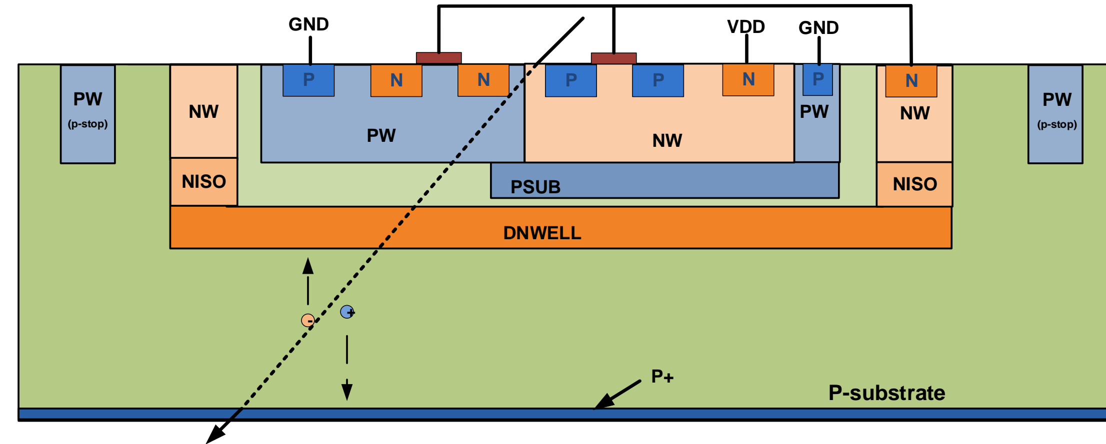


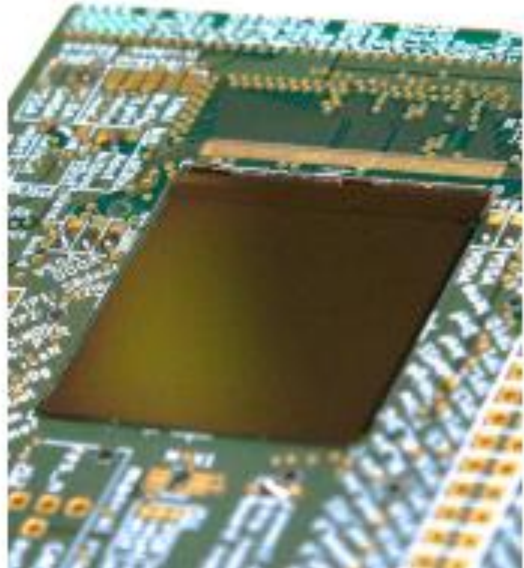
TJ-MonoPix2 / Malta2

TJ-Monopix2:

- Size: 20 x 18 mm^2
- Thickens: >50um
- Pixels size: 33 x 33 um^2
- Pixel array: 512 x 512
- Timing: 25ns
- Threshold: ~150e-

Large electrode

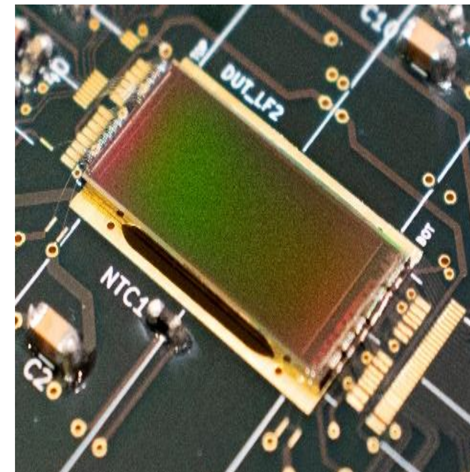




https://arxiv.org/abs/2012.05868

MuPix10:

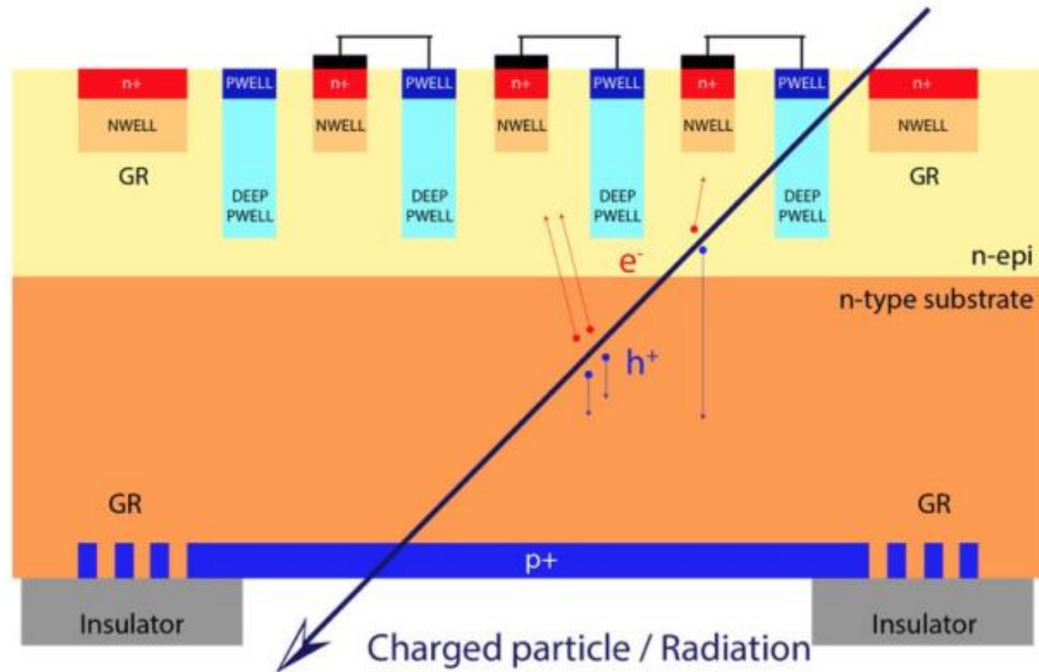
- Process: TSI 180nm
- Size: 23.1 x 20.7 mm^2
- Thickens: 50um
- Pixels size: 80x80 um^2
- Pixel array: 256 x 250
- Substrate: 200 Ohm-cm
- Bias: >60 – 100 V

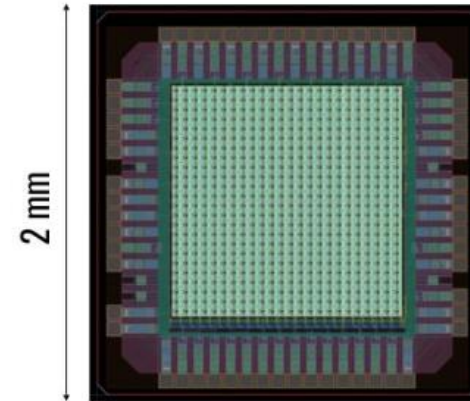


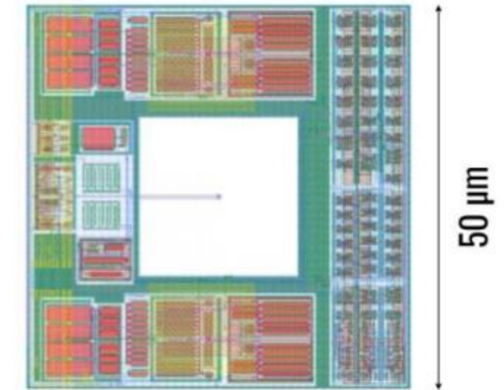
LF-Monopix2:

- Process: LFoundry 150nm
- Deep N-well/P-well
- Size: 19.8 x 9.5 mm^2
- Thickens: 75-200um
- Pixels size: 50x150 um^2
- Pixel array: 340 x 56
- Threshold: ~1000e-
- In pixel readout
- Substrate: >2000 Ω·cm
- Bias: > 250 V

Arcadia





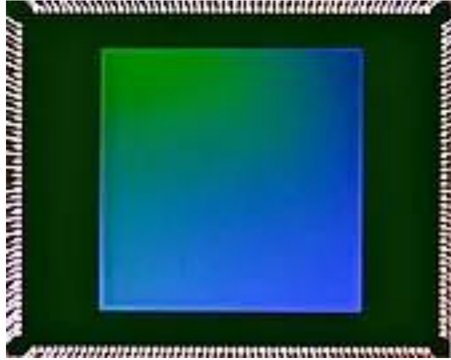


Matisse:

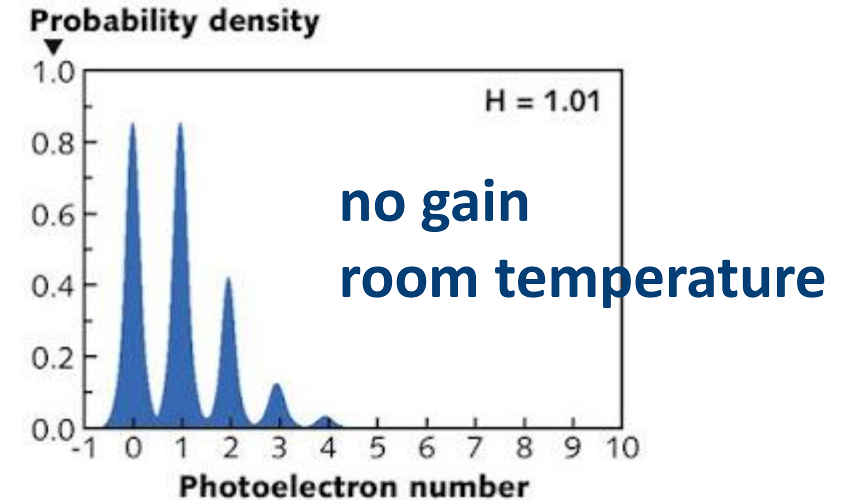
- Process: LFoundry 110nm
- Size: 2 x 2 mm^2
- Thickness: 100-**400um**
- Pixels size: 50x50 um^2
- Pixel array: 24x24

M. Rolo, AIDAinnova 2021

QIS – Quanta Image Sensors – Future?



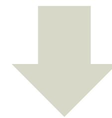
GJ01611 - **Photon Counting**
16 MP
Pixel Pitch: **1.1μm**
Frame rate: 30fps
Read noise: 0.19e-



no gain
room temperature

FIGURE 3. A room-temperature photon-counting histogram from a single QIS jot with 20,000 reads shows clear quantization of photoelectrons. Average exposure is one photoelectron, and read noise is 0.175 e- RMS.

3D integration + advance CMOS technology



for tracking binary readout and < 0.2μm resolution

Monolithic modules

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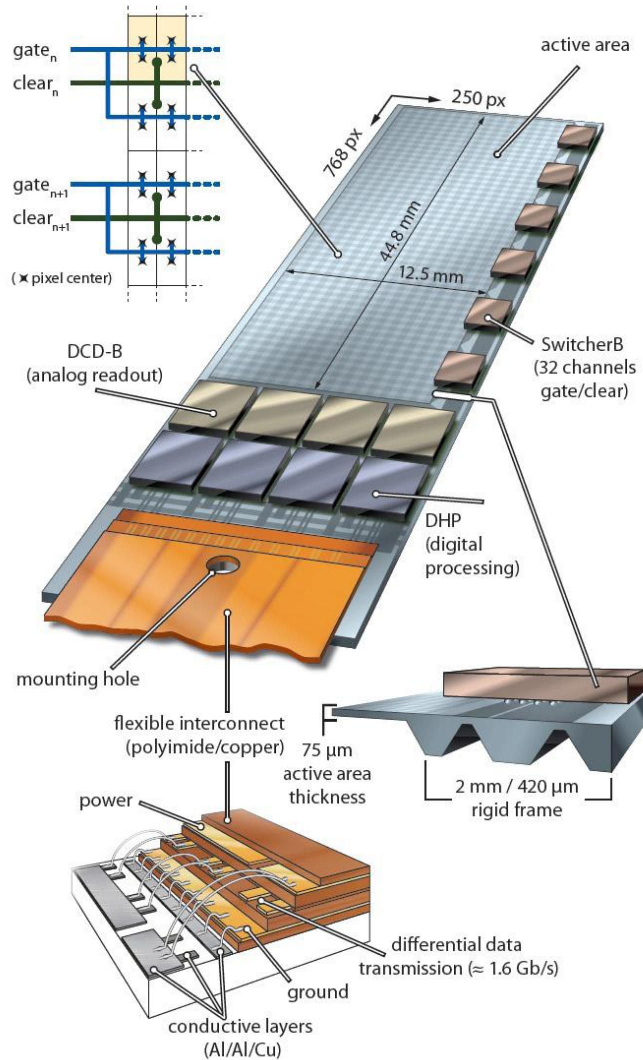
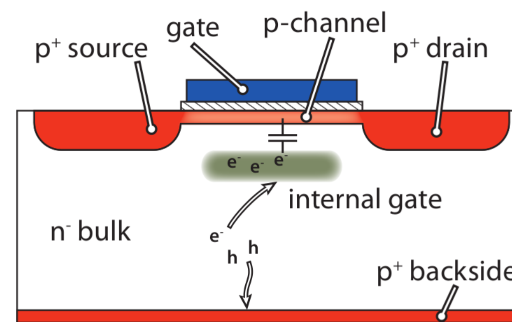
DEPFET module

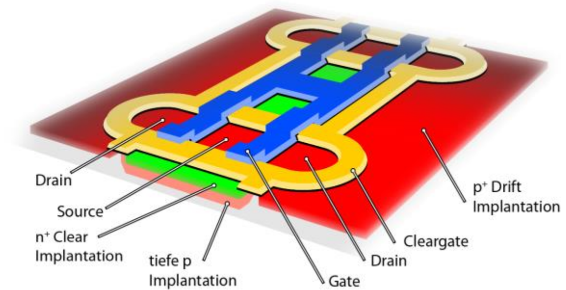


Thickness: 75 µm
Resolution: ~15 µm
Pixel size: 50x75 µm
Readout: rolling shutter (limited hit rate)

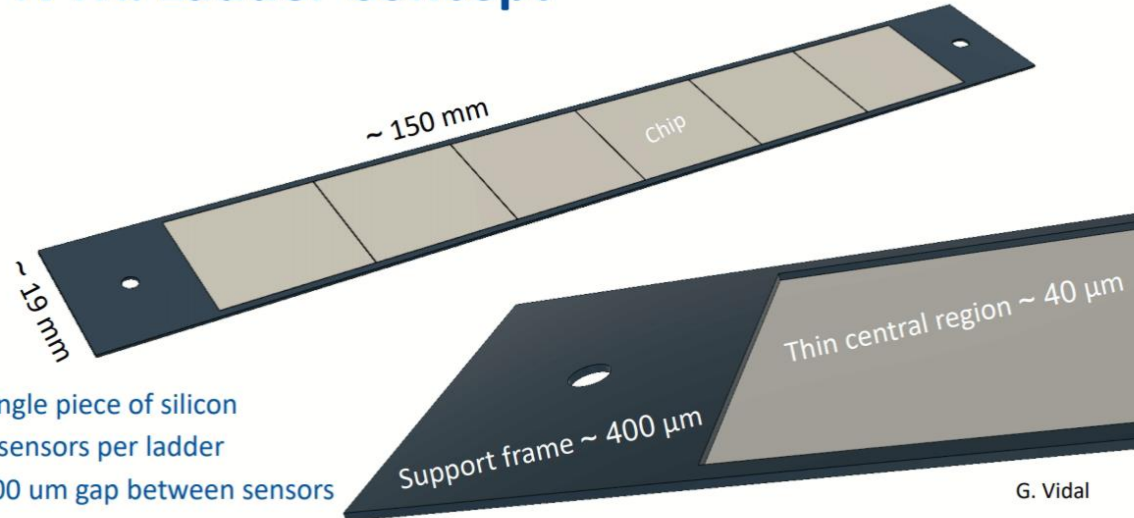
Exciting but challenging sensor technology.

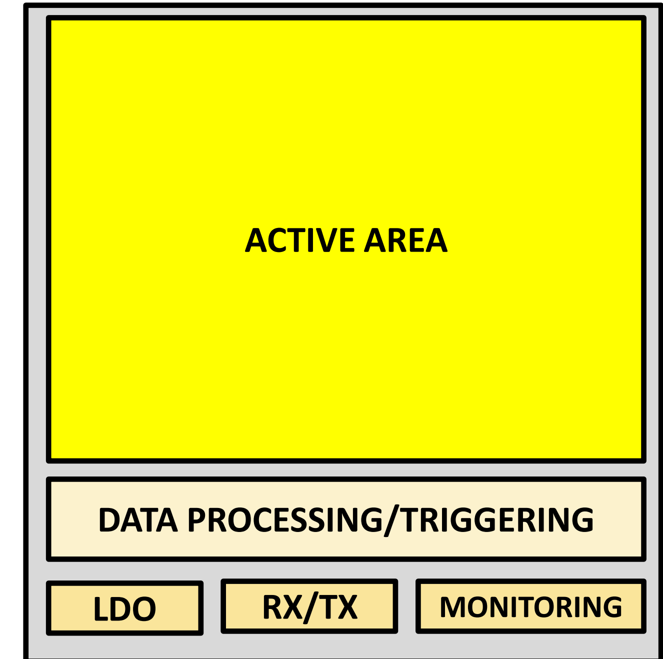
DEpleted **P**-channel **F**ield
Effect **T**ransistor (**DEPFET**)





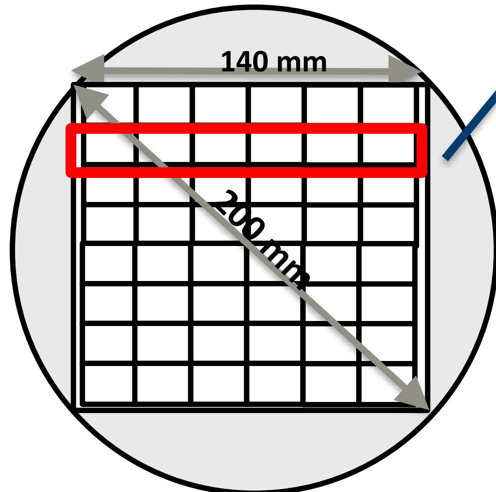
VTX/OBELIX

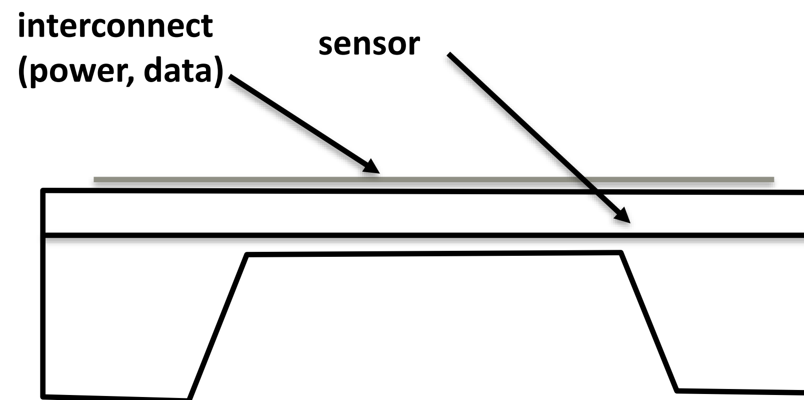




~2.5V
+BIAS

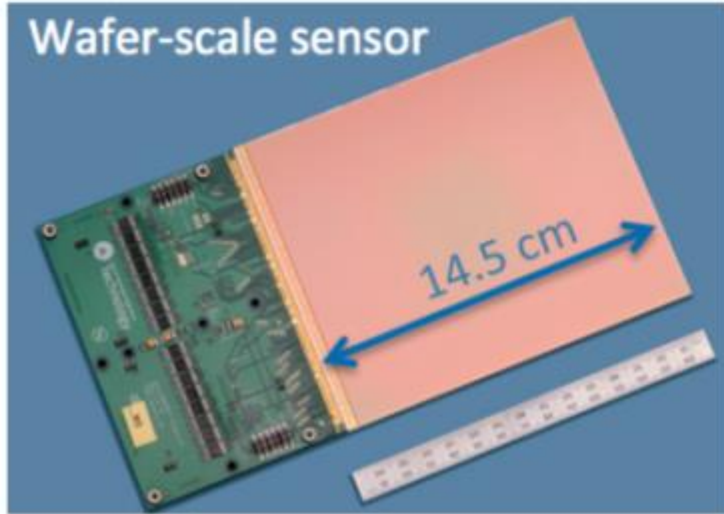
CLK
CMD
DATA

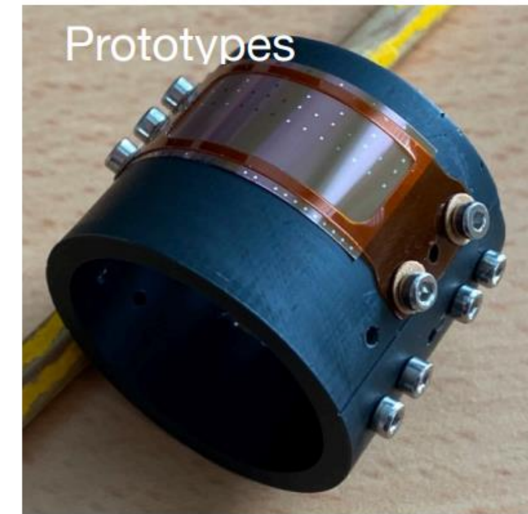


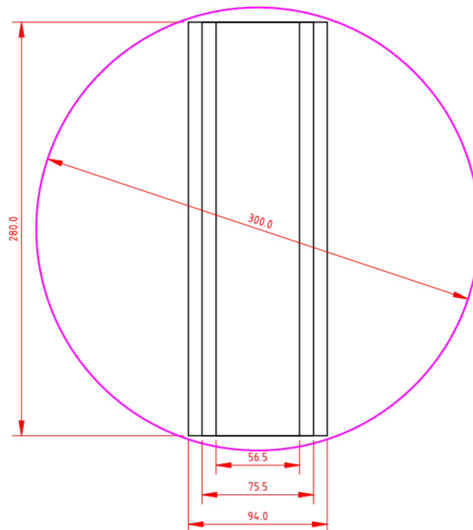


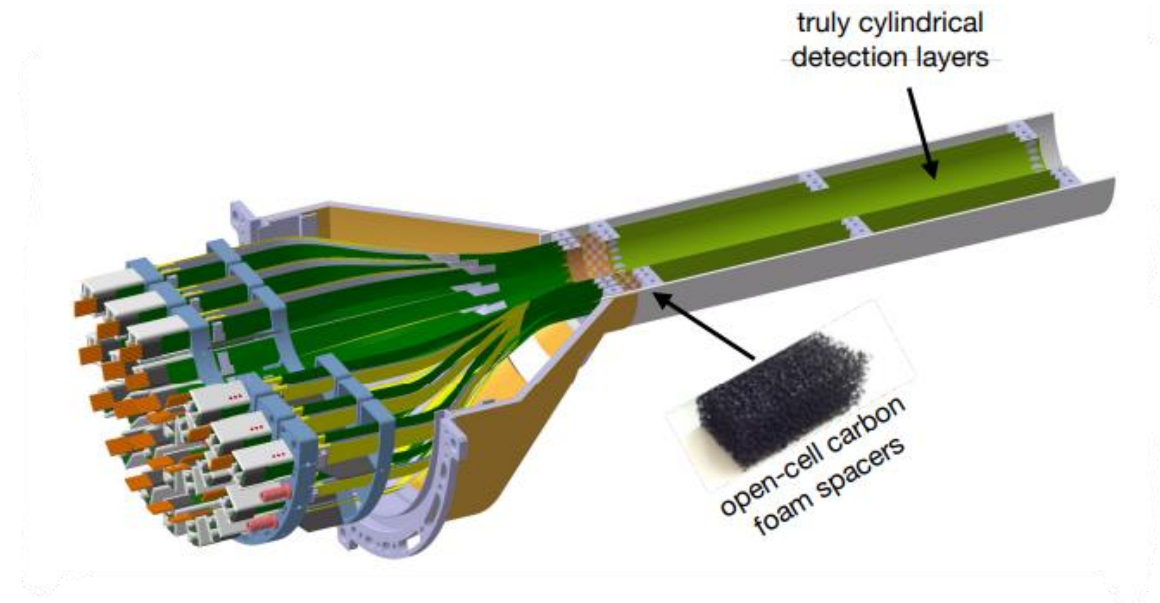
- ~40um2 pixel pitch
- 100-200 MHz/cm2 hit rate
- ~100ns timing resolution
- Triggered readout

Alice ITS3 / Small electrode 65nm









Integration / Interconnection

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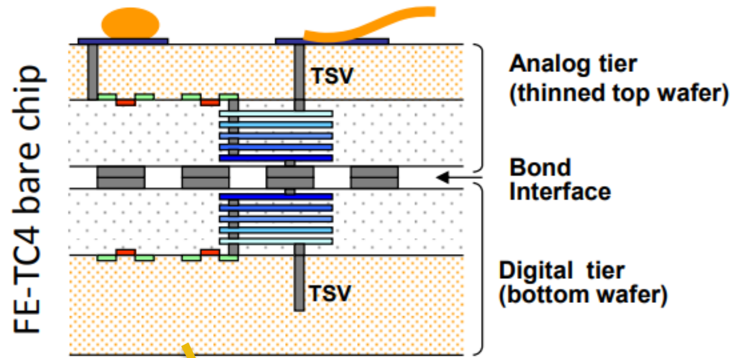
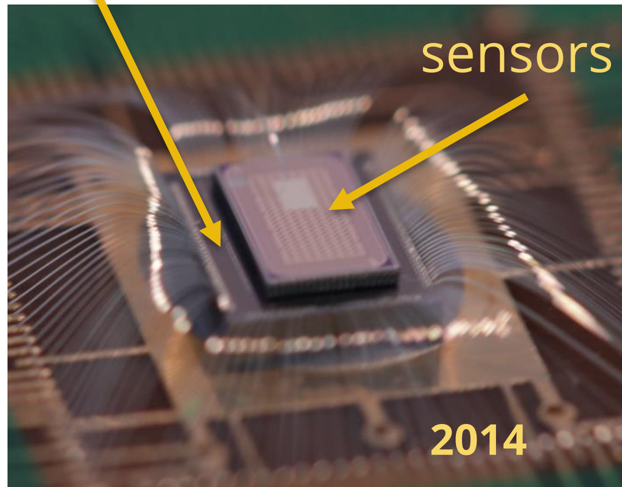
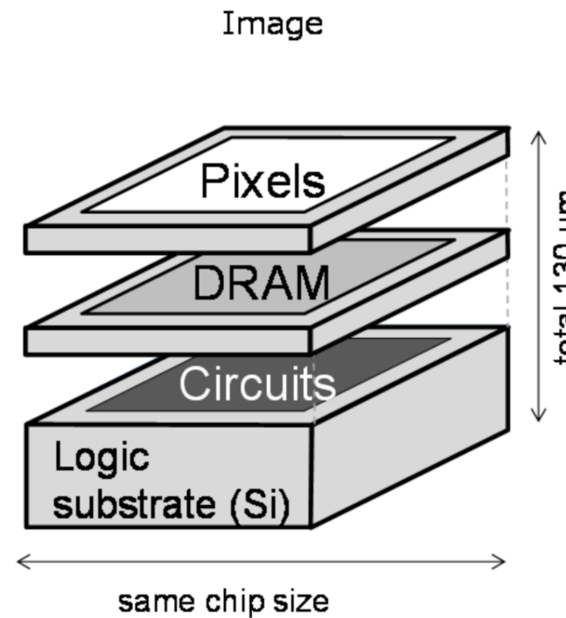
3D integration

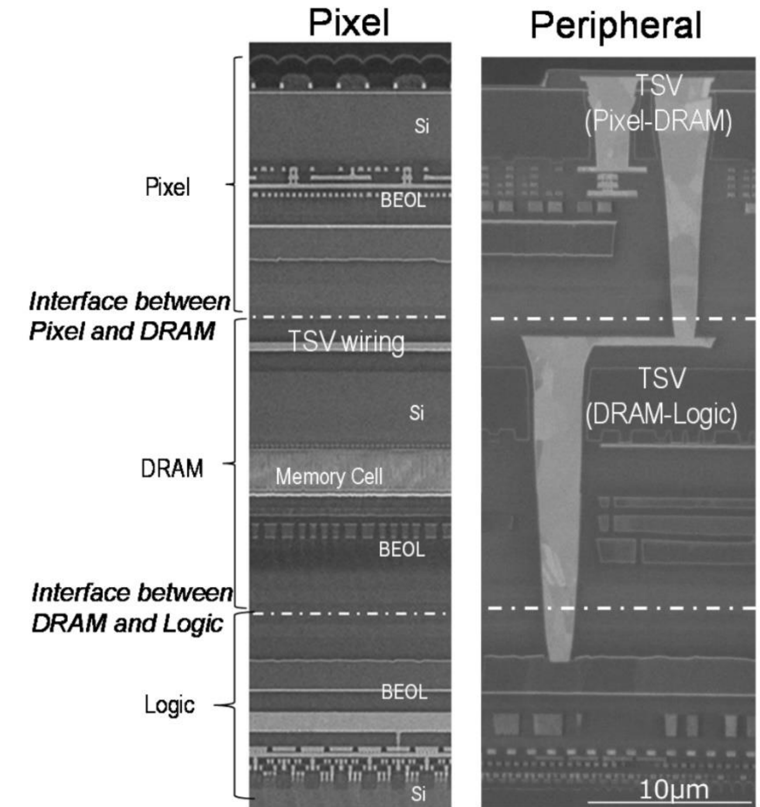
3D IC in HEP





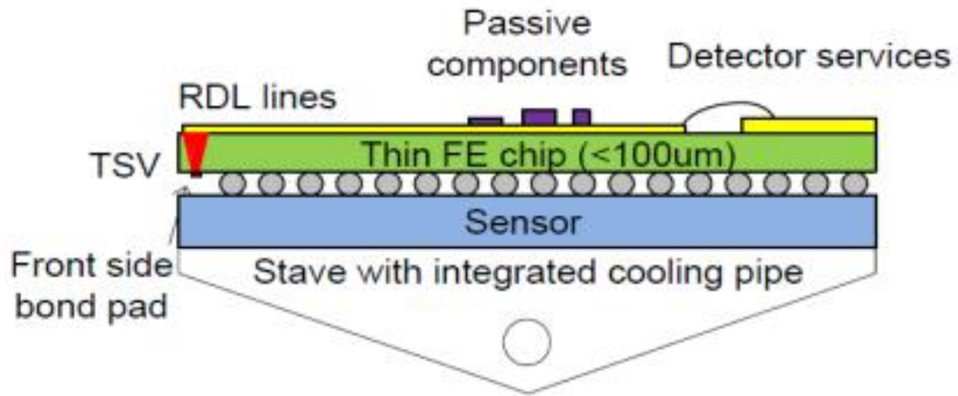
Sony's 3-layer stacked CMOS image sensor technology (2017)

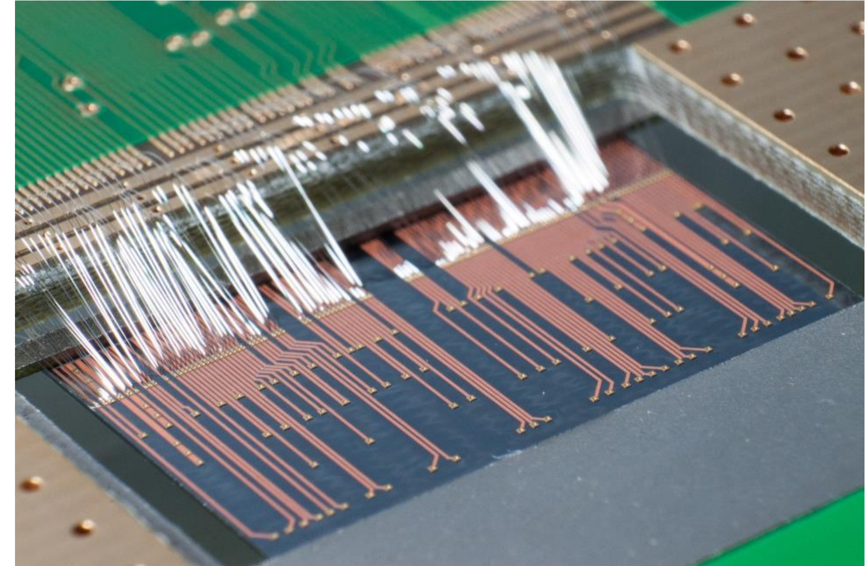


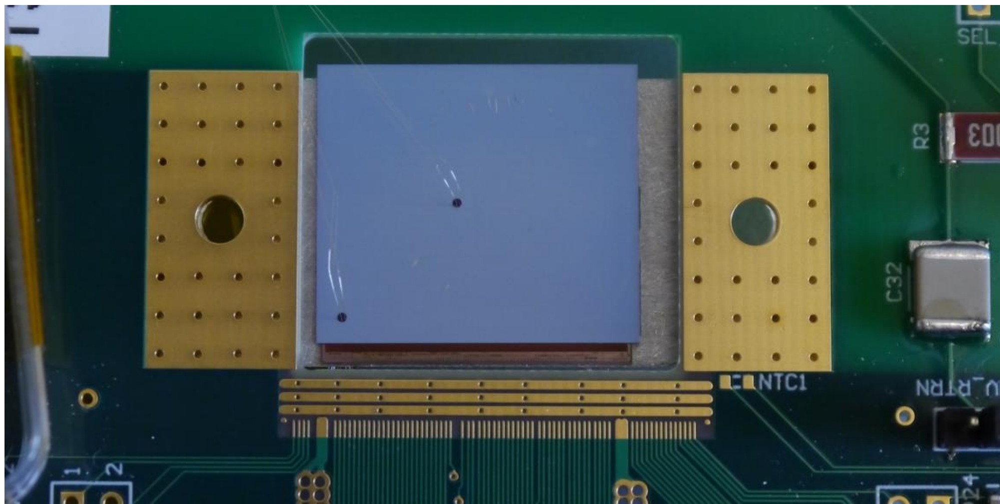


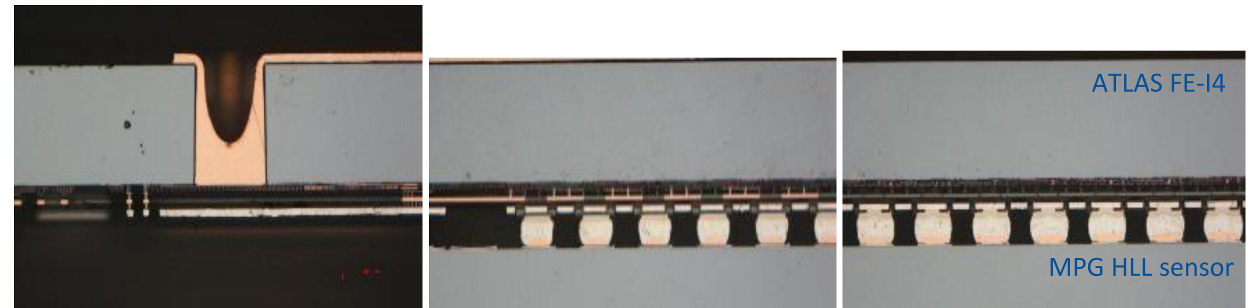
Require wafer bonding and TSV.

TSV Pixel Detector Modules









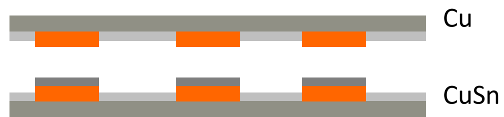
Cross section of module with 80µm thick ATLAS FE-I4 backside TSV ROC

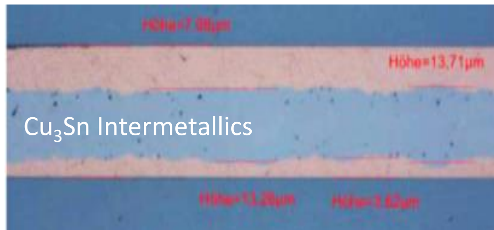
similar development with TimePix3

F. Huegging, AIDAinnova 2021

Wafer bonding

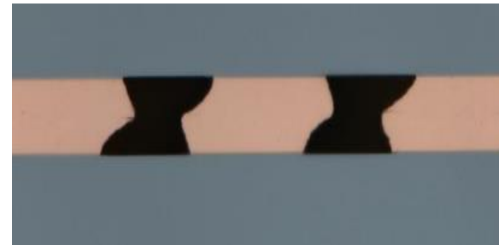
Transient Liquid Phase Bonding (TLPB/SLID)





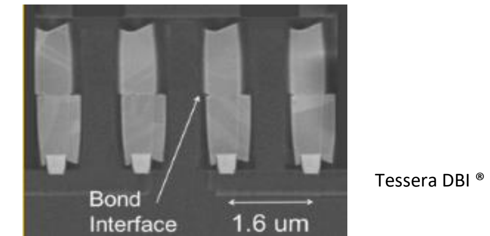
- ECD Cu and Cu-Sn pads
- High melting Cu_3Sn IMC
- Temperature, pressure

Metal-Metal Direct Bonding



- ECD pads (Cu, Au, Ni)
- Planarized surfaces, pre-conditioning
- Temperature, pressure

Metal – Oxide Hybrid Bonding

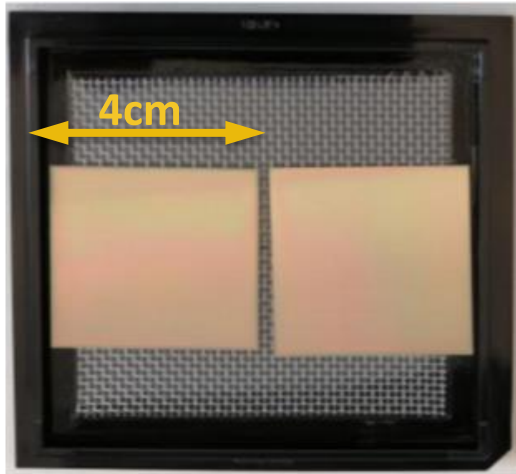


Tessera DBI ®

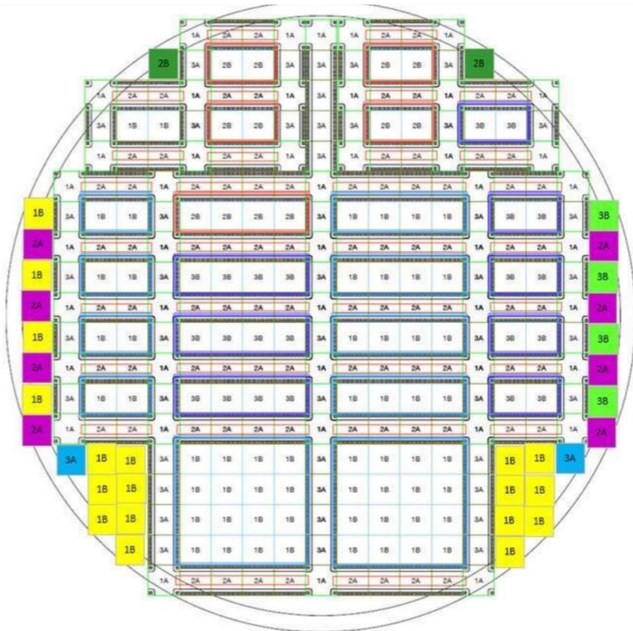
- ECD Cu pads (or Ni)
- Surface planarization (CMP)
- Surface activation (plasma)
- Room temperature bond
- Annealing step

T. Fritzsch, AIDAinnova 2021

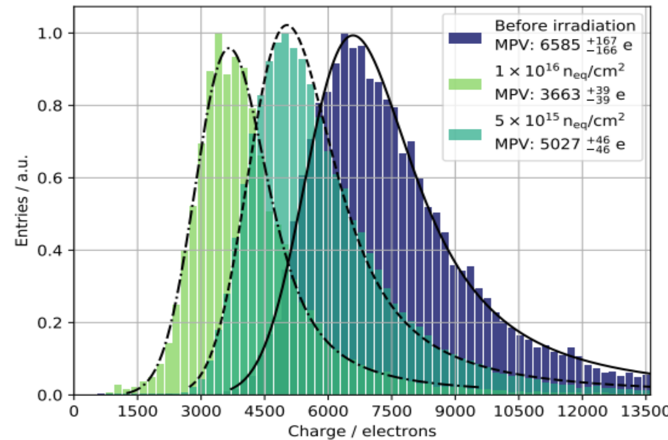
CMOS Passive sensors



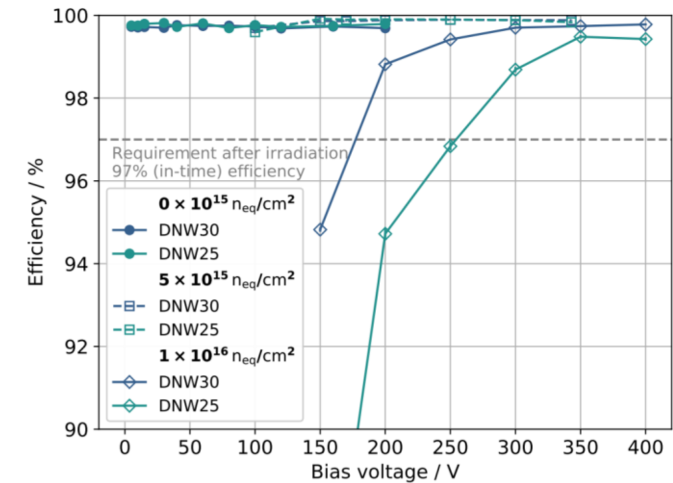
- Multiple metal layers
- **8” wafers**
- Custom thinness: 70-300µm
- Custom **backside process** after wafer processing -> thin entrance window possible (~20nm)
- **AC coupling** on pixel level (remove leakage current)
- **Integrate transistors** (amplifiers) in the sensor -> low-noise (multiplex multiple sensor pixels to one readout, …)



Charge spectrum (MIP)

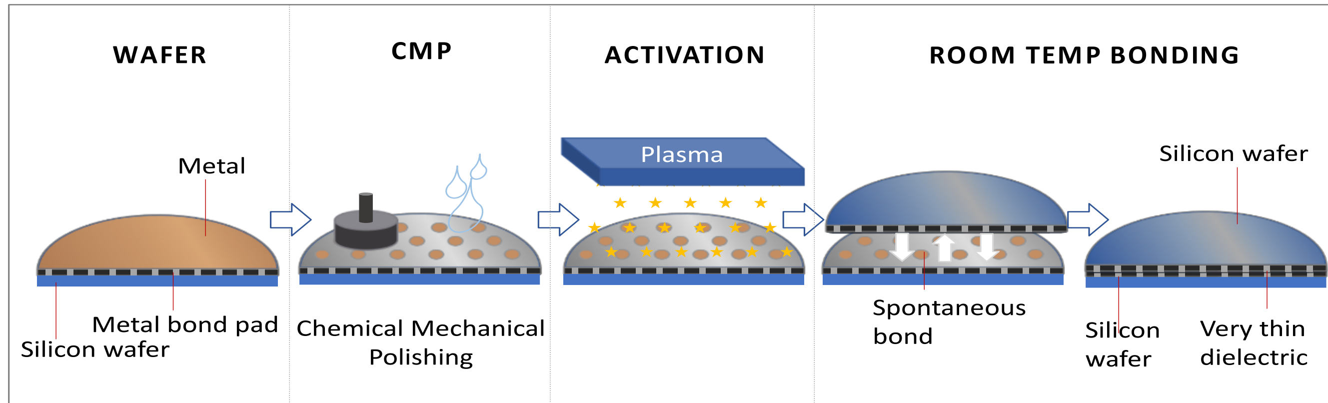


Hit detection Efficiency (MIP)

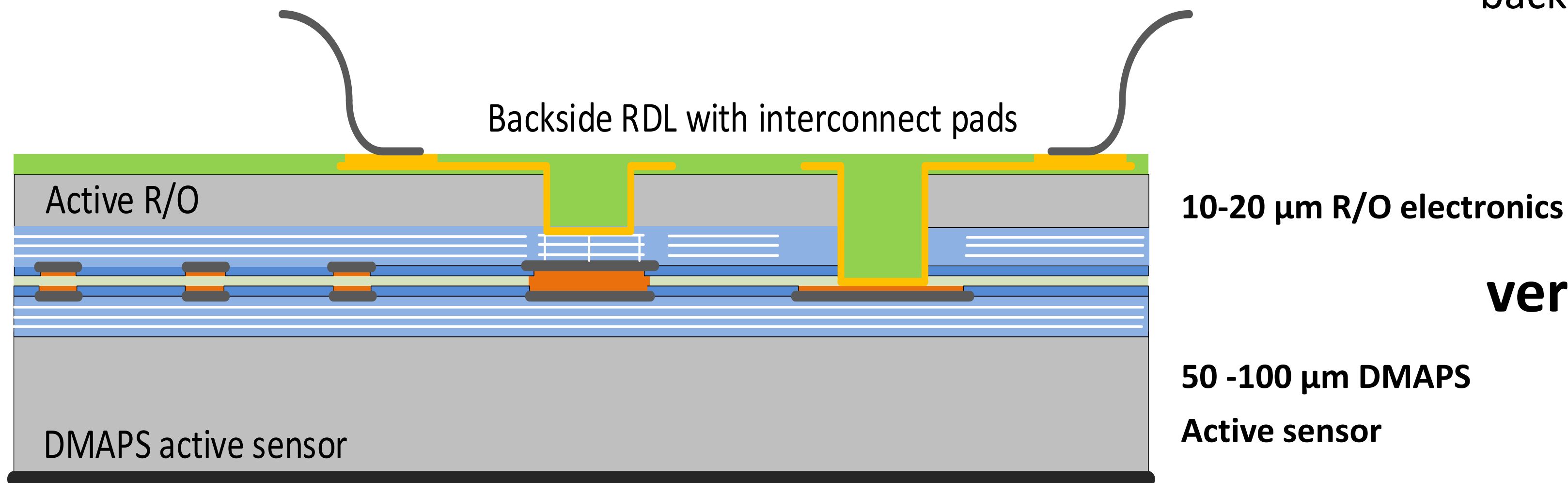


100µm thickness + RD53A

Low-Mass Hybrids



- R/O backside redistribution layer (RDL) with contact pads
- Thinned R/O wafer with backside via last interconnection
- Bonding layer with metal-metal or capacitively coupled contacts
- Thin DMAPS sensor with contact pads and backside processing



10-20 µm R/O electronics

very small pixels, lower cost?

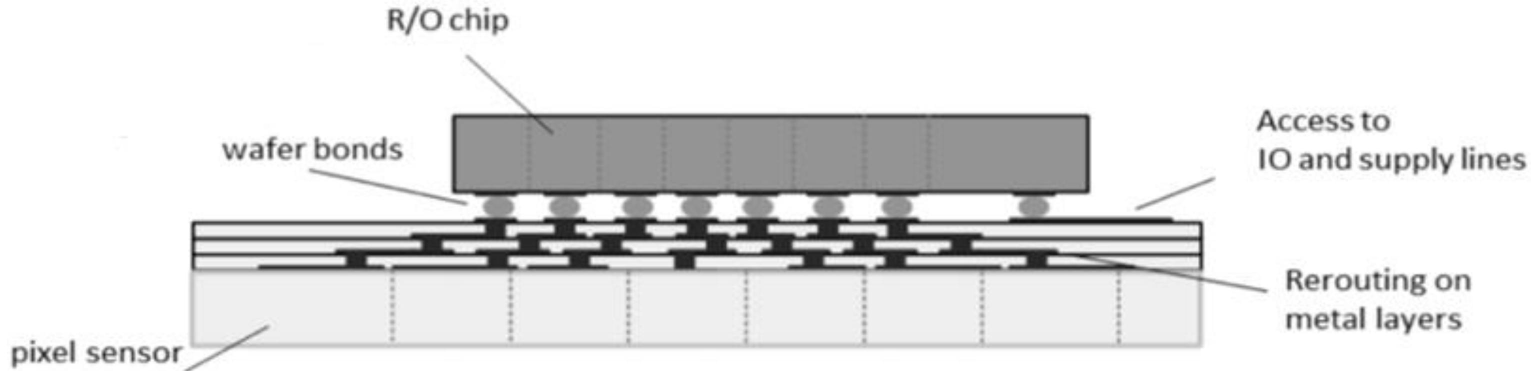
50 -100 µm DMAPS

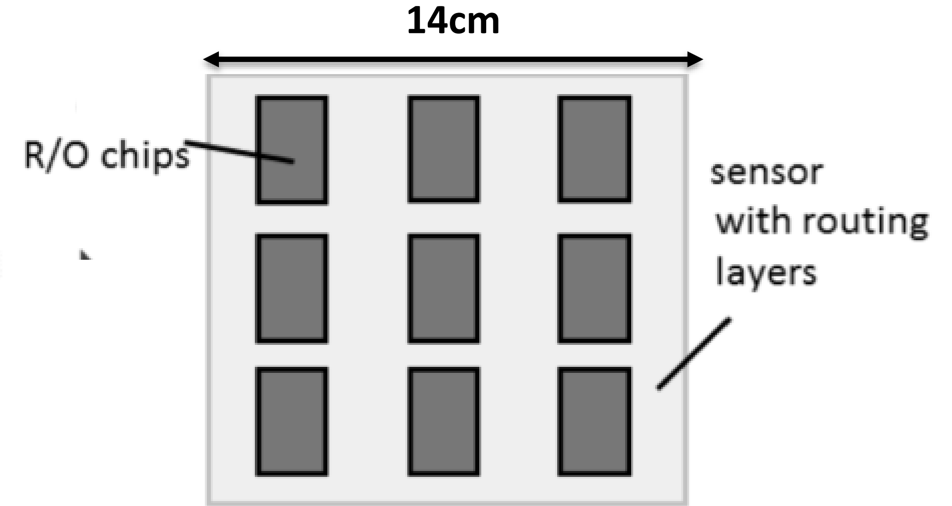
Active sensor

F. Huegging, AIDAinnova 2021

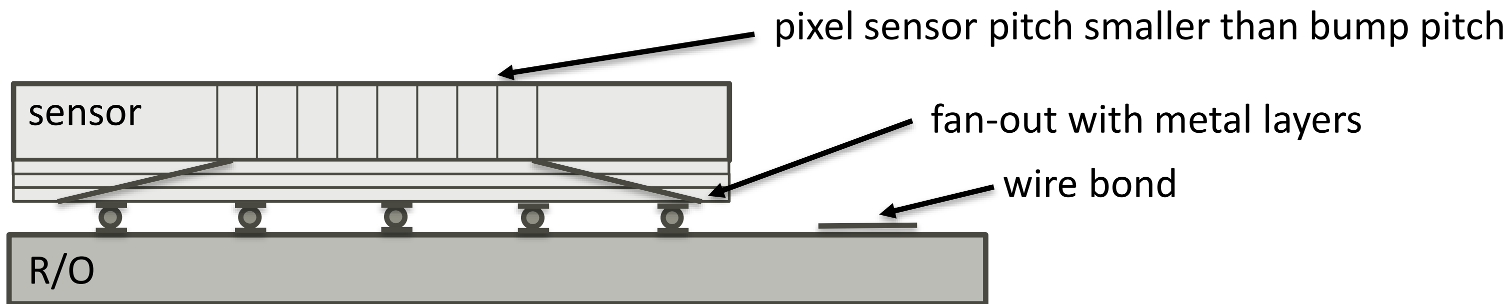
Possibilities having CMOS production

Large area (up to ~14x14cm²) and homogenous (all pixels same size) modules

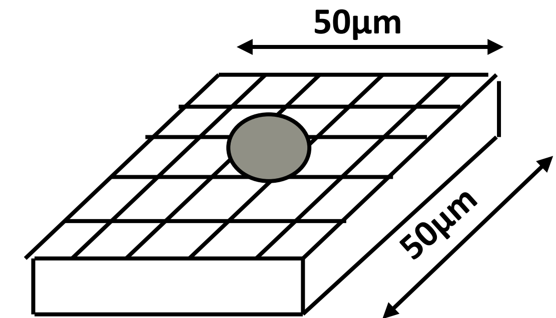




Higher resolution sensors and/or "faster" readout (rate/cm²)



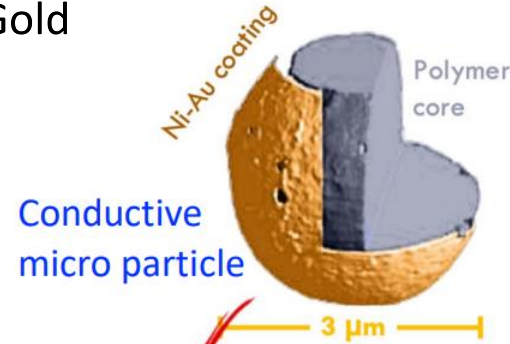
Active pixel multiplexing

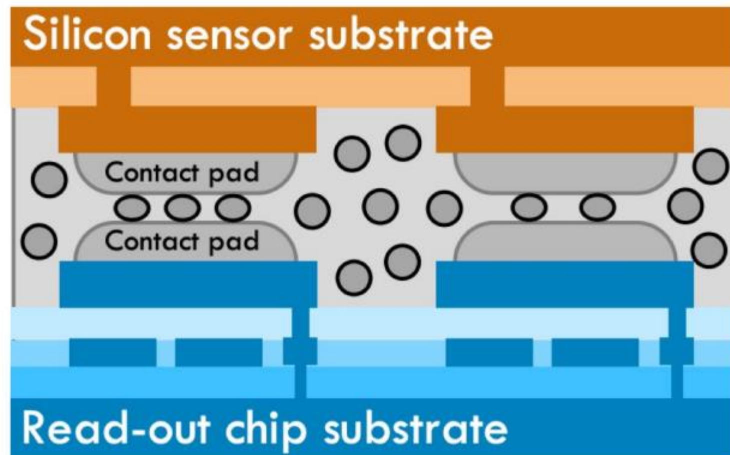


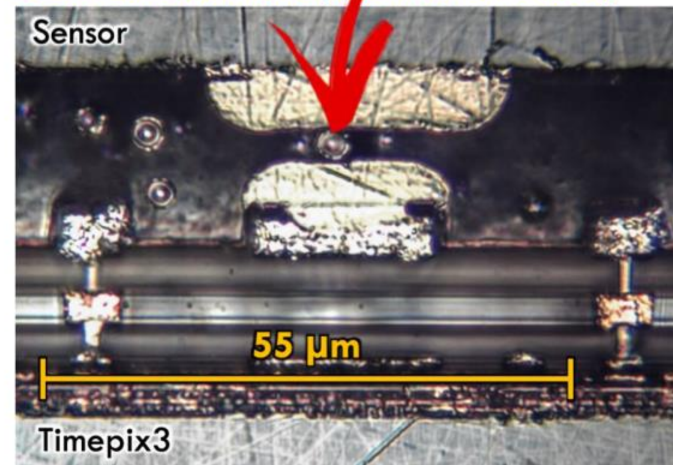
ACF - Anisotropic Conductive Films

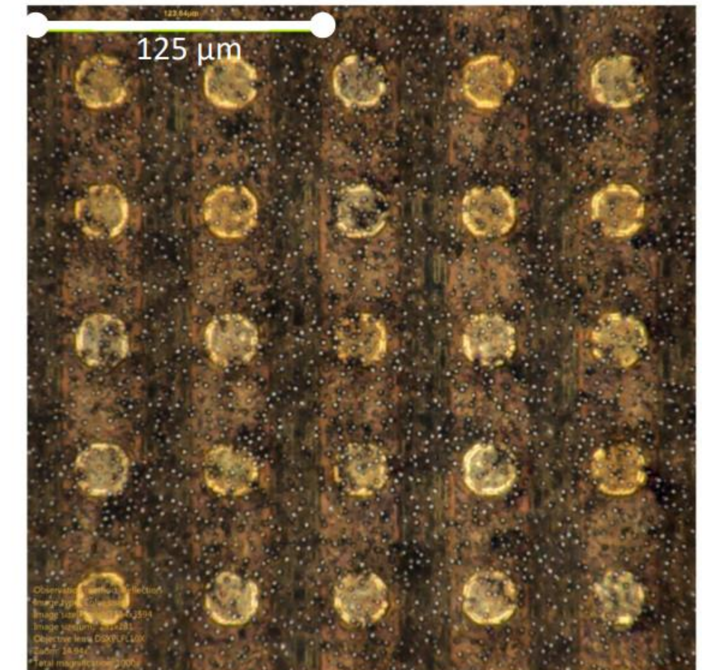
Bump bonding in specialized industry is costly / complex

- Alternative process: **Anisotropic Conductive Films (ACF)**
- **Epoxy film** for mechanical connection, embedded conductive particles for el. connection
- Mask-less sensor/ASIC **metallization**: Electroless Nickel Gold (ENIG) deposition
- In-house **flip-chip process**
- Challenge: **Optimization** of ACF material and flip-chip process for **fine pitch**









D. Dannheim, AIDAinnova Aprill 2021

Timing Detectors

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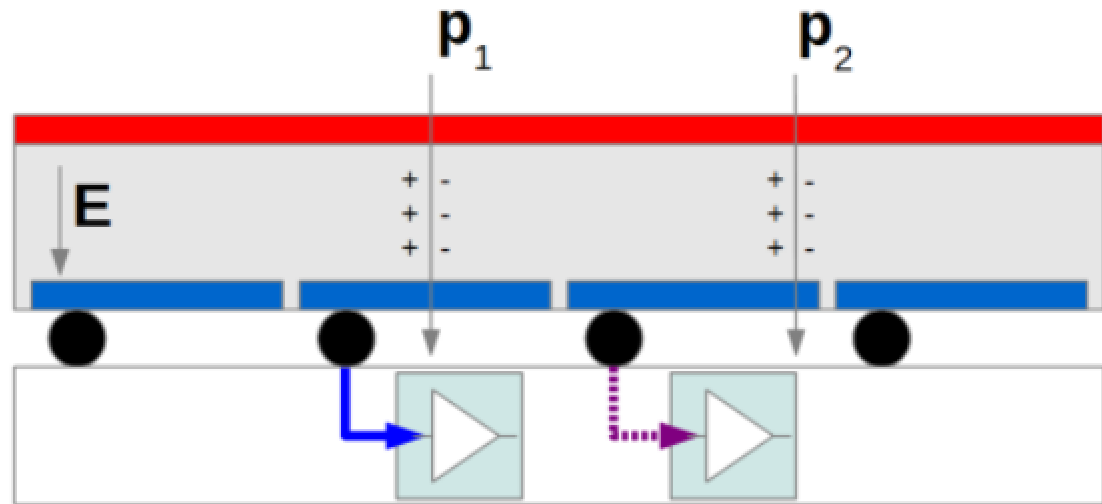
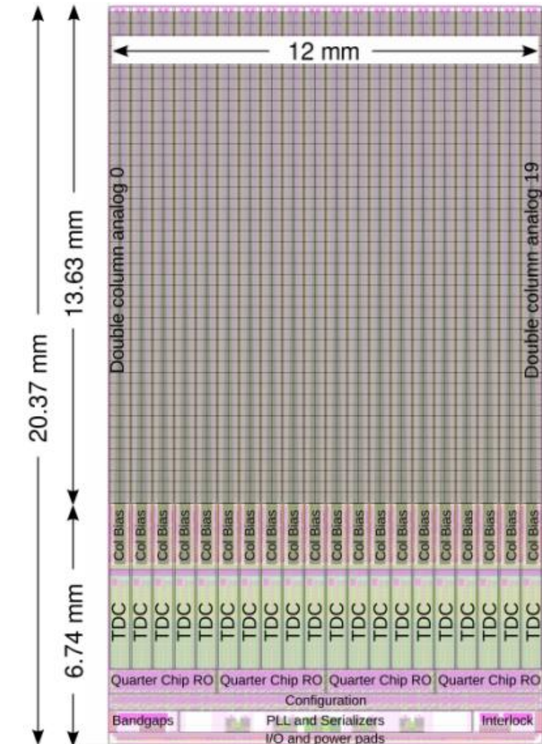
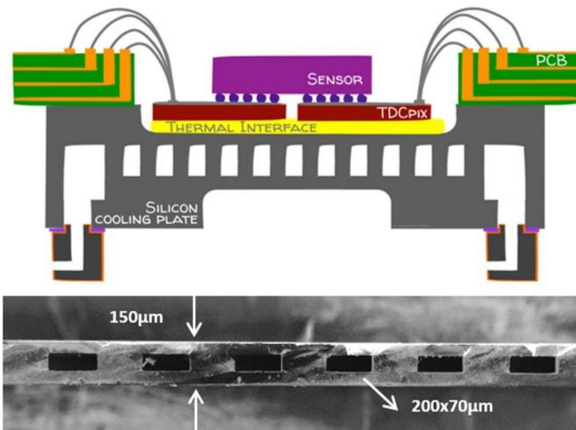
NA62 GigaTracKer

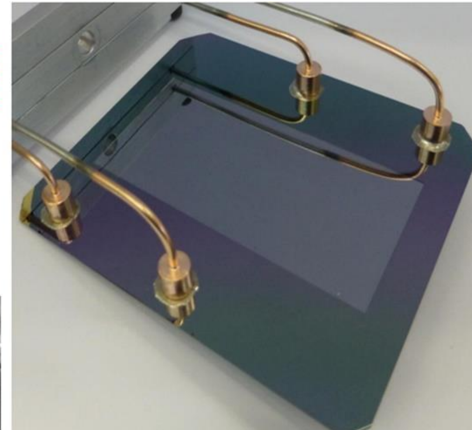


Si planar sensor
Thickness: 200um
Bias: 300-600 V

PixTDC

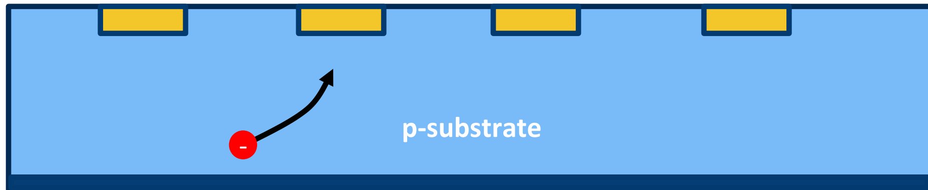




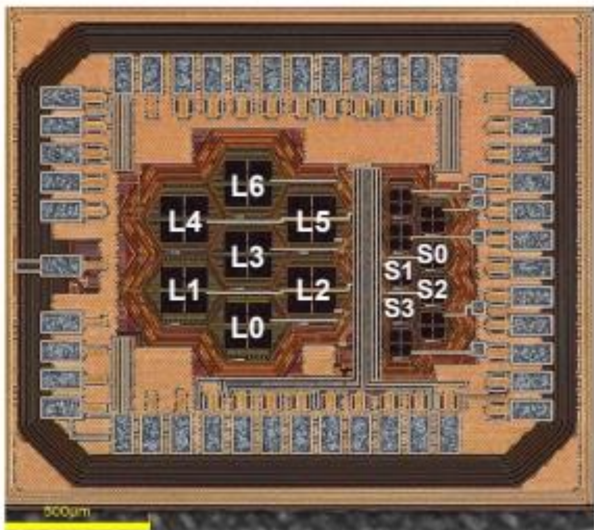


single hit time resolution : 115 ps
track time resolution of : 65 ps

Monolithic Timing (SiGe/CMOS)

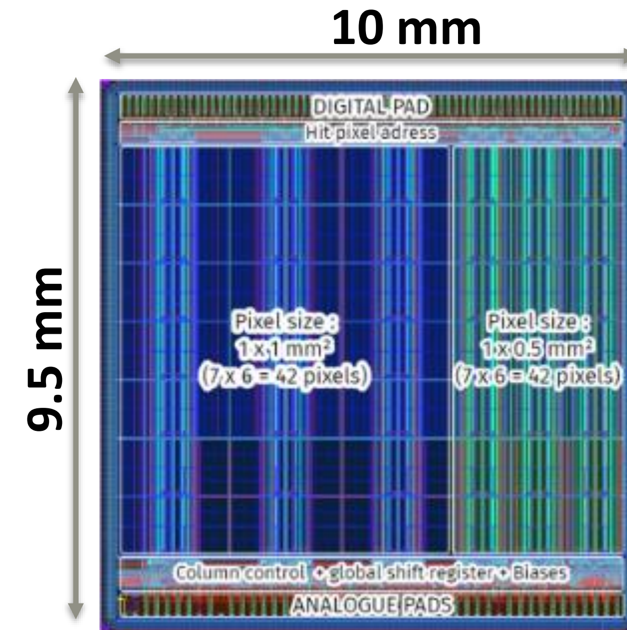


A monolithic silicon pixel in SiGe BiCMOS



Technology: IHP 130nm / SG13G2
Timing resolution: <50ps

A monolithic Silicon Planar (CAcTµS)

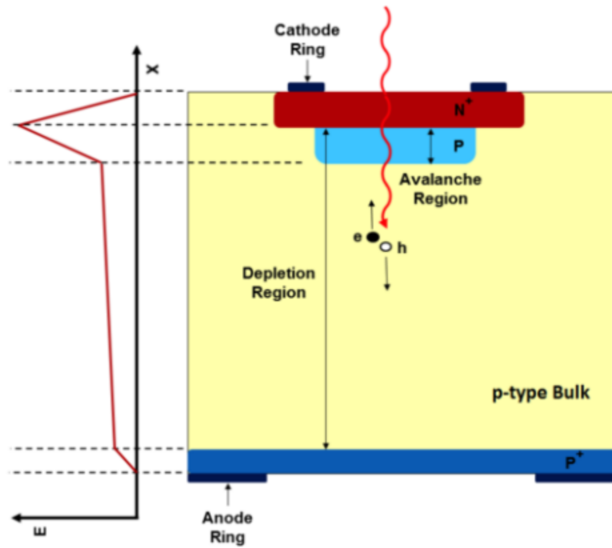


Technology: LFoundry 150nm
Pad size: 1 x 1 and 1 x 0.5mm^2
Thickness: <= 100 µm
Expected timing resolution: <100ps

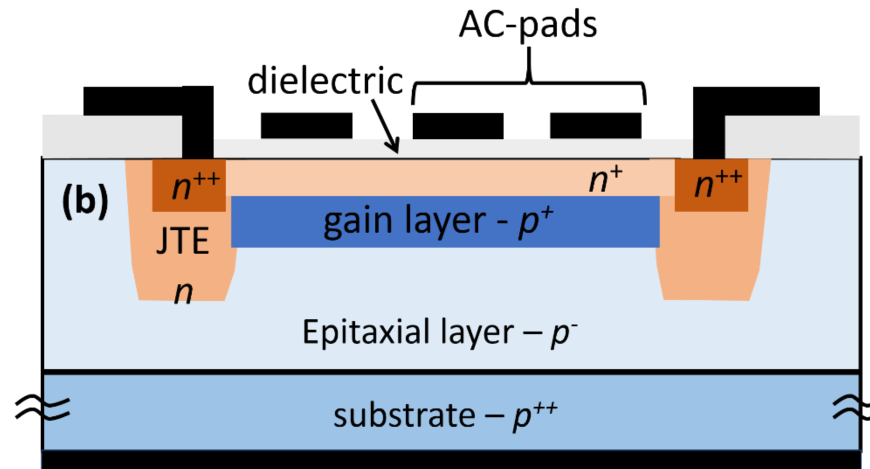
M. Munker, PSD 2021

Sensors with gain

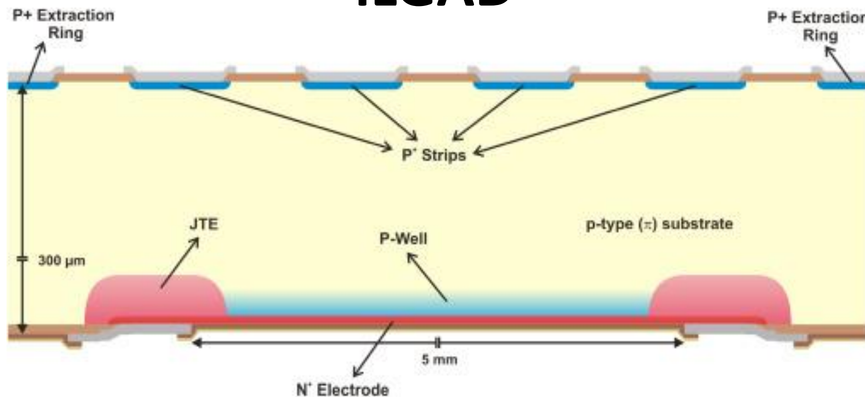
LGAD



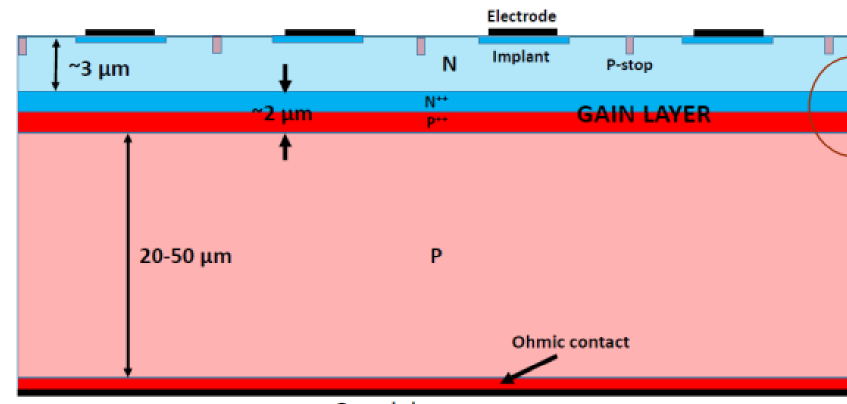
AC-LGAD



iLGAD



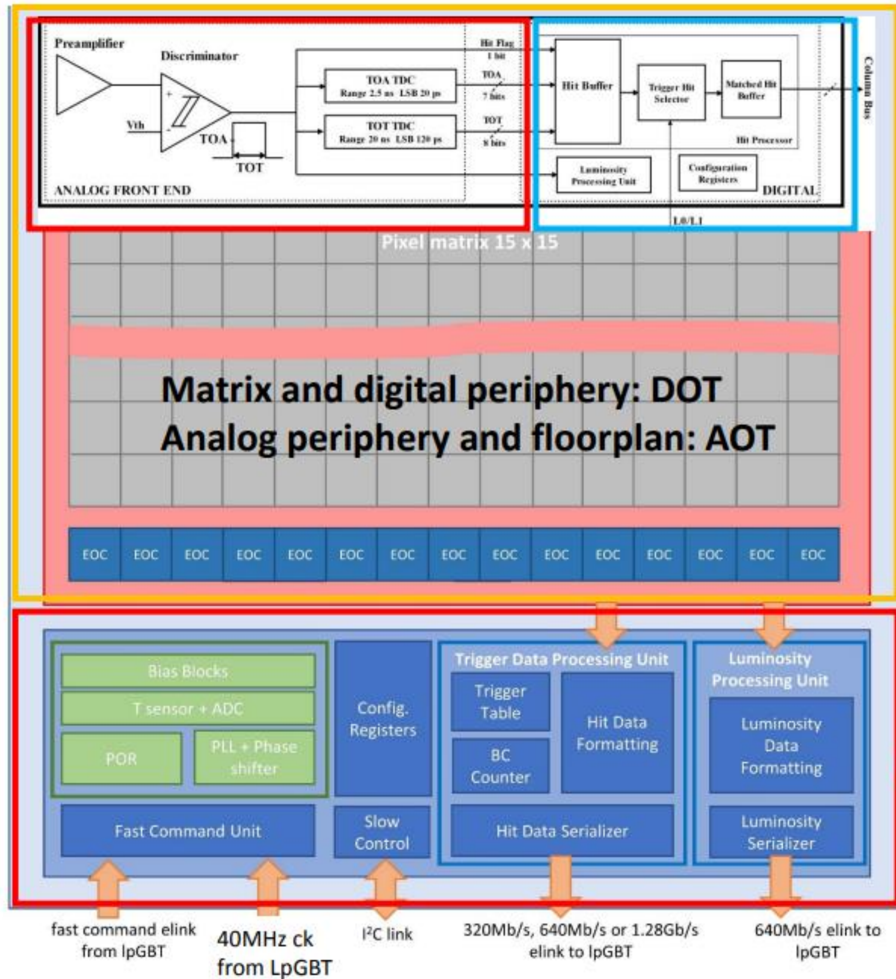
DJ-LGAD

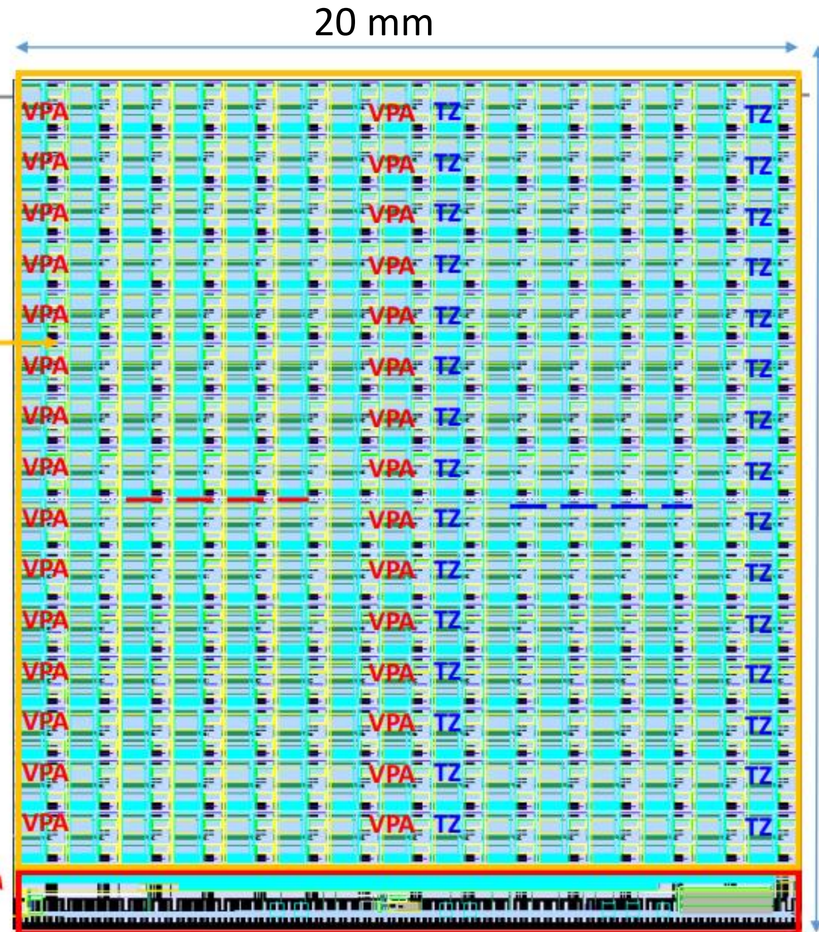


Timing resolution < 30ps

Signal gain for soft x-ray

Altiroc2 – ATALS





Array size: 15 x 15

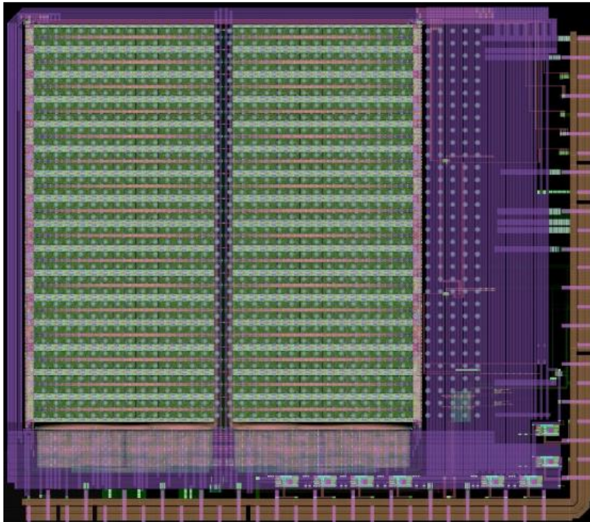
Pad size: 1.3 x 1.3 mm^2

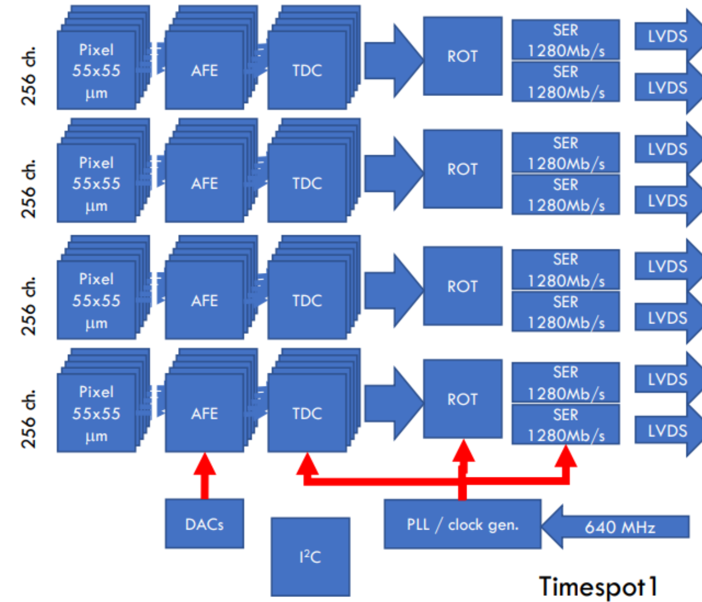
Timing resolution: 30ps

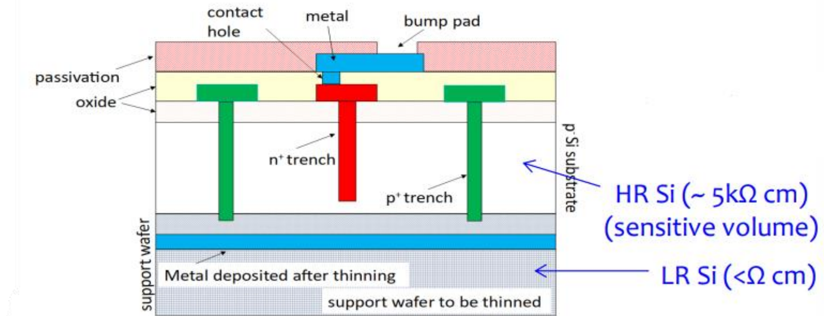
ETROC -> similar for CMS

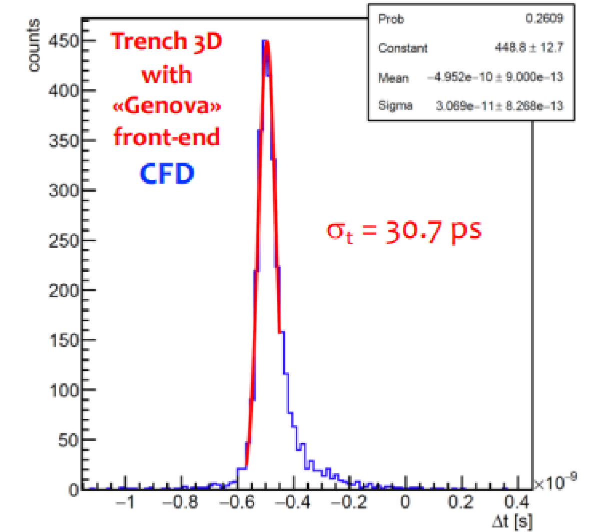
TimeSpot

MIP in 3D-Si

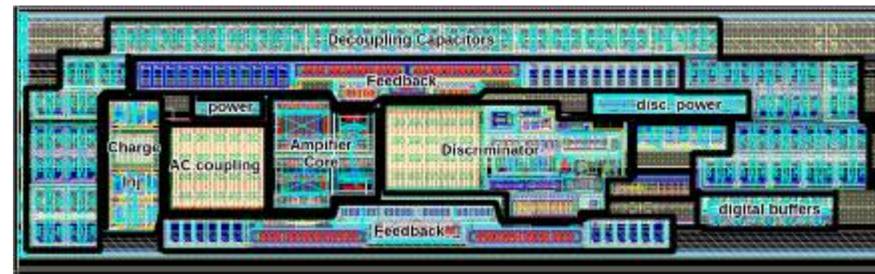








Analog pixel: 15x50µm^2



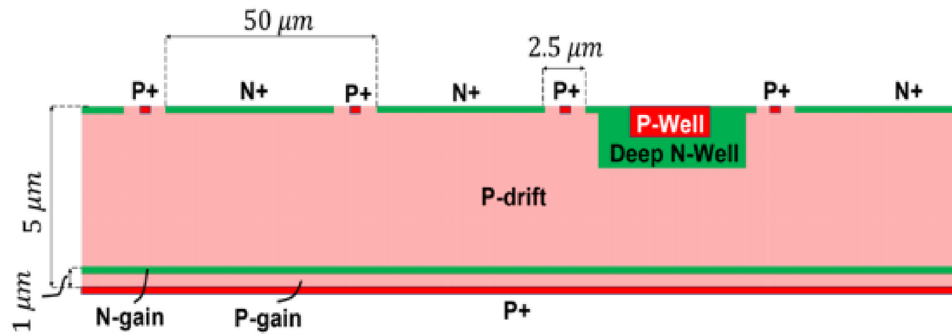
Technology: 28nm
Pixel size: 55x55 µm^2
Space resolution: ~10 µm
Time resolution: ≤ 50 ps per pixel
Sensors: Planar, 3D, LGAD

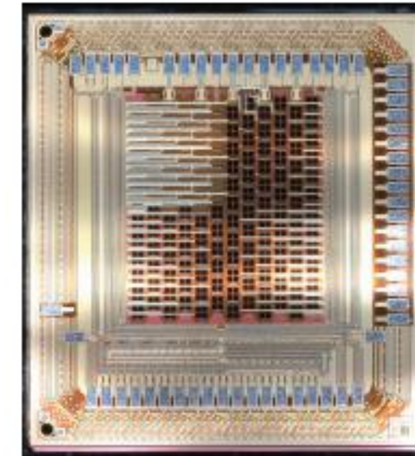
S. Cadeddu, Trento 2021

A. Lai, Hiroshima 2019

MonPicoAD/MONOLITH

SiGe BiCMOS





	MonPicoAD	Monolithic [2]	LGAD
Time resolution	**< 5 ps**	46 ps	30 ps
Internal Gain	**50-100**	-	50
Pixel size	**100×100 μm²**	100×100 μm²	1 mm²
Technology	**BiCMOS**	BiCMOS	CMOS

Monolithic + APD/LGAD more to come ;-)

M. Munker, PSD 2021

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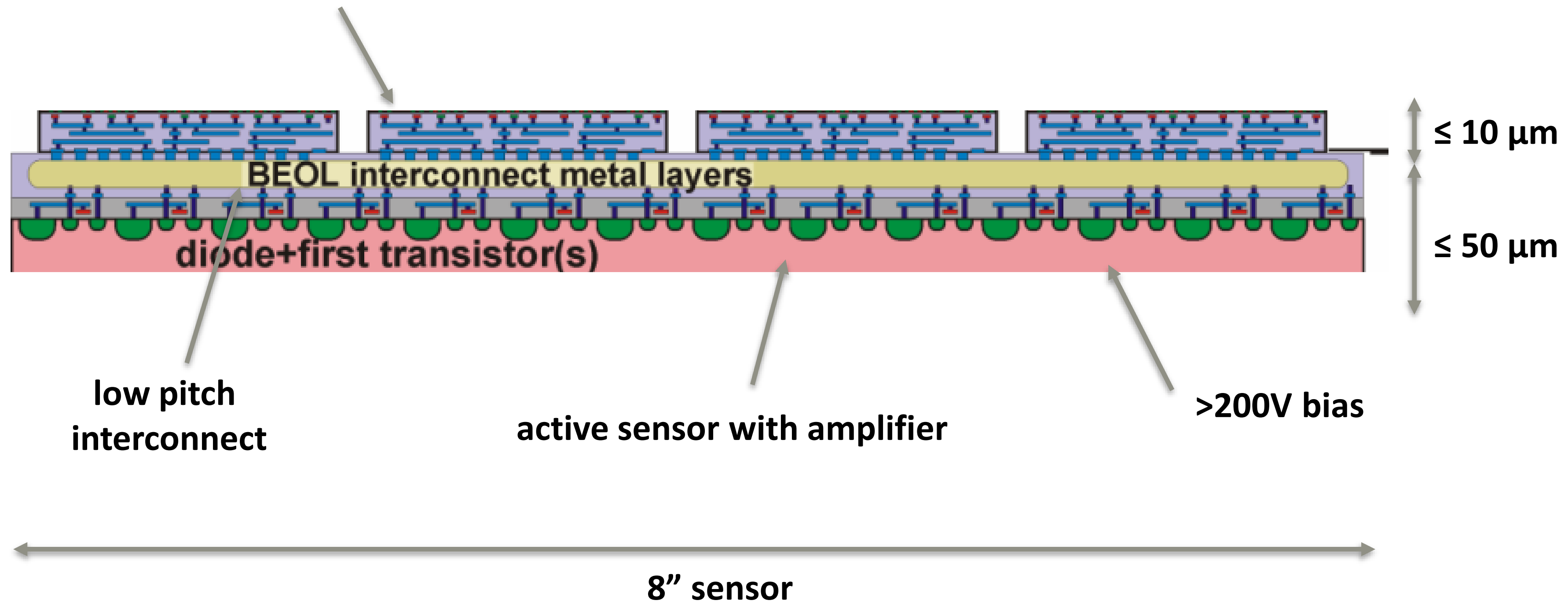
Future?



Conclusions

- Move to 28nm technology
- Data processing (FPGA?) part of readout chip
- Wafer level bonding is being investigated (8” sensors)
- Monolithic (DMAPS/HVMAPS) see adaption in experiments
- Monolithic 65nm technology prototyping
- Monolithic timing detectors development is ongoing
- Small pixel timing detectors are being build