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Overview of the latest developments in HV-CMOS detectors for particle physics

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Due to their capability to cope with very high rates in very harsh radiation environments, hybrid silicon detectors have been the preferred option to track particles in high energy physics experiments. However, their large material thickness, together with their laborious and expensive assembly process, have motivated the pursuit of a new generation of thin and cost-efficient position sensitive detectors. The industry standard High Voltage-CMOS (HV-CMOS) technology has emerged as a very attractive solution. Tracker detectors in HV-CMOS technologies merge on the same substrate the sensing diode, biased at a high voltage to create a large depleted volume for fast charge collection by drift and high radiation tolerance, and a high integration density of low-voltage CMOS readout electronics which can be embedded inside the collecting electrode. Novel developments have shown the feasibility of fully monolithic HV-CMOS detectors, which integrate analogue and digital front-end electronics on the same sensor chip, removing the need for bump bonded or glued readout ASICs.

In this talk, I will give an overview of the latest activities in HV-CMOS detectors developed by an international collaboration, in which the Liverpool group contributes to both the design and evaluation of the prototype sensors. I will review the design details of recent submissions, which include demonstrator size and small size prototypes in ams and LFoundry aimed at the ATLAS ITk upgrade and the Mu3e experiment. I will also report on recent electrical tests and measurements from monolithic matrices and test structures on these prototypes with radioactive sources and lasers. Finally, I will provide details of a planned R&D submission within the CERN/RD50 collaboration (an international project to develop radiation hard semiconductor devices for very high luminosity colliders), which aims at improving the timing resolution of HV-CMOS sensors with different solutions implemented at the readout circuit level.

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