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A new strips tracker for the upgraded ATLAS ITk detector

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The inner detector of the present ATLAS detector has been designed and developed to function in the environment of the present Large Hadron Collider (LHC). At the next-generation tracking detector proposed for the High Luminosity LHC (HL-LHC), the so-called ATLAS Phase-II Upgrade, the particle densities and radiation levels will be higher by as much as a factor of ten. The new detectors must be faster, they need to be more highly segmented, and covering more area. They also need to be more resistant to radiation, and they require much greater power delivery to the front-end systems. At the same time, they cannot introduce excess material which could undermine performance. For those reasons, the inner tracker of the ATLAS detector must be redesigned and rebuilt completely.

The design of the ATLAS Upgrade inner tracker (ITk) has already been defined. It consists of several layers of silicon particle detectors. The innermost layers will be composed of silicon pixel sensors, and the outer layers will consist of silicon microstrip sensors. This contribution focuses on the strip region of the ITk. The central part of the strips tracker (the “barrel”) will be composed of rectangular “short” (~ 2.5 cm) and “long” (~ 5 cm) strip sensors. The forward regions of the strips tracker (the “endcaps”) consist of 6 disks per side, with trapezoidal shaped microstrip sensors of various lengths and strip pitches. In response to the needs of the strip region for the ITk, highly modular structures are being studied and developed, called “staves” for the central region (barrel) and “petals” for the forward regions (end-caps). These structures integrate large numbers of sensors and readout electronics, with precision light weight mechanical elements and cooling structures. The silicon sensors are

fabricated in n-in-p float zone (FZ) technology. Low mass kapton-based circuit boards (the “hybrids”) are directly glued on top of the sensors, hosting the so-called ABCN130 binary readout ASICs. Those ASICs are fabricated in a 130 nm CMOS process. The ASICs are connected to the microstrips via wirebonds. There are 256 channels per ABCN130. Those silicon “modules” are then directly glued onto low-mass, carbon fiber-based stave and petal core structures, with embedded titanium cooling pipes and data and power rails. A data concentrator board on each stave and petal side (the “end of structure” board, EoS) sends all the multiplexed data to the outside world via optical links, and host most of the components of the Detector Control System (DCS). The staves and petals are then

arranged into cylinders and disks, respectively, by means of the integration and global structures. The service module elements, part of the global structure, provide data, power, and cooling to groups of petals and staves. In the baseline design, each of the service modules provides services to 8 staves/petals.

A strong prototyping effort has been put in place over the course of the last years in order to optimize the stave and petal structures. This contribution summarizes the R&D activities performed by the numerous institutes within the Strips ITk collaboration that culminated recently in the release of the ATLAS Strips ITk Technical Design Report (TDR).

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