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Minimizing guard ring dead space in the Si detector with n-guard ring at the edge of the detector

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Detectors for n-type silicon with an n+ -type guard ring have been investigated. The Si detectors in high-energy physics experiments require a reliable performance in irradiation conditions. Minimizing dead wafer space is an additional advantage as it enhances the efficiency of a detector [1]. The guard ring technique has evolved to minimize this dead space at the edge of the detector. Also the guard ring structure is used for improving the breakdown performance of the Si detectors.

In the present work, the new p+ / n / n+ detector structure with n+ guard ring is described. The guard ring is placed at the edge of the detector and the distance from p+ anode to the back edge of the guard ring is 300 μm, which is also the wafer thickness. The depth of the junction and the guard ring is 3 μm. Also the width of the guard ring is 3 μm.

The detector depletes also sideways, so the signal can be collected very close to the n-guard ring. In this kind of structure, the dead space of the detector is minimized and we have dead space only below the guard ring. This is proved by simulations done by Silvaco / ATLAS software.

References
[1] –K. Ranjan et al., Solid-State Electronics 48 (2004) 1587-1595
[2] –N. Egorov et al., Nuclear Instruments and Methods in Physics Research A 426 (1999) 197-205

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