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P-spray implant optimization for the fabrication of n-in-p

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One of the technological challenges of the fabrication of n-in-p and n-in-n microstrip silicon detectors is to obtain a good insulation of the n-strips while ensuring a satisfactory electrical performance of the devices. A common practice to avoid the formation of the conductive electron layer at the oxide-silicon interface is the definition of p-type zones (”p-stops”) that surround the n-strips, but it has the drawback of adding a mask level to the fabrication process that increases its complexity. Furthermore, the high electric fields present at the edge of the p-stops have been shown to induce pre-breakdown micro-discharges. Another solution consists on performing a uniform p-implant (”p-spray”) in the silicon surface, but it has to be carefully calibrated in order to ensure the strip isolation and avoid early breakdowns.

In this work we present an optimization study of the p-spray profile on n-in-p microstrip silicon detectors. A thorough simulation process, consisting on technological and electrical simulations, was carried out. The best technological options were chosen for the fabrication of miniature n-in-p microstrip detectors on high resistivity FZ wafers. A detailed analysis of the impact of the p-spray characteristics on the performance of the different fabricated devices will be presented.

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