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A Radiation Detector Design Mitigating Problems Related to Sawed Edges

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In pixelated silicon radiation detectors that are utilized for the detection of UV, visible, and Near Infra-Red (NIR) light it is desirable to utilize a relatively thick fully depleted Back-Side Illuminated (BSI) detector design. The benefit of the BSI configuration is that structures on the front side like metal wirings do not stand in the way of light enabling thus 100 % Fill Factor (FF). The advantages of the fully depleted configuration are considerably reduced Cross-Talk (CT) due to lack of diffusion and improved Quantum Efficiency (QE) due to lack of recombination.

Thicker fully depleted detectors have better QE for NIR light but the disadvantages are that more dark current is generated in the depleted bulk (which can be, however, mitigated by cooling), that a bigger bias is required at a conductive backside layer in order to fully deplete the bulk, and that the CT is larger, especially at the boundary of the pixel matrix. Thus there is an optimal detector thickness depending mainly on the optics, the magnitude of the bias on the conductive backside layer, and the pixel size.

In case thinner than 300 um thick detectors are required it is more or less mandatory to thin the detector wafer from the backside after the front side of the detector has been processed and before the conductive layer is formed on the backside. One option is to bond the front side of the detector wafer to a support wafer. The problem is, however, that it is not trivial to reach the contact pads located on the front side of the detector wafer especially if the detector is thicker than 40 um. This problem can be avoided in TAIKO thinning process since no support wafer is required but the detector thickness must be at least 40 um. The TAIKO process has, however, the problem that lithographic steps cannot be performed on the backside of the detector wafer. This means that the conductive backside layer must be homogenous throughout the wafer and that the contact to the conducting backside layer should be placed on the front side of the detector.

In order to provide good QE for blue and UV light the conductive backside layer should be as thin as possible and it should be of opposite doping type than the substrate (an inversion layer is not an option due to the relatively thick fully depleted substrate). Beside the use of TAIKO process it is hereby assumed that the detector chips are separated from the wafer by sawing which is a standard procedure in chip manufacturing. The problem with afore described arrangement is that it is difficult to bias the conductive backside layer from the front side. Another typical problem is that a lot of leakage current is generated at the sawed chip edge, which increases the power consumption.

In this paper a sawed TAIKO detector chip arrangement is presented comprising fully depleted BSI configuration, thickness between 40 and 300 um, low power consumption, as well as good QE for UV, visible, and NIR light.

Key words: detector chip design, process simulation, device simulation, fully depleted, back-side illuminated, high quantum efficiency, low crosstalk, low power consumption.

Authors: Mr AUROLA, Artto (Pixpolar Oy / Lappeenranta Univ. of Technology (FI)); Mr MAROCHKIN, Vladislav (Pixpolar Oy / Lappeenranta Univ. of Technology (FI))

Co-author: TUUVA, Tuure (Lappeenranta Univ. of Technology (FI))

Presenter: Mr AUROLA, Artto (Pixpolar Oy / Lappeenranta Univ. of Technology (FI))

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