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HEXITEC ASIC - a Pixellated Readout Chip for CZT Detectors

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HEXITEC is a collaborative project with the aim of developing a new range of detectors for high energy Xray imaging. High energy X-ray imaging has major advantages over current lower energy imaging for the life and physical sciences including improved phase contrast images on larger, higher density samples and with lower accumulated doses. However, at these energies conventional silicon based devices cannot be used, hence the requirement for a new range of high Z detector materials. Underpinning the HEXITEC programme are the development of a pixellated Cadmium Zinc Telluride (CZT) detectors, and a pixellated readout ASIC which will be bump-bonded to the detector. The HEXITEC ASIC is required to have low noise (20 electrons rms) and tolerate detector leakage currents. A prototype 20x20 pixel ASIC has been developed and is being manufactured. A description will be given of the design of the ASIC together with initial test results.

Author: JONES, Lawrence (STFC Rutherford Appleton Laboratory)
Presenter: JONES, Lawrence (STFC Rutherford Appleton Laboratory)
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