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A 4096-pixel MAPS device with on-chip data sparsification

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A prototype of a mixed-mode ASIC built up of a fast readout architecture that interfaces with a matrix of 4096 Monolithic Active Pixel Sensor (MAPS), via STM 130nm CMOS technology, was fabricated. Square groups of 16 pixels form a macro-pixel (MP). Each MP can be latched via single pixels (50 by 50 micron) and a time-stamp is associated with the frozen condition. The readout architecture is parallel and could overcome the readout speed limit of big matrixes. As the output port can only accept one-hit information at a time, an internal queuing system has been provided to face local high hit-rates. The ASIC can be connected to an actual full-custom matrix of MAPS or to a digital matrix emulator composed of standard cells, for testing facilities. For both operating modes a slow-control phase is required to load the chip configuration via mask bits to select which MPs are to be read and which are not, for example in case they are too noisy or burned up. Previous versions of similar ASICs were designed and properly tested. The work is aimed at improving the design of MAPS detector with an on-chip fast sparsification system, for particle tracking, to match the requirements of future high-energy physics experiments. The readout architecture implemented is data driven extending the flexibility of the system to be also used in first level triggers on tracks in vertex detectors. Preliminary simulations and tests prove that the readout system can cope with an average hit rate up to 100 MHz/cm2 if a master clock of 80 MHz is used, while maintaining an overall efficiency over 99%.

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