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Monolithic Pixel Sensors in 0.15um Fully Depleted SOI Technology

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A monolithic pixel sensor has been design and fabricated in a novel deep-submicron 0.15 micron Silicon-On-Insulator (SOI) CMOS technology. This combines a thin layer of CMOS electronics isolated from a high-resistivity silicon substrate that can be depleted as in standard reversely-biased silicon detectors. The first prototype chip features arrays of analog and digital pixels of 10 micrometer pitch. Results from extensive testing performed with focused infrared lasers and high-energy particle beams are presented. The radiation hardness of the process has been characterised with low energy protons and neutrons.
The design of a new prototype will be discussed in relation to its potential applications in high-energy physics, electron microscopy and beam monitoring.

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