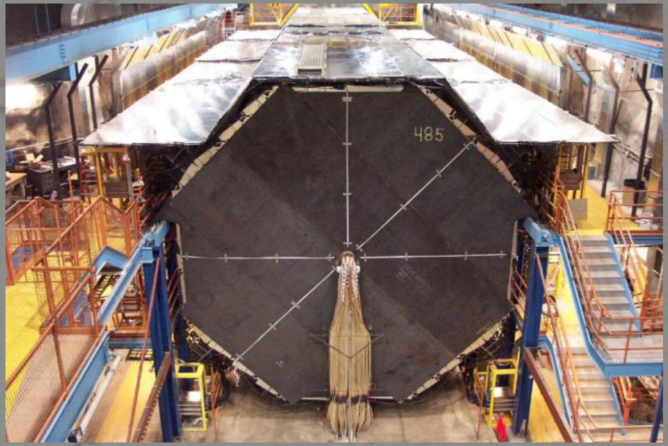
Adaptation of MINOS photomultipliers for low cost, large scale applications in contemporary particle physics experiments

Alex Sells

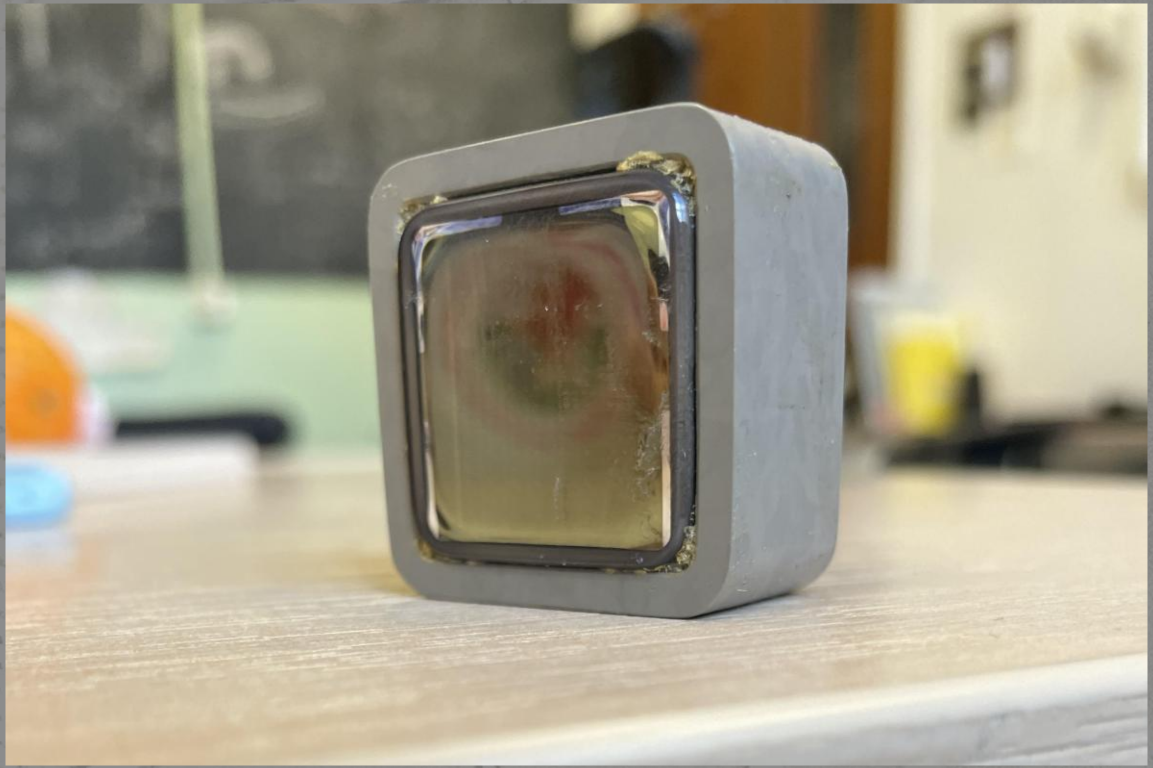
The MINOS experiment

- MINOS: long-baseline experiment measuring ν_μ disappearance from 2005 – 2016
- Detected ν interactions at a near detector close to the NuMI beam, and a far detector 735km away
- Detectors consist of alternating steel and scintillator strip planes, monitored by 1550 'M16' Hamatsu PMTs (Far) and 215 'M64' PMTs (near)
- Many of these are now not in use



Hamamatsu M64

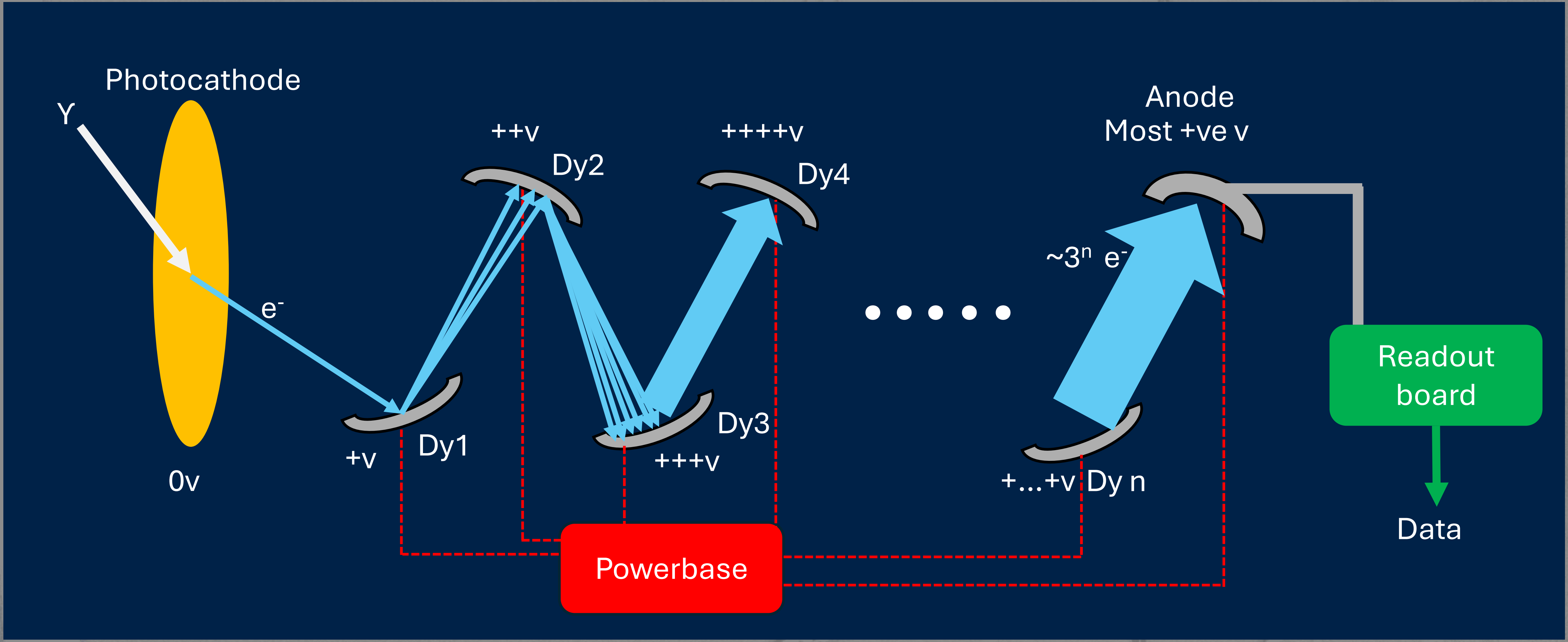
- The Hamamatsu R5900-00-M64 is a 64 anode metal channel dynode photomultiplier (PMT)
- PMTs detect light down to individual photon level
- Photocathode is ~3x3cm
- Operational voltage input is between 800 – 1000V
- Low level light detection (single photon), suitable for variety of different environments



Electronics for modern applications

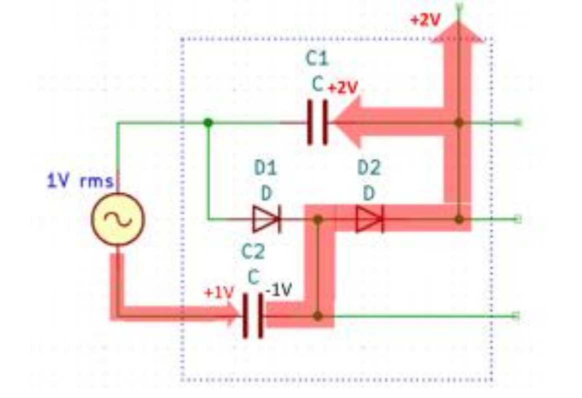
- Modern neutrino experiments are larger, with higher numbers of detector photo-channels
- One potential limiting factor is the HV required to power PMTs
- HV cable, safety infrastructure and generators are expensive, especially distributed over a wide area
- The CHIPS detector, an economical neutrino detector concept, aimed to address this problem in its electronics design

PMT Principles

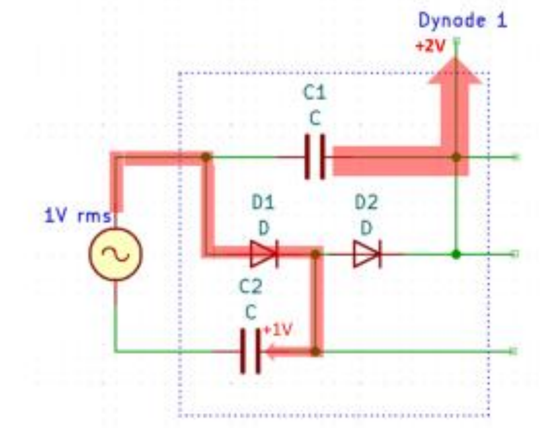


Cockroft Walton Voltage Multiplier

The two phases of a voltage multiplier circuit



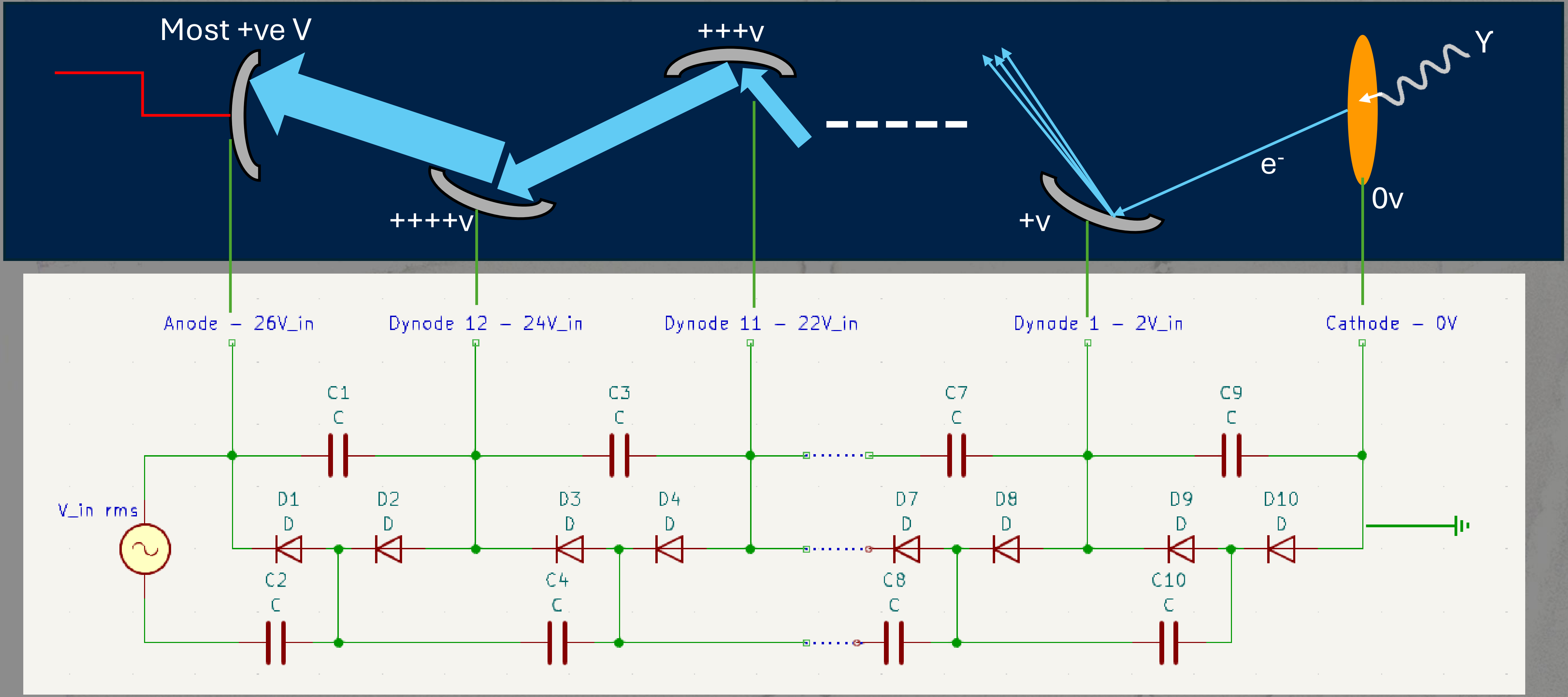
C2 discharges and with the source provides twice the voltage



As C2 recharges, C1 discharges to maintain output

- Series of voltage multiplier stages that each provide a potential difference of twice the AC input
- Output is rectified to DC
- A sequence of stages can produce very high voltage from relatively low input

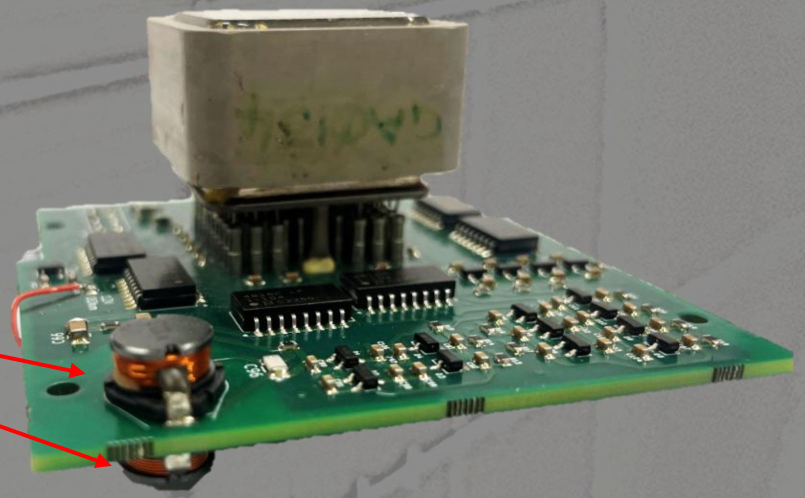
M64 powerbase

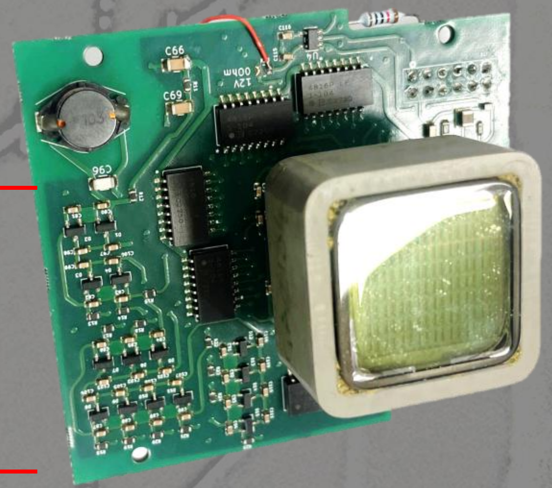


Positive polarity Cockroft Walton PMT powerbase: COUPP experiment; Crisler, M. et al., 2010, October. The Chicagoland Observatory Underground for Particle Physics cosmic ray veto system. In IEEE Nuclear Science Symposuim & Medical Imaging Conference (pp. 808-812). IEEE.

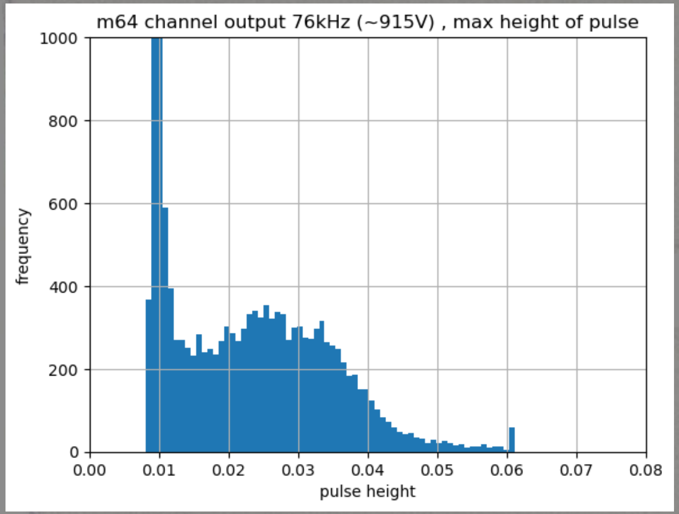
Design of powerbase

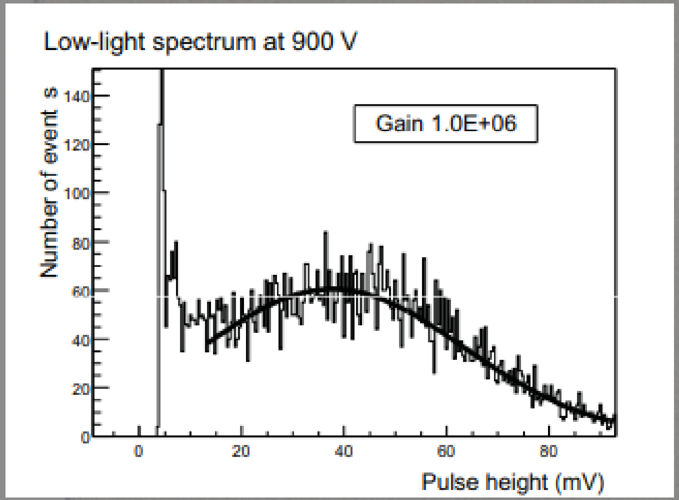
- Standard digital 3.3V PWM signal as input
- 'LC tank' uses the resonance of an inductor and capacitor to shape the input and increase its amplitude
- 15 stage Cockroft Walton Chain connected to the dynodes
- ADC for voltage monitoring connected to an untapped CW stage
- All relatively low cost, commercially available components

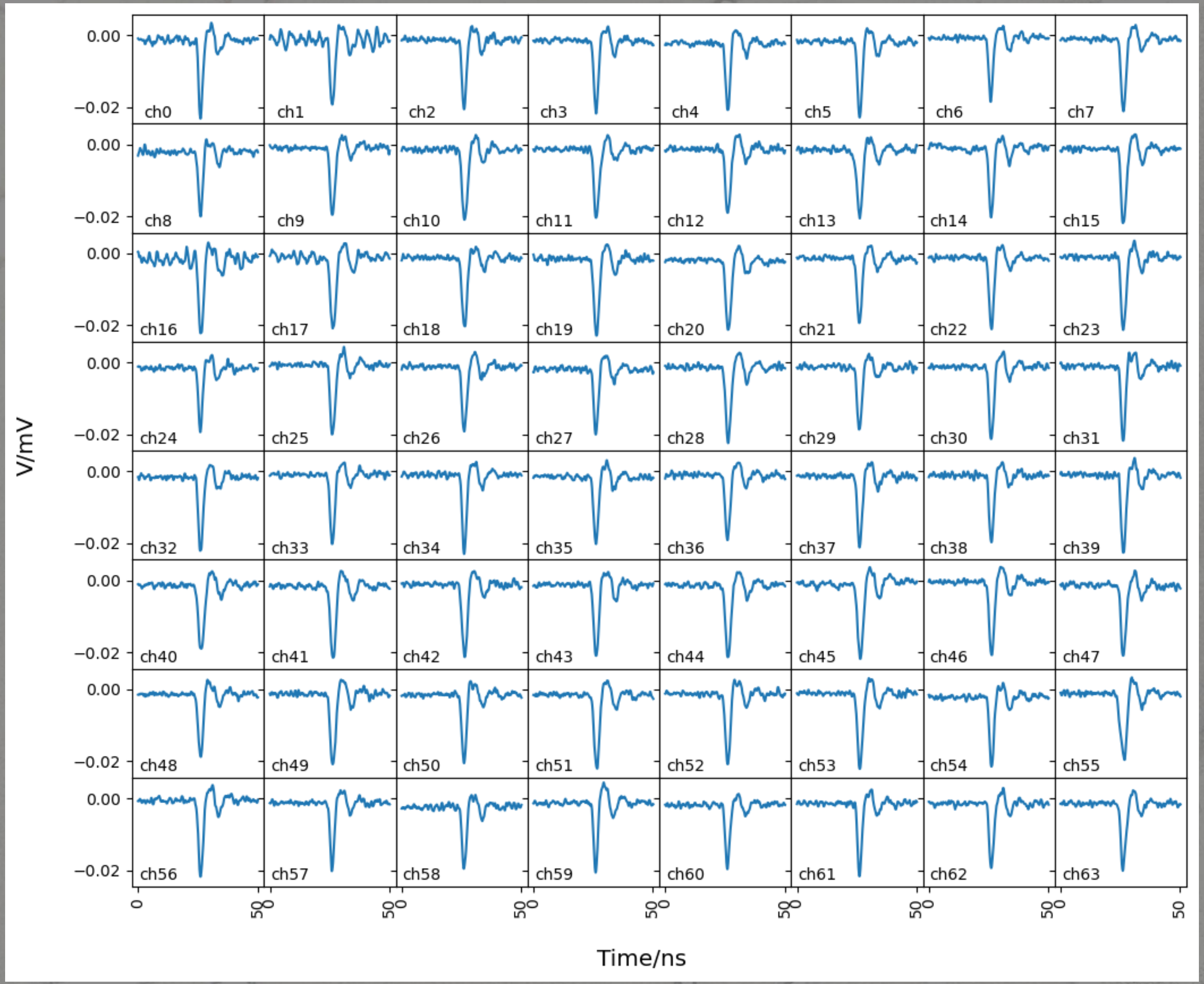




Performance

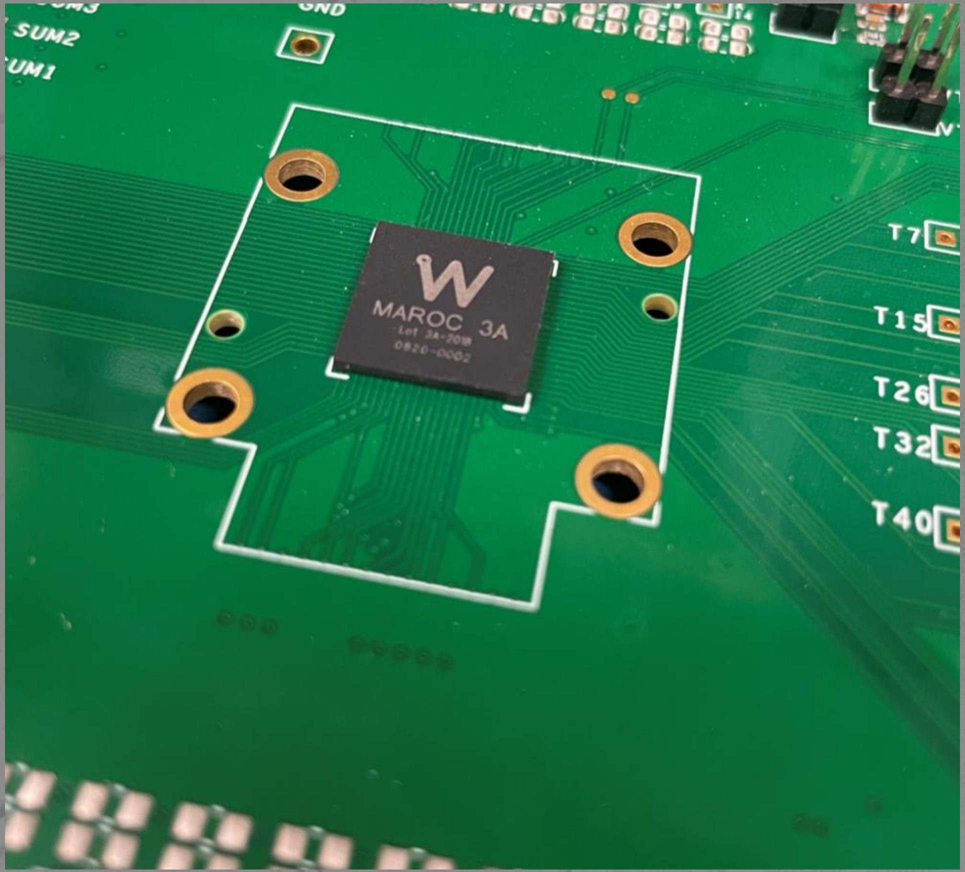






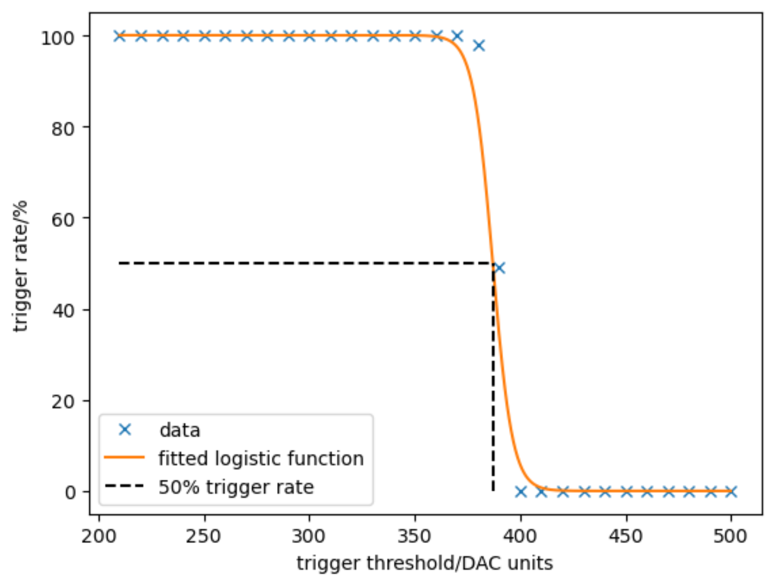
Readout – The MAROC3A

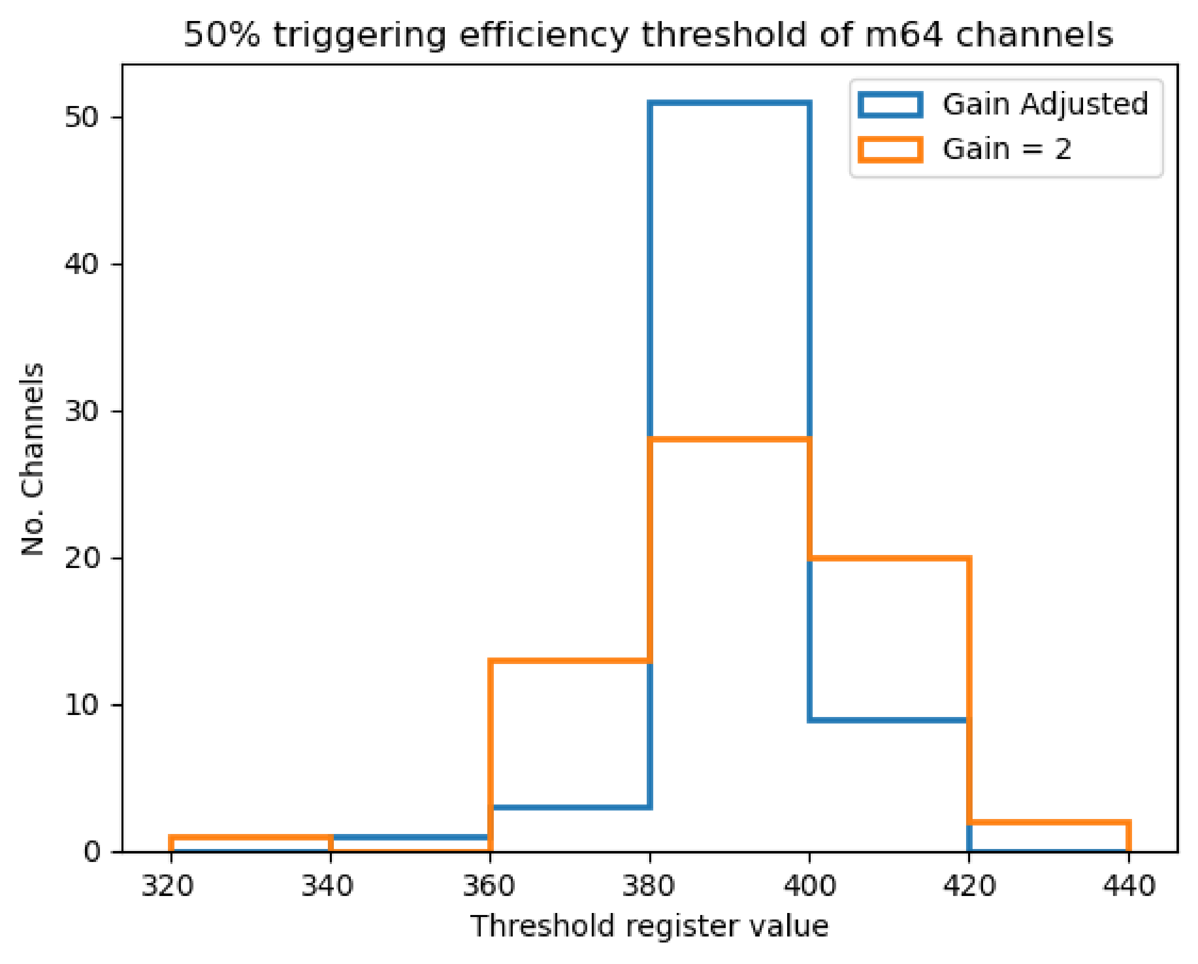
- Version of readout chip designed for ATLAS ‘Roman Pot’ detectors
- Readout chip designed for multi-anode PMTs, with 64 channels ideal for M64
- Provides individual channel gain settings, pulse discrimination, charge measurement – all in one
- Interfaced with FPGA in our design



Status of readout

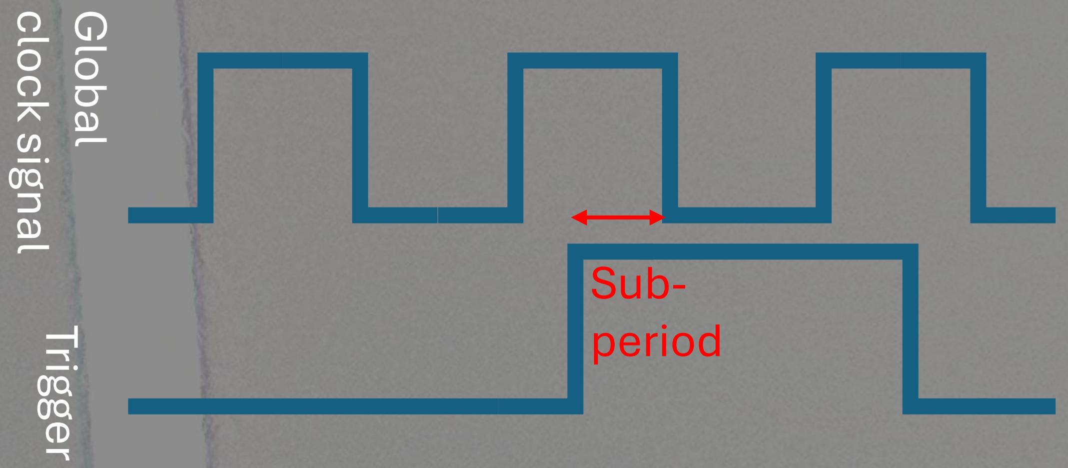
- Gain (amplification) calibration process has been developed to correct the trigger dispersion of the channels

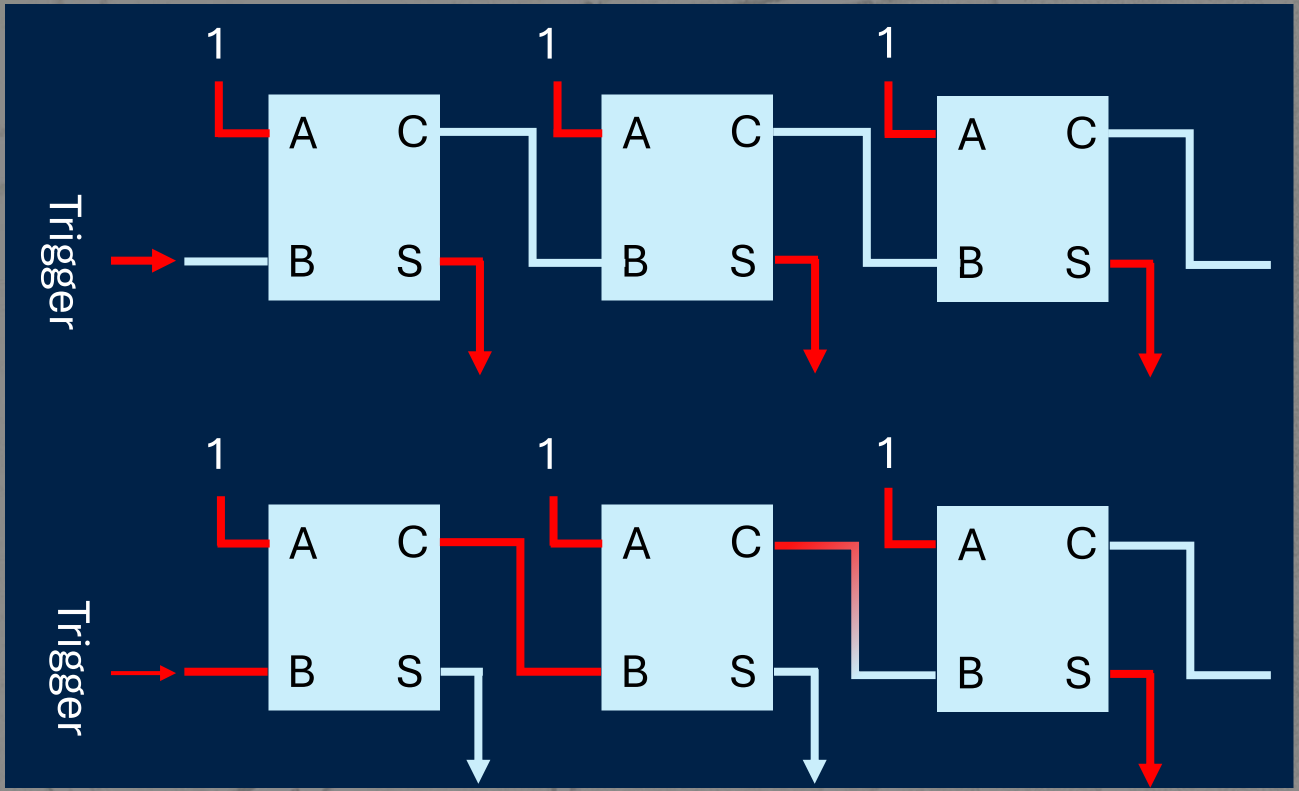




Future plans

- Tapped delay lines in FPGA
- Allow for division of clock period
- Current clock period 5ns, potential for sub-nanosecond time over threshold resolution

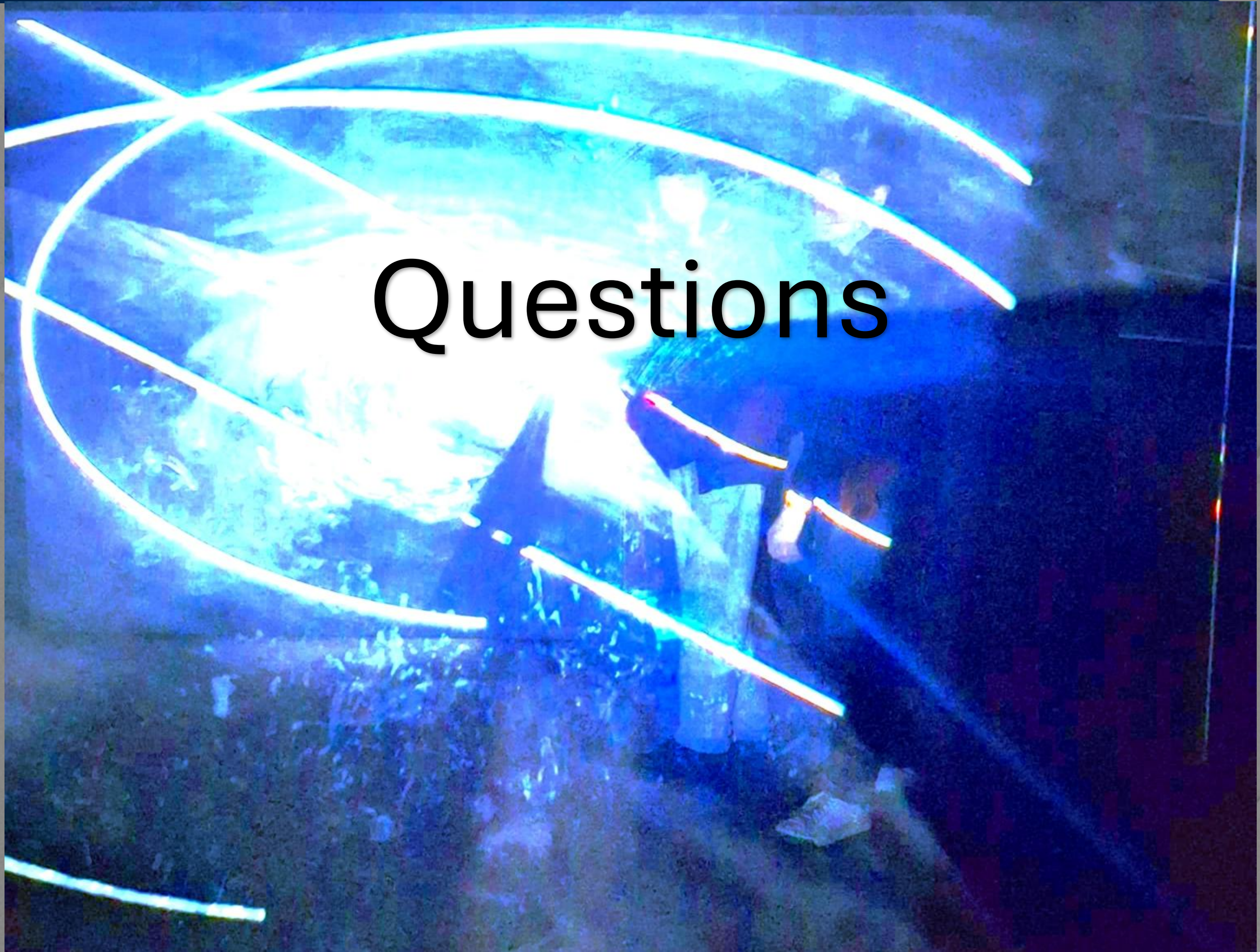




See: Wang, Yonggang, et al. "Performance analysis and IP core implementation of two high performance time-to-digital converters on Xilinx 7-series FPGA." *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1020 (2021): 165866.

Conclusions

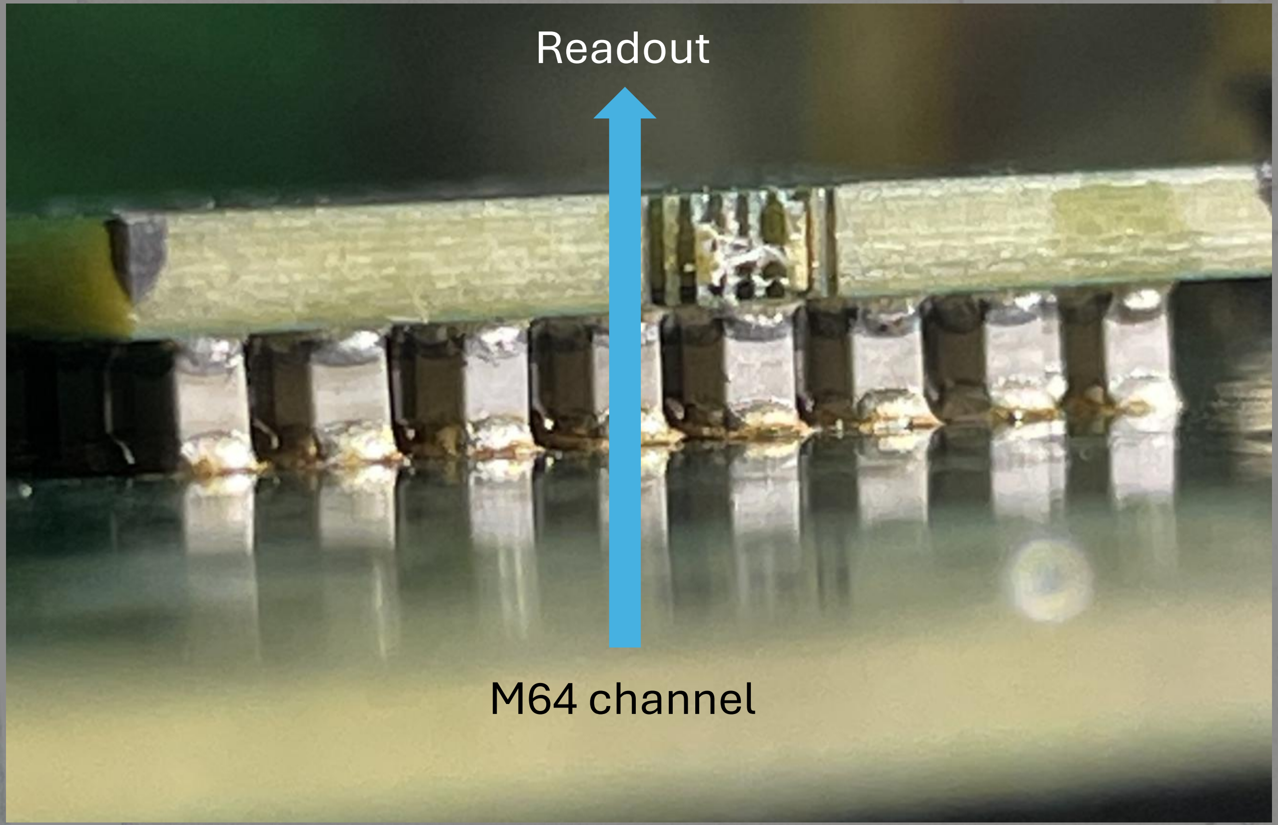
- Successfully built powerbase for Hamamatsu M64 that does not require high voltage
- Assembled at low cost using standard components
- Complimentary readout board being developed using MAROC3A chip
- Time over threshold of sub-nanosecond resolution anticipated

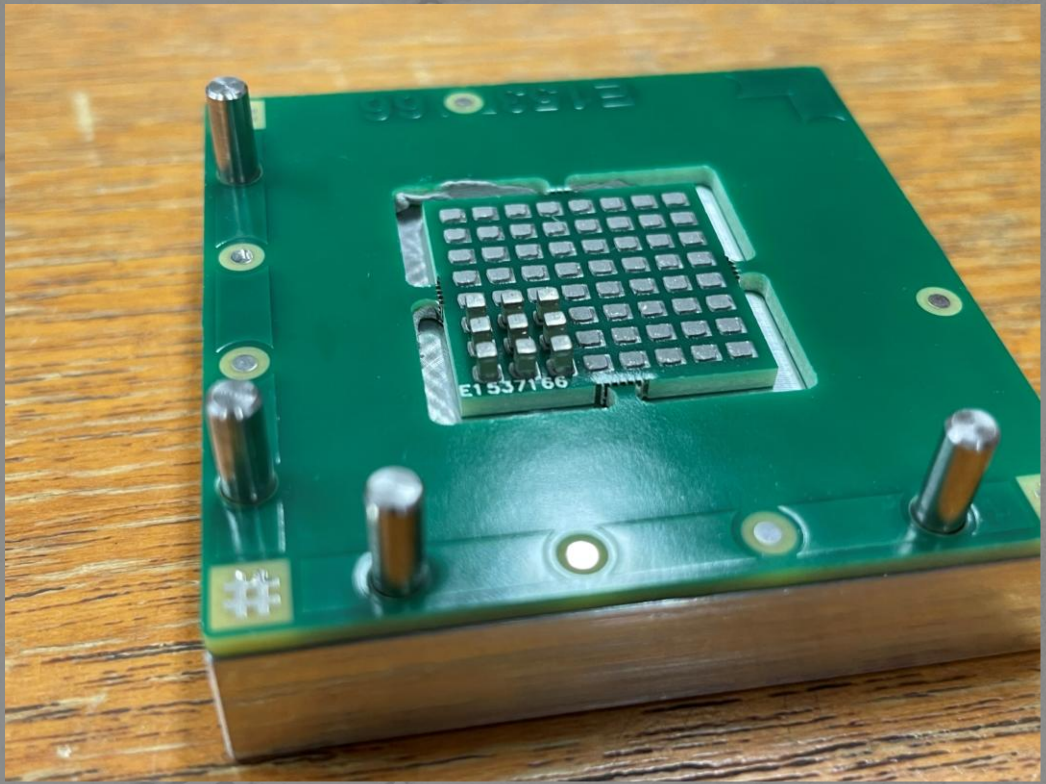


Questions

Backup Slides

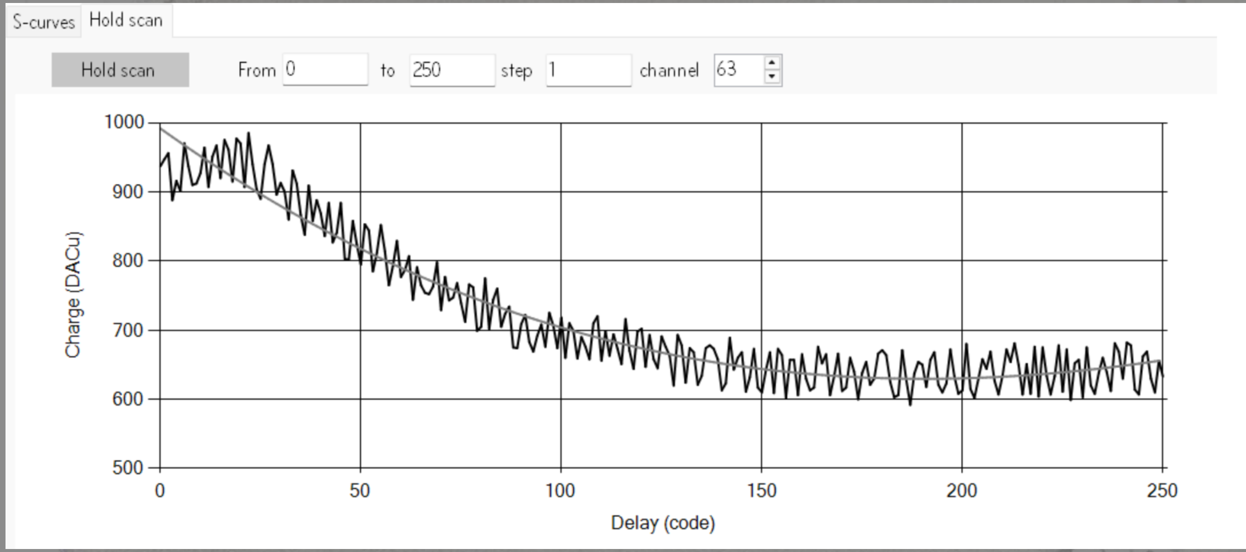
Layout considerations

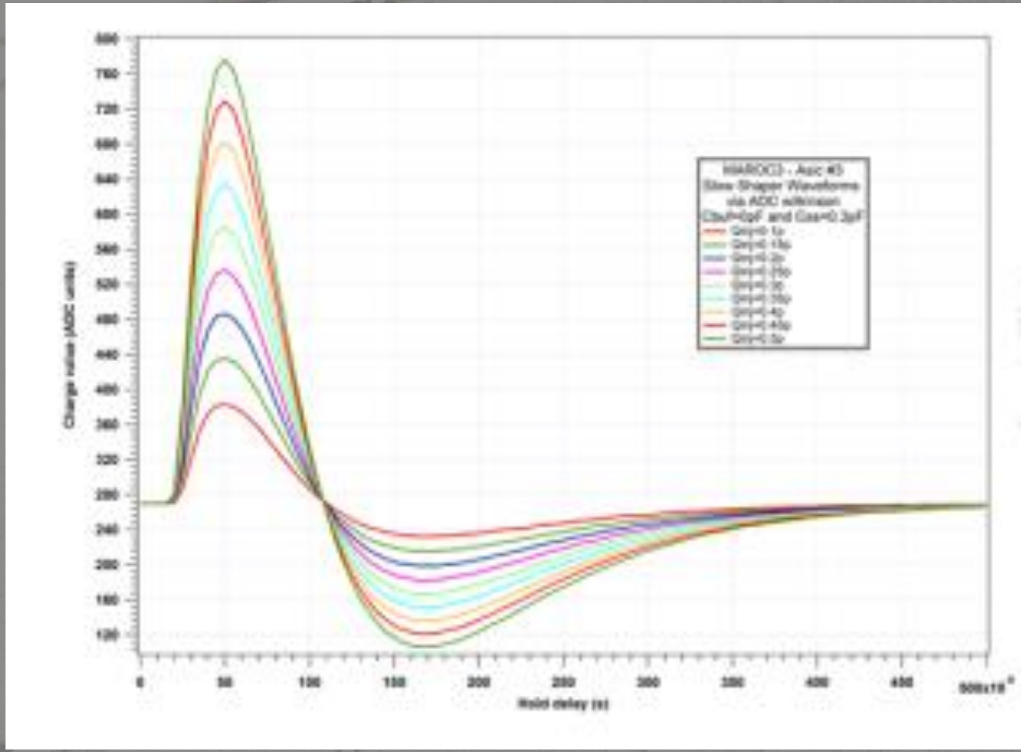




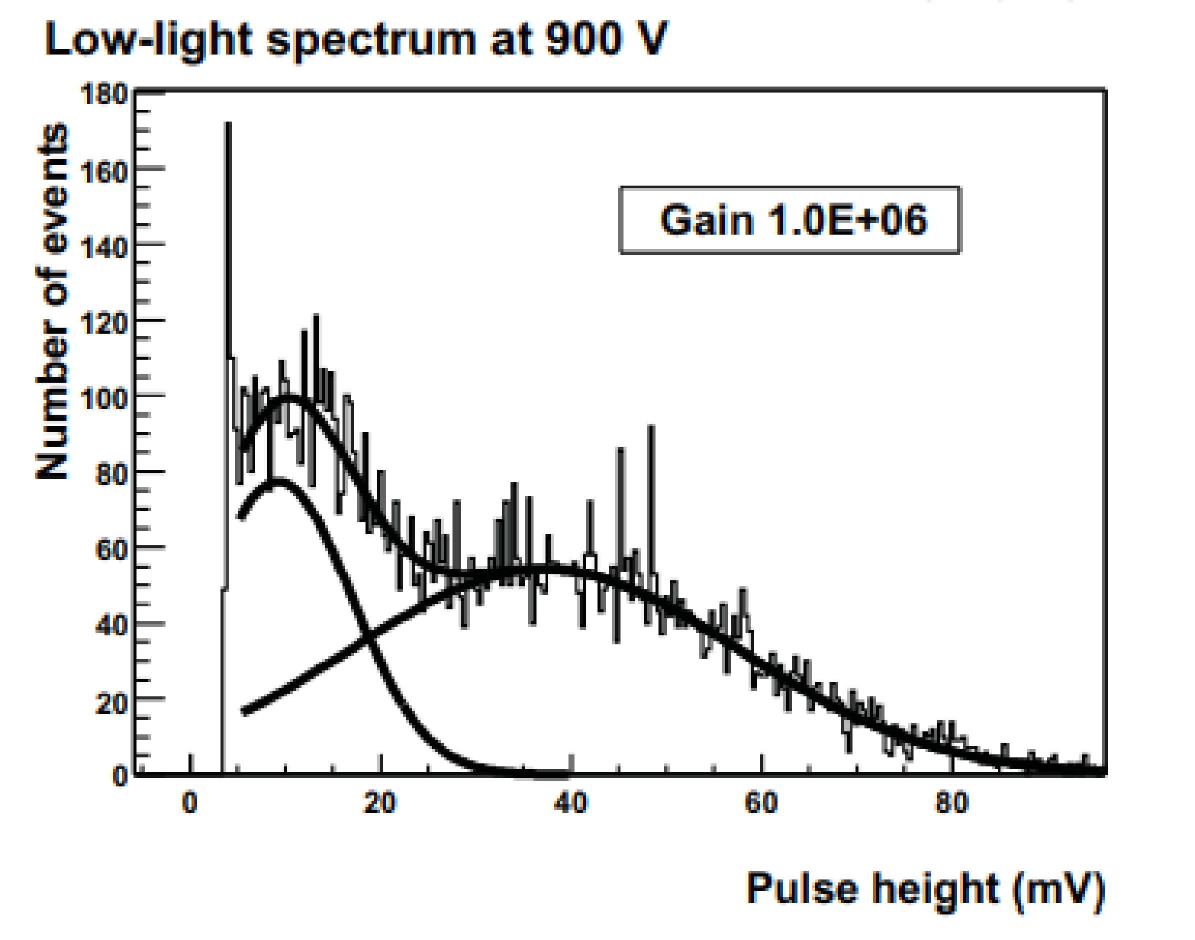
Slow Shaper Waveforms

- Next goal is to calibrate charge ADC readings with known charge inputs
- This requires tuning of Slow Shaper parameters and 'hold' delay



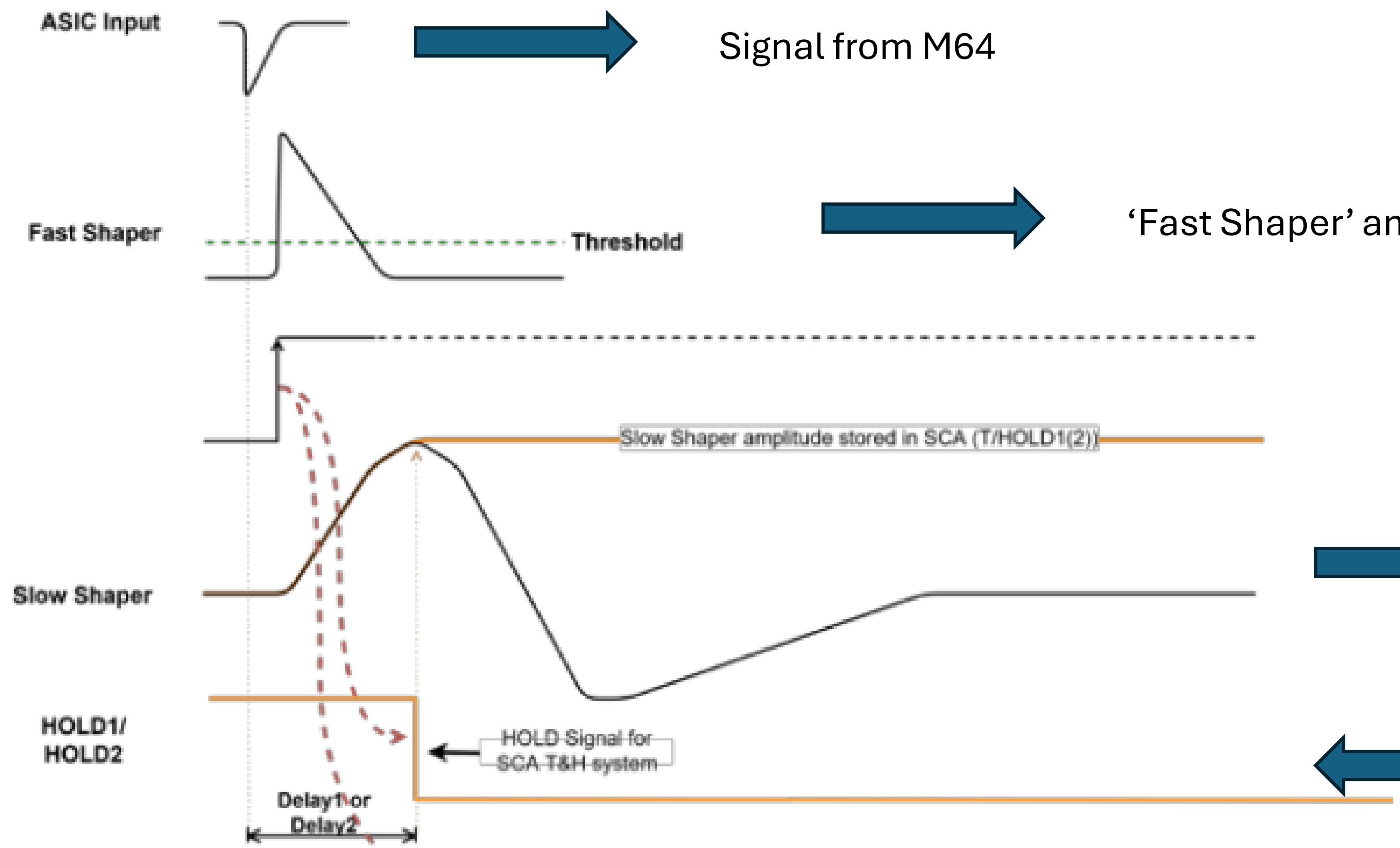


MAROC3 datasheet
(available @ weeroc.com)



Low-light spectrum at 900 V
Gain 1.0E+06
Number of events
Pulse height (mV)
0
20
40
60
80
100
120
140
160
180

Readout Design



Signal from M64

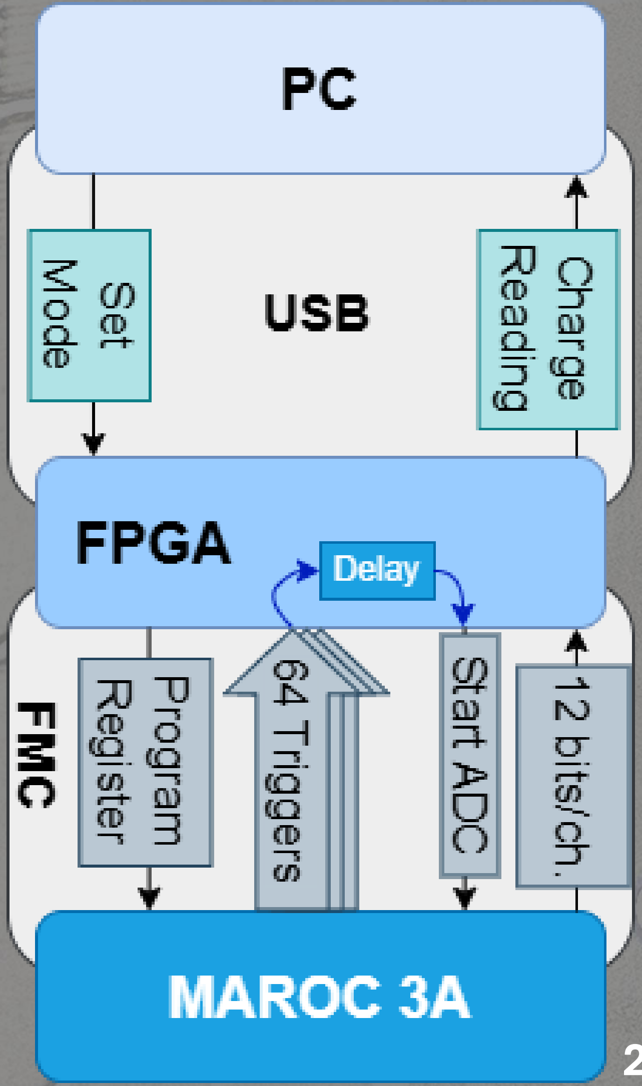
'Fast Shaper' amplified for triggering

Simultaneous 'Slow Shaper' waveform with variable peaking time

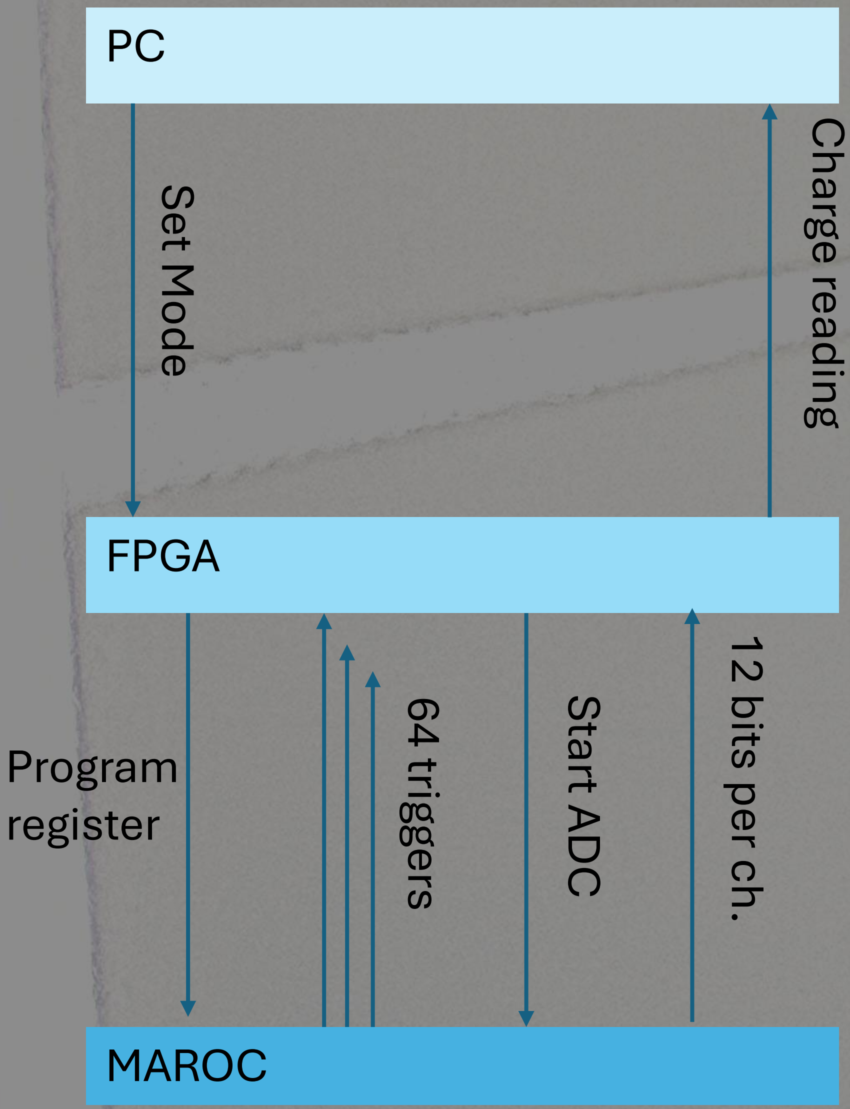
'Hold' signal stores amplitude for ADC after user-defined delay following trigger

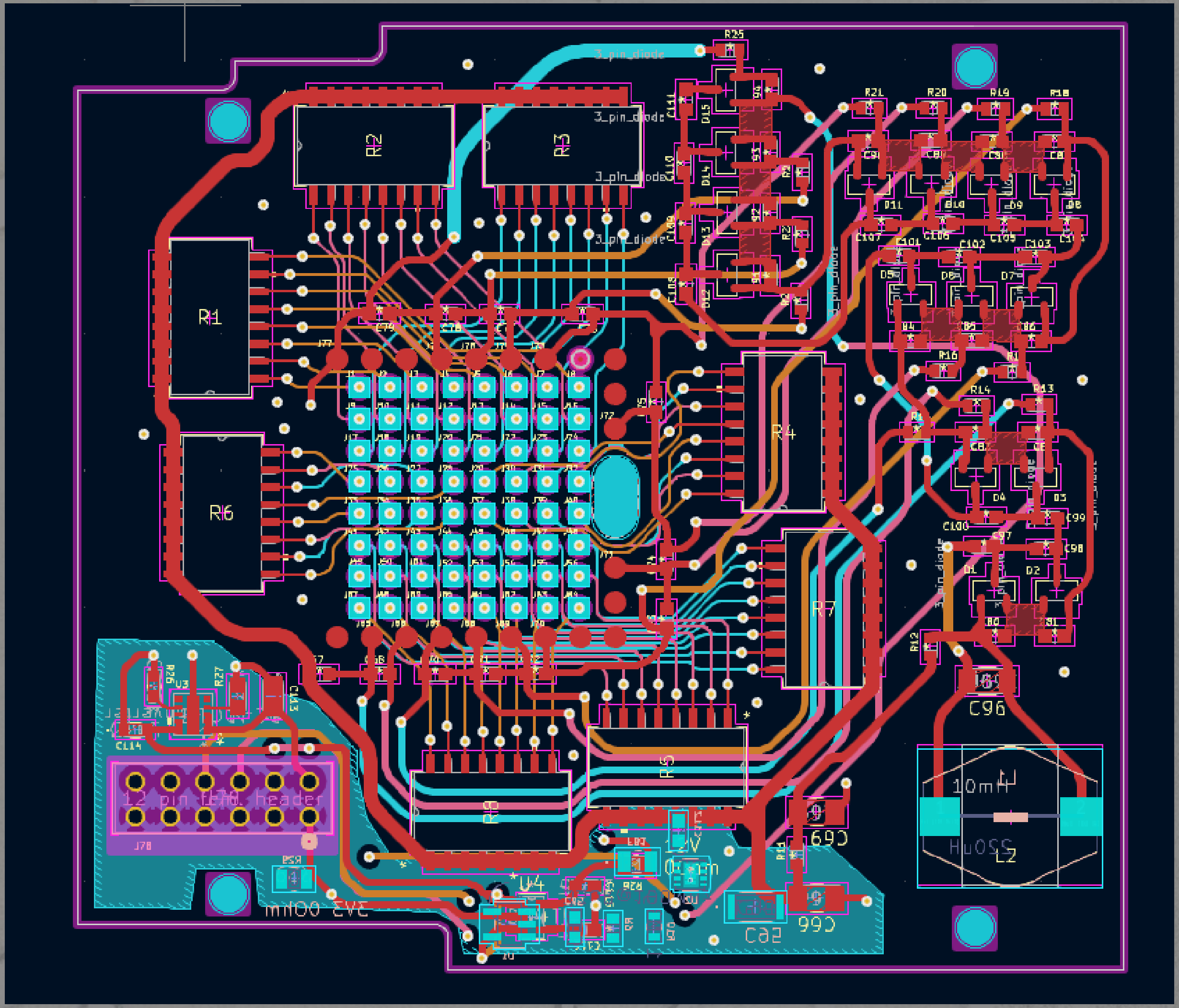
Using the Genesys 2 as an interface

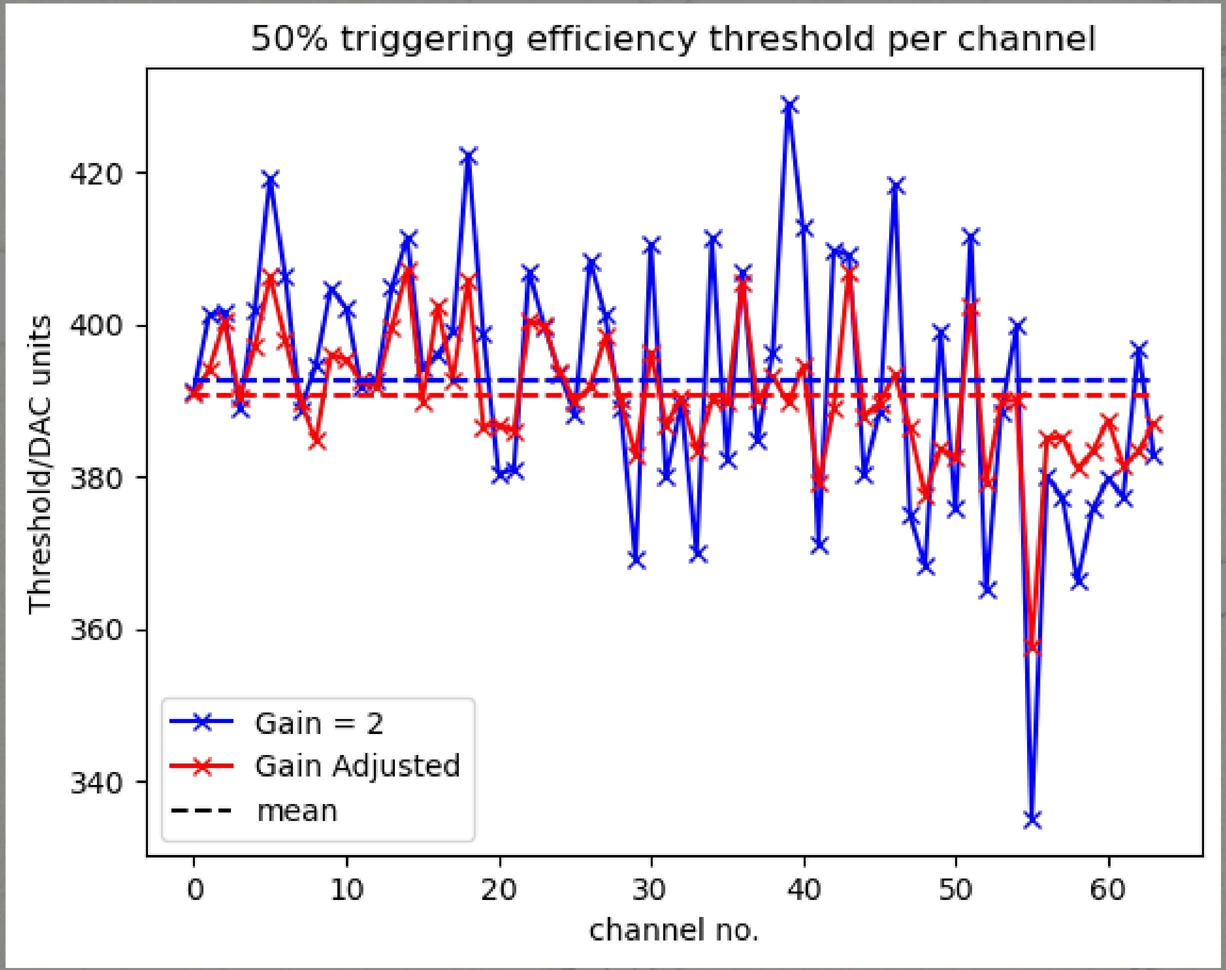
- User interface on computer serially communicates with FPGA to set modes of operation – ‘machine states’
- FPGA programs MAROC with 829 bit register
- MAROC has 64 channel trigger outputs
- FPGA initiates charge measurement process in MAROC based on triggers
- 12 bit ADC measurement for each channel is read by FPGA and transmitted via serial to PC for storage



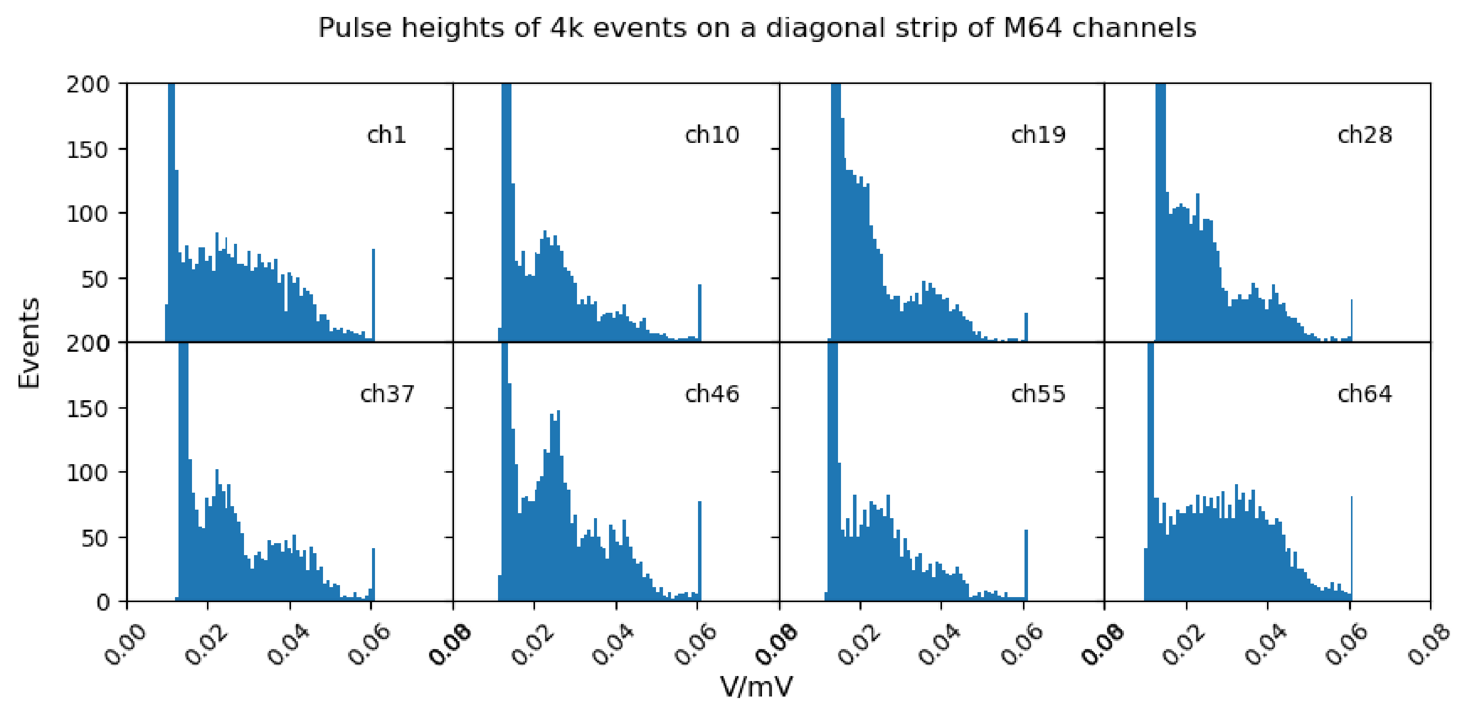
Unused


PC
Set Mode
Charge reading
FPGA
Program register
64 triggers
Start ADC
12 bits per ch.
MAROC





50% triggering efficiency threshold per channel
Threshold/DAC units
420
400
380
360
340
0
10
20
30
40
50
60
channel no.
Gain = 2
Gain Adjusted
mean


Pulse heights of 4k events on a diagonal strip of M64 channels
Events
V/mV
ch1
ch10
ch19
ch28
ch37
ch46
ch55
ch64
200
150
100
50
0
0.00
0.02
0.04
0.06
0.08