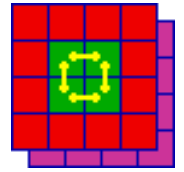




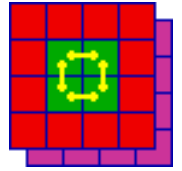
ATLAS Level-1 Calorimeter Trigger (L1Calo)



- Alan Watson
 - Offline software (simulation), UK Project Leadership
- Paul Thompson
 - DCS
- Richard Staley
 - Hardware/firmware development and maintenance
- Sasha Mazurov
 - Offline software (simulation, monitoring, infrastructure)
- Steve Hillier
 - Online software, general trouble-shooter
- Francesco Gonnella
 - Firmware for upgrade
- Juraj Bracinik
 - Online software, calibration
- Current students:
 - Rhys Owen, online software
 - Andrew Foster, calibration
 - James Kendrick, upgrade simulation



Last year in a nutshell

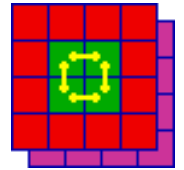


- **Lots of data**

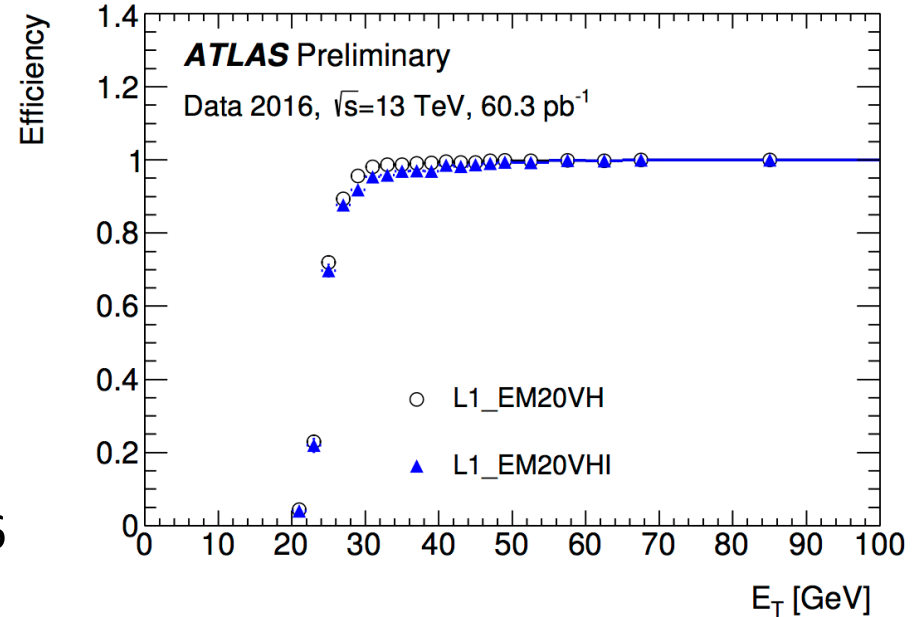
- Bulk of 2015 data ($\sim 4 \text{ fm}^{-1}$) came late in year
 - About 25 fm^{-1} and counting in 2016
 - All of this data taken at 25 ns bunch spacing and high pile-up (up to 40 collisions per bunch on average)
 - LHC finally reached design luminosity
- The high- μ and 25ns environment is challenging
 - But one that L1Calo was well prepared for
 - Nevertheless some teething troubles in 2015
 - Operation in 2016 has been very smooth
 - But requires constant vigilance and occasional interventions



Operation highlights

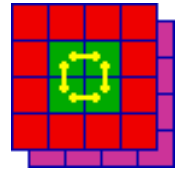


- Electron trigger using isolation
 - LS1 development by Richard et al
 - Studied by Rhys and others
 - Finally used seriously in 2016
- MET threshold maintained in 2016
 - Despite far harsher conditions
 - Similar or lower than end of Run 1
 - (ATLAS MET currently more HLT than Level-1 limited)
 - Birmingham contributed to ideas and performance studies for MET improvements

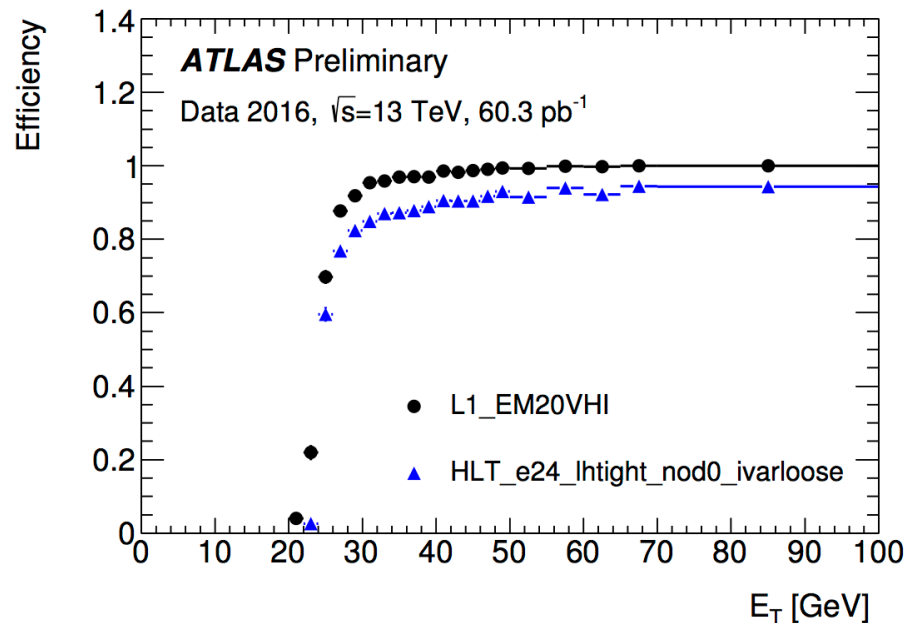
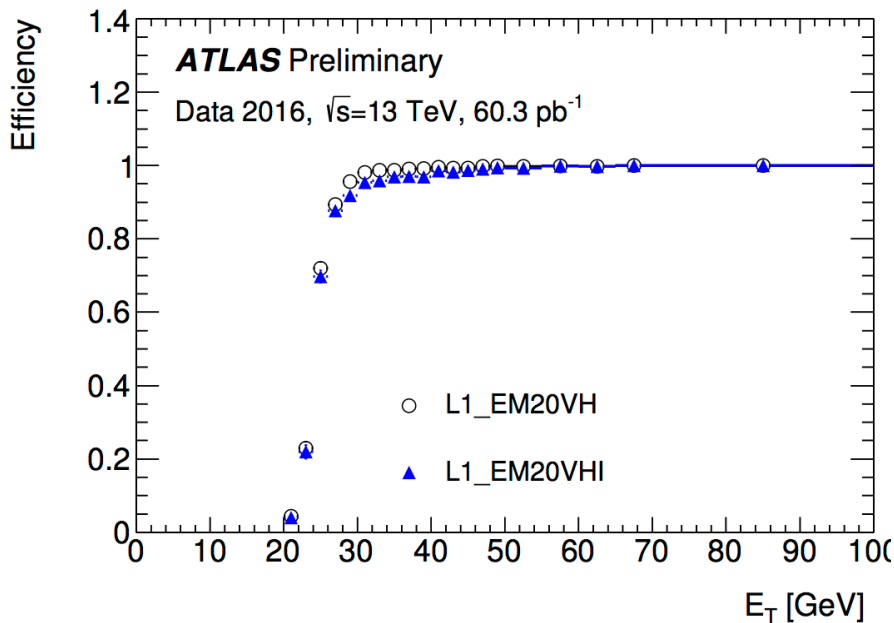




Electron isolation, Level-1 and HLT

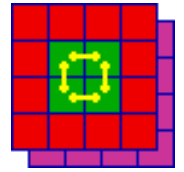


- At Level-1, about 2% loss in efficiency
 - In electron p_t range 20-50 GeV
 - Rate reduction close to factor of two
 - Nevertheless, electron trigger takes $\sim 20\%$ of Level-1 bandwidth
 - Hence the need to upgrade

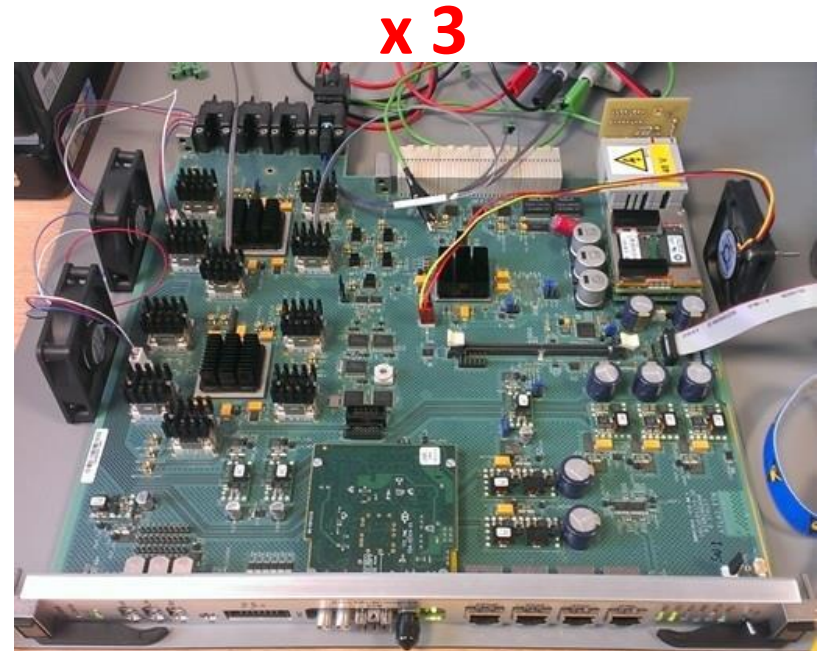
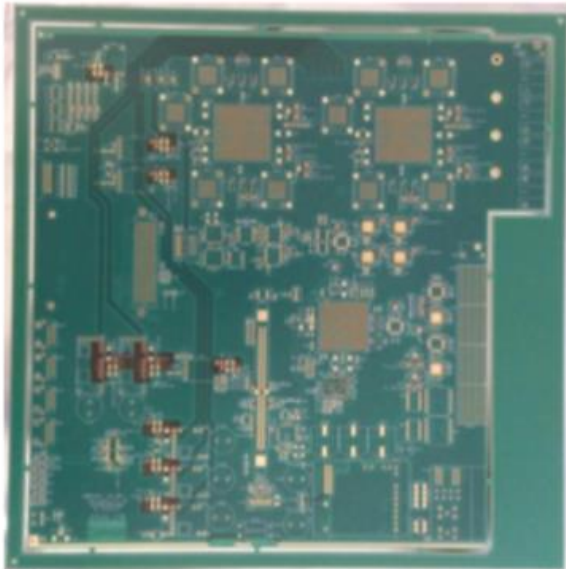




Phase-1 Upgrade: eFEX and FTM

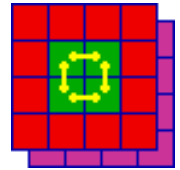


- Current electron/gamma processors to be replaced by new eFEX
 - Hardware design RAL, algorithm firmware B'ham
 - Birmingham designed test module FTM
- FTM status:

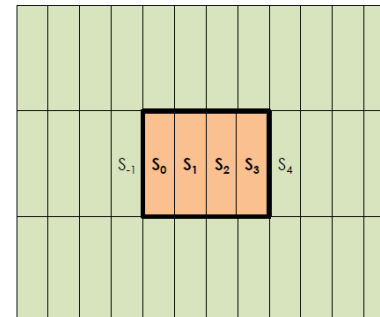
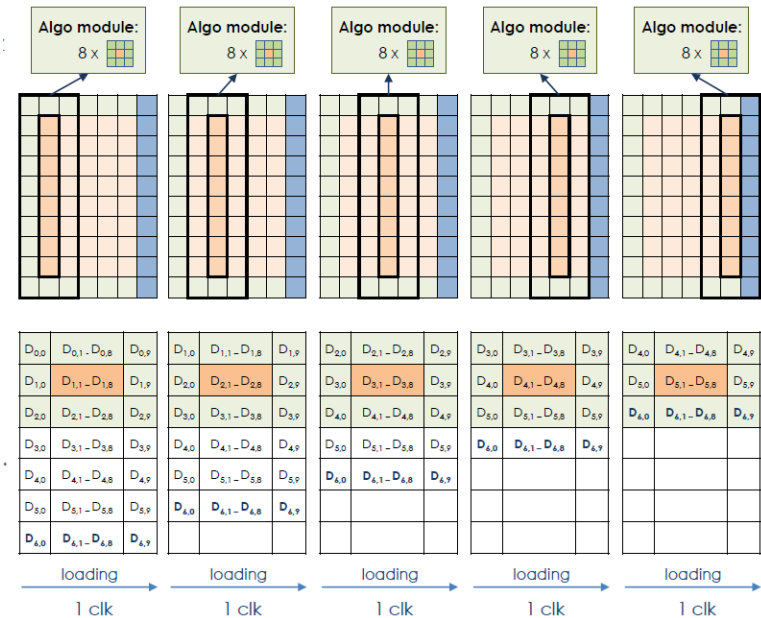




Phase-1 Upgrade



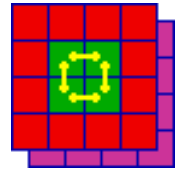
- Francesco getting teeth into algorithm in firmware
- James making progress on simulation
- Timescale:
 - Will keep all of us very busy for at least 5 years
 - Prototyping/production in next two years
 - Installation/commissioning over LS2 (2019-2020)



Comparison	0	1	2	3
$S_0 > S_{-1}$	T			
$S_1 > S_0$	F	T		
$S_2 > S_1$		F	T	
$S_3 > S_2$			F	T
$S_4 > S_3$				F
$S_3 > S_1$		F		T
$S_3 > S_0$	F			T
$S_2 > S_0$	F		T	



Phase-2 Upgrade



- Difficult to summarise the current situation
 - ATLAS is discussing 3 triggering scenarios
 - Most crucially 1 or 2 level hardware trigger
 - Has big impact on need for future hardware development
 - In principle, decision should be soon
 - Then have to quickly take a position on UK involvement
 - A bit of a head-ache for Alan
 - More news in a few weeks, hopefully