

ATLAS LI Calo

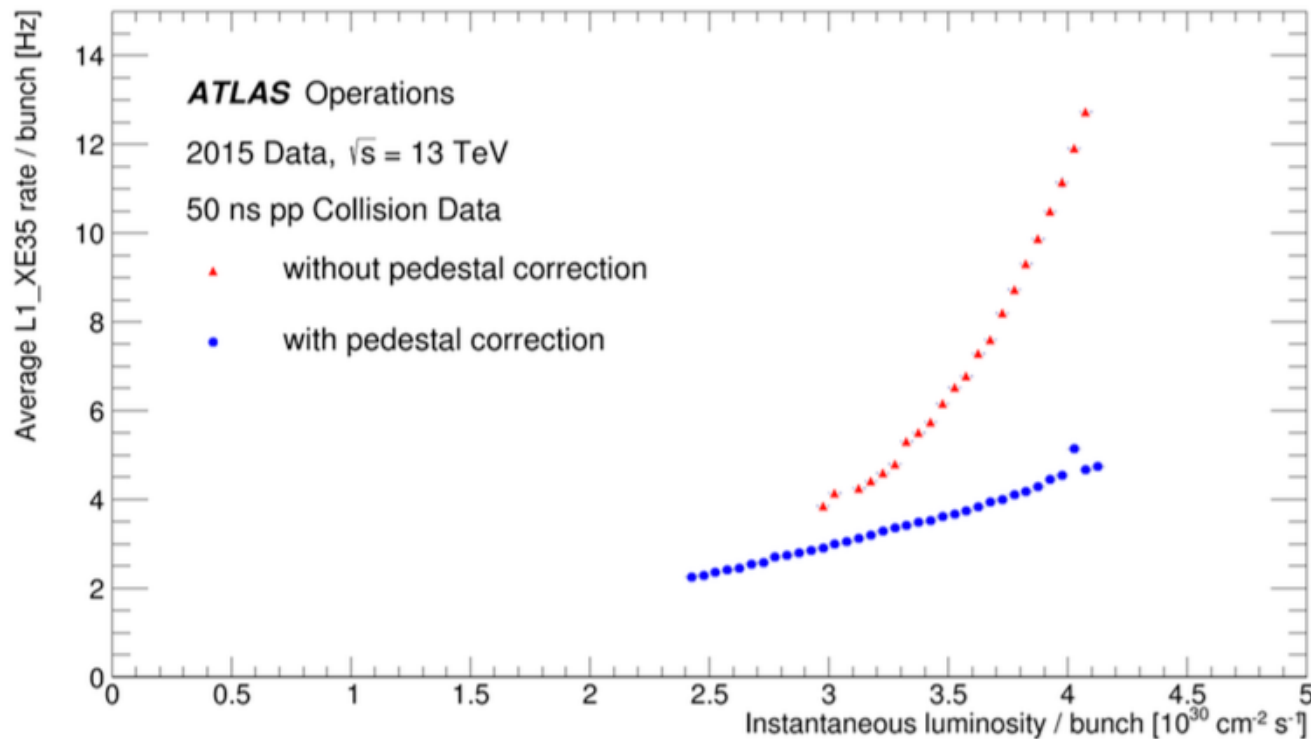
Status Report



Alan Watson

Current System: Developments

- New PreProcessor MCM
 - More pileup-robust filters
 - BC-dependent baseline correction
 - Large input from Andrew Daniels



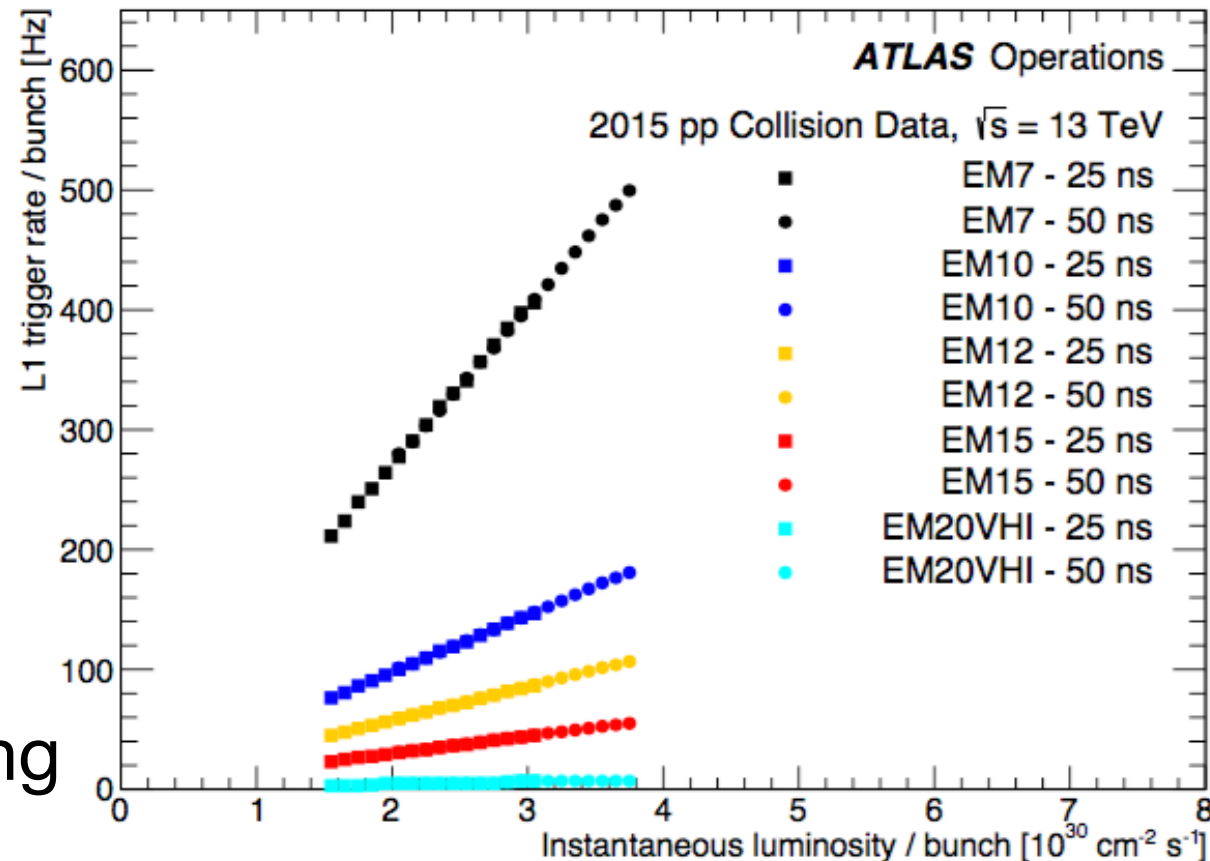
Current System: Developments

- EM/Tau Trigger

- Changes to dataflow to support L1Topo
- Changes to isolation algorithms (LUT-based, ET-dependent)
- Changes to data supplied to CTP

- B'ham Contribute

- Firmware, hardware
- Software (on/off-line)
- Operations
- Calibration, Monitoring



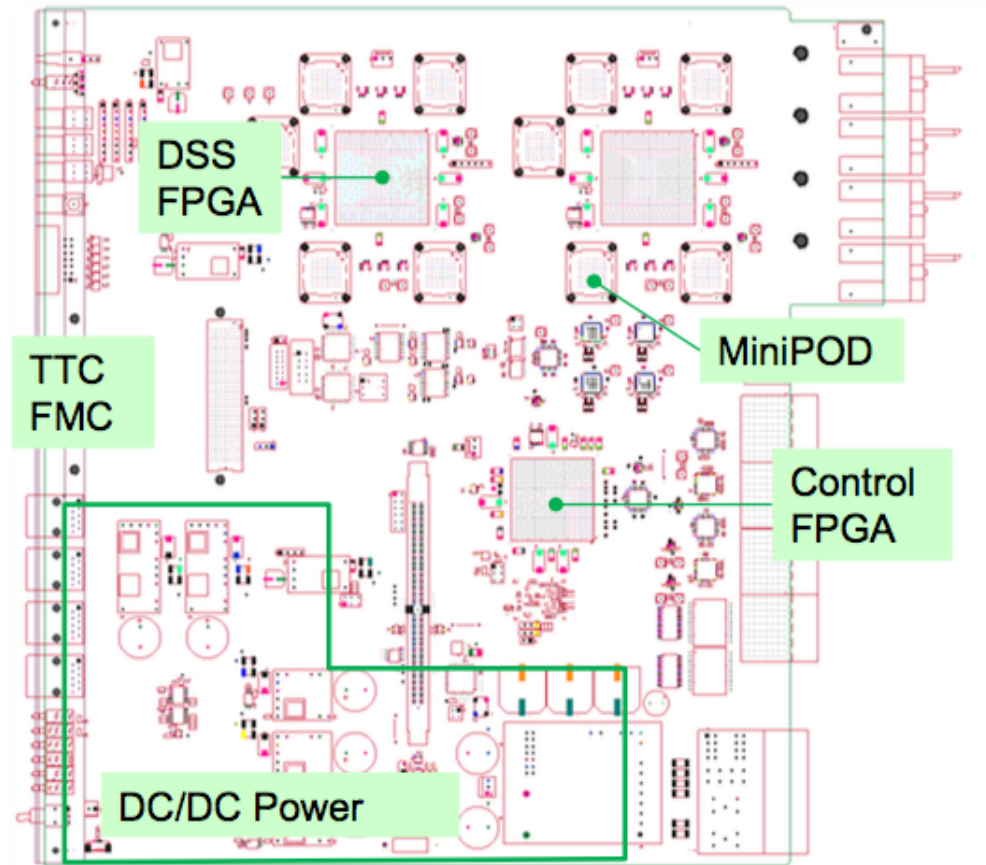
- Fex Test Module

- Multi-purpose high-speed data source for testing of Phase I processors

- Hardware
- Timescales
- Firmware



- Designed by Richard Staley



4 bare PCBs ordered (Isola I-Tera material, 22 layer)

1 retained by fabricator

3 delivered to Assembly company

1 dispatched to RAL (9th Sept)

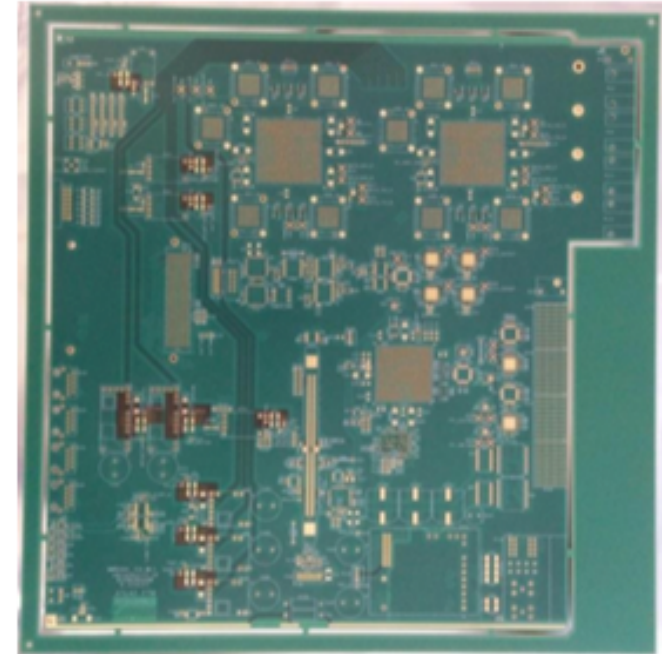
Impedance OK +/- 10%

Module Assembly

2 PCBs being assembled.

Est. delivery 2nd Oct to RAL

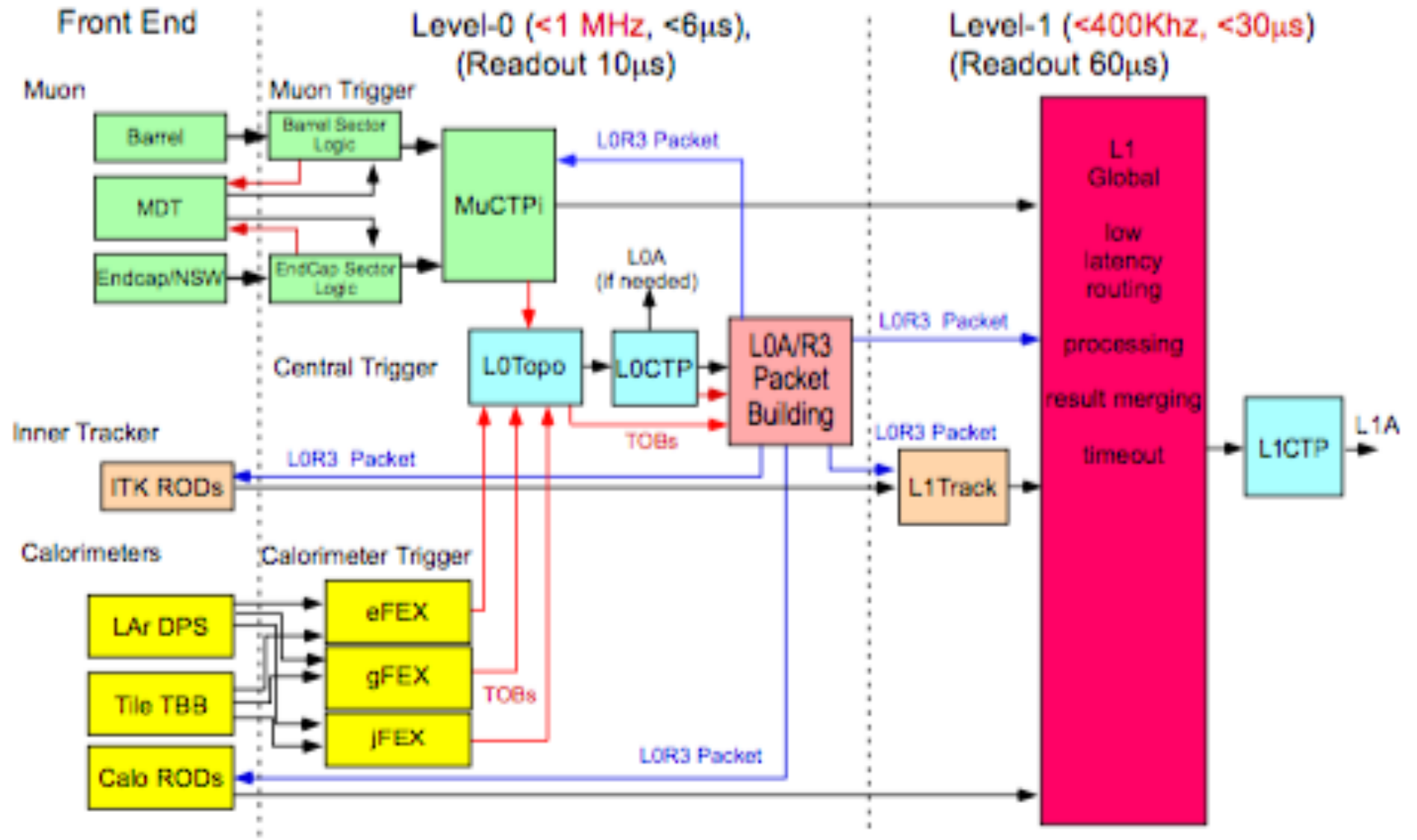
Power + JTAG, then onto B'ham



Replacement bare PCB
expected 19th October
(+ 2 to 3 weeks Assy.)



Upgrade: Phase-II



Level-1 Global chapter in IDR

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