Precision Timing at the High Energy Frontier with the CMS MIP Timing Detector

Lake Louise Winter Institute 2023, 2.26.2023

Federico Siviero

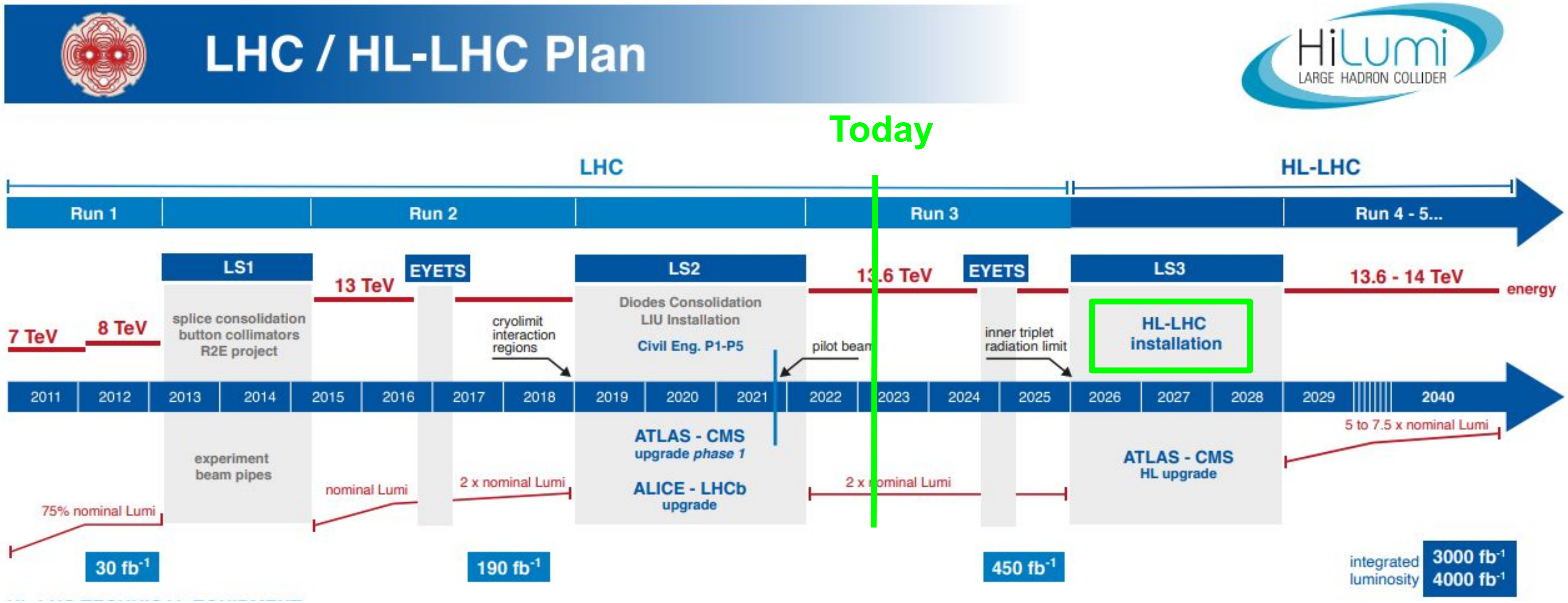
on behalf of the CMS MTD group

Outline

- The CMS MIP Timing Detector
- Status of the Barrel Timing Layer
- Status of the Endcap Timing Layer

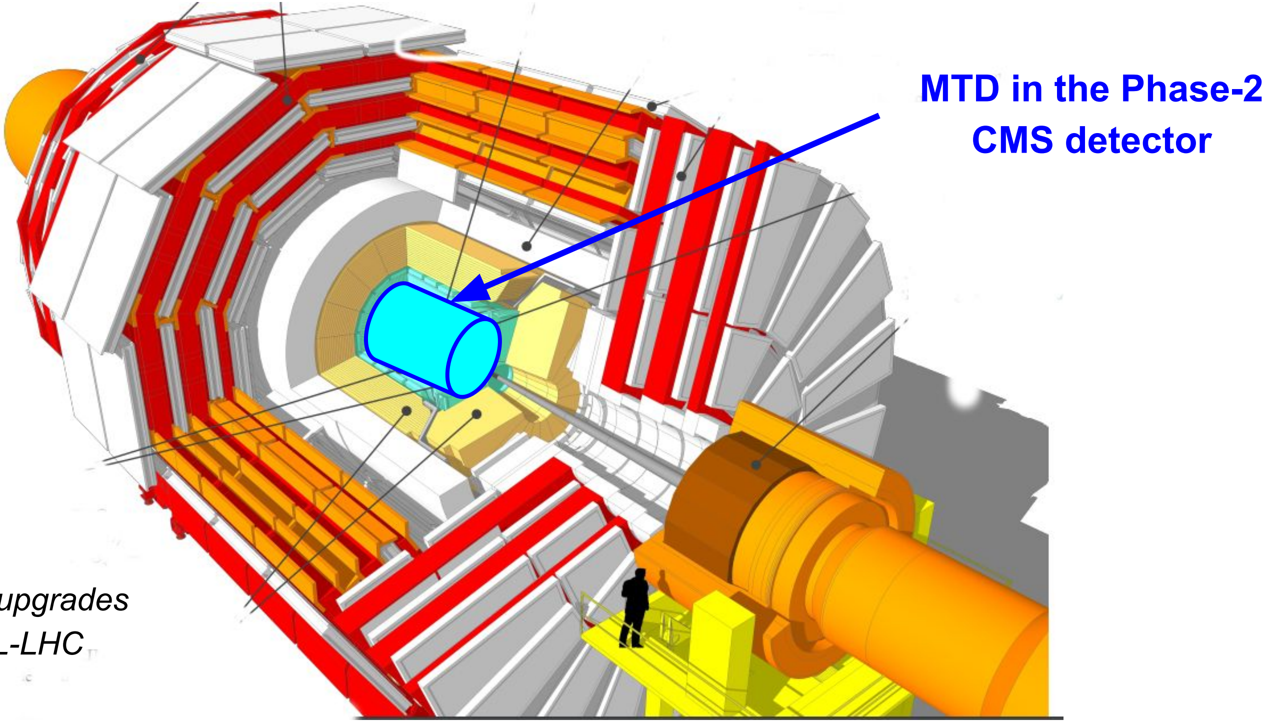
Outline

➢ **The CMS MIP Timing Detector**



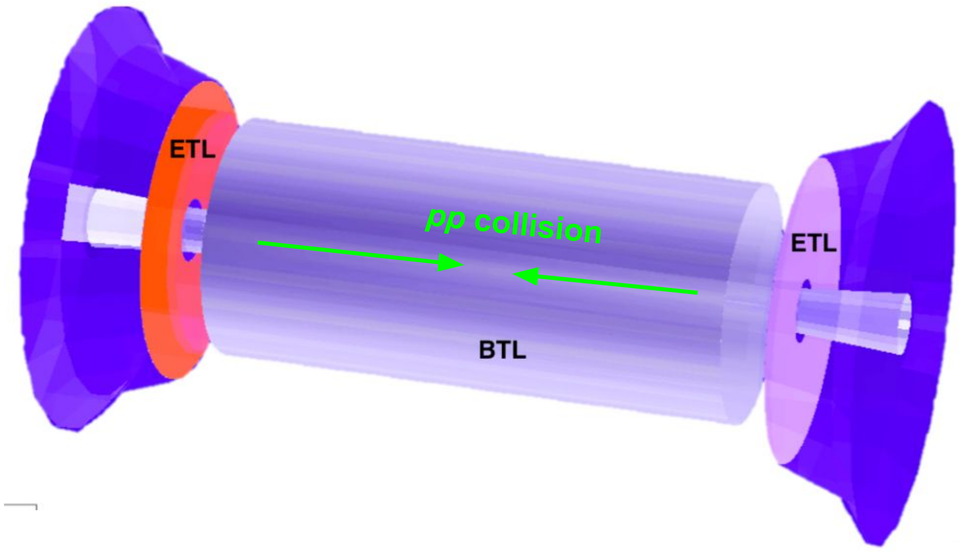
The CMS MIP Timing Detector (MTD)

MTD will provide **accurate timing** of charged tracks during the High-Luminosity phase of the LHC (**HL-LHC**)



MTD is one of the several upgrades occurring in CMS for HL-LHC

The CMS MIP Timing Detector (MTD)



MTD will be divided in 2 sub-detectors

Barrel Timing Layer (BTL): LYSO + SiPM

- tracker / ECAL interface, $|\eta| < 1.45$
- ~5 m long
- 38 m^2 surface, 332k channels
- Fluence @ end of life ~ 2e14 n_{eq}/cm^2

Endcap Timing Layer (ETL): LGAD

- ±3 m away from interaction point
- 0.31 m < R < 1.2 m
- 2x (7 m^2) surface, ~8M channels
- Fluence @ end of life = up to ~ 2e15 n_{eq}/cm^2

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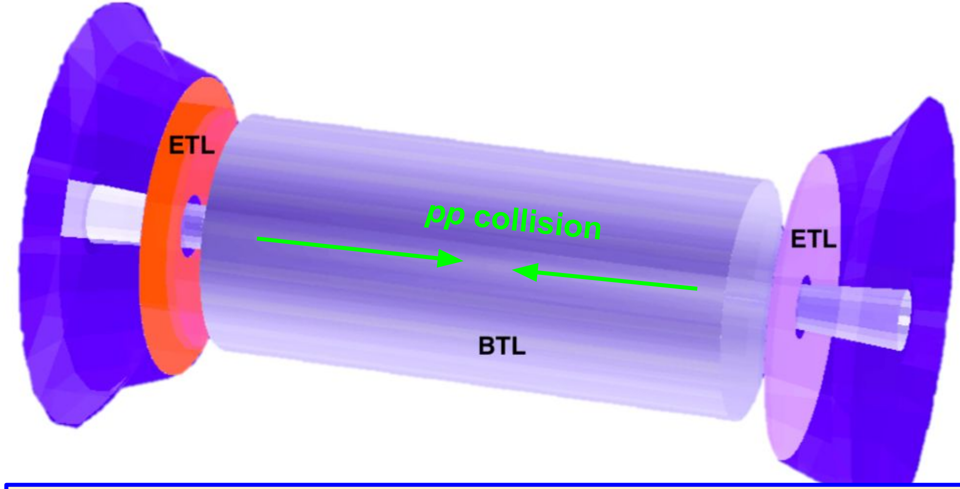

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Key figure: time resolution per track

- ETL: < 35 ps
- BTL: 30-40 ps (~60 ps) at the beginning (end) of life

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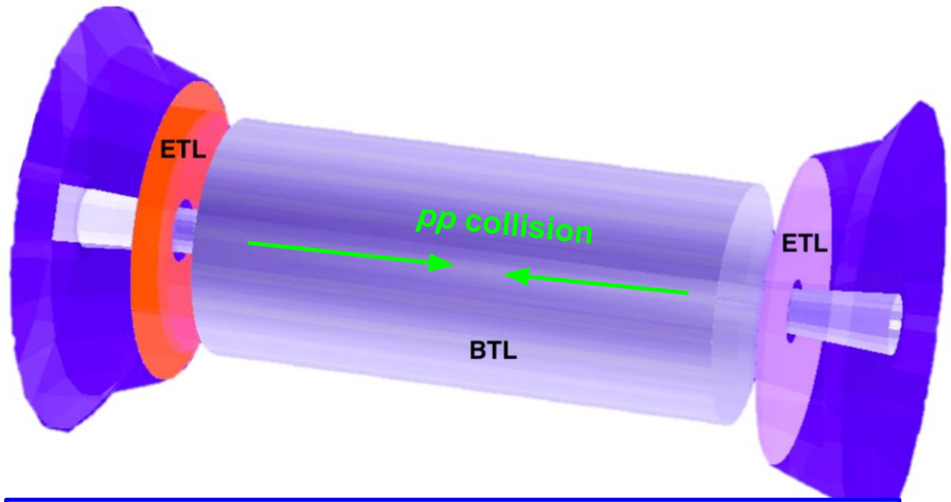

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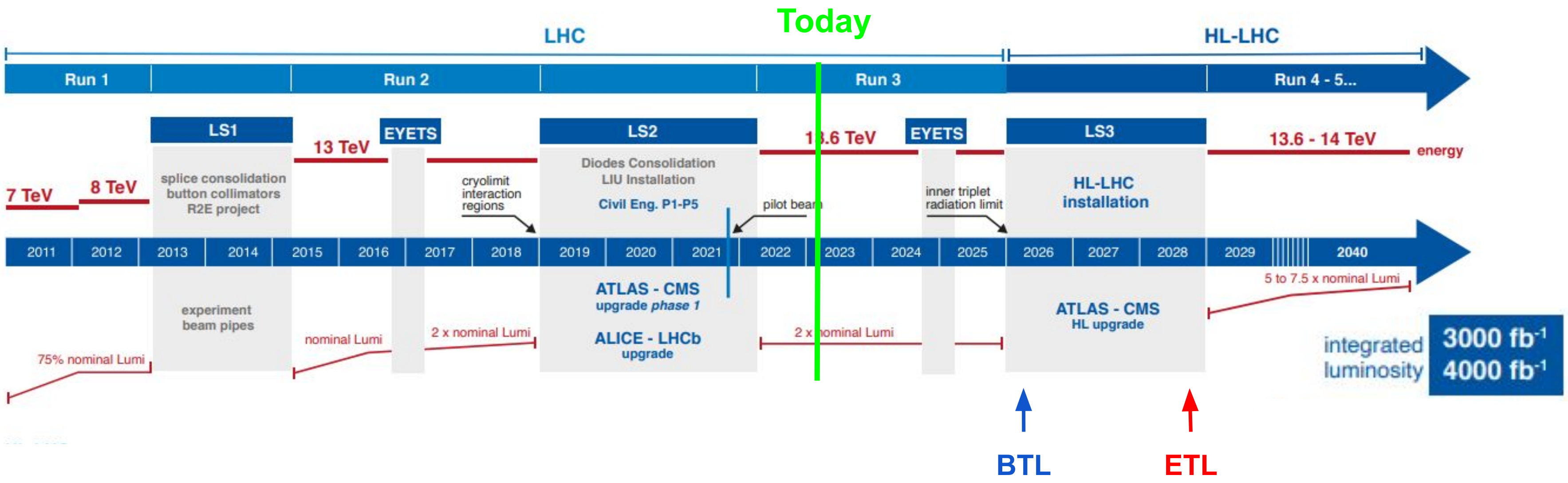
Different sensor technologies in the sub-detectors because of: **larger surface of BTL, different irradiation conditions, different schedules**

LHC / HL-LHC Plan



- **BTL** to be installed at the beginning of LHC long shutdown (LS3), before the tracker
  → **now in pre-production phase**
- **ETL** will have more time, installation at the end of shutdown
  → **now moving from prototyping to pre-production**

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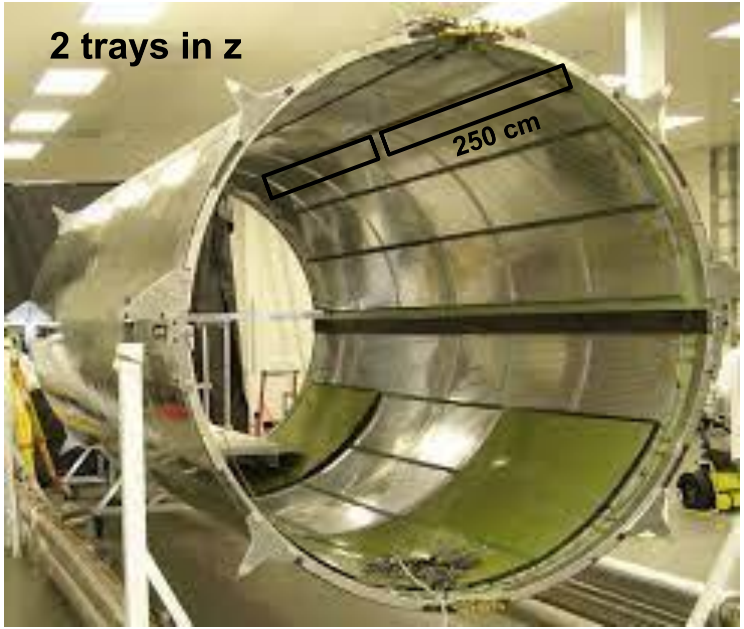
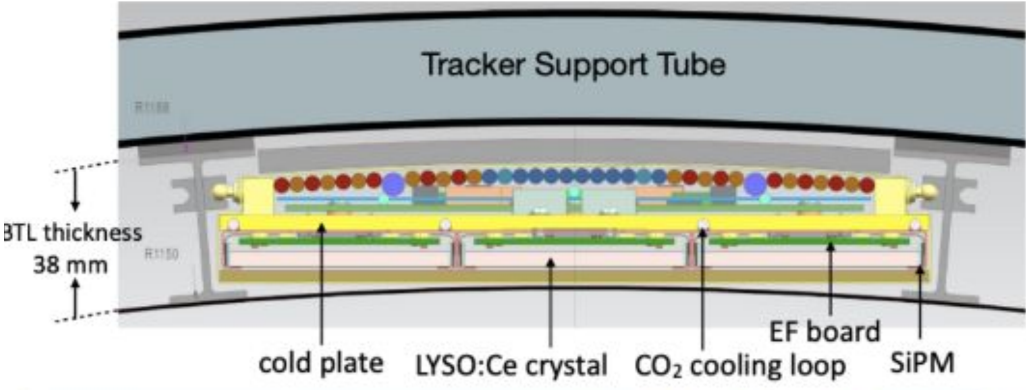
- ➢ **Status of the Barrel Timing Layer**
- ➢ Status of the Endcap Timing Layer

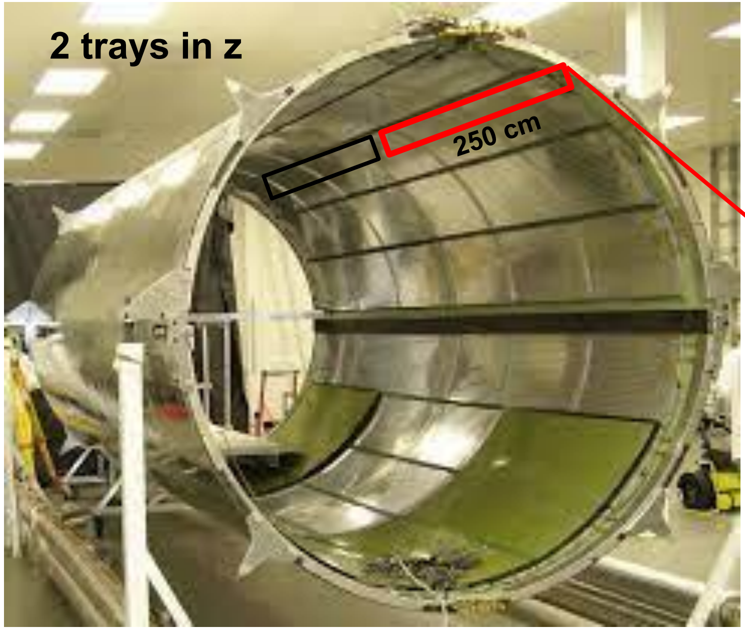
BTL design overview

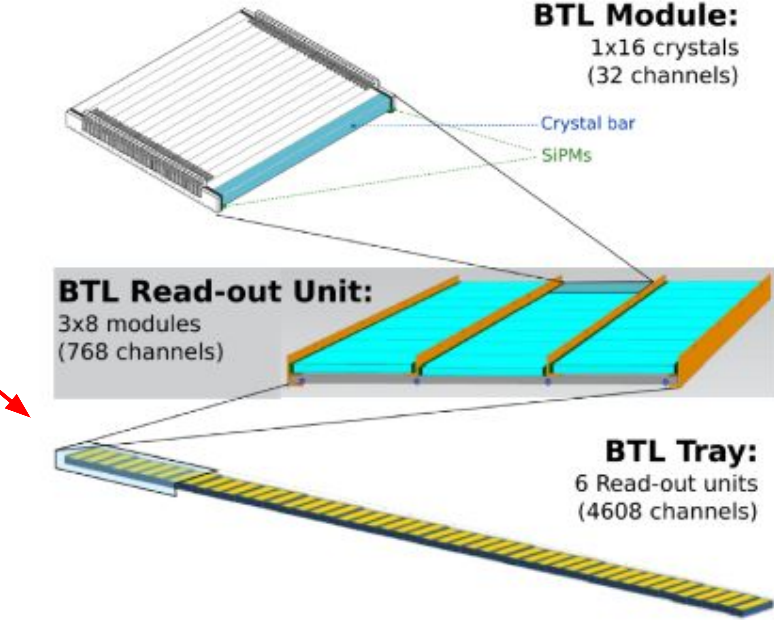




- Thin (~4 cm) cylindrical detector housed inside the tracker support tube
- Made of **72 trays**: 36 (φ) x 2 (z)

BTL design overview



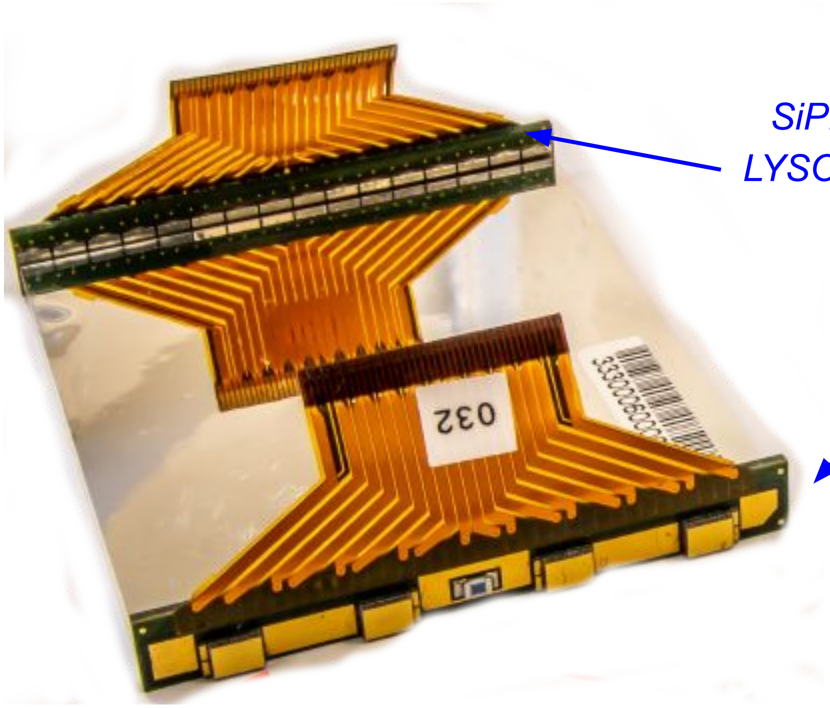


- Thin (~4 cm) cylindrical detector housed inside the tracker support tube
- Made of **72 trays**: 36 (φ) x 2 (z)
- The "building block" is the **BTL module**, made of **1x16 crystals read out by SiPMs**

BTL sensors

LYSO:Ce* crystal scintillators coupled to silicon photomultipliers (SiPM)

*Cerium-doped Lutetium Yttrium Orthosilicate



SiPMs arrays reading out the LYSO scintillation light from both ends of the crystals

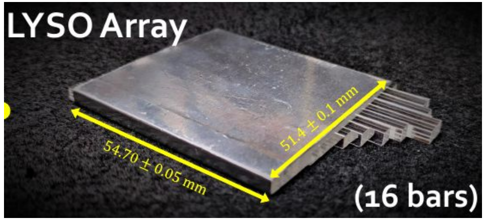
BTL sensors

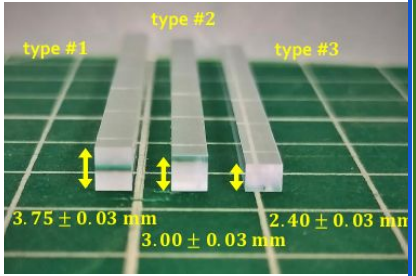
LYSO:Ce* crystal scintillators coupled to silicon photomultipliers (SiPM)

*Cerium-doped Lutetium Yttrium Orthosilicate

LYSO:Ce

- Well-established technology (PET)
- High light yield: 4000 γ/MeV
- Fast risetime ~ 100 ps
- Radiation hardness proven up to 3e14 n_{eq}/cm^2
- Crystal bar having ~5 cm length, ~3 mm width, variable thickness depending on η

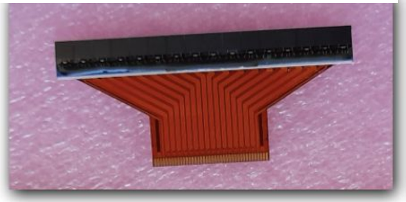




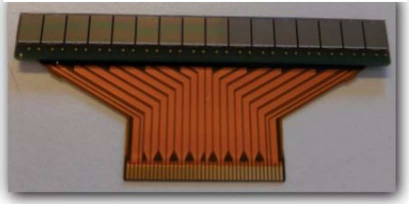
SiPM

- Well-established technology
- photon detection efficiency @ LYSO emission peak 20-40 %
- Radiation hardness proven up to 2e14 n_{eq}/cm^2

FBK



HPK



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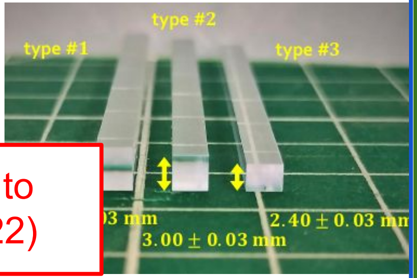


6 qualified vendors invited to LYSO tender (November ‘22)

SiPM

- Well-established technology
- photon detection efficiency @ LYSO emission peak 20-40 %
- Radiation hardness proven up to 2e14 n_{eq}/cm^2

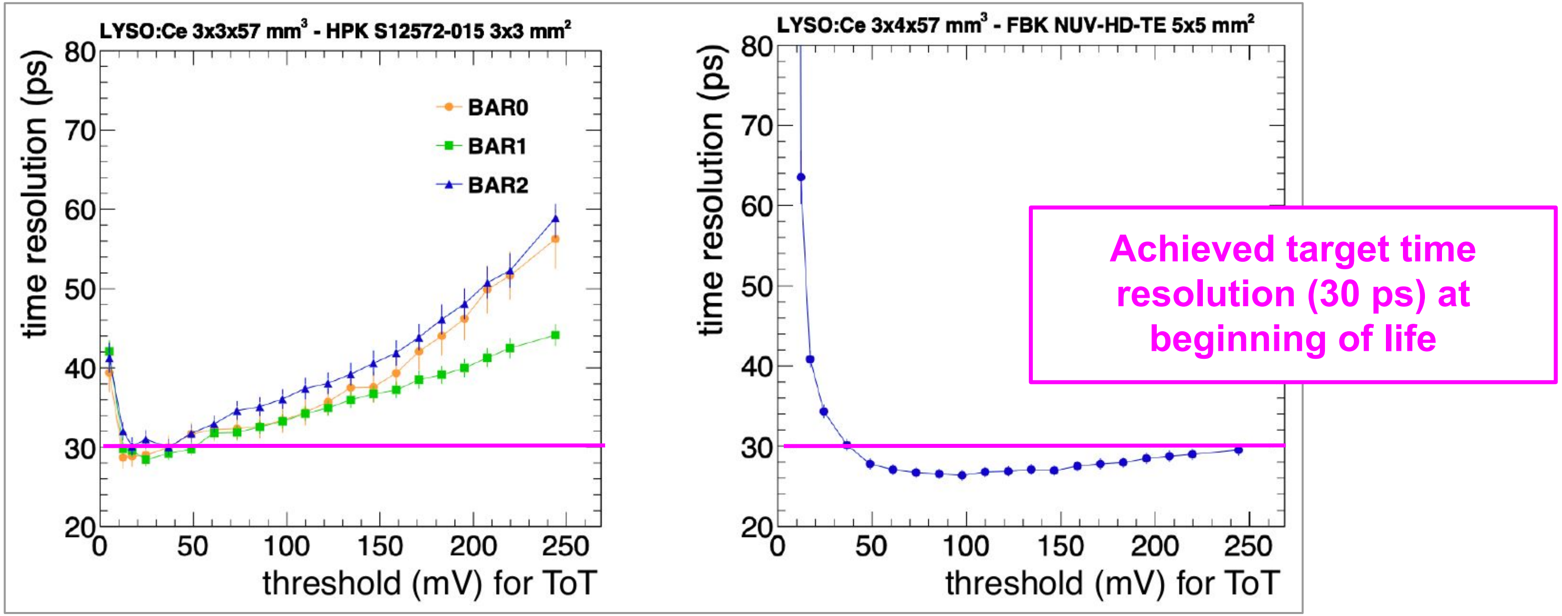
FBK

HPK

2 vendors identified, optimization of SiPM cell size ongoing

Performance of BTL unirradiated sensors

- ➢ **Measured during FNAL test beam with 120 GeV protons**
- ➢ **Tested crystal bars with 3 different sizes + SiPMs from 2 producers (HPK, FBK)**



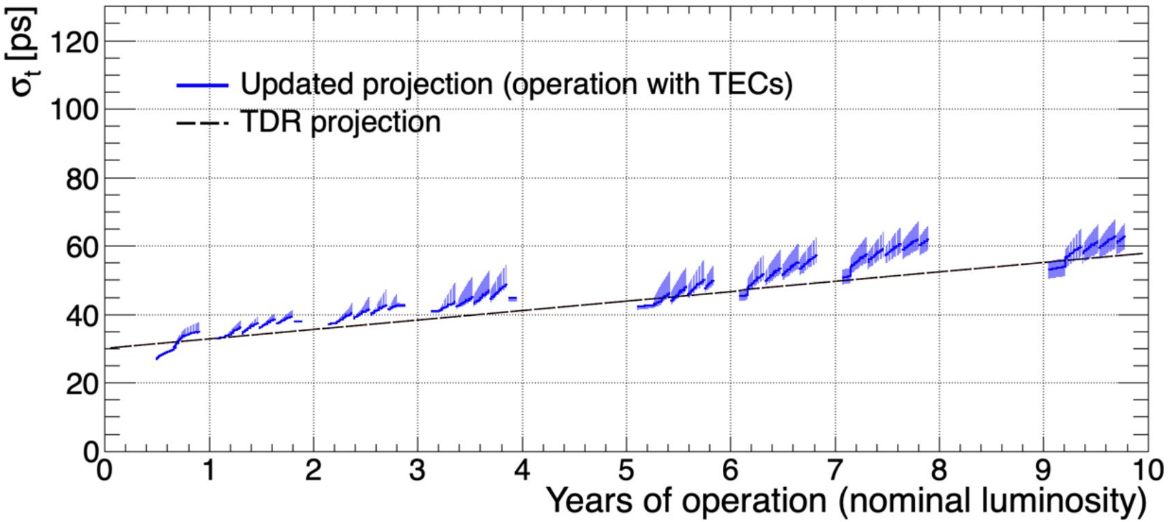
BTL performance evolution with irradiation

Performance degradation with irradiation driven by increased **dark count rate in SiPMs**

Solutions:

- Lower operation voltage, to optimize signal-to-noise ratio
- Use thermoelectric coolers (**TECs**): operation at -45°C and annealing during HL-LHC shutdowns
- Use **SiPMs with larger cell size → increase of photon detection efficiency** (PDE)

Expected evolution of BTL resolution



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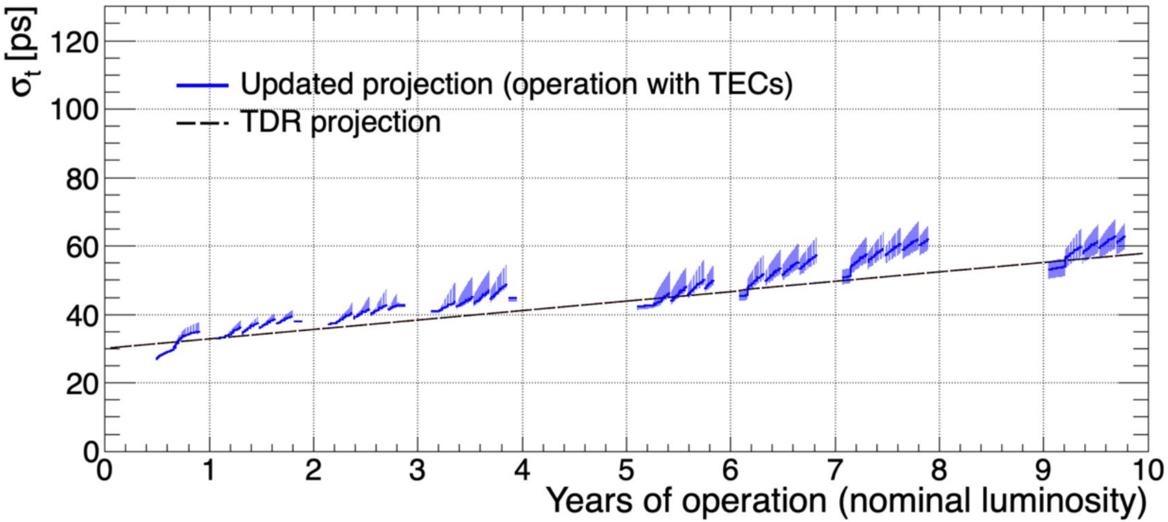


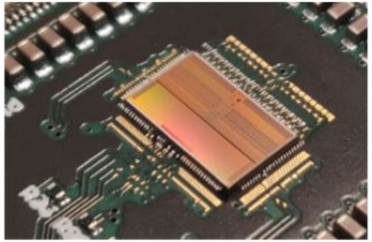
→ Thanks to these solutions, the **resolution at end-of-life is within the target (~ 60 ps)**

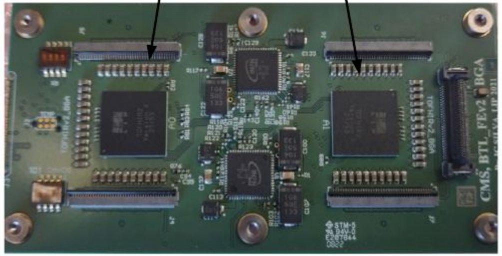
test beams planned in Spring '23

BTL electronics

- SiPMs read out by a dedicated ASIC: **TOFHIR** (Time-of-flight, High Rate)
  - 32 independent channels
  - timing measurement
  - amplitude measurement for time walk correction

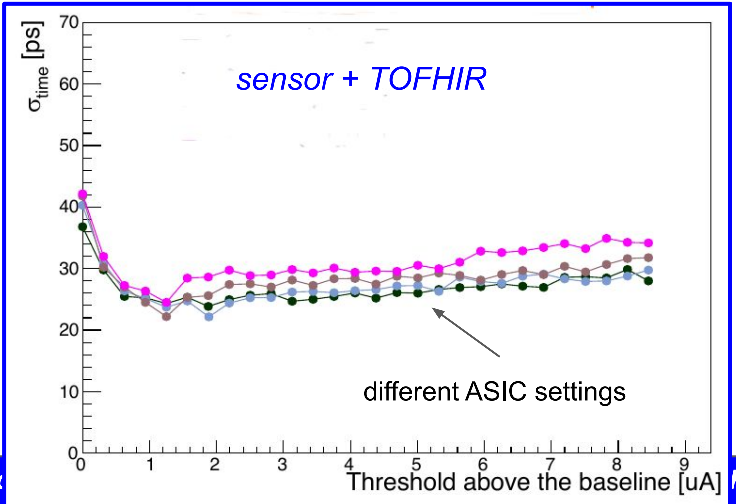
- Ongoing engineering run for the production of the latest TOFHIR version (expected end of February ‘23)





Time resolution as measured with UV laser exciting the LYSO

→ within requirements

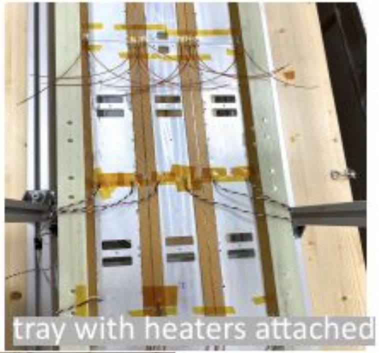


BTL system test and integration

A large and complex detector like BTL is only made of sensor and ASIC

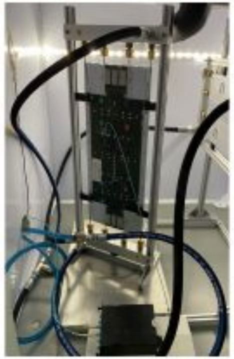
Several activities ongoing to develop system test and integration → **we're actually building it!**

BTL cooling tray



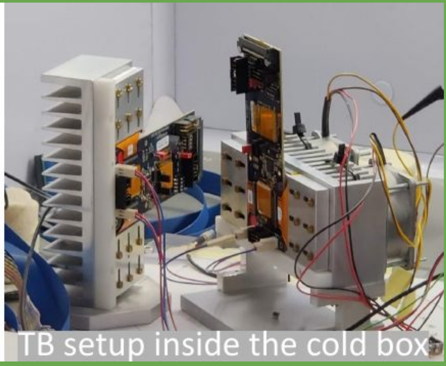
tray with heaters attached

BTL DAQ integration test

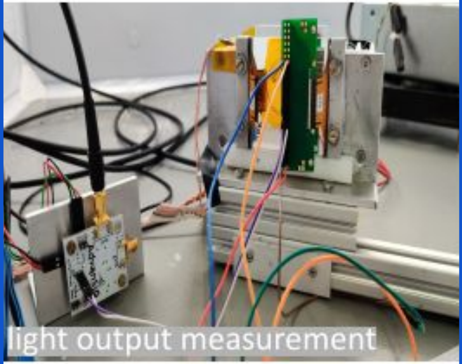


BTL rail attachment exerc-ise on TST mockup

BTL cold box



TB setup inside the cold box



light output measurement

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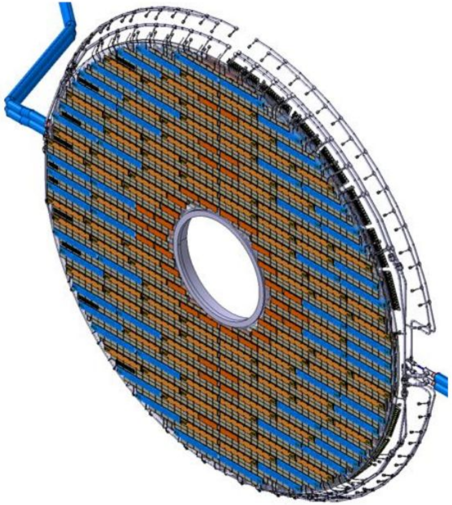
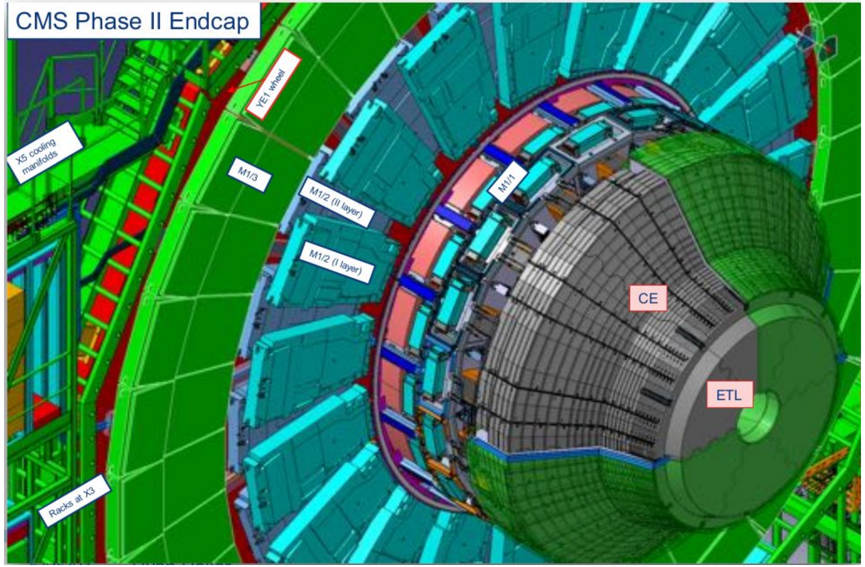
ETL design overview

- ETL will be mounted on the nose of the CMS CE calorimeter
- 2 double-sided disks for each endcap side, assembled into D's



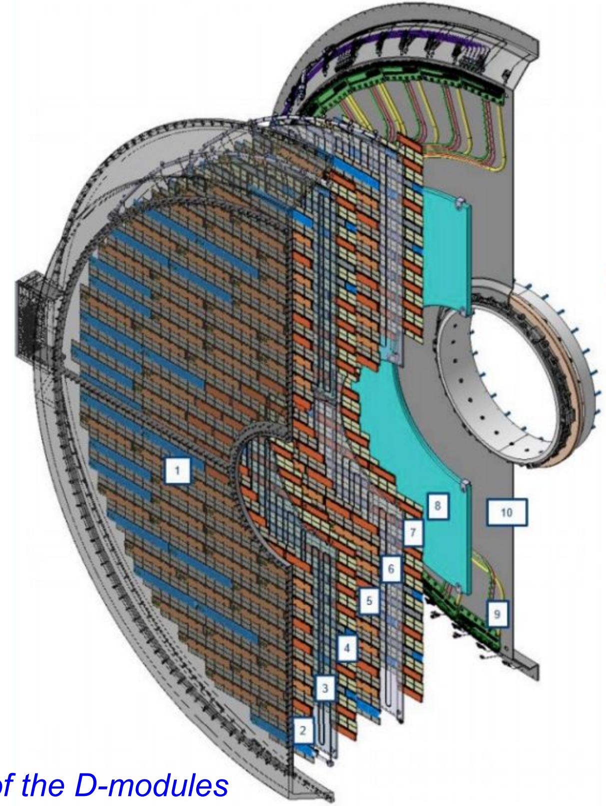
ETL disk



Endcap region of the CMS detector:
ETL will be mounted on the CE nose

ETL design overview

- ETL will be mounted on the nose of the CMS CE calorimeter
- 2 double-sided disks for each endcap side, assembled into D’s
  - double-sided disk → large geometrical acceptance (85% / disk)
  - 2 disks to achieve:
    - **Single hit time resolution (sensor + ASIC) < 50 ps**
    - **track time resolution (sensor + ASIC) < 35 ps**
- Equipped with 50 um-thick silicon sensors **based on the Low-Gain Avalanche Diode (LGAD) technology**

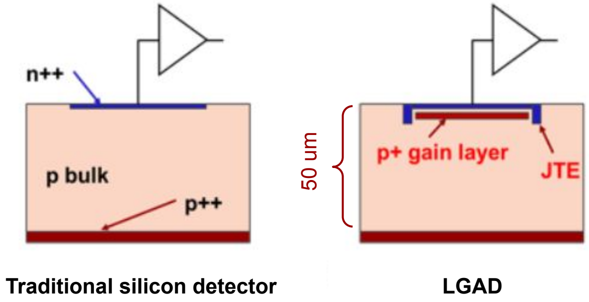


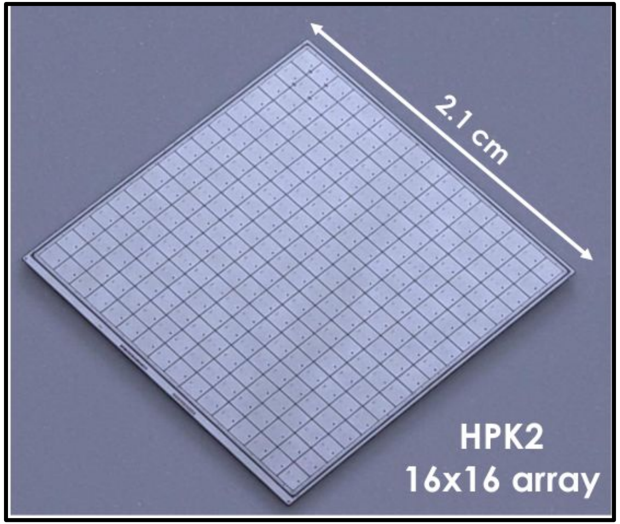
Exploded view of one of the D-modules composing the ETL disks

Sensors for ETL : the final 16x16

The final ETL sensor will be a 16x16 LGAD

- 1.3 x 1.3 mm^2 pads for a total surface of 21.4 x 21.6 mm^2
- From the beginning to the end of HL-LHC lifetime, sensors expected to:
  - achieve single hit time resolution < 50 ps when coupled to the ASIC (30-40 ps for the bare sensor)
  - deliver > 8 fC of charge
- ETL sensors need also to be **radiation-hard** to survive the harsh radiation environment @ HL-LHC
  - **LGADs** suited for this: unchanged performance **up to 1.5e15 n_{eq}/cm^2**

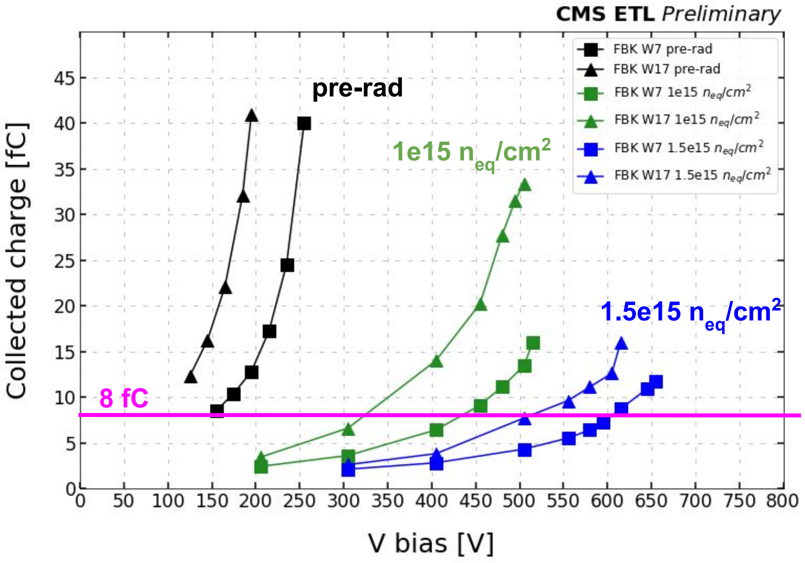


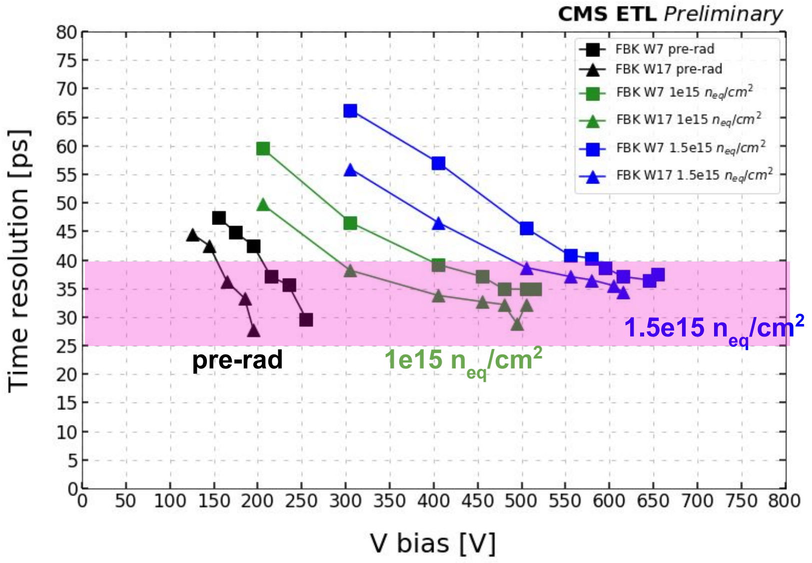


Performance of ETL sensors

- Market Survey for the procurement of the final LGADs for ETL recently completed
  - Identified 4 vendors able to produce the final ETL sensors

FBK samples measured with a beta-source setup





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Resolution and delivered charge of bare sensors within requirements

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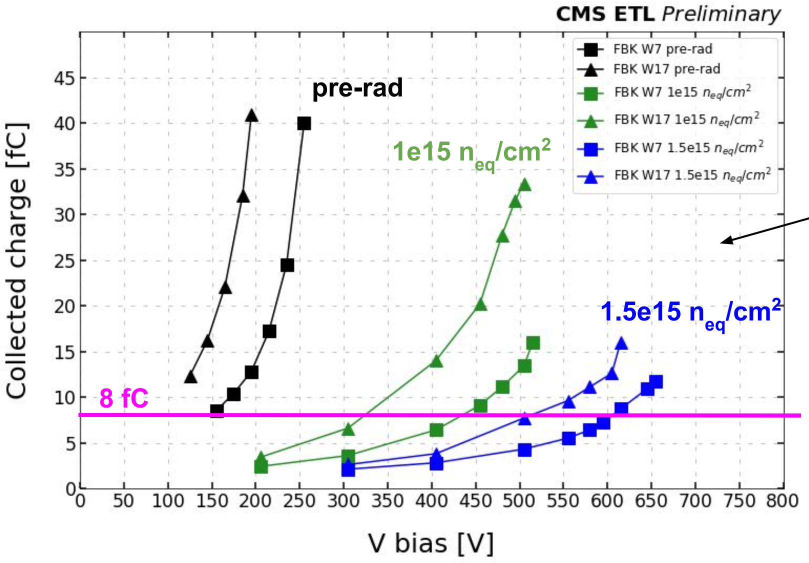
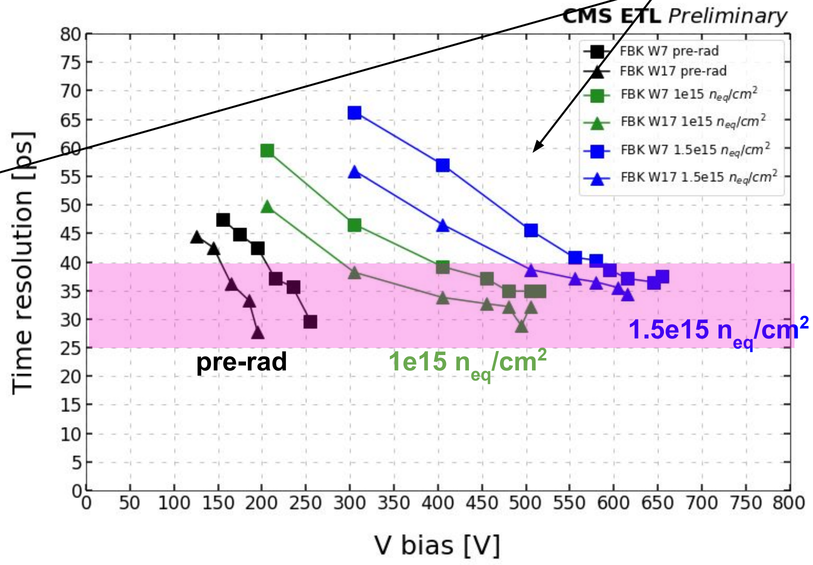




ETL electronics

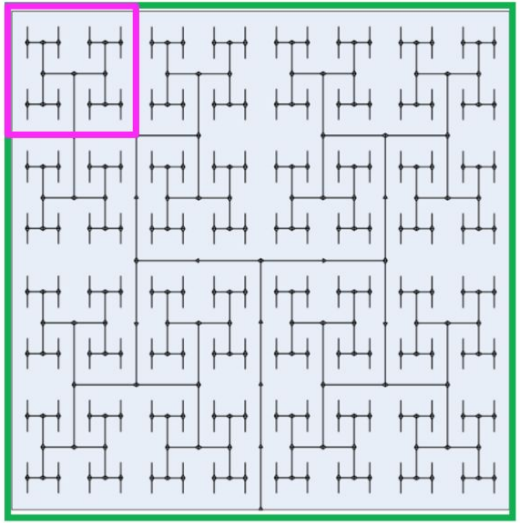
- **ETROC is the ETL read-out ASIC**
- **To achieve time resolution < 50 ps per single hit:**
  - low noise + fast rise time
  - power budget: 1 W/chip, 3 mW/channel

ETROC1

- **proved able to reach ~ 40 ps resolution coupled with a prototype LGAD (measured during a test beam with 120 GeV protons)**
- **Used in the first ETL full system DAQ**

ETROC2 (full-scale 16x16 ASIC)

- **expected in March ‘23 (test board ready)**
- **meanwhile, practicing with FPGA-based ETROC2 emulator**

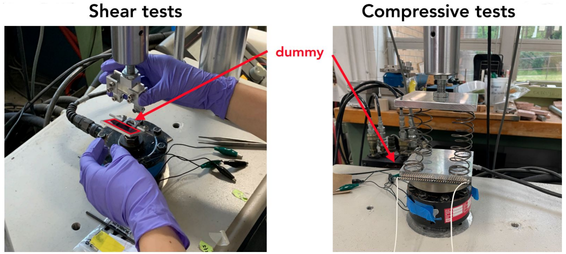


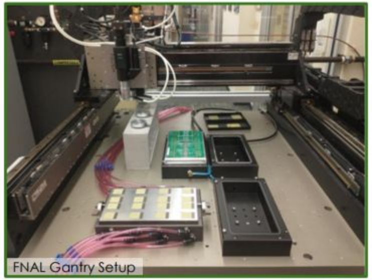
✓ ETROC0: single analog channel
✓ ETROC1: with TDC and 4x4 clock tree
◉ ETROC2: full functionality + full size
◉ ETROC3: 16x16 full size chip

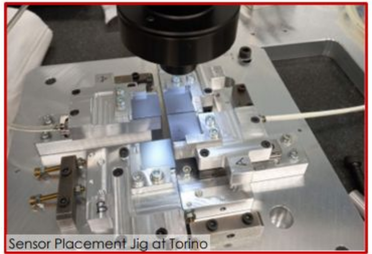
ETL system test and integration

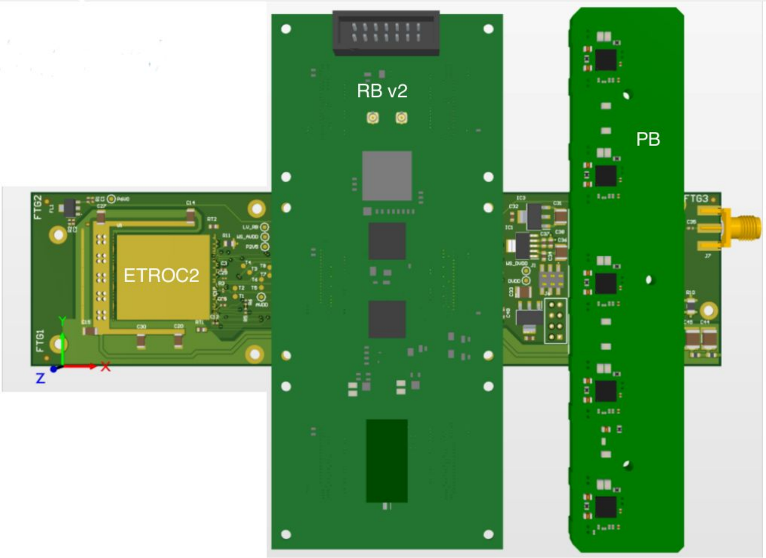
ETL installation coming later than BTL: prototyping just concluded, started working on system test and integration

- We are designing a **testing-optimized module** compatible with ETROC2, read-out board and power board, and with a bump-bonded 16x16 → **will enable a full system test!**
- **Practicing with bump-bonding procedure with dummy sensors**
- **Defining module assembly with gantry / jig**









Summary

- **The CMS MIP Timing Detector will accurately measure charged tracks** during the Phase-2 of the experiment **at the High-Luminosity LHC**
  - MTD divided in 2 sub-detectors: BTL (barrel region) and ETL (endcaps)

- **BTL** will be instrumented with LYSO crystals + SiPMs, read-out by the TOFHIR
  - Beginning of life performance (30-40 ps) within requirements
  - End-of-life performance (~ 60 ps) close to requirements → optimization of SiPM cell size ongoing
  - 6 qualified vendors invited to LYSO tender
  - Engineering run for the production of the TOFHIR2C ASIC ongoing
  - Assembly, integration and full system test progressing well

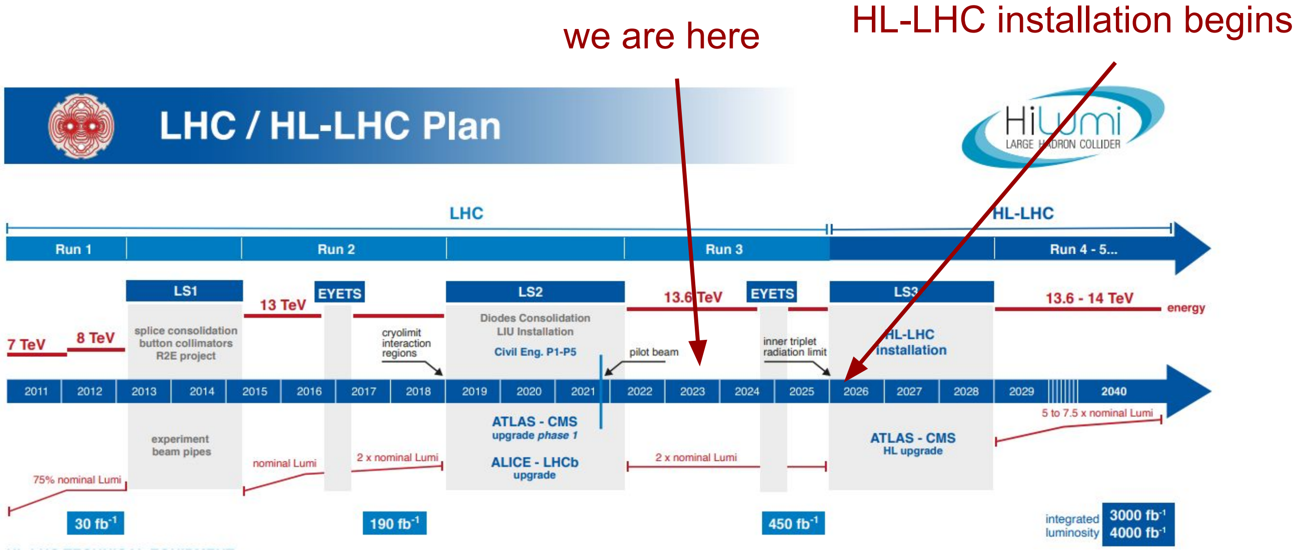
- **ETL** will be instrumented with LGADs read out by the ETROC
  - Performance at beginning and end of life within requirements (single hit resolution < 50 ps)
  - Sensors market survey recently completed → vendors for the final sensors production identified
  - full-scale 16x16 ETROC2 arriving soon
  - Defining modules assembly, bump-bonding procedure

Thank You!

BACKUP

High-Luminosity LHC (HL-LHC)

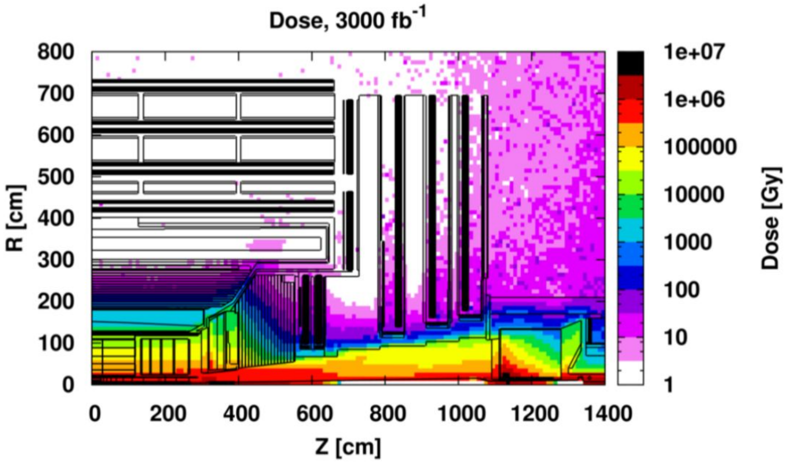
- Starting from 2026, LHC will be upgraded
  - will resume operations in **2029**, beginning the **High-Luminosity era** (HL-LHC)
  - Luminosity increase: x3 (instantaneous) / x10 (integrated)



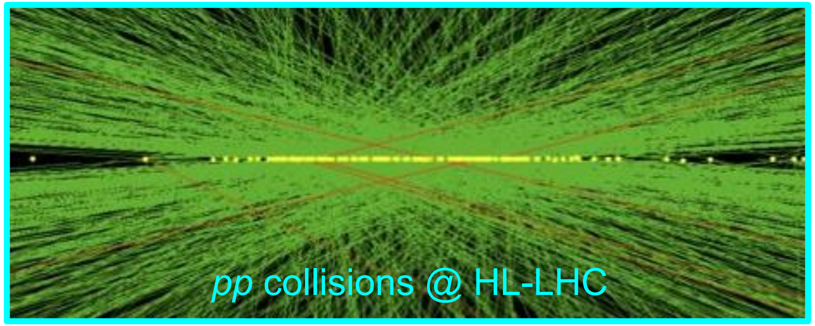
Challenges posed by the HL-LHC

Two main challenges posed to the experiments at the HL-LHC

- **Radiation damage**: annual dose absorbed by detectors at the HL-LHC a factor x10 higher than present LHC
- **Pileup (PU)**: 140-200 interactions overlapping with the hard-scatter interaction expected at each bunch crossing
  - Presently PU ~ 40 at the LHC

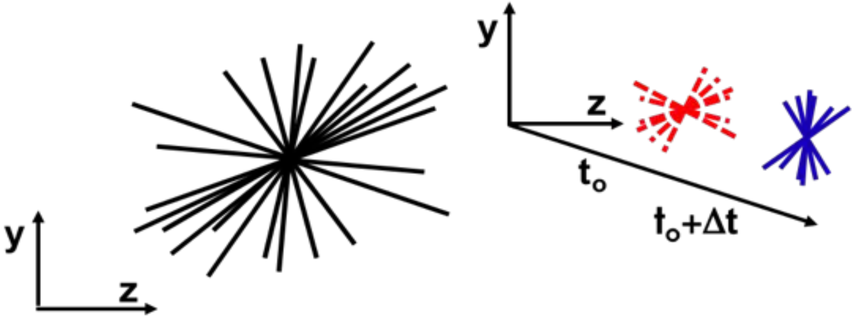


To address these challenges, the CMS detector will be upgraded



Why timing?

- The MTD task: help CMS to maintain its present performance in the high-luminosity environment
- MTD will provide track timing with ~30 ps resolution



Shifting from space to space-time

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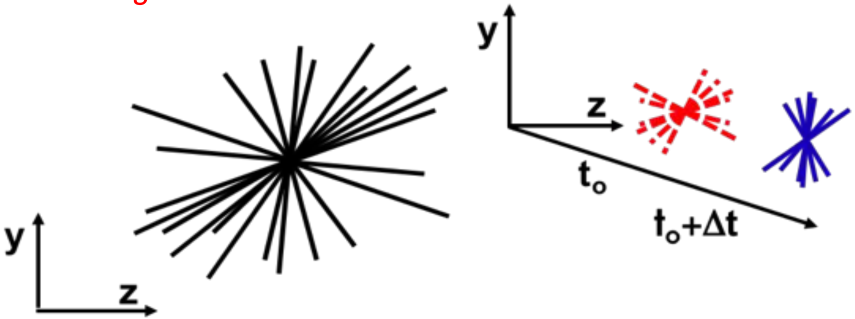
a single vertex?



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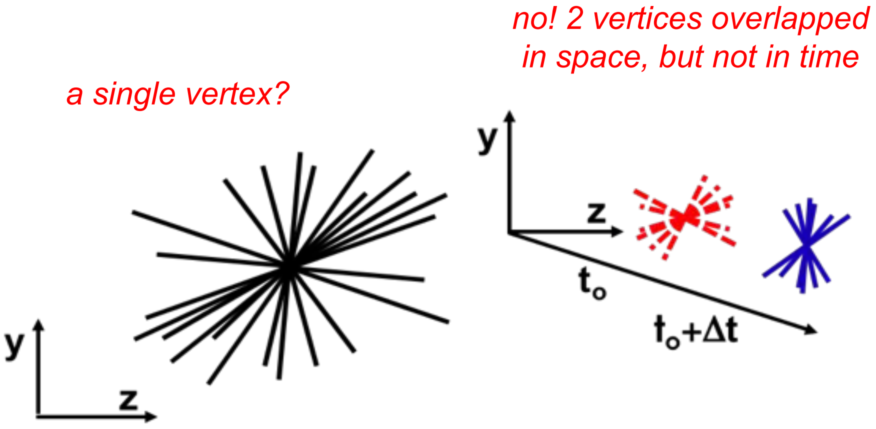

Shifting from space to space-time

Why timing?

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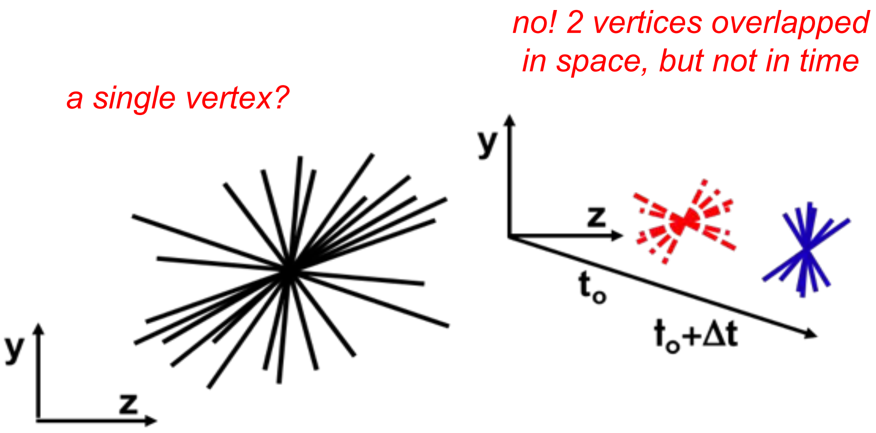

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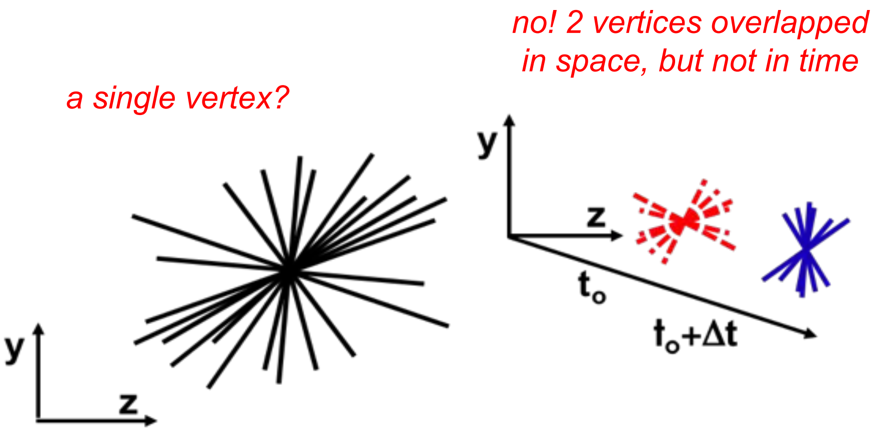
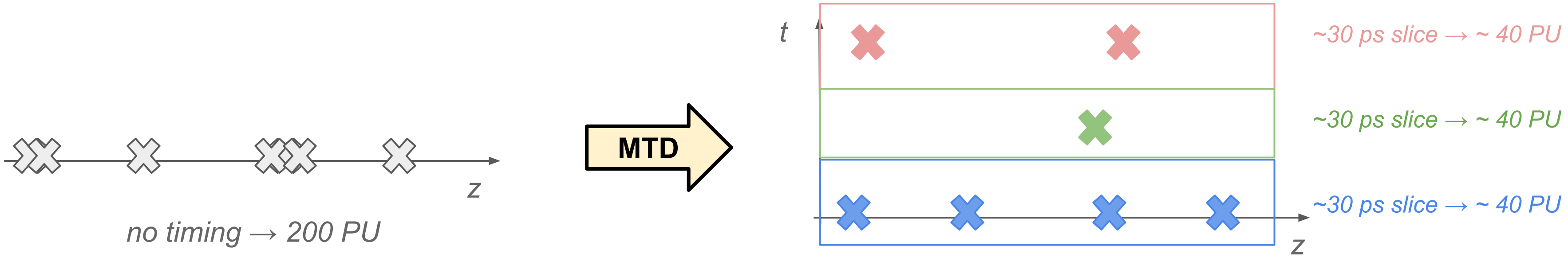
  - PU level drops from 200 to 40





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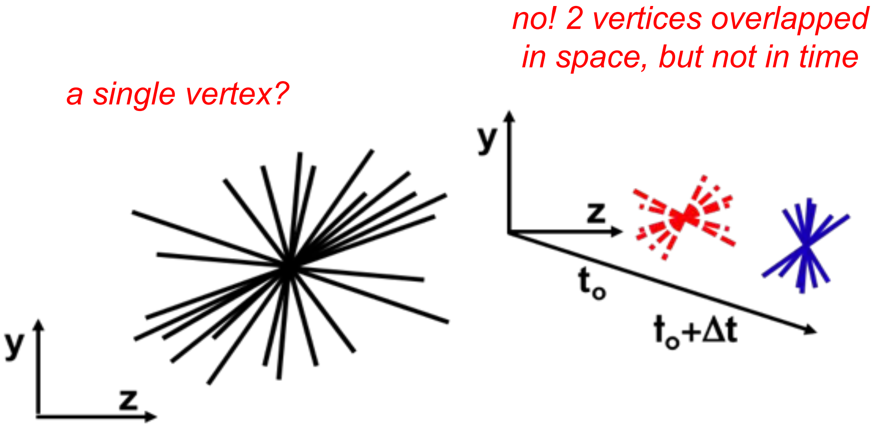
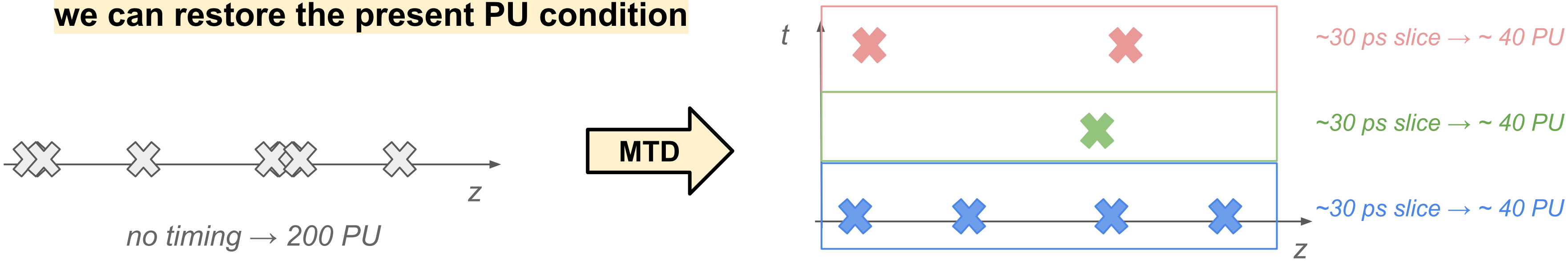
- The number of concurrent interactions in a 30 ps exposure drops by a factor 5-6
  - PU level drops from 200 to 40 → **with MTD, we can restore the present PU condition**

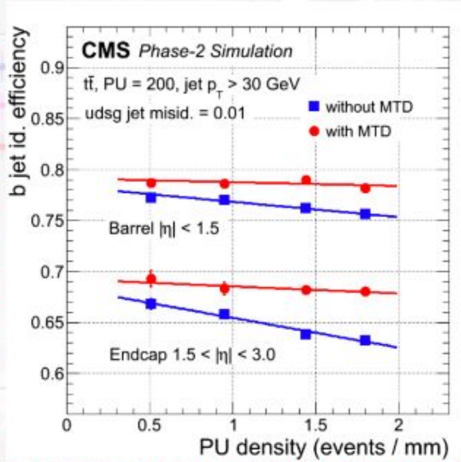


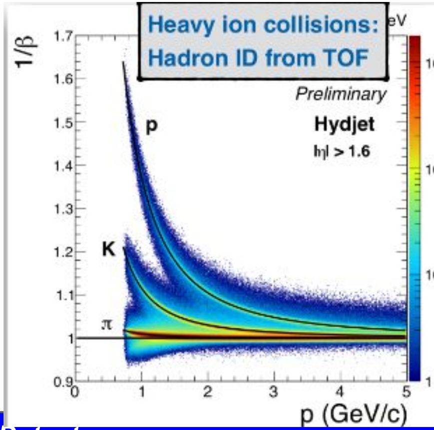


Impact of MTD on physics performance

Just a glimpse: list of improvements too long to go through every item in this talk

- Fraction of vertices merged during reconstruction drops from 15% to 1% (shift from 3D-reco to 4D-reco) → **improvements in physics object identification and reconstruction** (b-tagging, lepton isolation, missing energy)
- Up to 30% reduction of spurious secondary vertices → **3-5% increase in b-tagging efficiency**
  - HH → 4b: 18% increase in signal yield
- MTD will also **add new capability to CMS**: e.g. particle identification of low-p_T charged hadrons thanks to time-of-flight measurements
  - important for heavy-ion physics





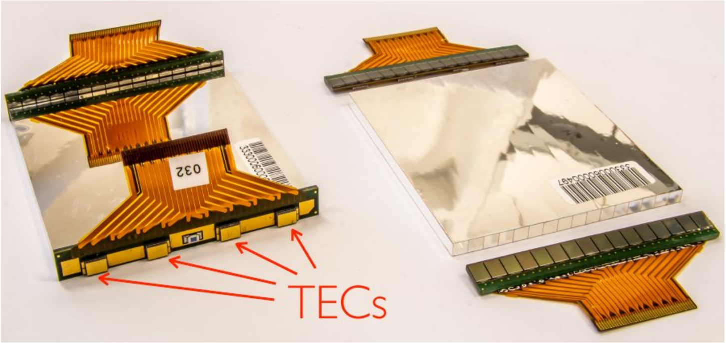
BTL time resolution

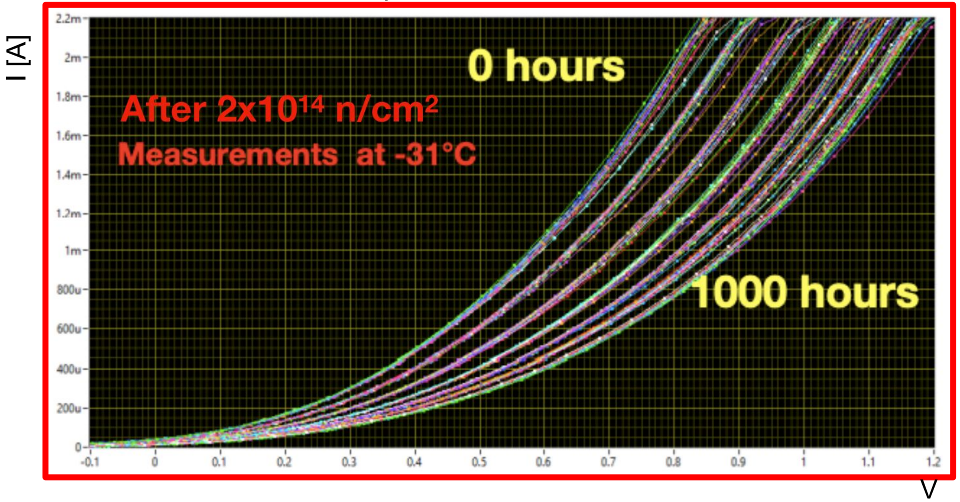
$$\sigma_t^{BTL} = \sigma_t^{clock} \oplus \sigma_t^{digi} \oplus \sigma_t^{ele} \oplus \sigma_t^{phot} \oplus \sigma_t^{DCR}$$

- BTL time resolution main contributors are:
  - electronics noise
  - photo-statistics
  - SiPMs Dark Count Rate (DCR)

BTL performance evolution with irradiation

- Sensors performance degradation with irradiation driven by increased dark count rate (DCR) in SiPMs
- Solutions to cope with it:
  - Lower operation voltage, to optimize signal-to-noise ratio
  - Noise filtering with signal processing technique in TOFHIR
  - Use thermoelectric coolers (TECs): enable SiPM operation at -45°C (lower noise) and **annealing at +40°C** during HL-LHC shutdowns (beneficial for the dark current)

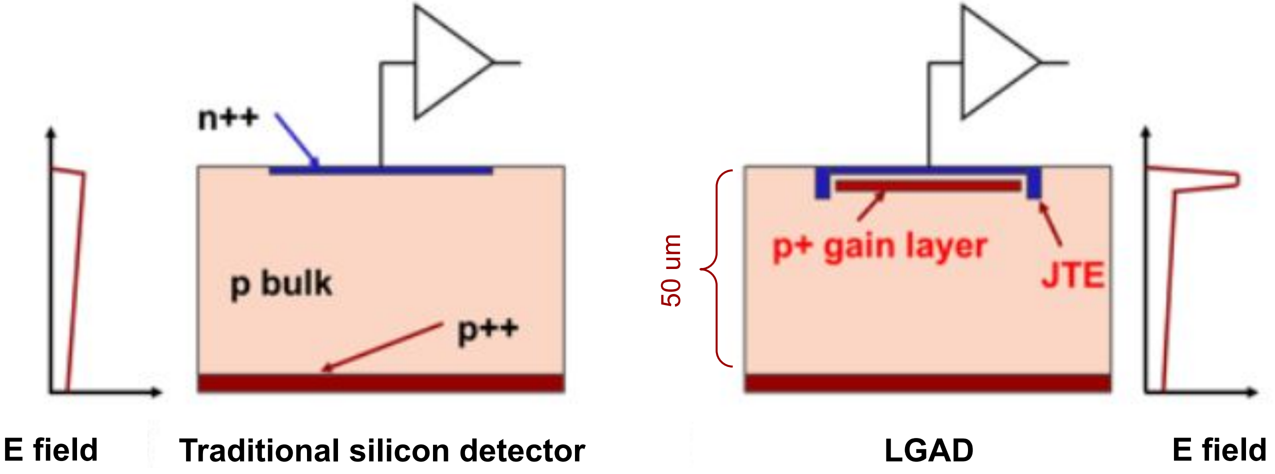




Sensors for ETL : LGAD

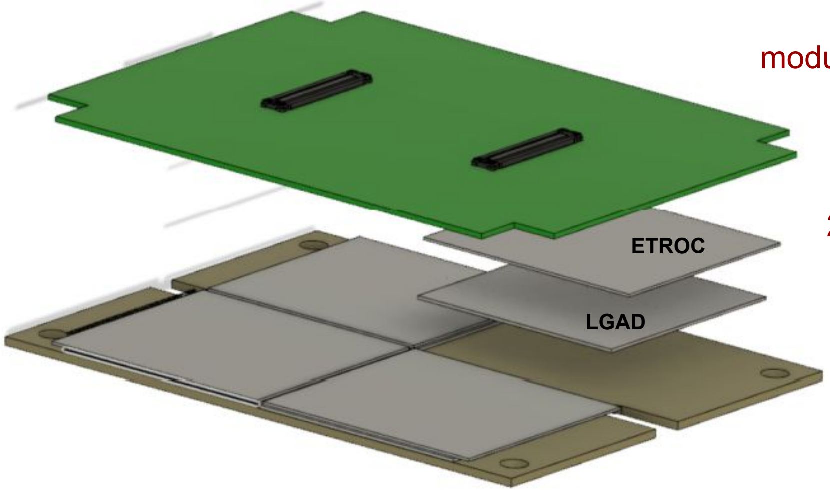
- **50 µm-thick silicon sensors based on the Low-Gain Avalanche Diode (LGAD) technology**
  - p^+ gain layer implanted underneath n^{++} electrode
  - electron charge multiplication for $E > 300\ kV/cm$
  - moderate internal gain: 10-30

- **Thin sensor + LGAD technology → excellent timing performance**



ETL design overview

ETL will be populated with modules → the "building block" of the ETL disks



module PCB (allows connection to the read-out board)

2x2 ASIC + sensor

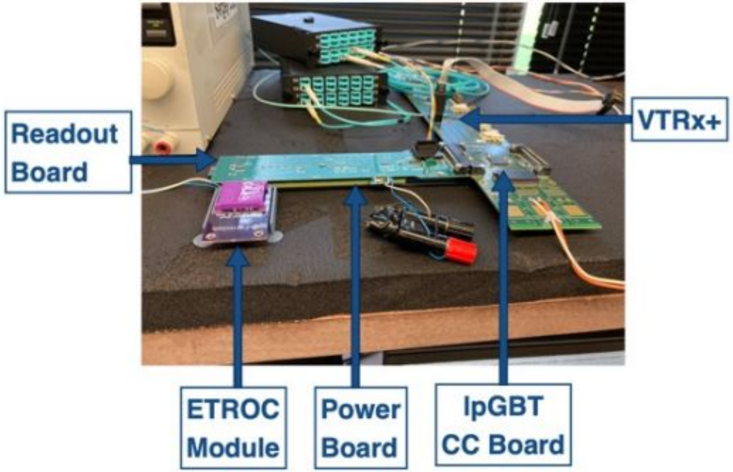
ceramic baseplate (for thermal contact and mechanical support)

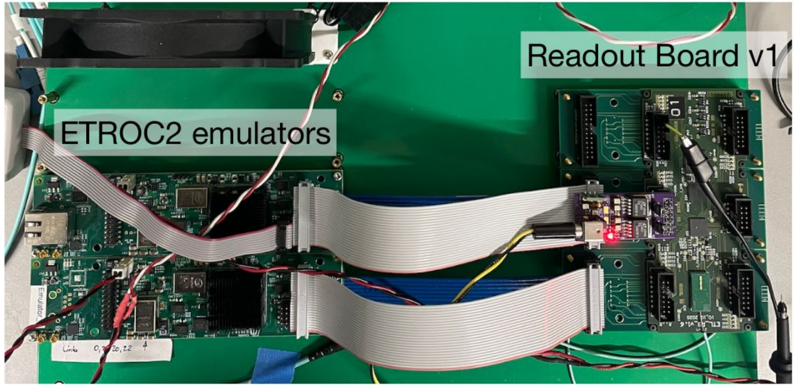
ETL electronics

The full-size 16x16 ETROC2 expected in March '23 → several activities ongoing while waiting for it

Established 1st generation system based on ETROC1 (4x4)

- full system DAQ using ETROC1
- Signal can come from either internal charge injected with ETROC chip or from the LGAD sensor





- FPGA-based emulation of ETROC2: enable development of DAQ and testing of readout board in advance of ETROC2