Photon-to-Digital Converters – 3D Integrated Digital Single-Photon Detector Arrays Enabling Time-of-Flight PET and CT

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CAP Congress, Saskatoon, June 2025

Institut interdisciplinaire d'innovation technologique UdS
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Outline

UDS

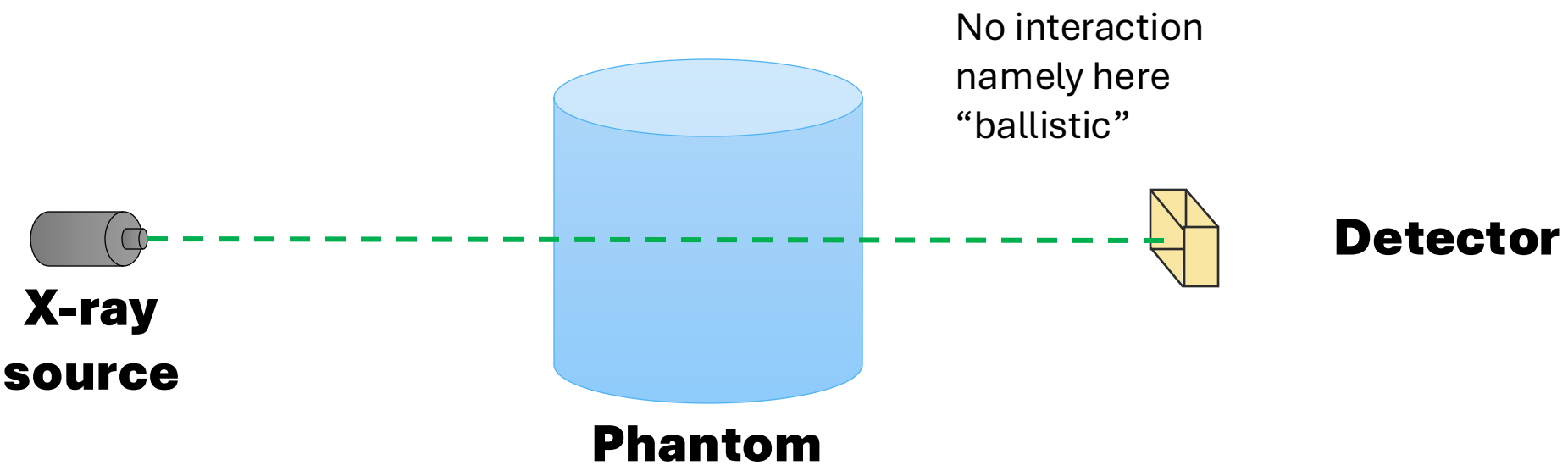
- Using photon time-of-flight information to reduce radiation dose in medical imaging
  - Requires measuring single photons
  - Timestamping the detection of each photon
- Photon-to-Digital Converter
  - Concept and fabrication
- Embedding digital signal processing
  - Towards 10 ps Time-to-Digital Converters
  - Aligning, sorting, binning timestamps

ToF Computed Tomography

Using time-of-flight to exclude noise from scattering X-ray photons

Physical interaction processes

How is build an image?

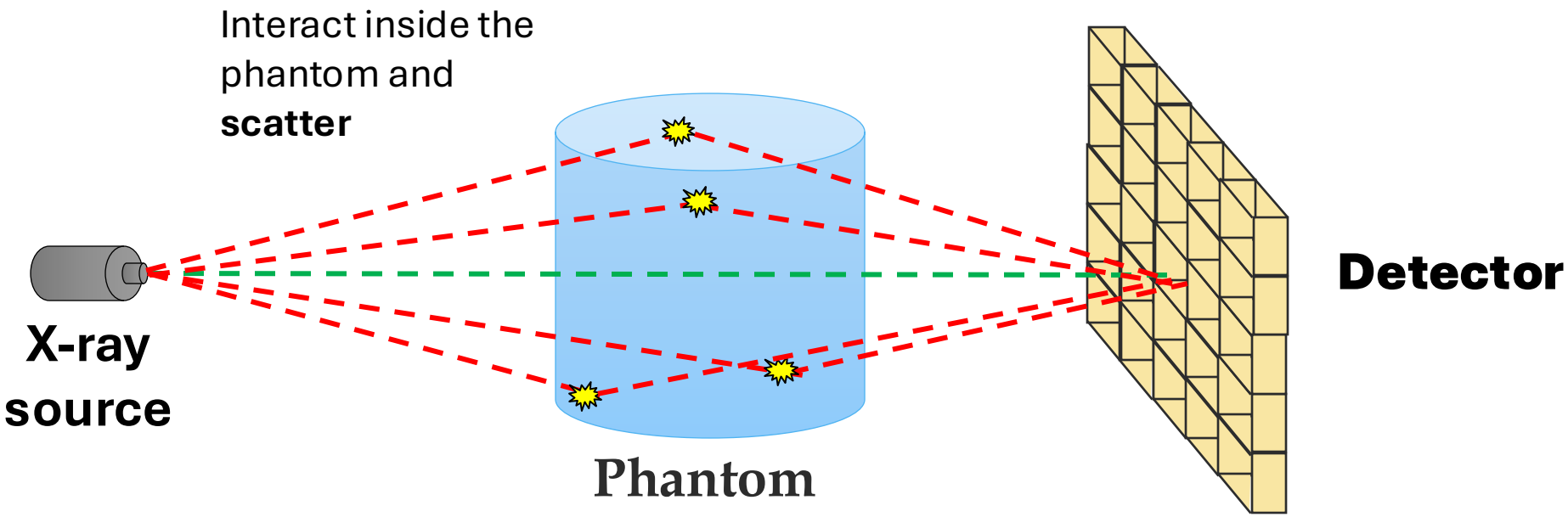


$$\mu = \mu_{pe} + \mu_{Com} + \mu_{Ray}$$

- The image is created by the contrast of the photons that are absorbed by photoelectric effect and the ballistics.
- We measure the total attenuation, which is the sum of the attenuation from the photoelectric effect, Compton and Rayleigh scattering.

Physical interaction processes

A scattering problem



$$\mu = \mu_{pe} + \mu_{Com} + \mu_{Ray} - f(\mu_{Com+Ray})$$

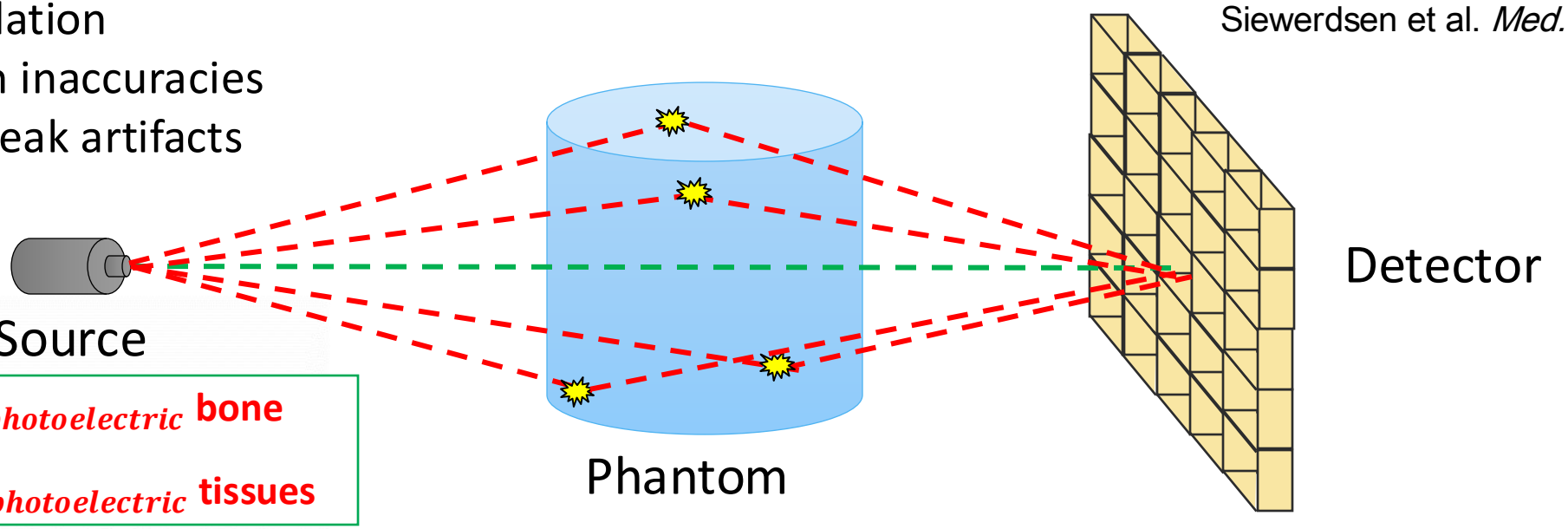
Need for diagnostic quality

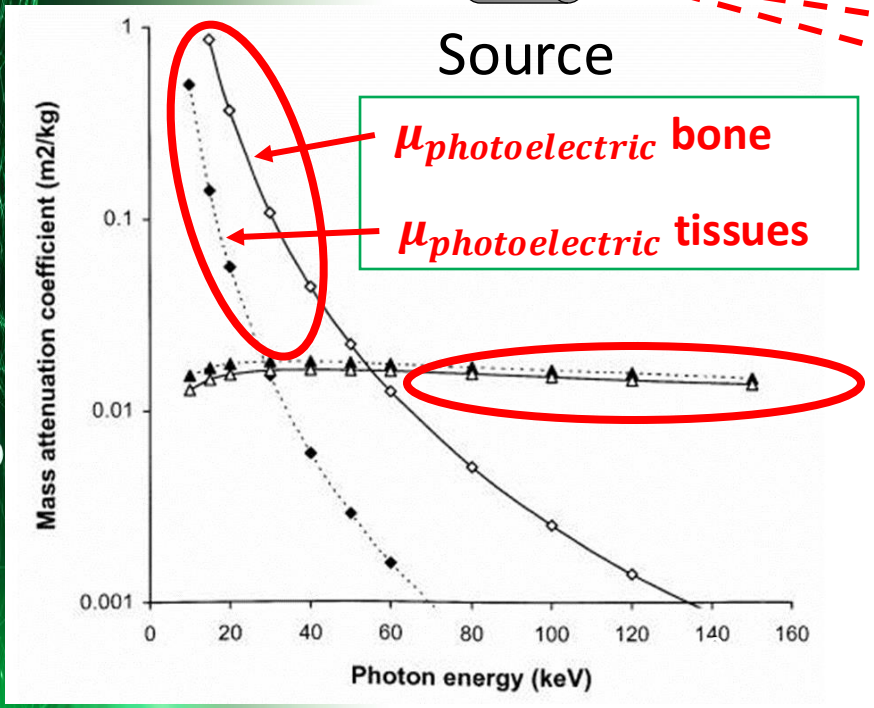
CNR high with low dose

Negative impacts from scatters:

- CNR degradation
- Attenuation inaccuracies
- Cup and streak artifacts

Siewerdsen et al. *Med. Phys.* (2001).





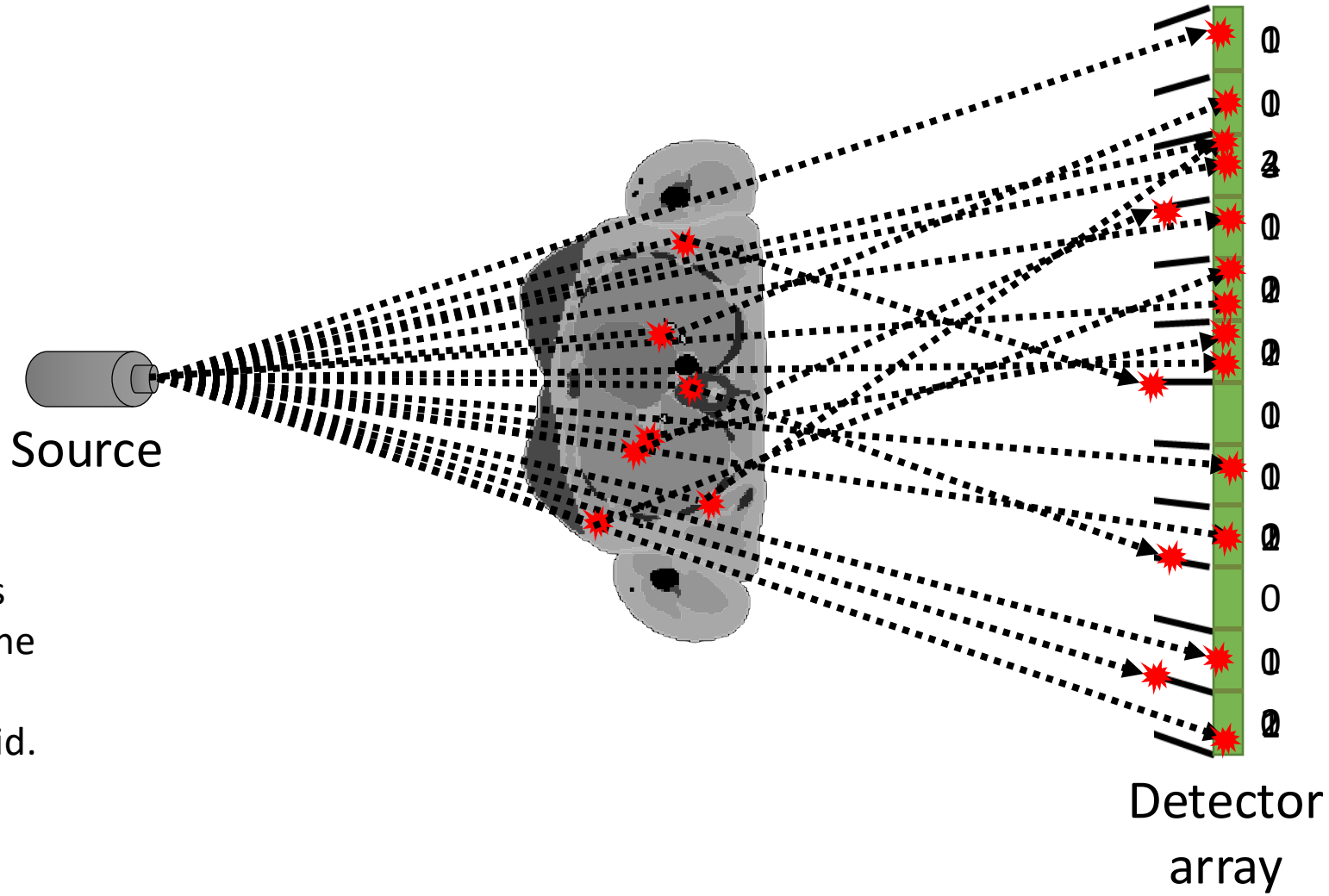
Scatters dominate for body imaging but do not generate contrast

Energy above 70keV carries more information because it passes more easily through the human body but..

$$\mu = \mu_{pe} + \mu_{Com} + \mu_{Ray} - f(\mu_{Com+Ray})$$

Physical interaction processes

Scatter rejection principle : anti-scatter grid



Try to reduce scatters as much as possible, and the solution adopted is to install an anti-scatter grid.

ToF Scatter Rejection Principle

How do that?

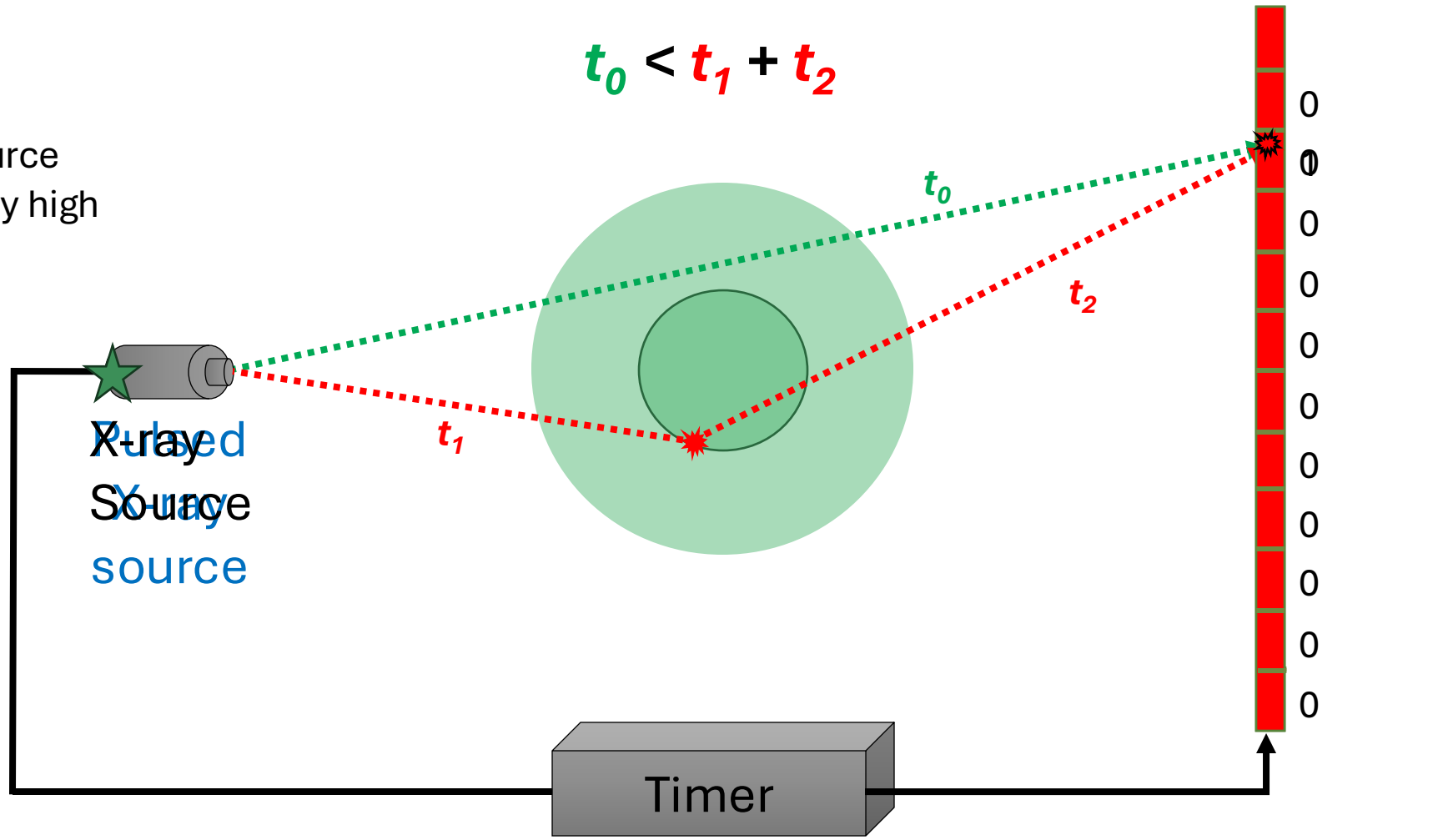
To do this we need:

- Synchronized pulsed X-ray source
- Time-resolved detectors of very high precision (~10-200 ps FWHM)

Threshold for rejection:

t_{th} ~10-500 ps FWHM

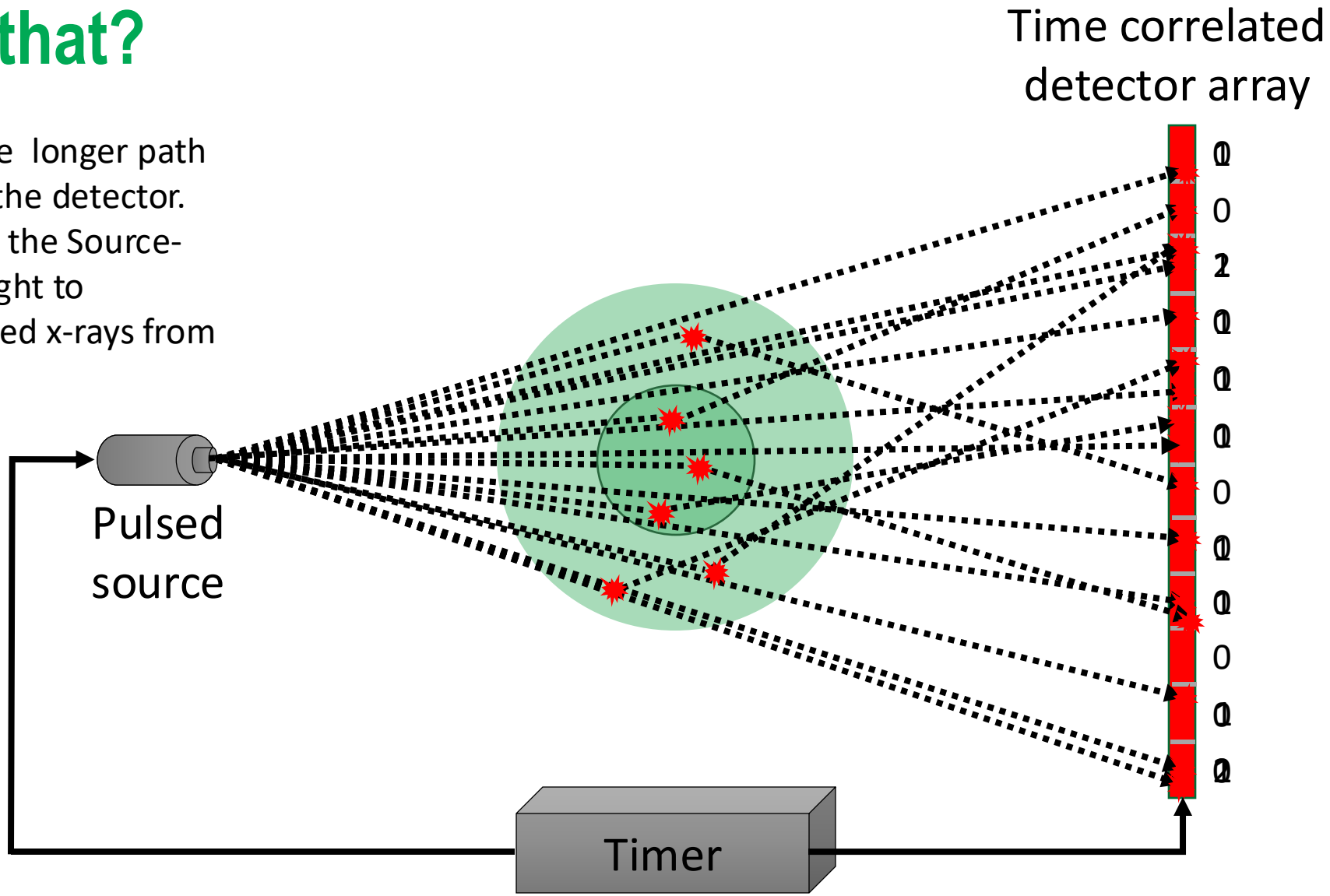
$$t_1 + t_2 > t_0 + t_{th}$$



ToF Scatter Rejection Principle

How do that?

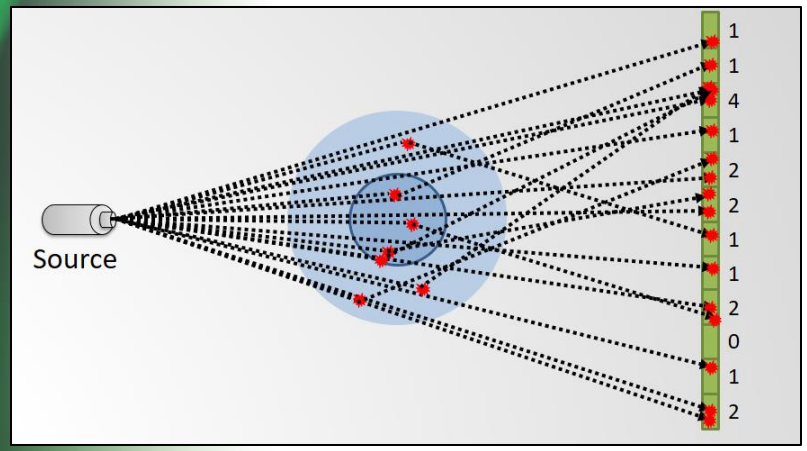
Scattered x-rays take longer path from the source to the detector.
→ We can measure the Source-Detector time-of-flight to discriminate scattered x-rays from primary x-rays

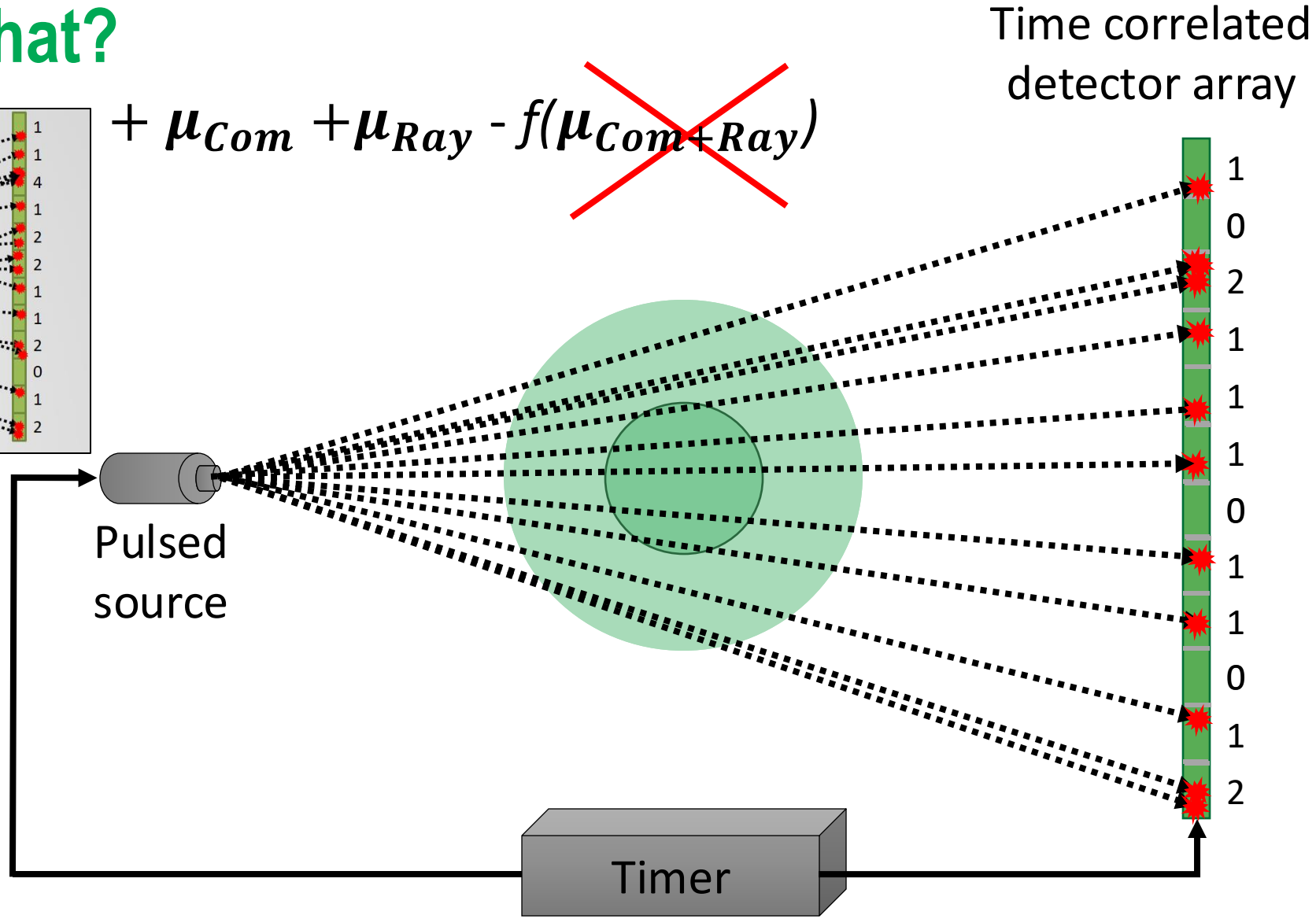


ToF Scatter Rejection Principle

How do that?

$$+\mu_{Com} + \mu_{Ray} - f(\mu_{Com+Ray})$$





How to reduce the dose?

A new path is proposed at Sherbrooke for dose reduction

X-ray without anti-scatter grid
&
Photon counting
with energy measurement

→

Time of flight
scatter rejection

Objective:

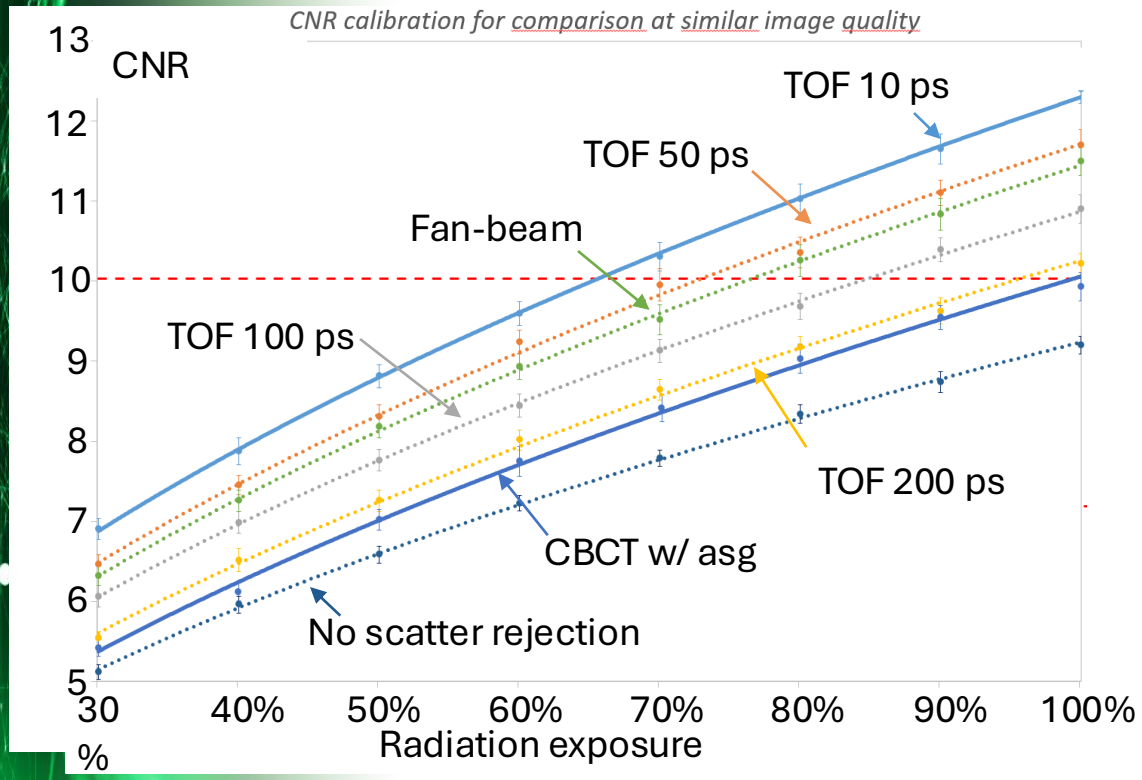
Reject scattered X-rays without the use of an anti-scatter grid

- **Larger fraction of X-ray photons effectively used in the image**
  - Dose reduction at constant Contrast-to-Noise (CNR)
  - Increase Contrast-to-Noise at constant dose

- Can lead **to dose reduction factor of 2x**

Dose reduction at equivalent image quality CBCT vs ToF CBCT

- With a constant dose, CNR improve with TOF-CT threshold
- Dose reduction increase with TOF CT Threshold at



Simulation	CNR at 100% photon ($\alpha = 1$)	Dose reduction (at $\mathrm{CNR}_\alpha = 9.9$)
CB TOF 10 ps	12.4	35%
CB TOF 50 ps	11.7	28%
CB TOF 100 ps	10.9	15%
CB TOF 200 ps	10.2	5%
Fan Beam	11.5	25%
CB with ASG	9.9	0%

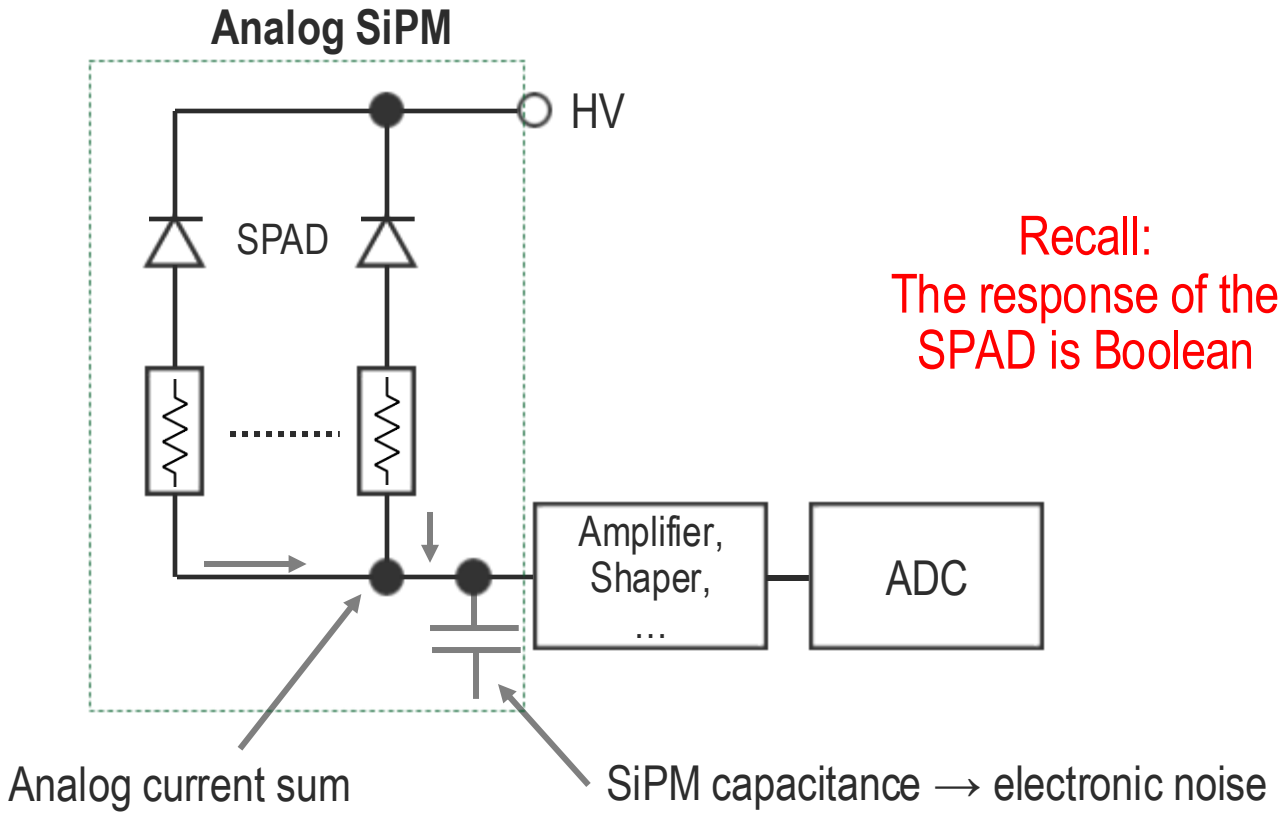
- Dose reduction depend on the grid it is compared with

From G. Belanger, J.Rossignol, , Y. Berube-Lauziere, and R. Fontaine (2024), *Not submitted at this time*

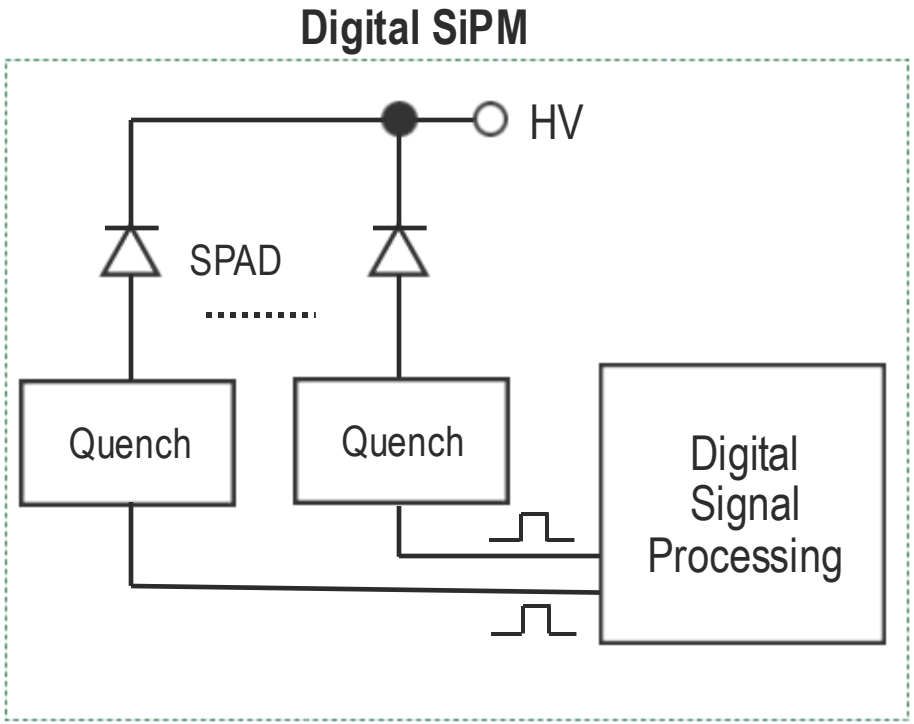
The Photon-to-Digital Converter Concept

How to turn a single photon into a digital pulse

SiPM – Silicon Photo Multiplier: an array of SPADs



Recall:
The response of the SPAD is Boolean



The amplifier transforms charge into voltage and then BACK to digital.

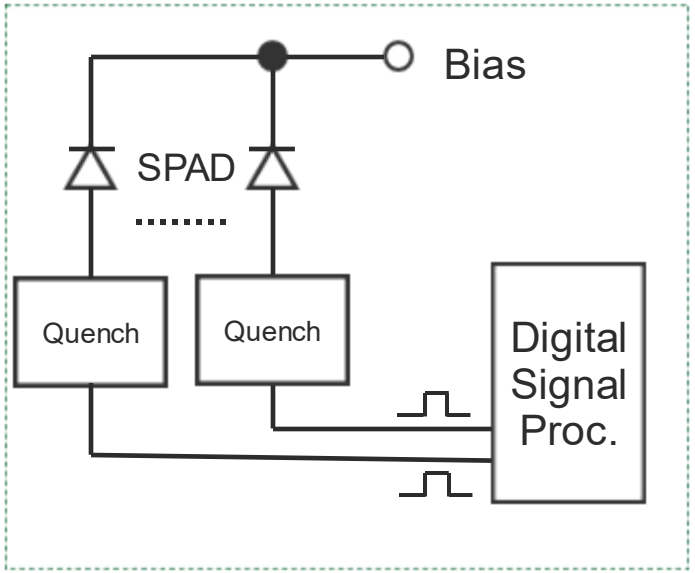
Individual SPAD readout, no D/A+A/D conversion. Everything stays digital.

3D Photon-to-Digital Converters

UDS

- **Digitally readout array of Single Photon Avalanche Diode (SPAD)**

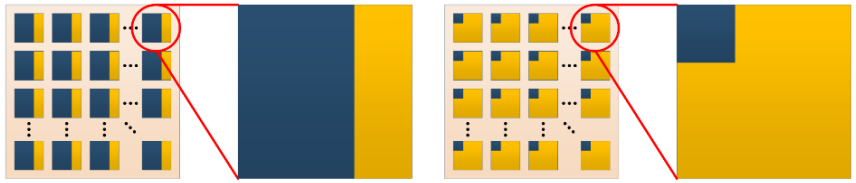
Photon-to-Digital Converter



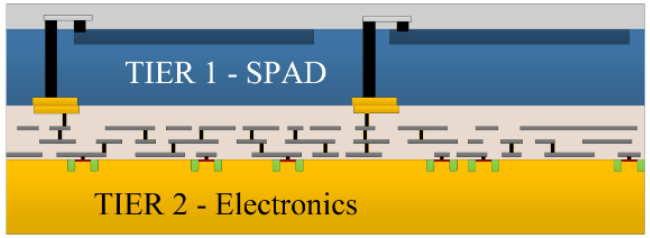
- Direct digital conversion:
  - Single photon resolution on the whole dynamic range
  - Can lower power significantly consumption
- Disabling noisy SPADs: reducing noise
- Programmable hold-off delay: mitigation of afterpulsing
- Embedded signal processing: sum, dark count filters, time-to-digital conversion, etc.

Pratte JF et al. "3D Photon-to-Digital Converter for Radiation Instrumentation: Motivation and Future Works" (2021) Sensors;21(2):598. doi: 10.3390/s21020598

- **SPAD array and CMOS readout vertically stacked (3D) to form a single detector chip**



in 2D: loosing sensitive area



(c)

Development of the SPAD array layer and low power PDC

Thinned TSV-less Frontside Illuminated SPAD Array

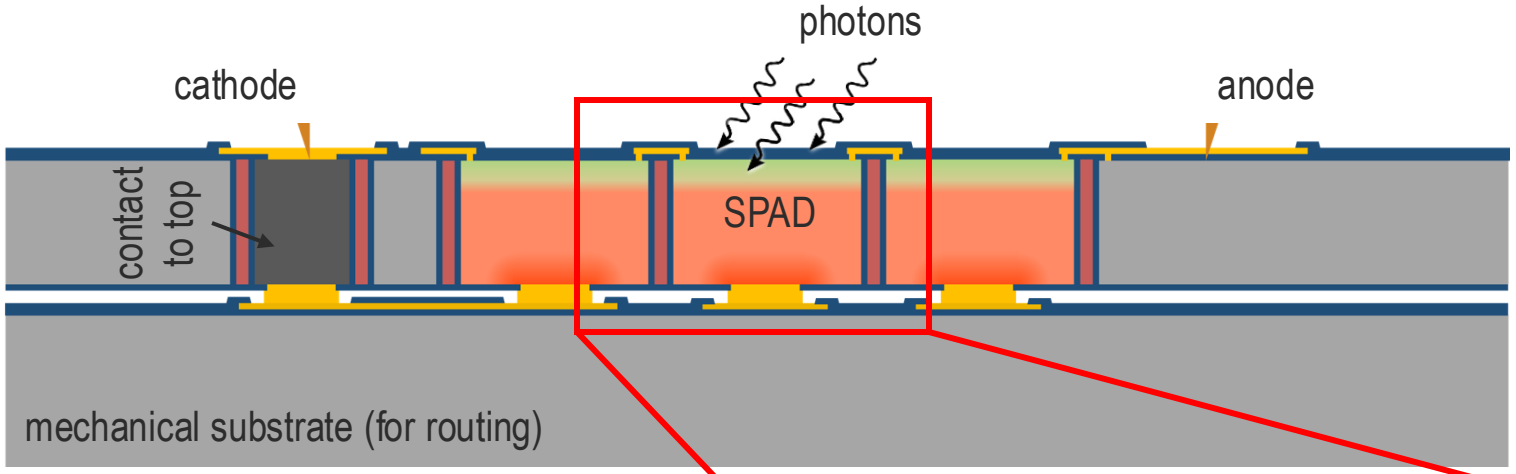
UDS

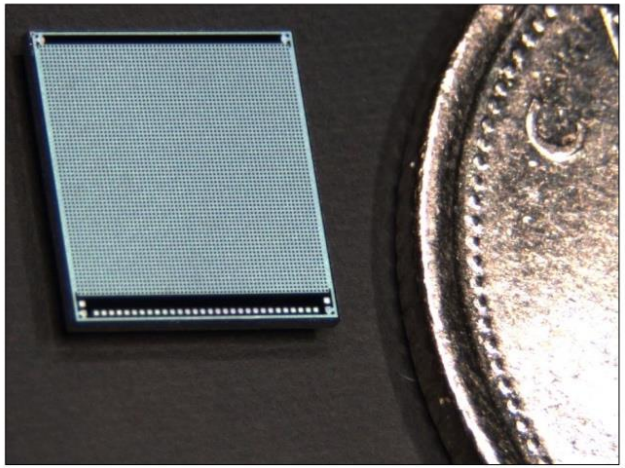
1st fabrication run completed

(Octobre 2024)

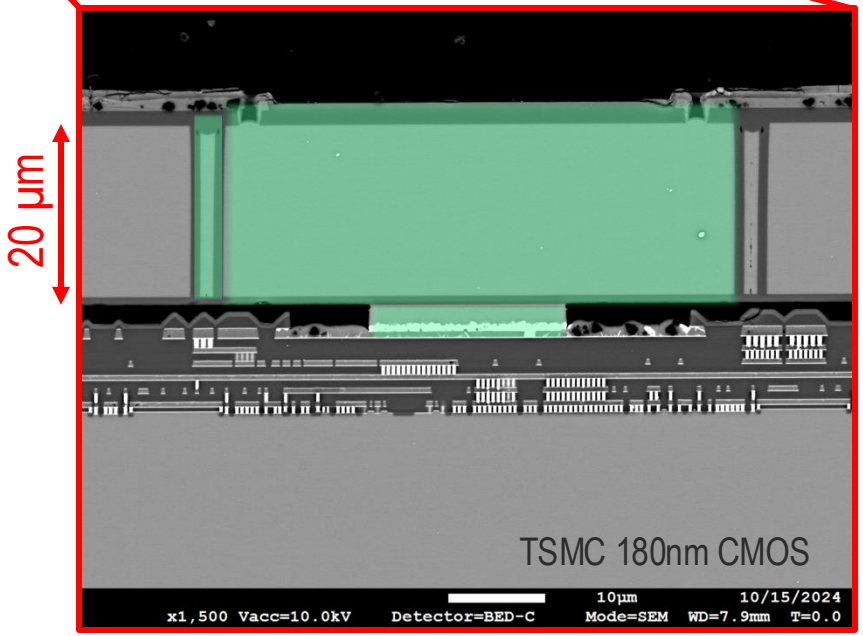
Thin SPAD layer + CMOS readout

- p^+n SPAD [1]
- 64 × 64 SPAD Array
- 78 µm pitch
- Al-Ge eutectic bonding
- 5.85 × 5.25 mm^2 die





3D SPAD array
(canadian 10¢ for reference)



SEM cross section image

1. Parent, Samuel, et al. "Single photon avalanche diodes and vertical integration process for a 3D digital SiPM using industrial semiconductor technologies." 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC). IEEE, 2018.

Fabricated by Teledyne DALSA

UDS

<u>High-end CCD process line</u>

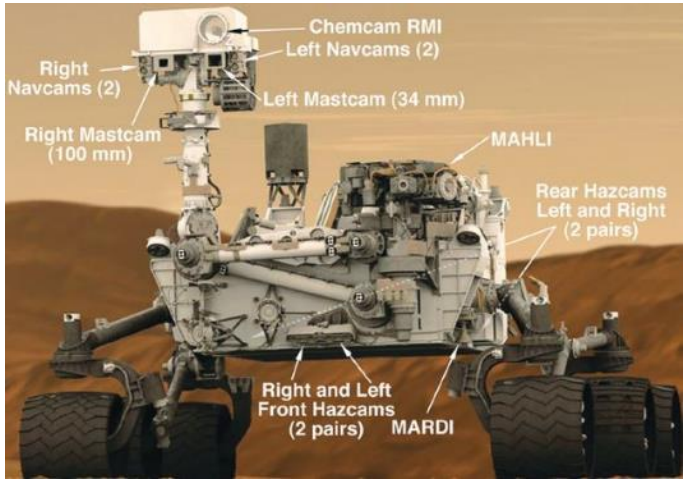
--> excellent for SPAD R&D

- 150 mm process line
- low contaminant / gold free clean rooms

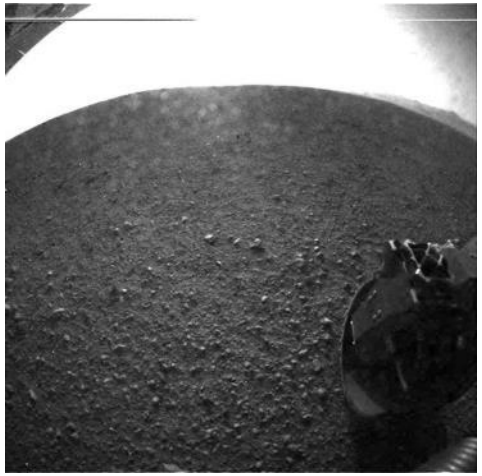
<u>World top 5 MEMS Foundry</u>

--> excellent for wafer level integration

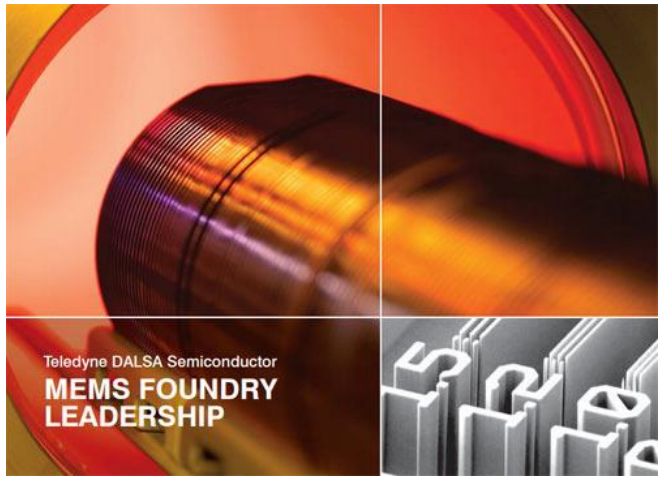
- 150 mm and 200 mm process line
- Wafer thinning, deep etching, bonding, ...



The Eyes of the Mars Curiosity Rover. Tech Briefs (2012)



Life on Mars: Rover landing gives boost to Canadian tech sector. The Globe and Mail (2012)



Courtesy of Teledyne DALSA

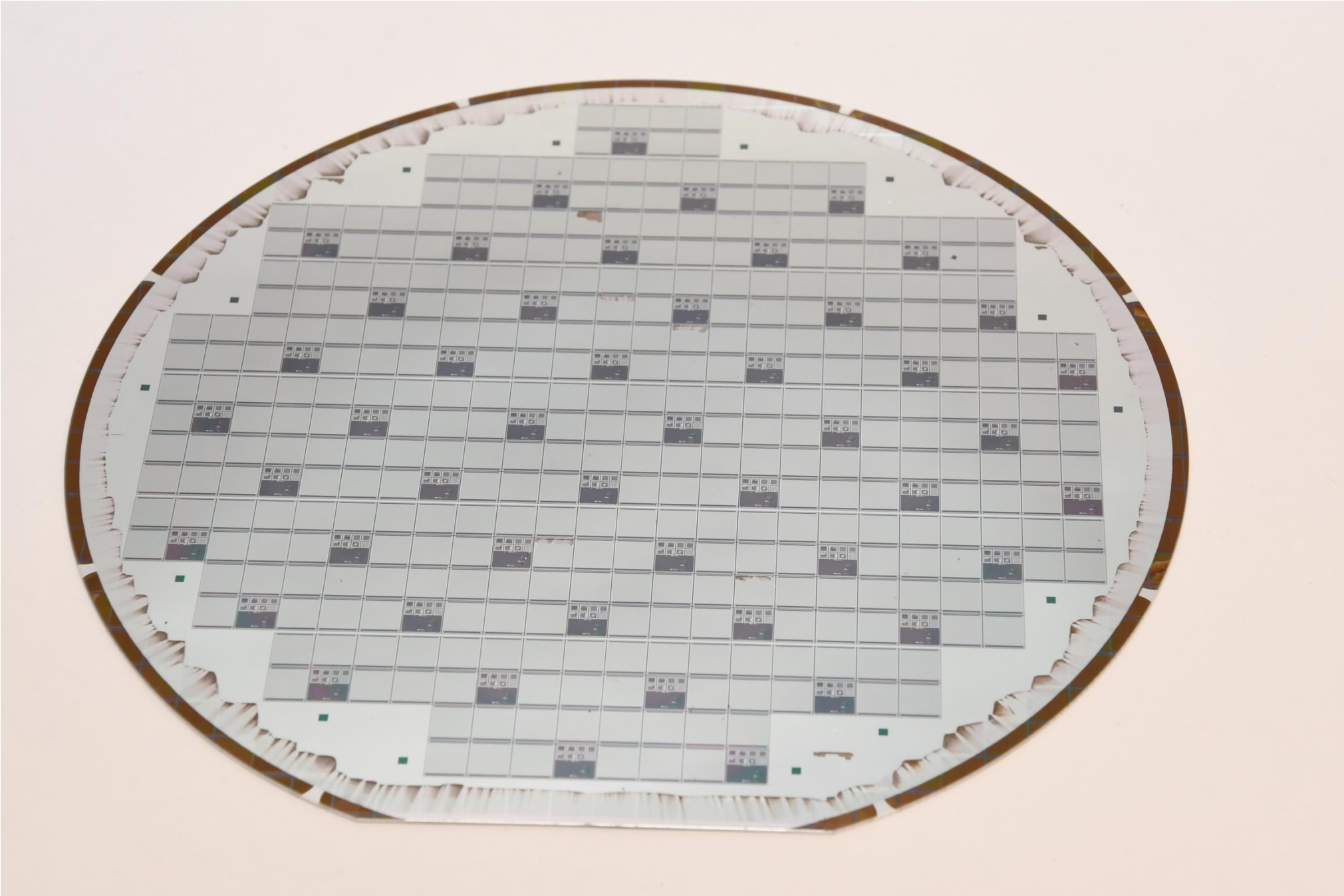
MEMS Foundry Rankings (2017 sales in US$M)	
STMicroelectronics	174
Teledyne DALSA	60
Silex Microsystems	50
TSMC	47
X-Fab	42

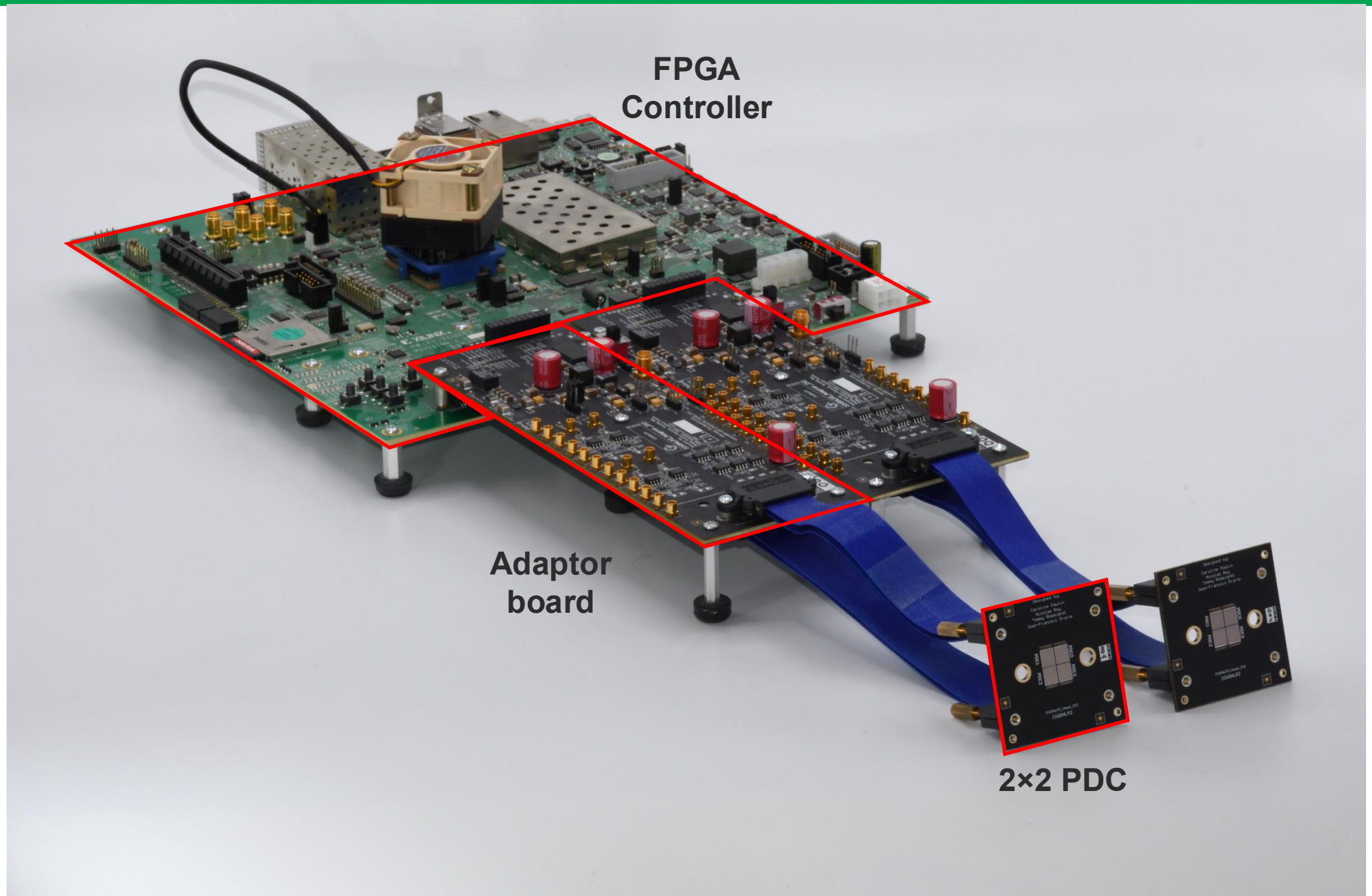
Status of the MEMS Industry 2018 Market and technology Report Yole Development (2018)

TELEDYNE DALSA
Everywhereyoulook™

Teledyne DALSA Semiconductor (est. 1980)

~ 500 employees located at Bromont near Montreal, Canada




FPGA
Controller
Adaptor
board
2×2 PDC

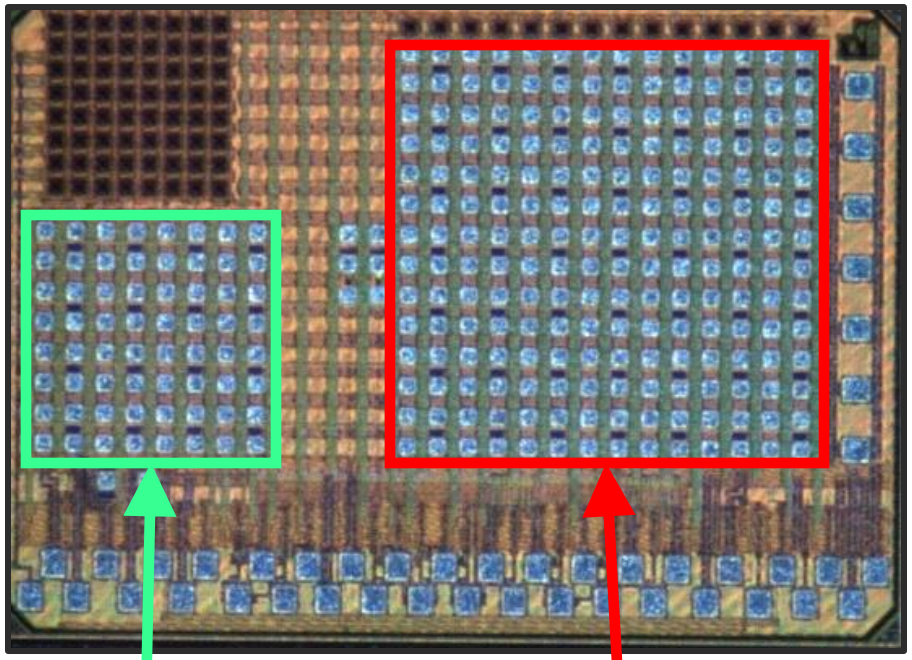
PDC designed for Time-of-Flight PET

(and ToF-CT,
and QKD,
and wavefront sensing,
and more)

Overview of the Second 65nm ASIC: PET + CT + QKD

UDS

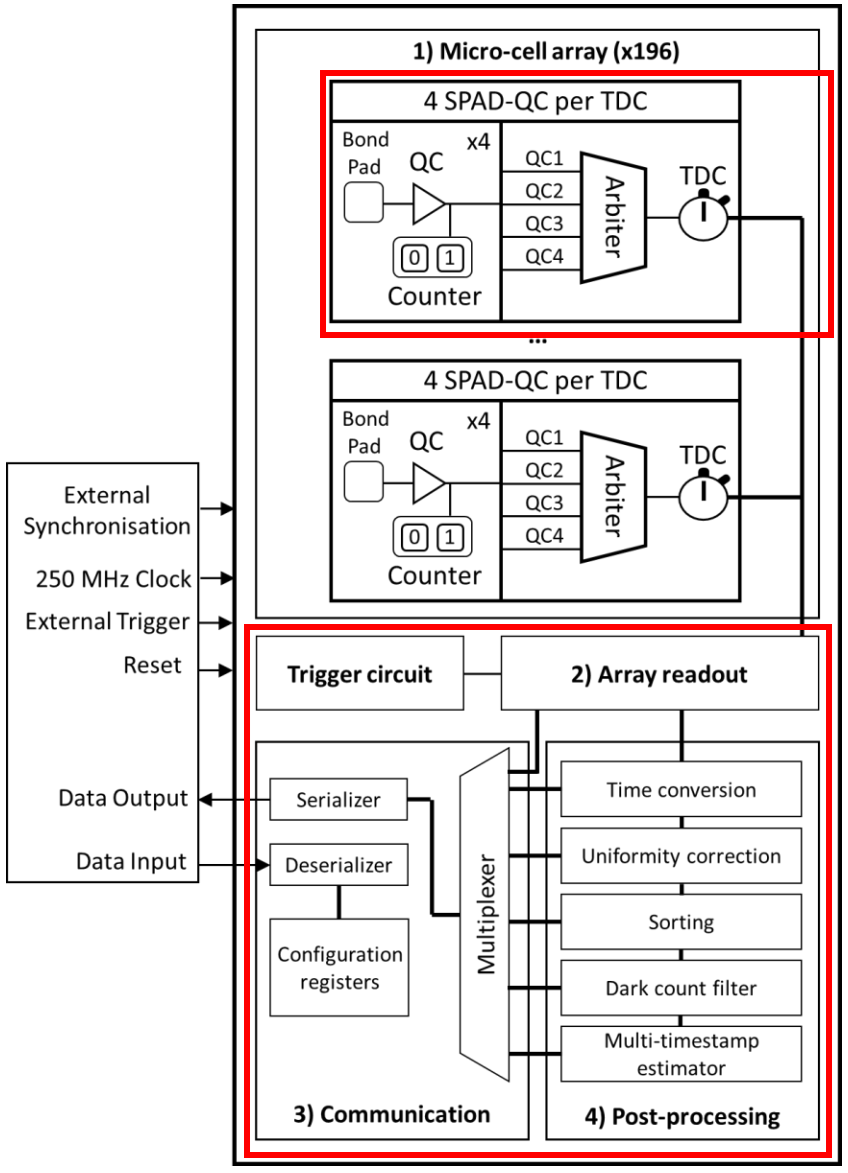
- TSMC 65 nm CMOS
- 16 × 16 pixels in 1.1 × 1.1 mm^2



Rev 2. 2021

QKD

PET/CT



1 Sub-20 ps TDC for 4 SPADs

Advanced digital signal processing:

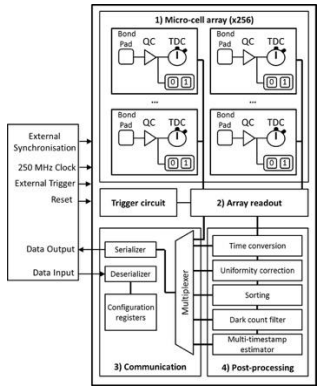
- Time windowing
- TDC code to time conversion
- Uniformity correction
- Timestamp sorting
- Dark count filtering
- BLUE

And for QKD

- Time categorization

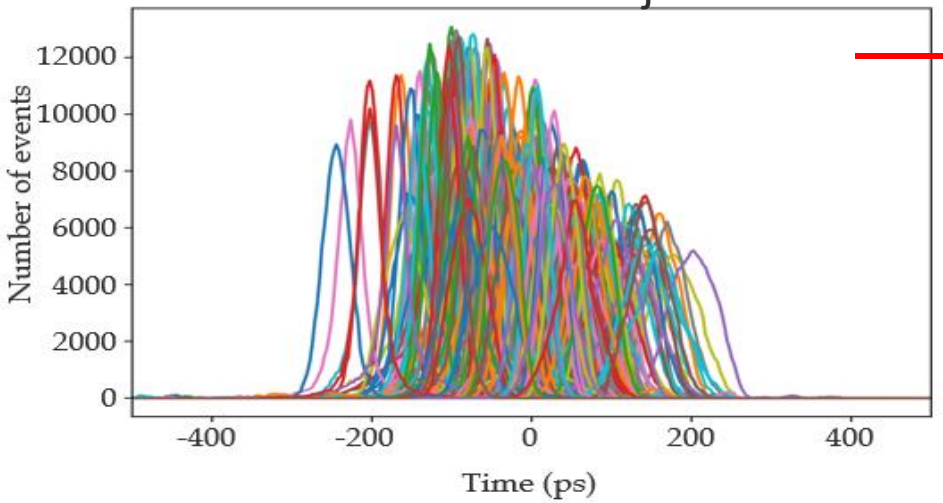
Embedded Digital Signal Processing Example: Uniformity Correction

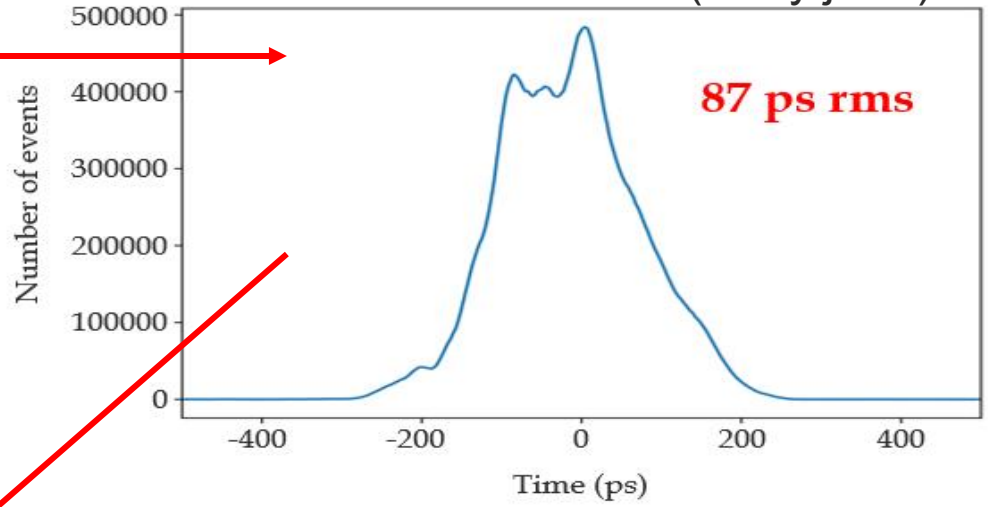
UDS

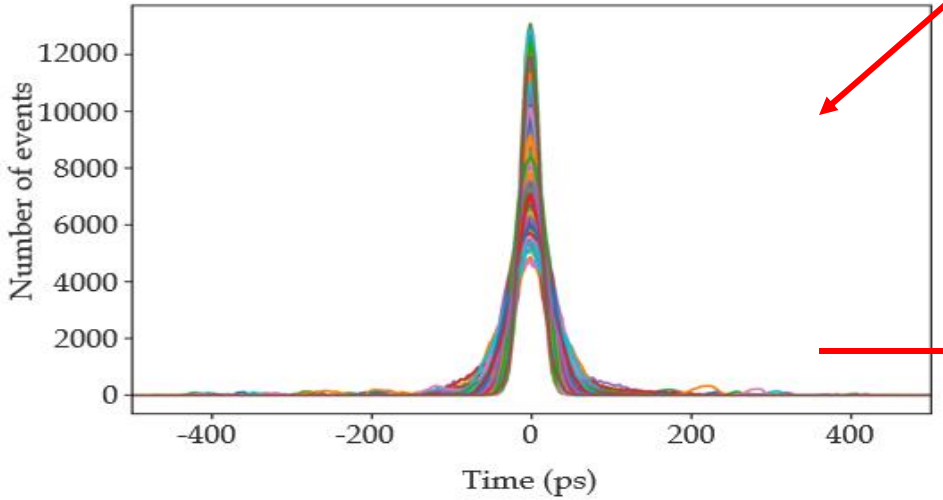


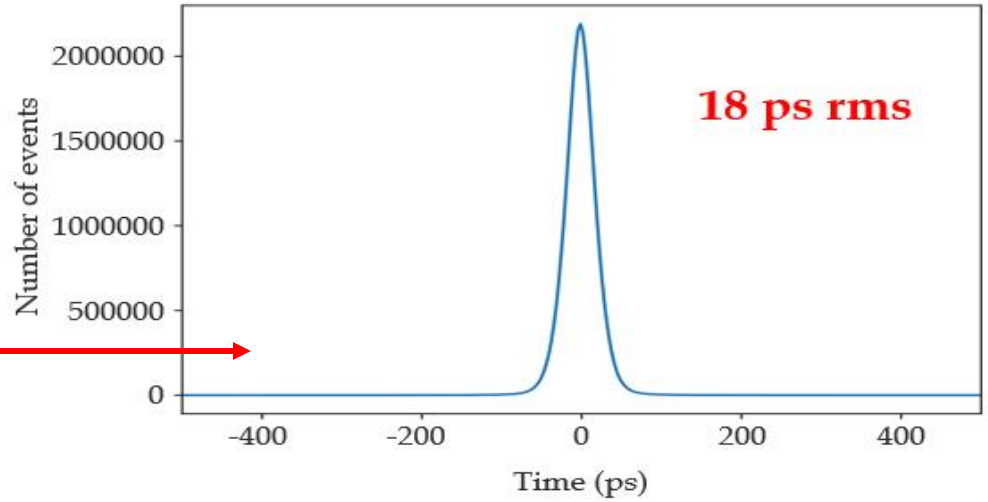
256 channels jitter

Sum of all channels (array jitter)







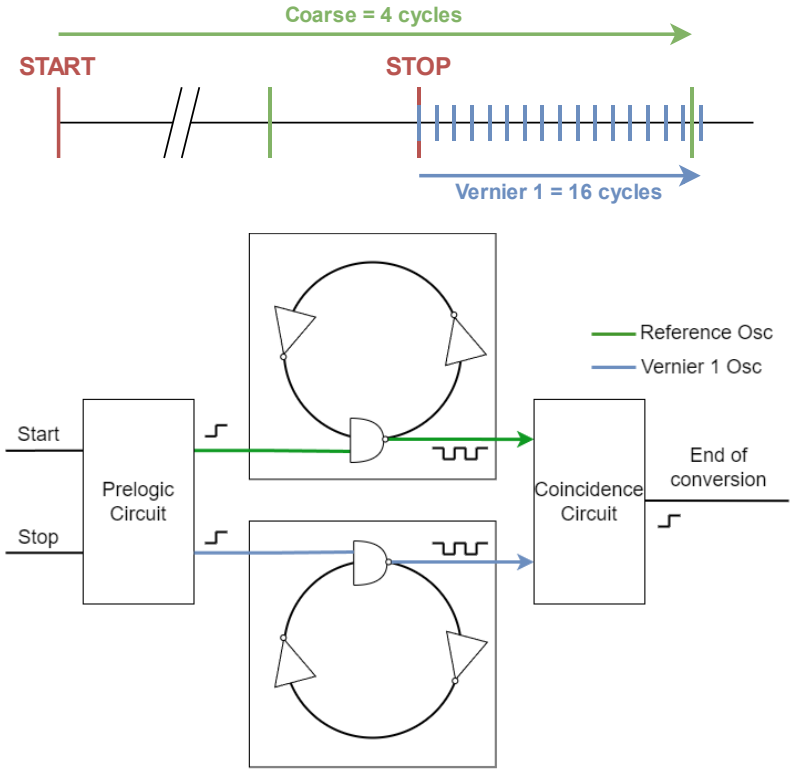


From single-vernier to multi-vernier TDC

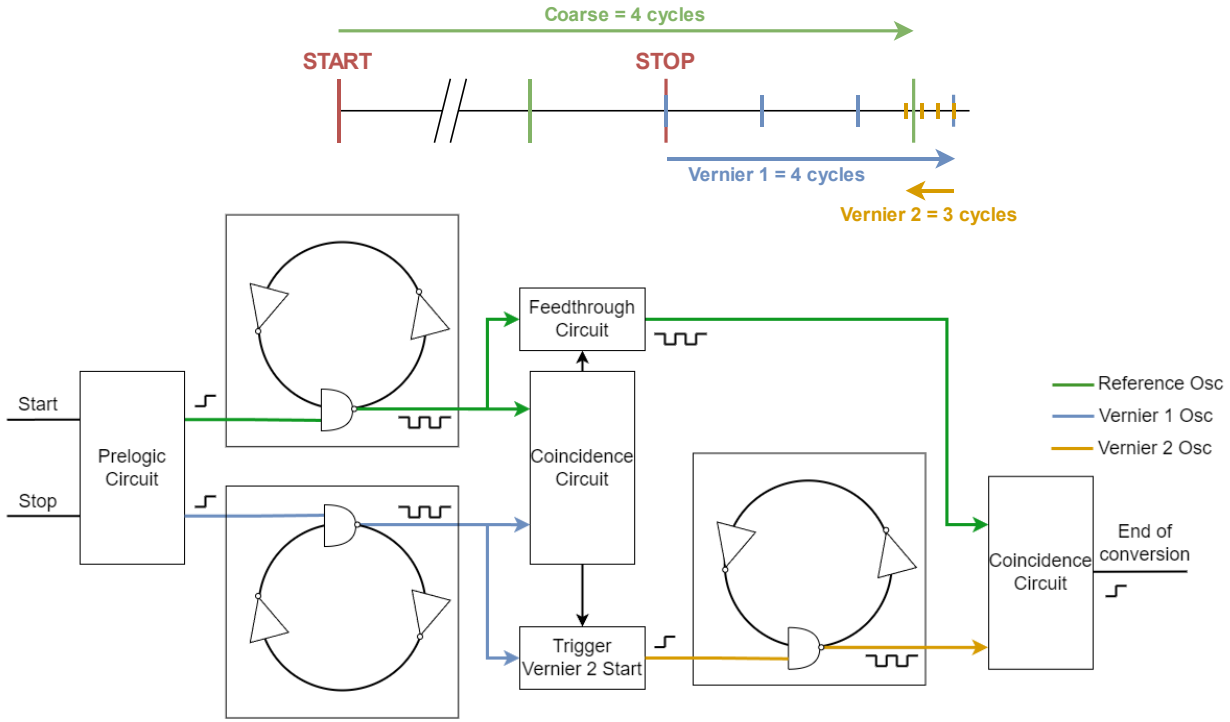
UDS

- To reduce conversion time (lower number of cycles for a given time interval)
- While improving (or at least maintaining) resolution and precision (jitter)

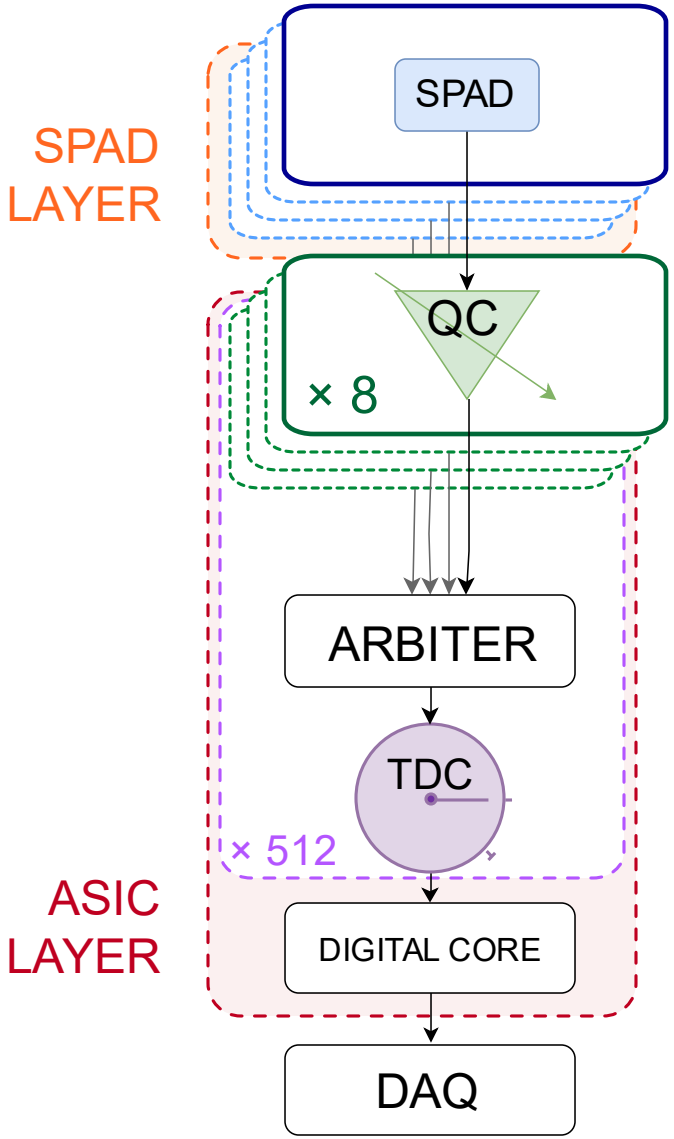
Single vernier TDC



Multi-vernier TDC

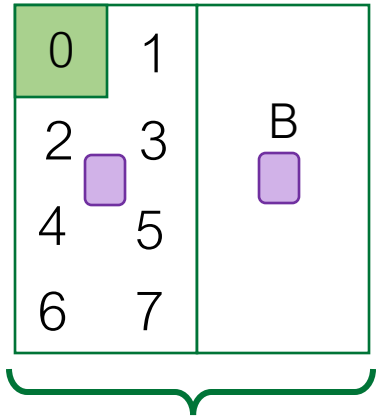


PDC – Architecture 8-to-1

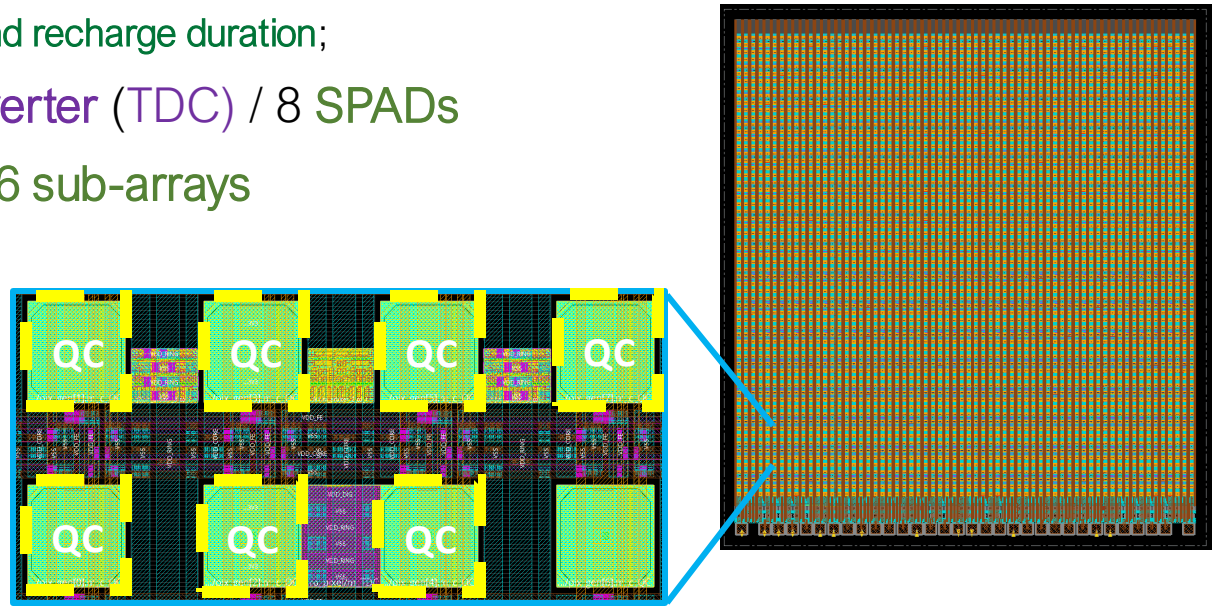


The future 5 × 5 mm^2 65 nm PDC will feature:

- CMOS layer designed in TSMC 65 nm LP technology;
- 4096 SPADs designed in collaboration with Teledyne DALSA;
- SPAD pitch = 78 × 78 μm^2;
- Individual quenching circuit (QC) per SPAD;
  - Inverter FE with configurable threshold;
  - Expected sub-10 ps QC timing jitter;
  - Configurable holdoff and recharge duration;
- 1 Time-to-Digital Converter (TDC) / 8 SPADs
- Large array split into 16 sub-arrays with local processing

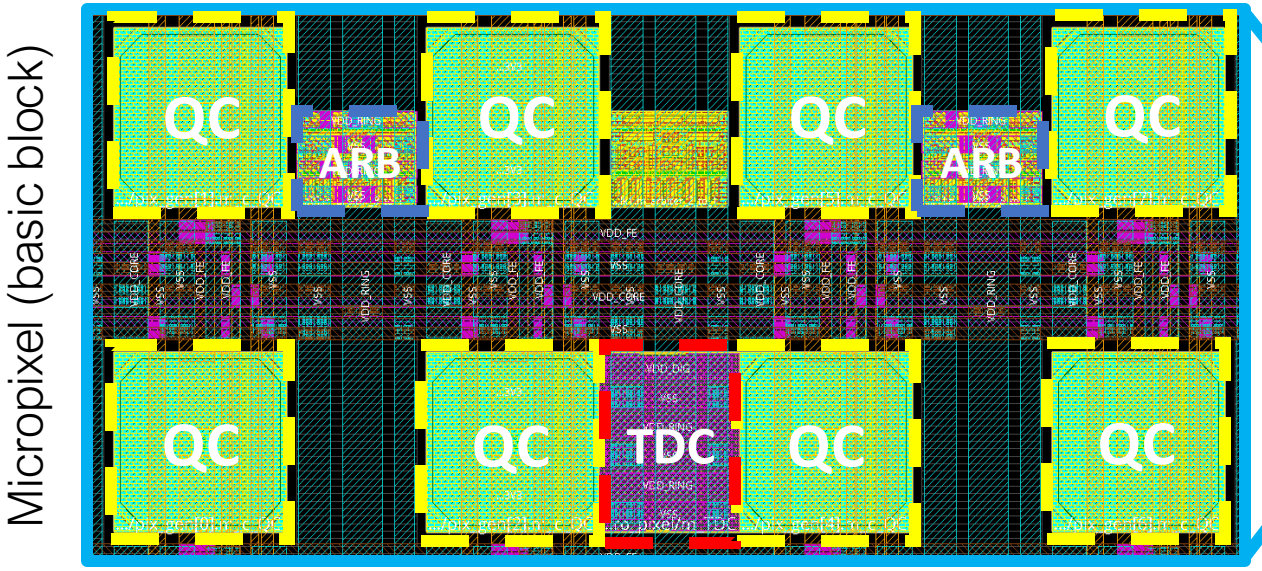


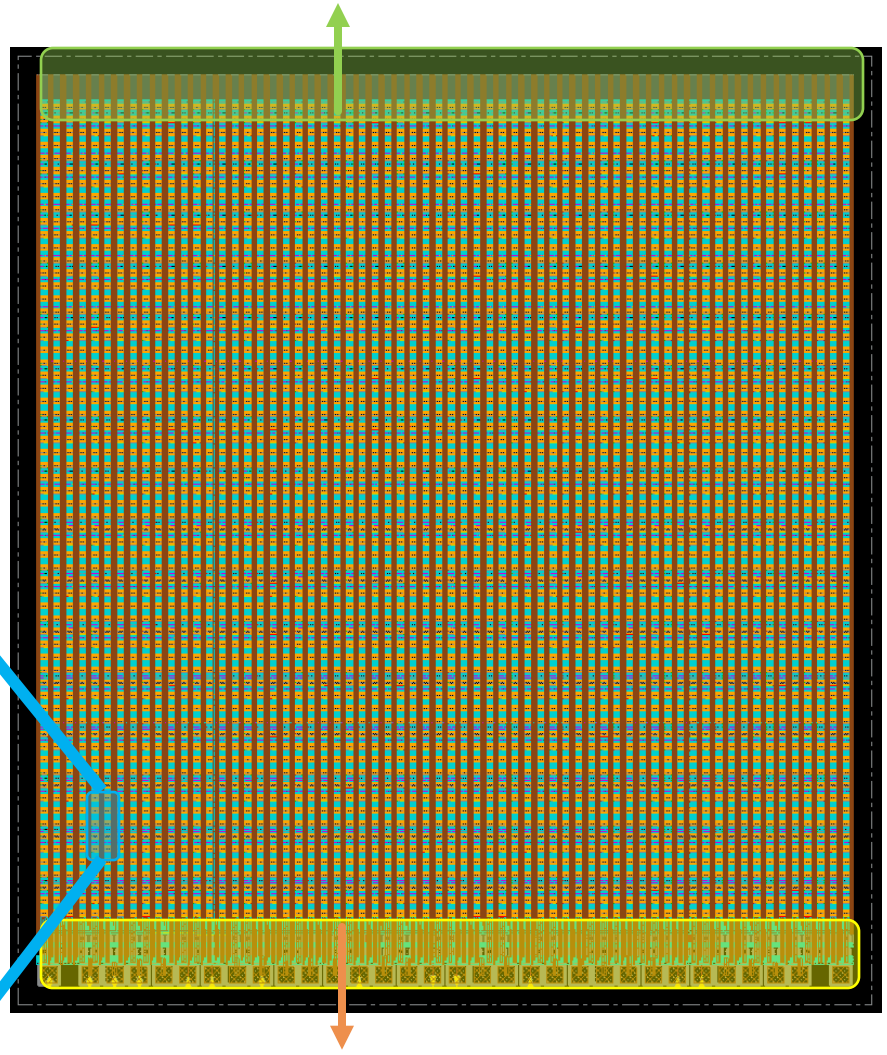
16 SPADs, 2 TDCs



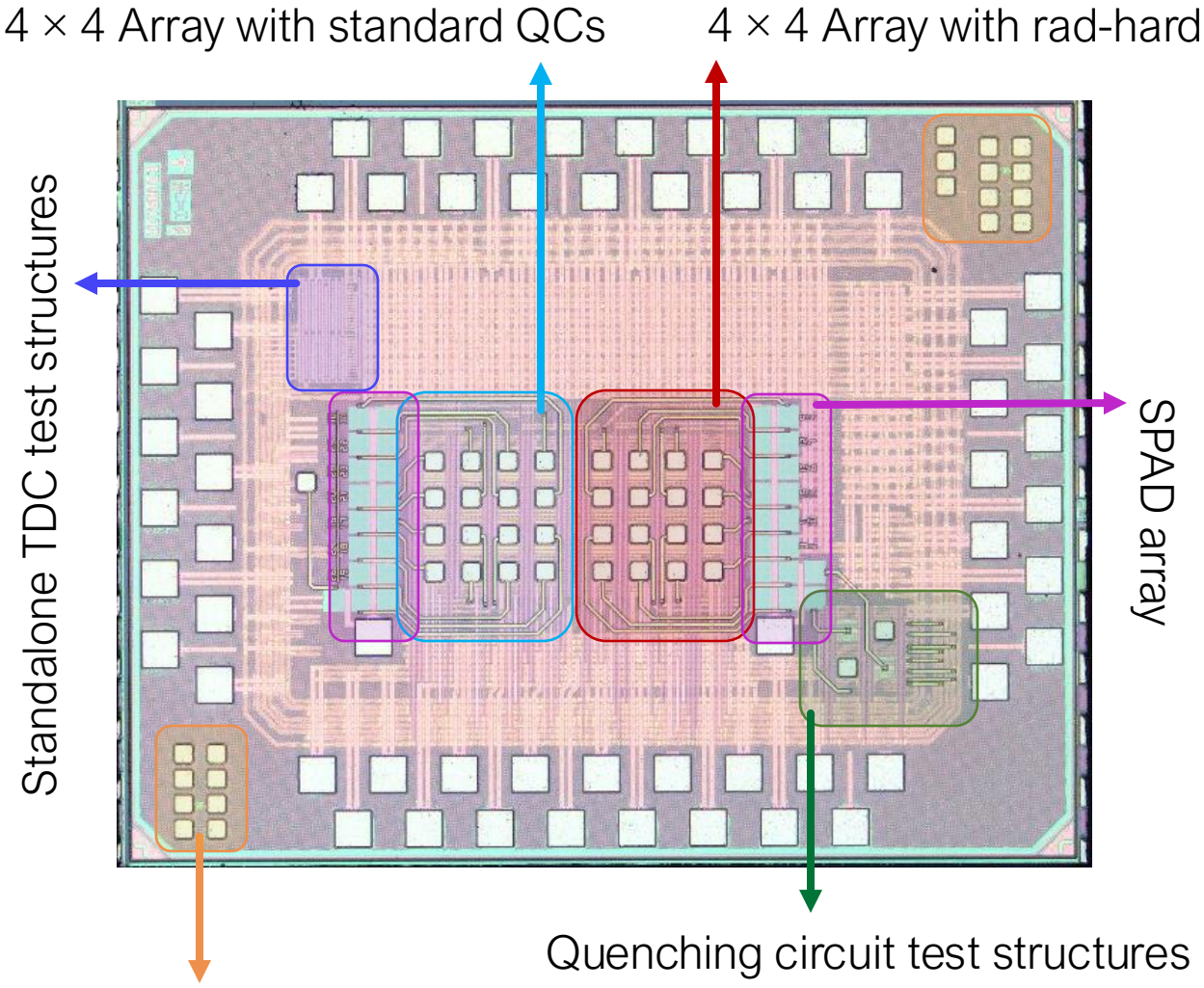
PDC Floorplan

- All analog components placed (40% array area)
- Digital component area known (P&R)
- Top level architecture complete
- Reconfigurable floorplan

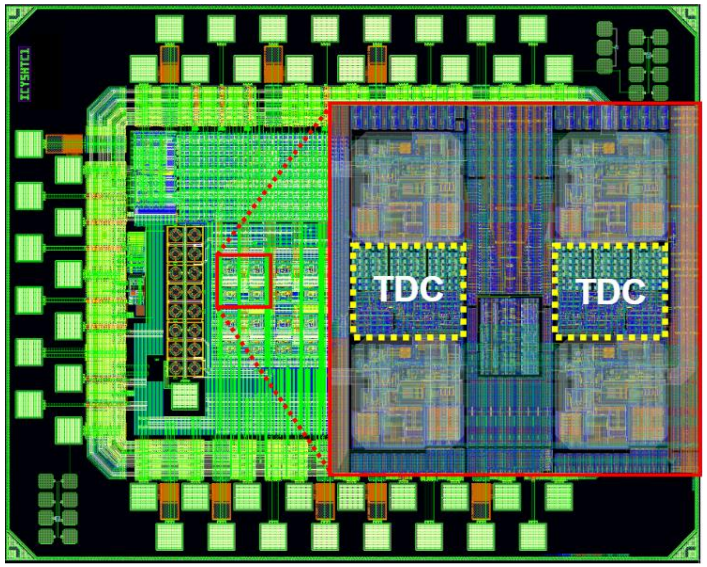




PDC - test-chip implementation



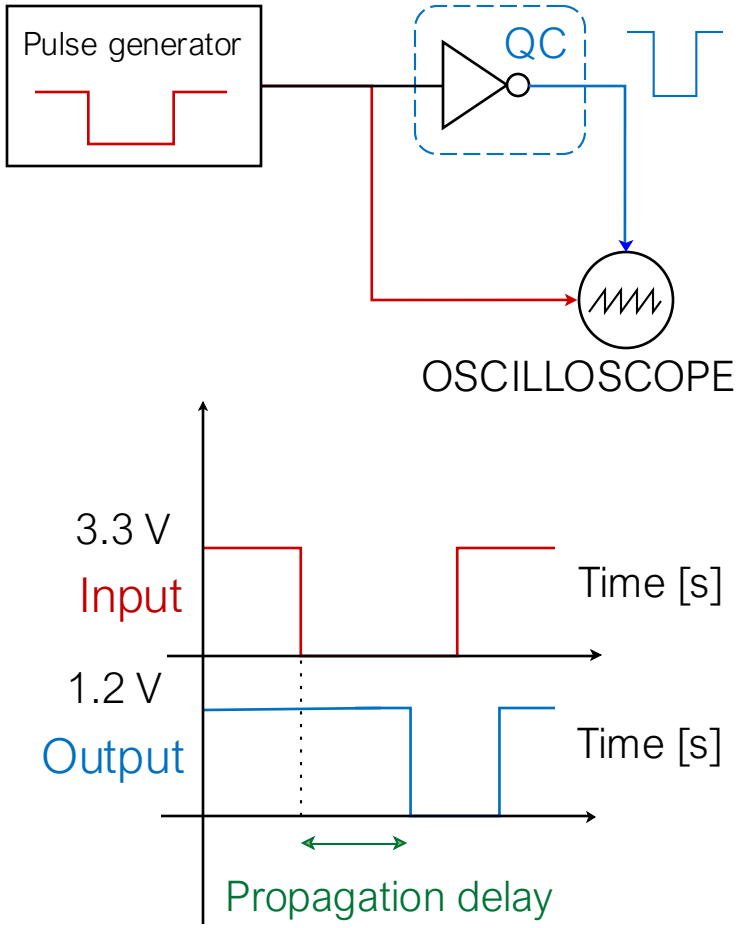
Time-to-Digital Converter 65 nm implementation

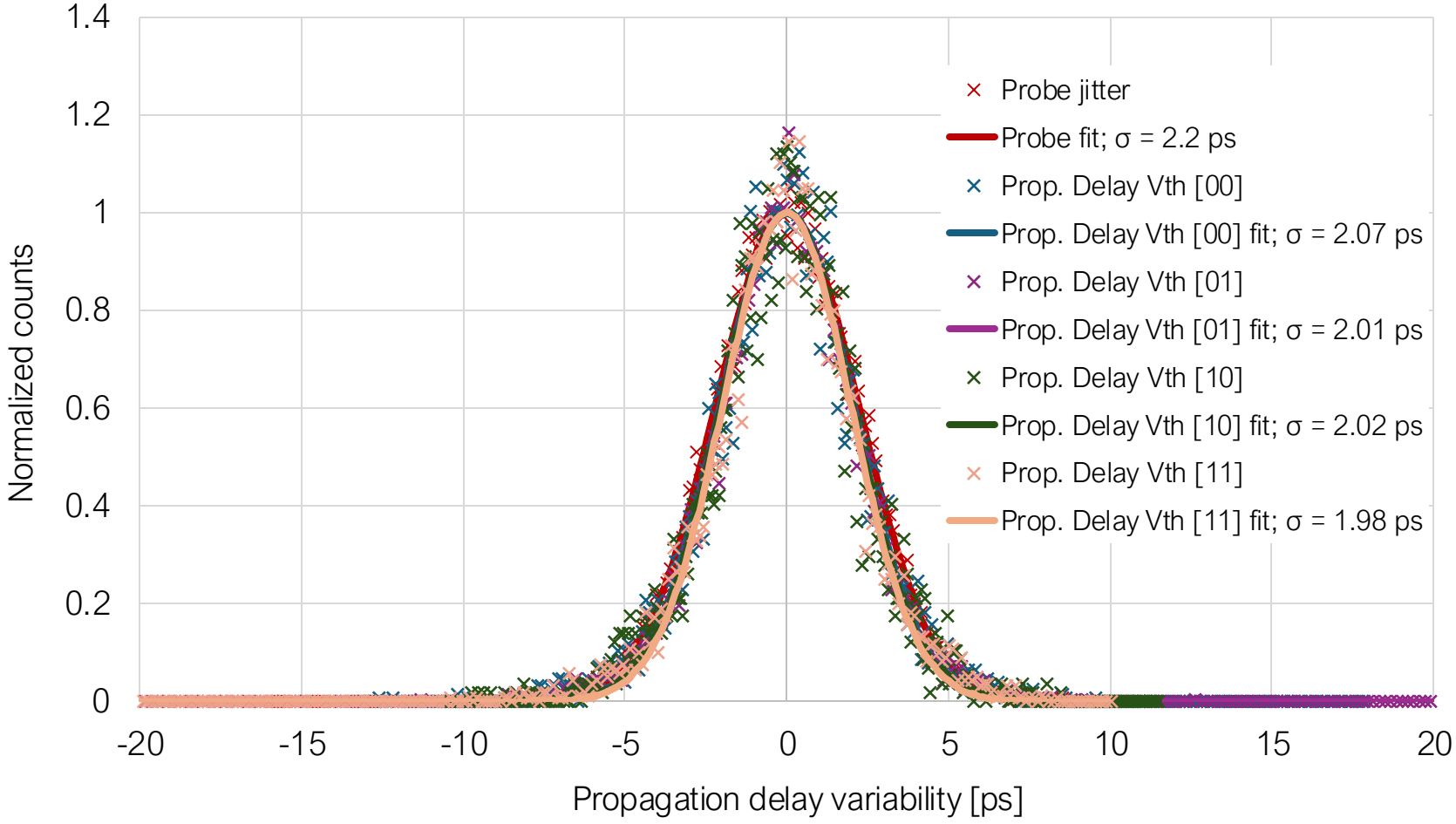


- The TDC uses a patented multi-Vernier architecture
- A single TDC is 35 × 43 μm^2
- Individually configurable
  - A calibration step is required
- Test implementation includes 2 TDCs for 4 QCs
  - Enables uncorrelated TDC analysis
- Resolution (LSB) can be changed

First results - Quenching circuit jitter

To measure the timing jitter we sent a steep pulse to the input of the QC and measured the **propagation delay variability**.



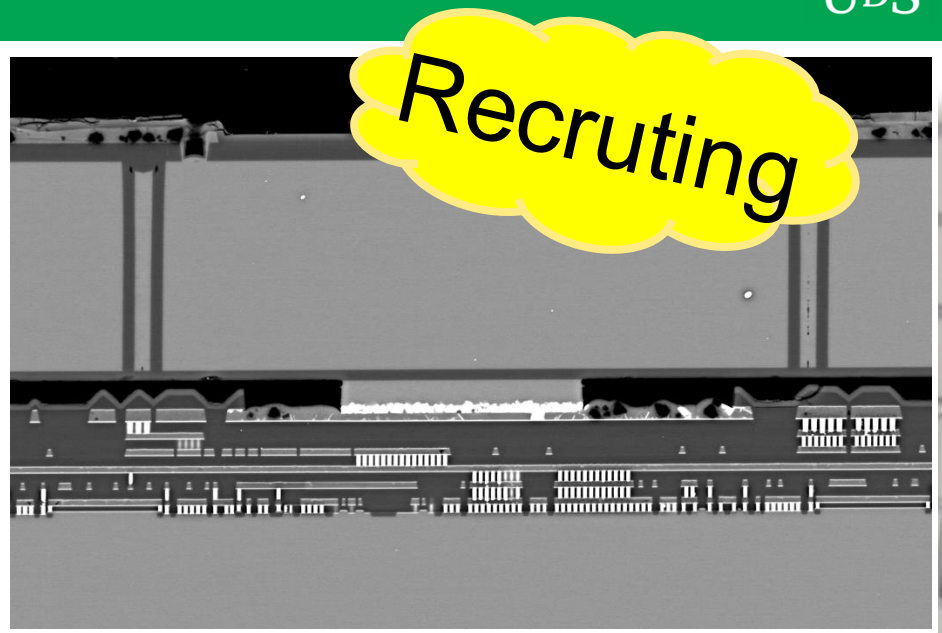


Conclusion

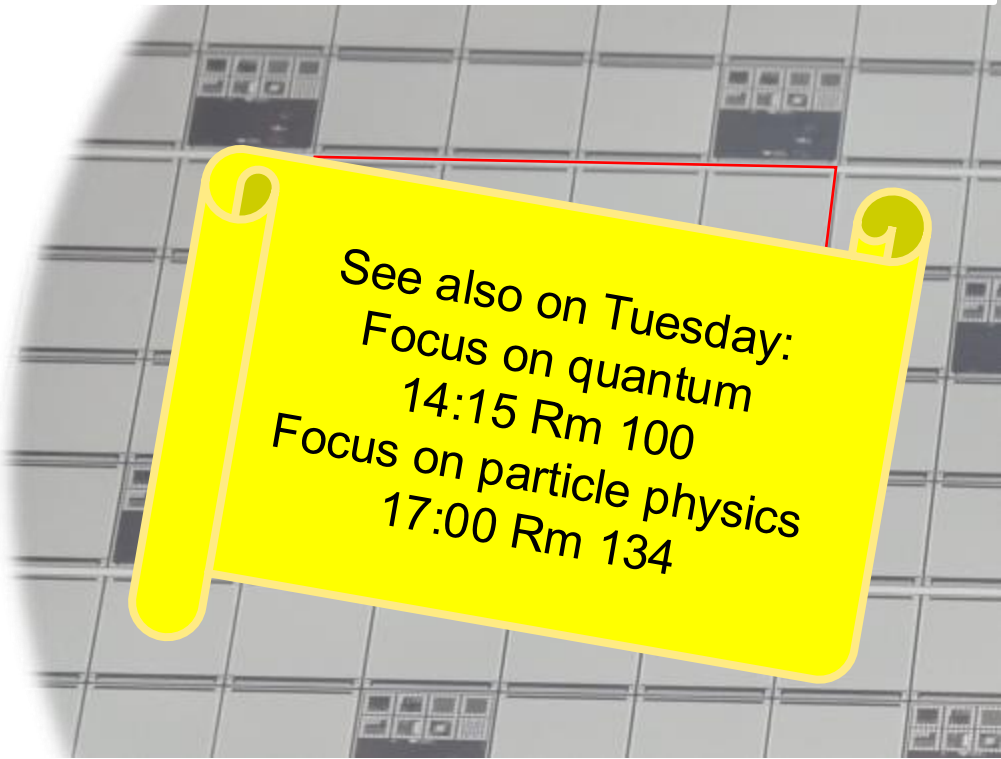
Conclusion

UDS

- 3D Photon-to-Digital Converters in fabrication
  - Low power readout
  - 2 lots completed, more coming each 6 months to mature process
  - Extended characterization underway
- Dissemination of test platforms to collaborators



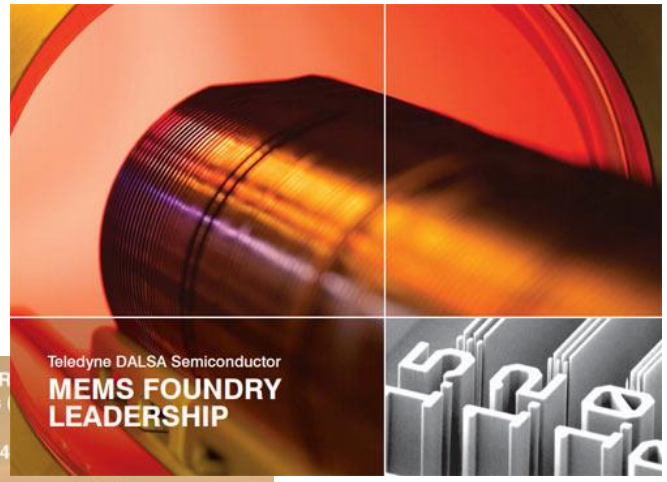
- High performance Photon-to-Digital Converter
  - New quenching circuit, new TDC architecture
  - Small array demonstrated: quenching σ<5 ps, TDC σ<10 ps
  - Completing design/validation of 5×5 mm^2 array → 2026
    - Readout prototyping → 2026
  - Wafer level 3D assembly with SPADs → 2027

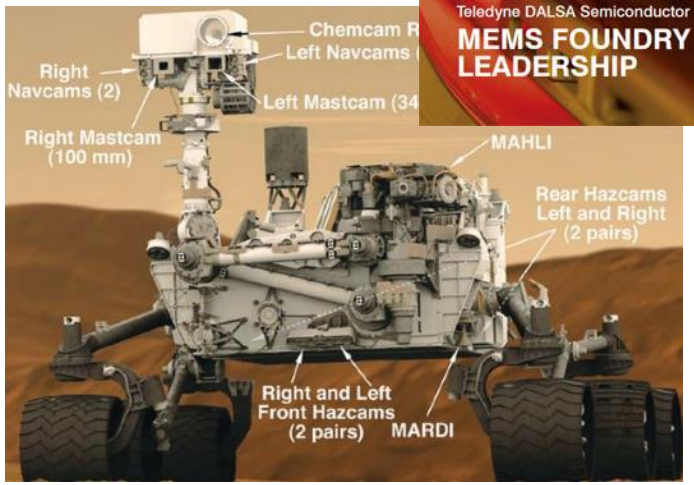


A perfect synergy

UdS

TELEDYNE DALSA
Everywhereyoulook™





L'UdeS fait partie des 10 plus grandes universités de recherche au Canada

UDS

On PDC development

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- S. Parent et al., “Wafer-Level Characterization and Monitoring Platform for Single-Photon Avalanche Diodes,” IEEE J. Electron Devices Soc., vol. 12, pp. 127–137, 2024, doi: 10.1109/JEDS.2024.3359088.
- J.-F. Pratte et al., “Fast neutron radiography-based on single-photon digital photosensor: concept and demonstration,” in Hard X-Ray, Gamma-Ray, and Neutron Detector Physics XXV, N. J. Cherepy, M. Fiederle, and R. B. James, Eds., San Diego, United States: SPIE, Oct. 2023, p. 12. doi: 10.1117/12.2682610.
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- S. Carrier et al., “Towards a Multi-Pixel Photon-to-Digital Converter for Time-Bin Quantum Key Distribution,” Sensors, vol. 23, no. 7, p. 3376, Mar. 2023, doi: 10.3390/s23073376.
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On ToF CT

- D. Gaudreault, J. Rossignol, Y. Bérube-Lauzière, and R. Fontaine (2021), IEEE Transactions on Radiation and Plasma Medical Sciences, vol. 5, no. 3, pp. 343–349
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On ToF PET

- Pratte, J.-F., et al. "3D Photon-to-Digital Converter for Radiation Instrumentation: Motivation and Future Works" (2021) Sensors;21(2):598. doi: 10.3390/s21020598
- Parent, S., et al. "Single photon avalanche diodes and vertical integration process for a 3D digital SiPM using industrial semiconductor technologies." 2018 IEEE Nuclear Science Symposium and Medical Imaging Conference Proceedings (NSS/MIC). IEEE, 2018.
- Parent, S., et al. “Characterization and Monitoring Platform for Single-Photon Avalanche Diodes in the Development of a Photon-to-Digital Converter Technology.”, 2022 IEEE International Conference on Microelectronic Test Structures Proceedings (ICMTS). IEEE, 2022.
- Parent, S., “Design of a Vertically Integrated Single-Photon Avalanche Diodes, Manufactured at Wafer level, for a Photon-to-Digital Converter Technology”, PhD Thesis (to be published), 2022.
- Nolet, F. et al., “Quenching Circuit and SPAD Integrated in CMOS 65 nm with 7.8 ps FWHM Single Photon Timing Resolution”, Instruments 2018, 2, 19.
- Nolet, F. et al., “Digital SiPM channel integrated in CMOS 65 nm with 17.5 ps FWHM single photon timing resolution”, Nuclear Instruments and Methods in Physics Research Section A, 912, 29-32, 2018.
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- Lemaire, W. et al., “Embedded time of arrival estimation for digital silicon photomultipliers with in-pixel TDCs”, Nuclear Instruments and Methods in Physics Research Section A, 959, 163538, 2020.
- Roy, N., et al. “Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM”, IEEE Transactions on Radiation and Plasma Medical Sciences, 1(6) 2017.
- Therrien, A. C., et al. “Energy discrimination for positron emission thomography using the time information of the first detected photons”, Journal of Instrumentation, 13, 2018.
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Extras

PDC designed for Time-of-Flight PET

(and ToF-CT,
and QKD,
and wavefront sensing,
and more)

instruments MDPI

Article

Quenching Circuit and SPAD Integrated in CMOS 65 nm with 7.8 ps FWHM Single Photon Timing Resolution

Frédéric Nolet *, Samuel Parent, Nicolas Roy, Marc-Olivier Mercier, Serge A. Charlebois, Réjean Fontaine and Jean-Francois Pratte

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Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

Digital SiPM channel integrated in CMOS 65 nm with 17.5 ps FWHM single photon timing resolution

Frédéric Nolet *, Frédérik Dubois, Nicolas Roy, Samuel Parent, William Lemaire, Alexandre Massie-Godon, Serge A. Charlebois, Réjean Fontaine, Jean-Francois Pratte

Interdisciplinary Institute for Technological Innovation and Department of Electrical and Computer Engineering, Université de Sherbrooke , Sherbrooke, Québec, Canada

With TDC

ASIC Overview (originally for PET)

UDS

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

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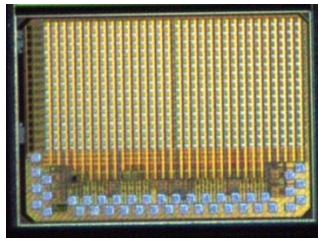
A 256 Pixelated SPAD readout ASIC with in-Pixel TDC and embedded digital signal processing for uniformity and skew correction☆

Frédéric Nolet *, William Lemaire, Frédérik Dubois, Nicolas Roy, Simon Carrier, Arnaud Samson, Serge A. Charlebois, Réjean Fontaine, Jean-Francois Pratte

Interdisciplinary Institute for Technological Innovation and Department of Electrical and Computer Engineering, Université de Sherbrooke, Sherbrooke, QC, J1K 2R1, Canada

- TSMC 65 nm CMOS (LP)
- 16 × 16 pixels in 1.1 × 1.1 mm^2
- Jitter: 18 ps RMS for 256 pixels



Rev 1. 2019

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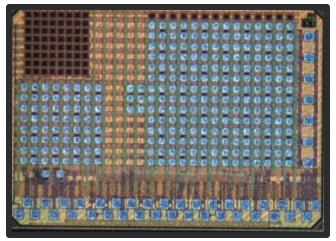
Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

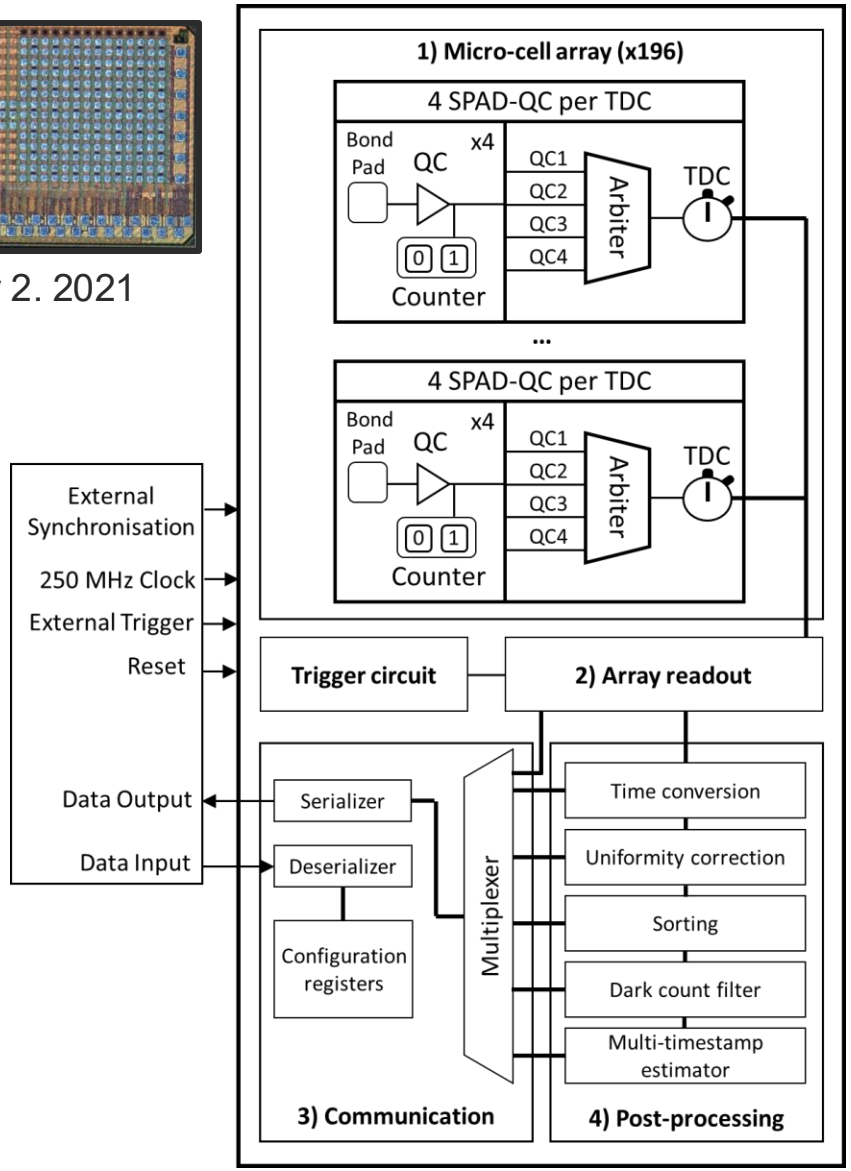
Embedded time of arrival estimation for digital silicon photomultipliers with in-pixel TDCs☆

William Lemaire *, Frédéric Nolet, Frédérik Dubois, Audrey C. Therrien, Jean-François Pratte, Réjean Fontaine

Interdisciplinary Institute for Technological Innovation and Department of Electrical and Computer Engineering, Université de Sherbrooke, Sherbrooke, QC, J1K 2R1, Canada

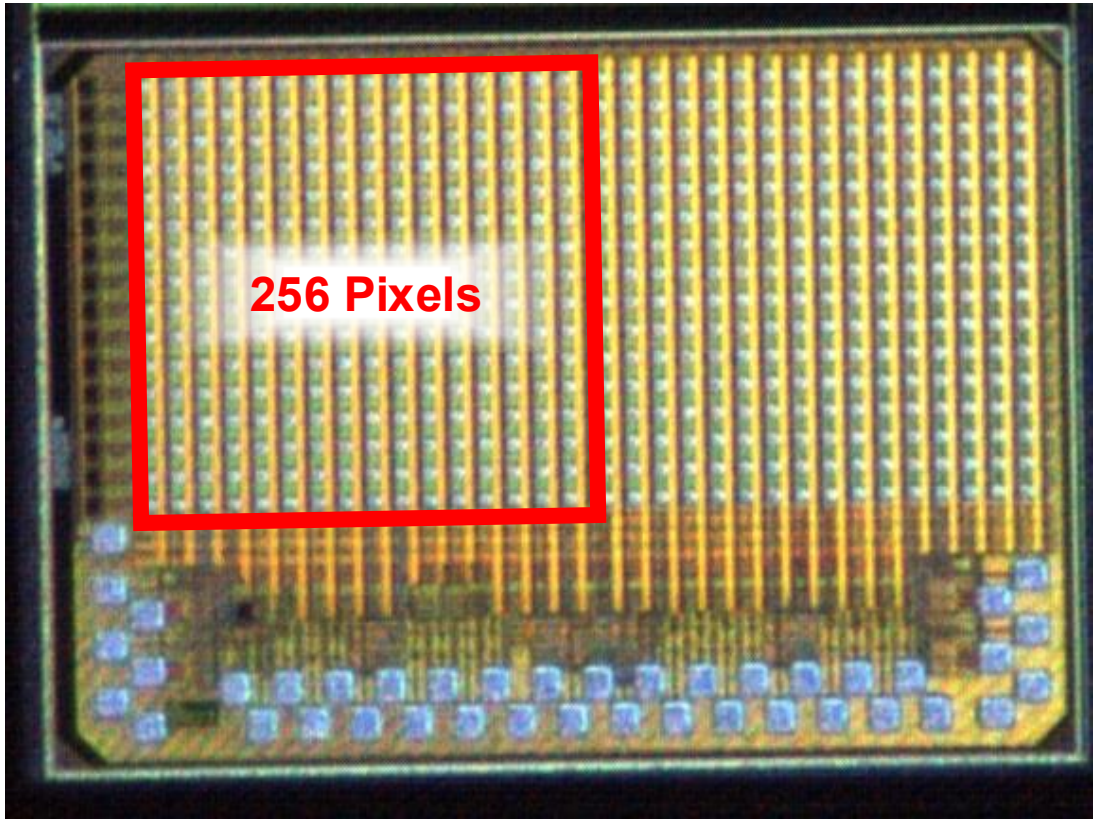


Rev 2. 2021



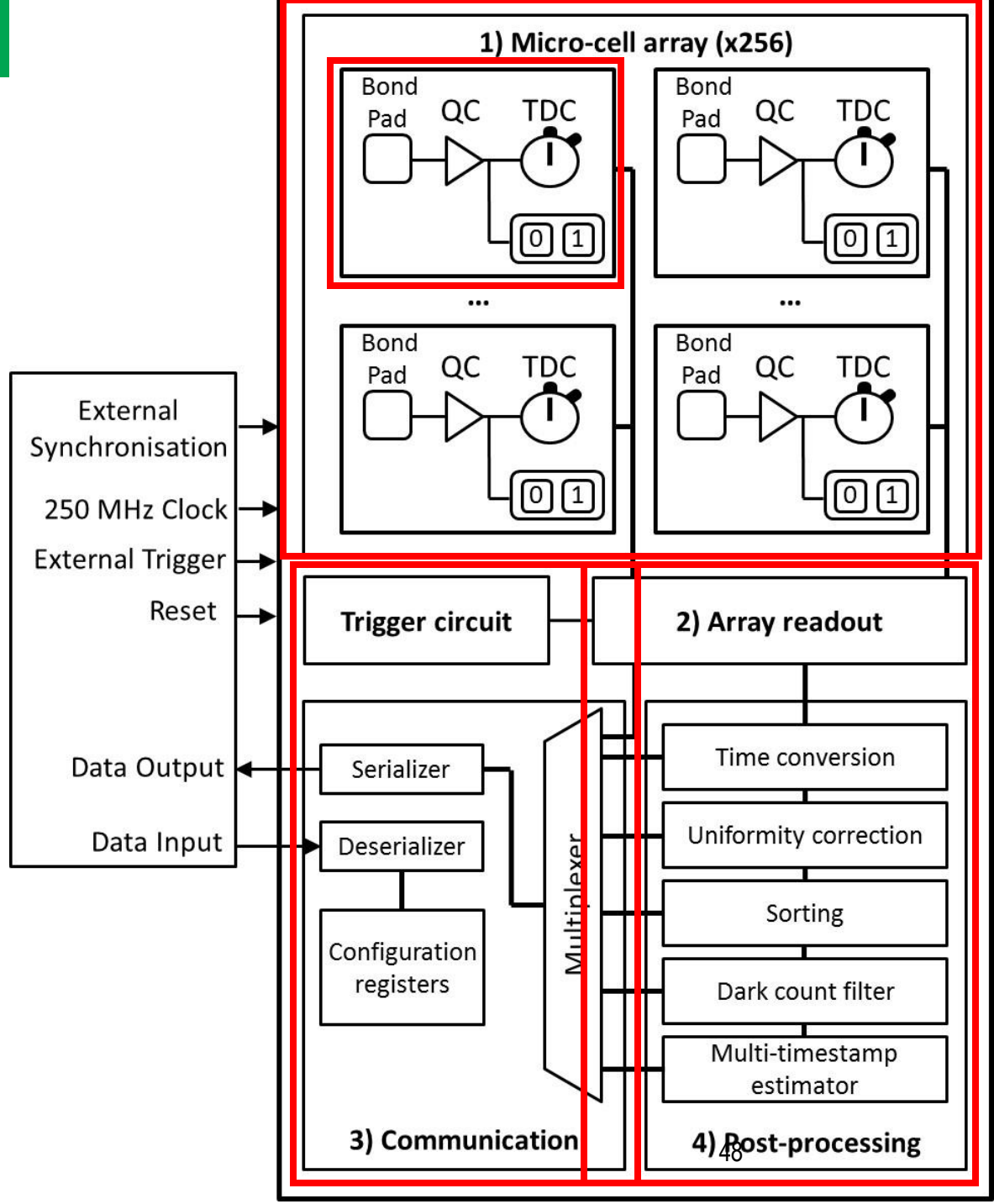
Overview of the First 65nm ASIC : PET

- TSMC 65 nm CMOS (GP)
- 16 × 16 pixels in 1.1 × 1.1 mm^2 (red box)
  Jitter: 18 ps RMS for 256 pixels

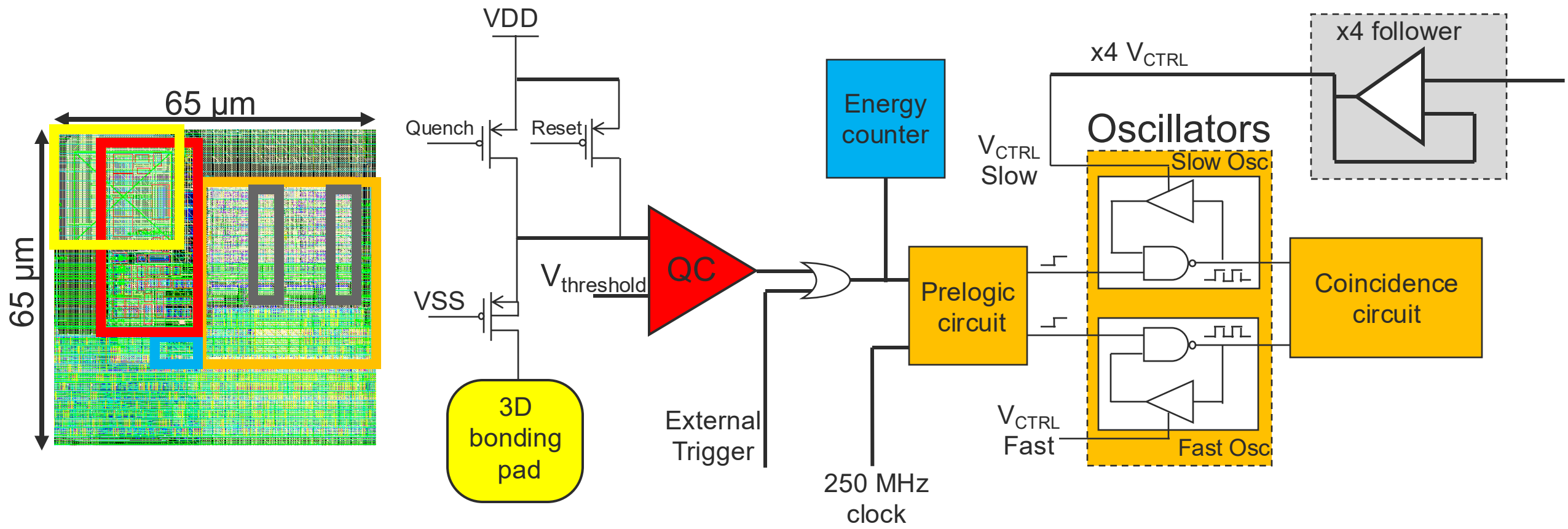


Nolet, Frédéric, et al. "A 256 pixelated SPAD readout ASIC with in-pixel TDC and embedded digital signal processing for uniformity and skew correction." NIMA, 949 (2020): 162891.

Lemaire, William, et al. "Embedded time of arrival estimation for digital silicon photomultipliers with in-pixel TDCs." NIMA, 959 (2020): 163538.



Pixel electronics in TSMC 65 nm CMOS



Ring Oscillators based Vernier Time-to-Digital Converter

UDS

486 IEEE TRANSACTIONS ON RADIATION AND PLASMA MEDICAL SCIENCES, VOL. 1, NO. 6, NOVEMBER 2017

Low Power and Small Area, 6.9 ps RMS Time-to-Digital Converter for 3-D Digital SiPM

Nicolas Roy, Frédéric Nolet, *Student Member, IEEE*, Frédérik Dubois, Marc-Olivier Mercier, Réjean Fontaine, *Senior Member, IEEE*, and Jean-François Pratte, *Member, IEEE*

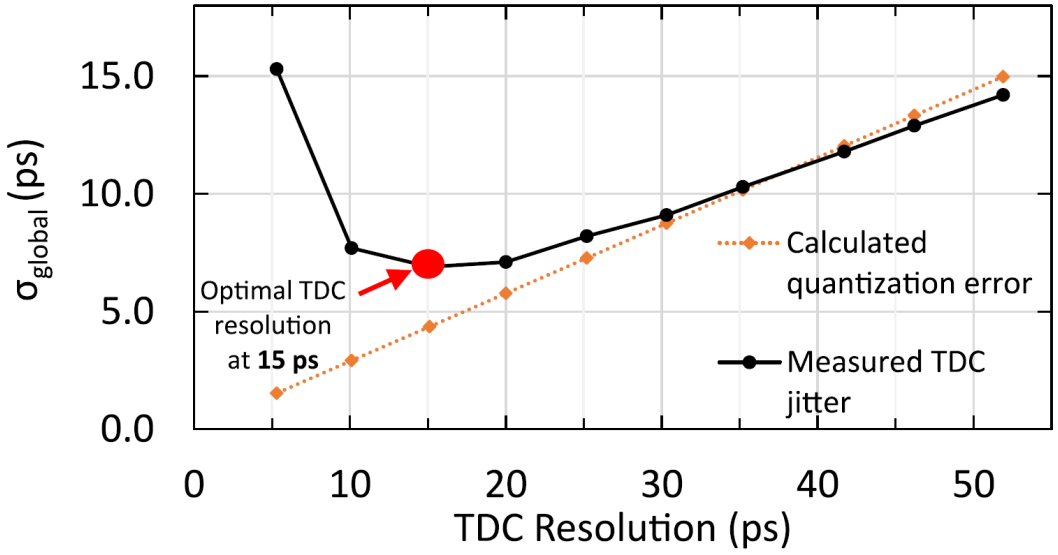


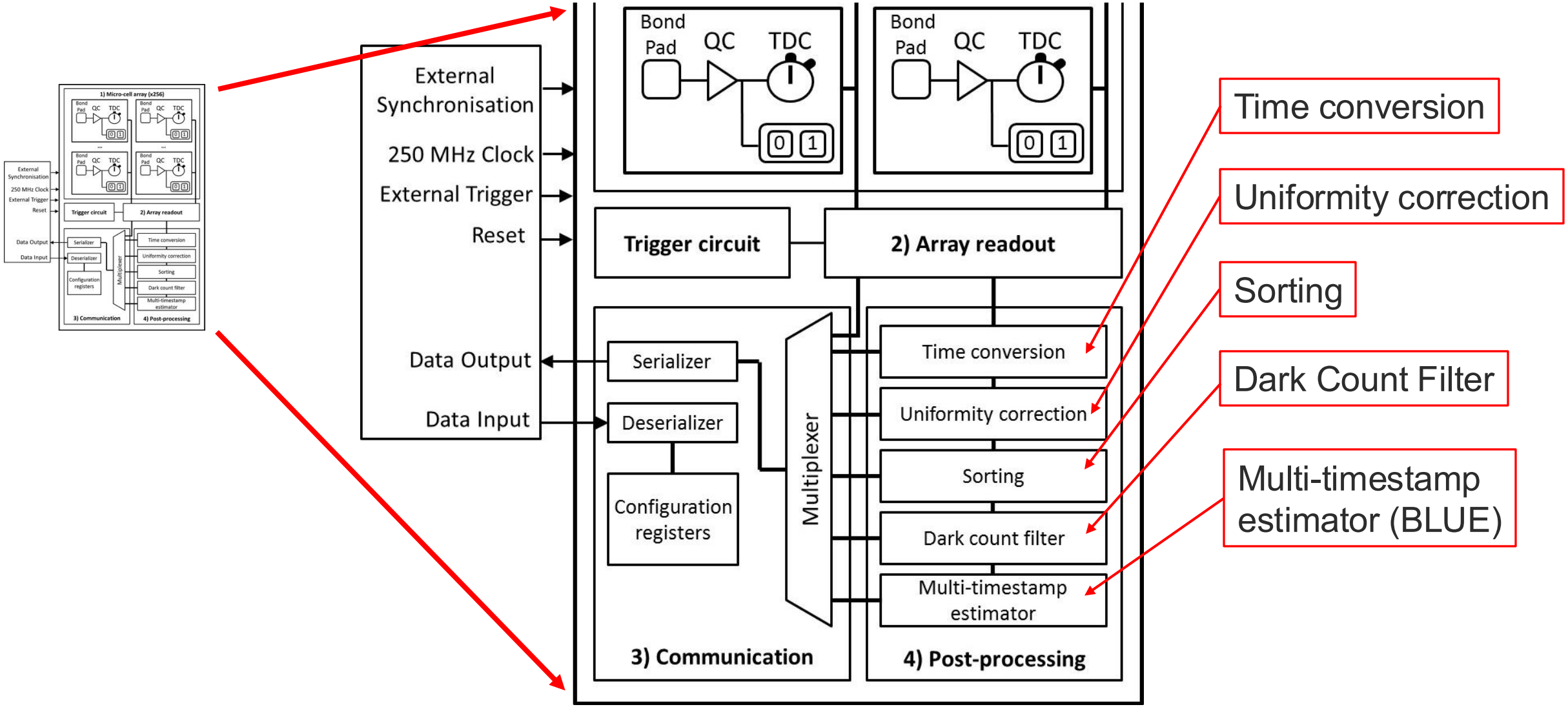
Fig. 11. TDC timing accuracy as a function of the TDC resolution. The optimal timing resolution is at 15 ps.

$$\mathrm{FOM} = \frac{\mathrm{Power}\ (\mu\mathrm{W}) \times \sigma_{\mathrm{global}}\ (\mathrm{ps}) \times \mathrm{Area}\ (\mathrm{mm}^2)}{\mathrm{Events\ Rate}\ (\mathrm{Mevents/s})} \left[\mathrm{pJ/event} \cdot \mathrm{ps_{rms}} \cdot \mathrm{mm}^2\right]. \quad (21)$$

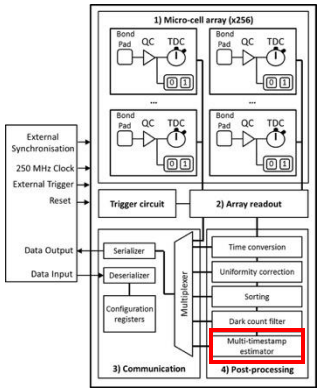
Dual Phase-Locked Loop System for TDC Resolution Calibration (#1182)

F. Nolet[1], F. Dubois[1], N. Roy[1], W. Lemaire[1], S. A. Charlebois[1], R. Fontaine[1], J.- F. Pratte[1]
[1] Université de Sherbrooke, 3IT and Department of Electrical and Computer, Sherbrooke, Québec, Canada

Frédéric Nolet, Ph.D.

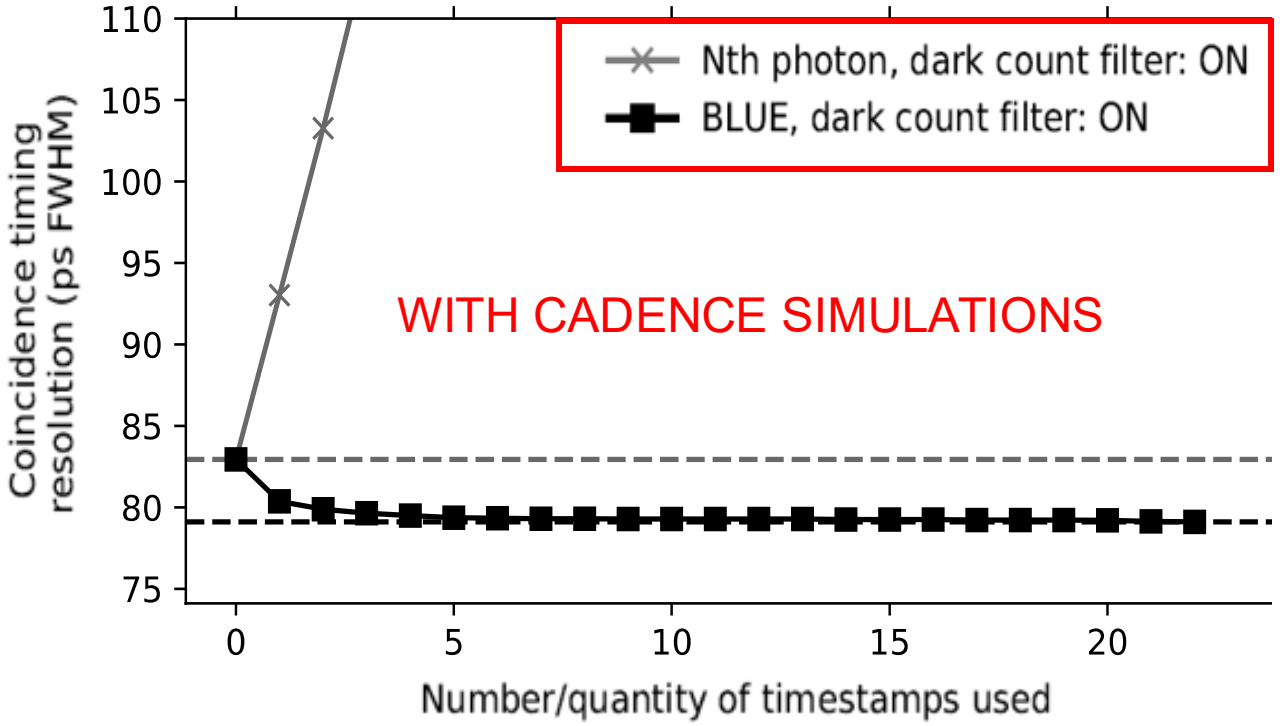

External Synchronisation
250 MHz Clock
External Trigger
Reset
Data Output
Data Input
Bond Pad
QC
TDC
0
1
Trigger circuit
2) Array readout
Serializer
Deserializer
Configuration registers
Multiplexer
3) Communication
Time conversion
Uniformity correction
Sorting
Dark count filter
Multi-timestamp estimator
4) Post-processing

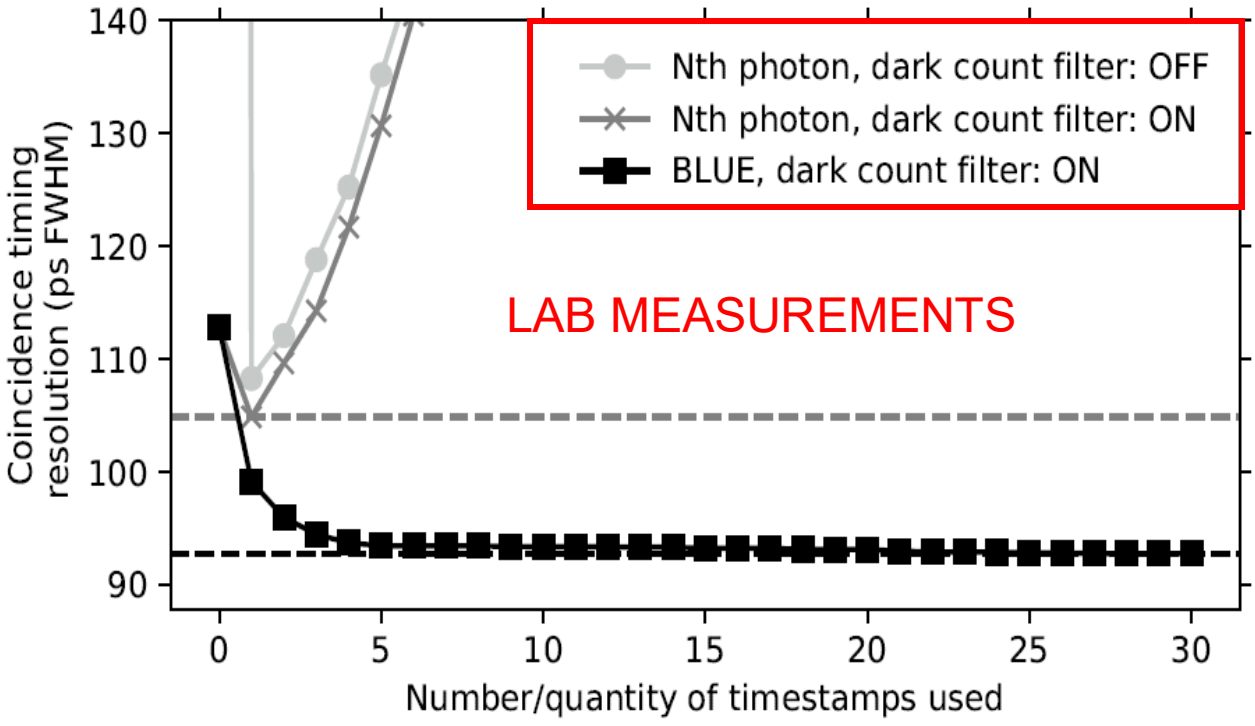
Best Linear Unbiased Estimator



Scintillator characteristic for Geant4 simulation

Material	LYSO
t_{rise} / t_{fall}	70 ps / 40 ns
Size	$1 \times 1 \times 3$ mm^3
Surface treatment	ESR reflector and optical grease
Single SPAD SPTR	35 ps
Array PDE	30%





PET: Energy Discrimination using Timestamps

UDS

Jinst

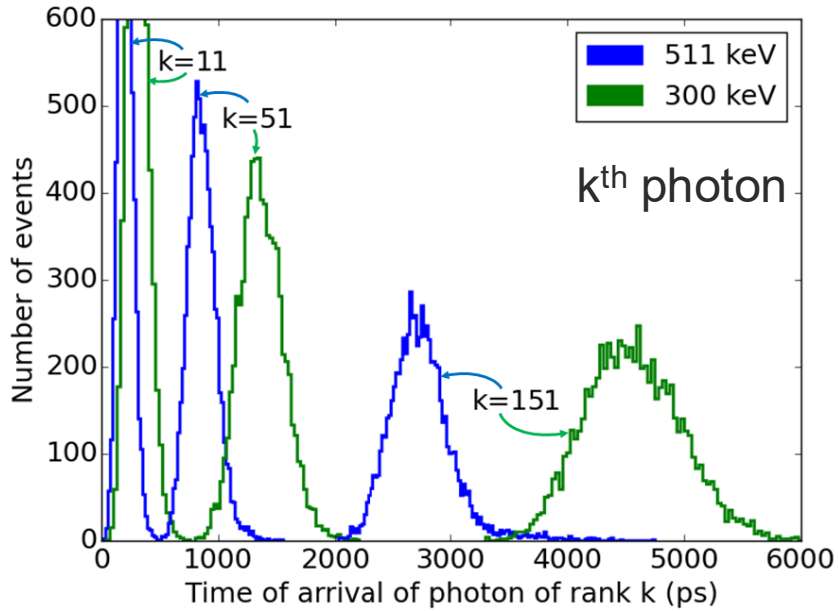
Published by IOP Publishing for Sissa Medialab

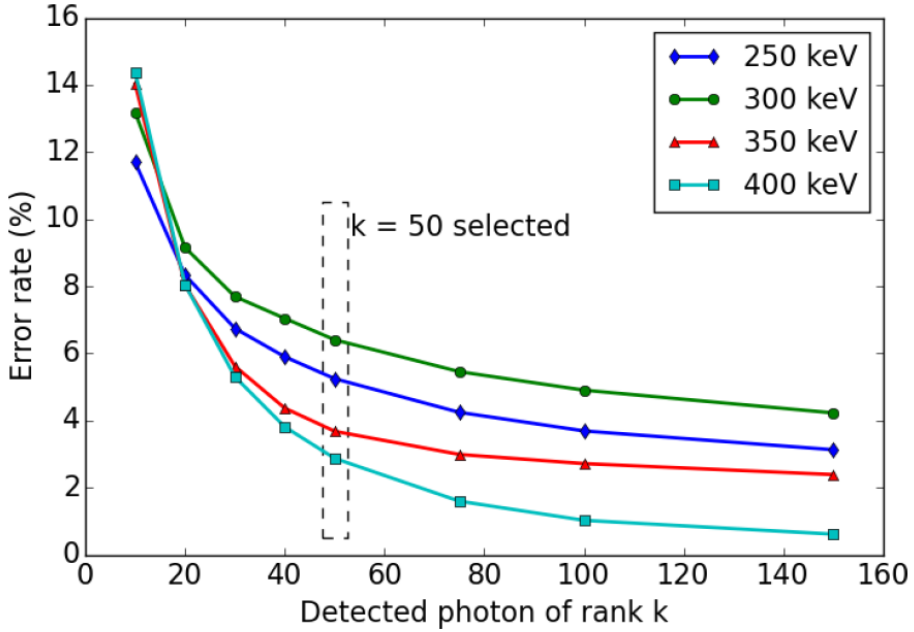
Received: *July 18, 2017*
Revised: *October 30, 2017*
Accepted: *January 2, 2018*
Published: *January 15, 2018*

Energy discrimination for positron emission tomography using the time information of the first detected photons

A.C. Therrien,[a,1] W. Lemaire,[a] P. Lecoq,[b] R. Fontaine[a] and J.-F. Pratte[a]

- Use the first 5 ns timestamps at the beginning of the event
- The same data used previously with BLUE
- **Strategy based on timestamps**
- **Error rate < 3% for threshold at 400 keV**
  - Dark count rate up to ≤ 100 cps/μm^2
  - Time-to-digital converter resolution up to 50 ps
  - PDE: 10 % to 70 %

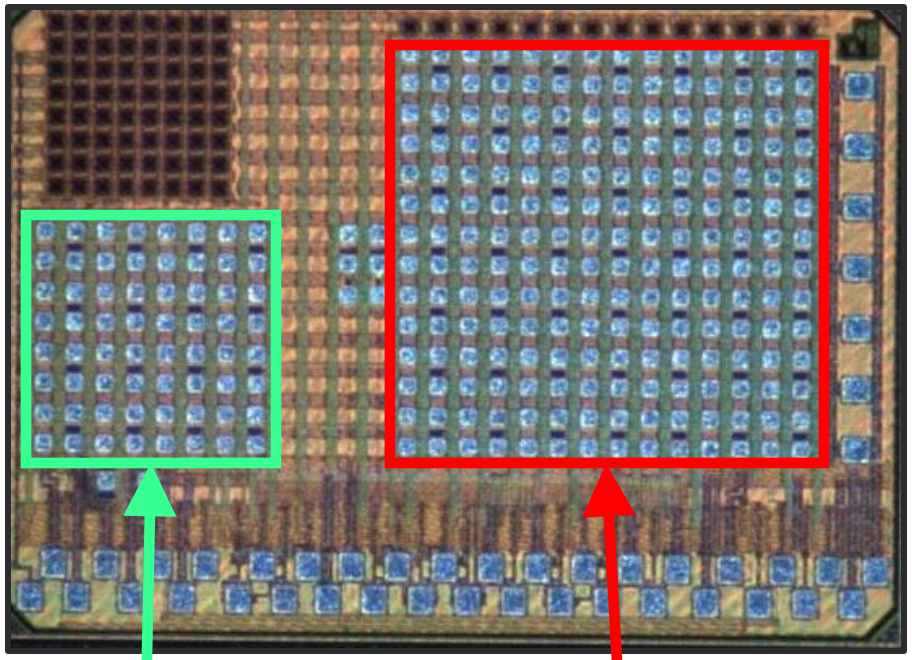




Overview of the Second 65nm ASIC: PET + CT + QKD

UDS

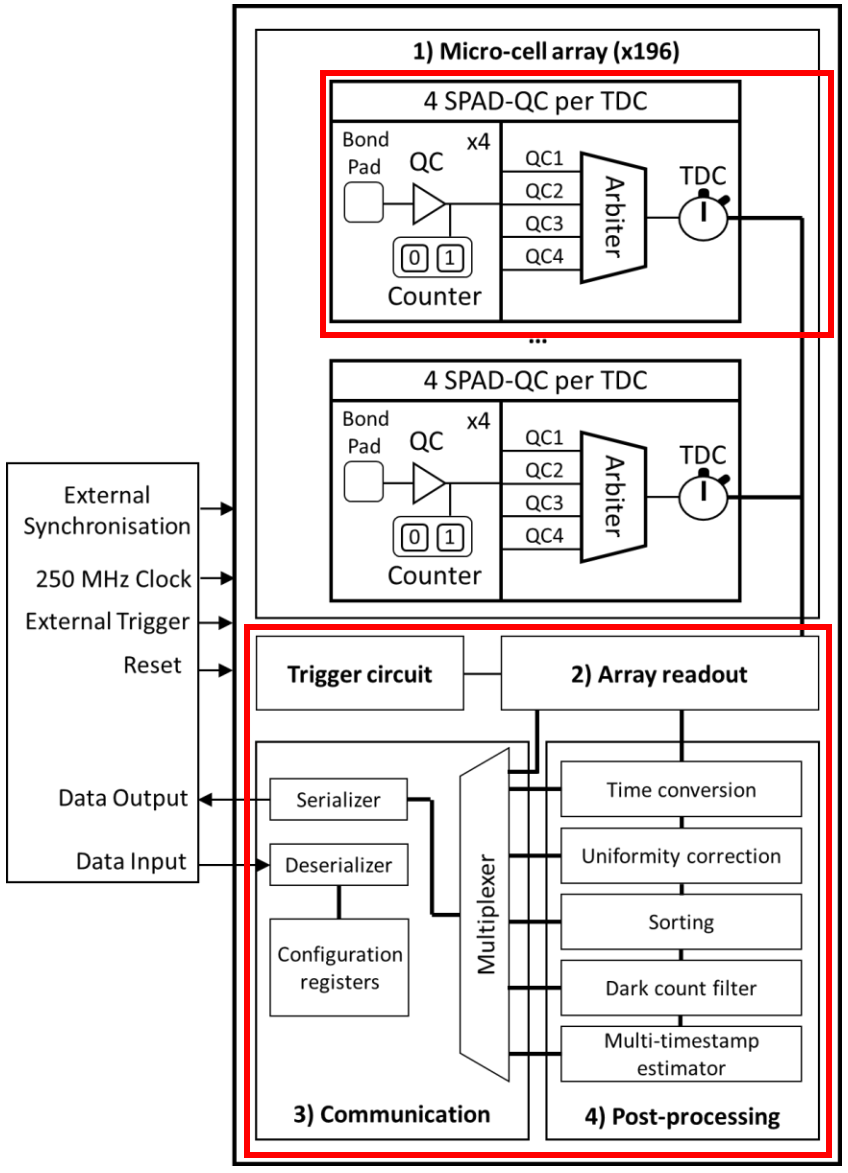
- TSMC 65 nm CMOS
- 16 × 16 pixels in 1.1 × 1.1 mm^2



Rev 2. 2021

QKD

PET/CT



1 Sub-20 ps TDC for 4 SPADs

Advanced digital signal processing:

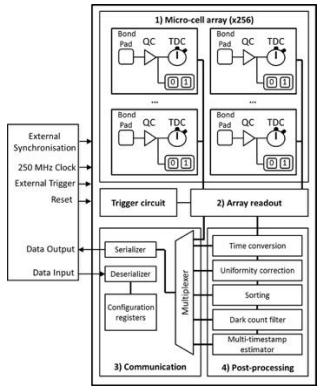
- Time windowing
- TDC code to time conversion
- Uniformity correction
- Timestamp sorting
- Dark count filtering
- BLUE

And for QKD

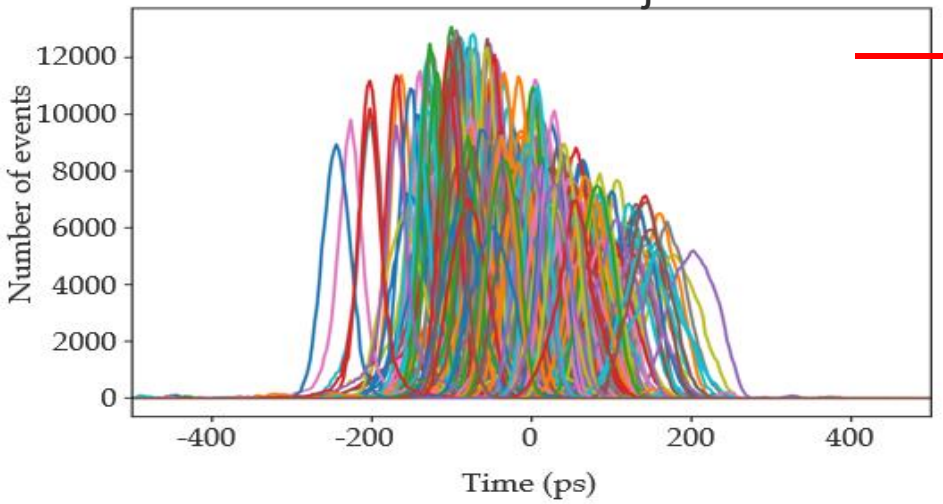
- Time categorization

Embedded Digital Signal Processing Example: Uniformity Correction

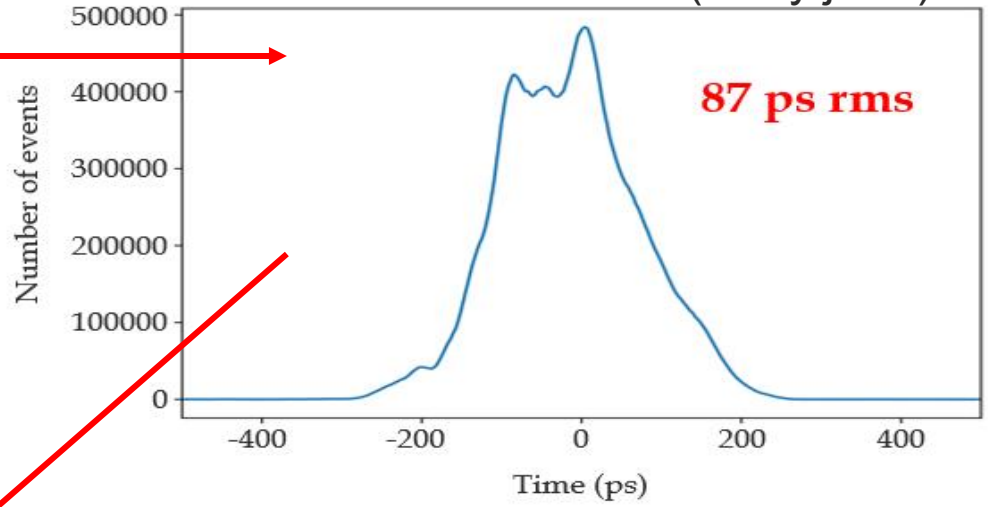
UDS

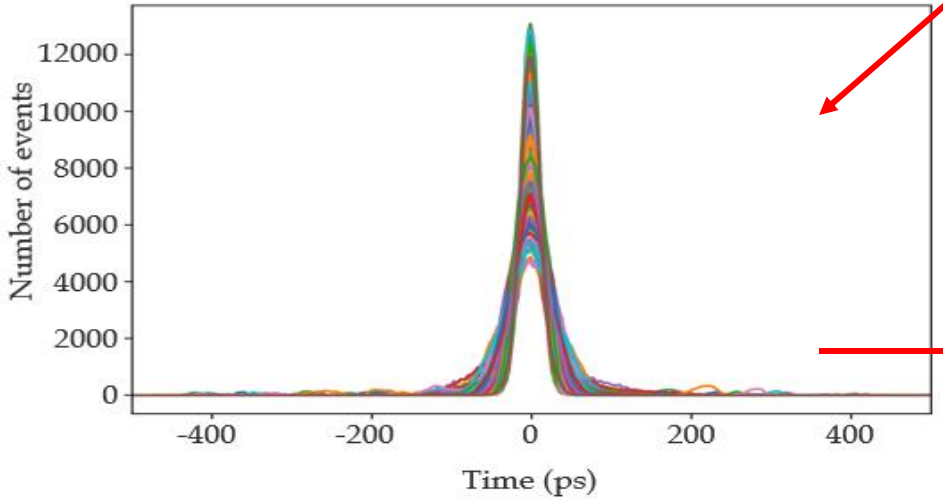


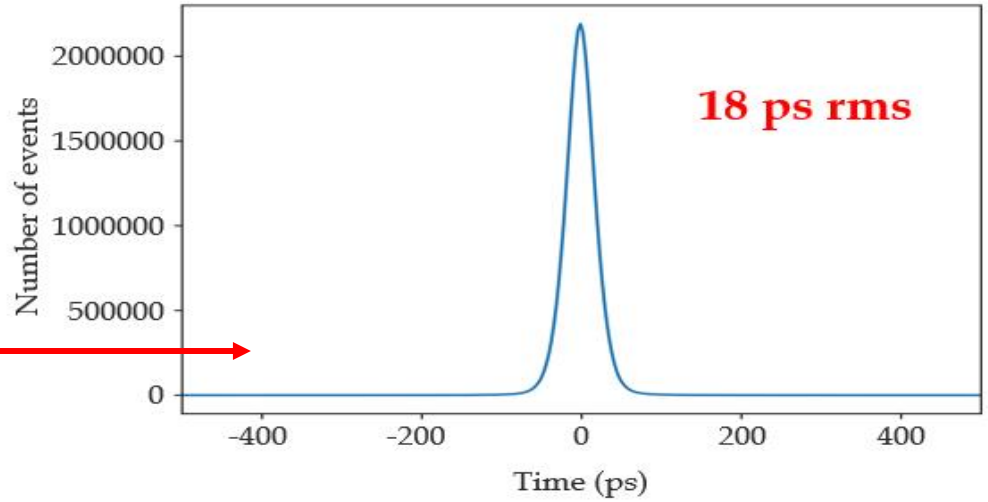
256 channels jitter



Sum of all channels (array jitter)





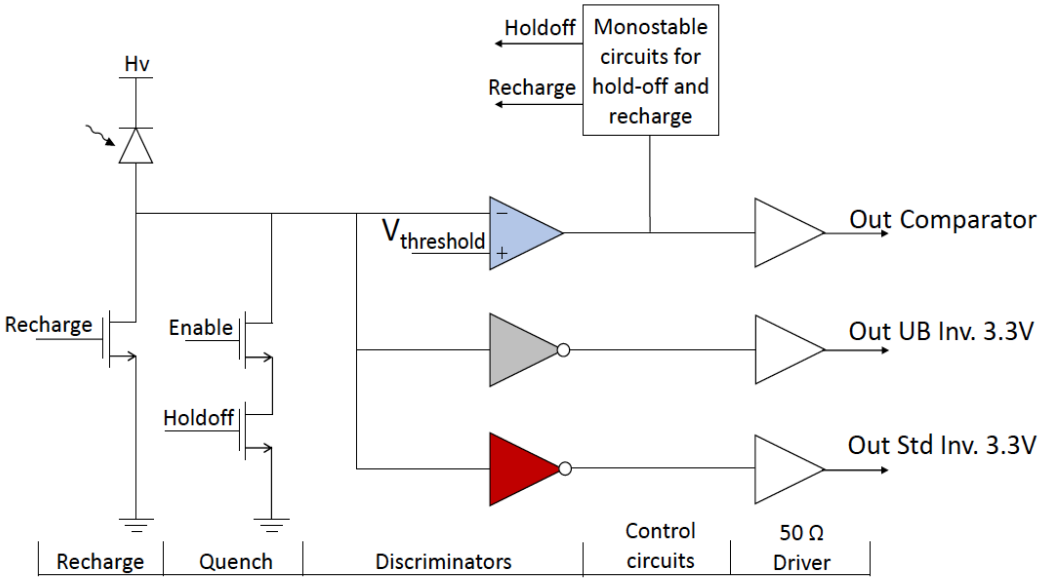


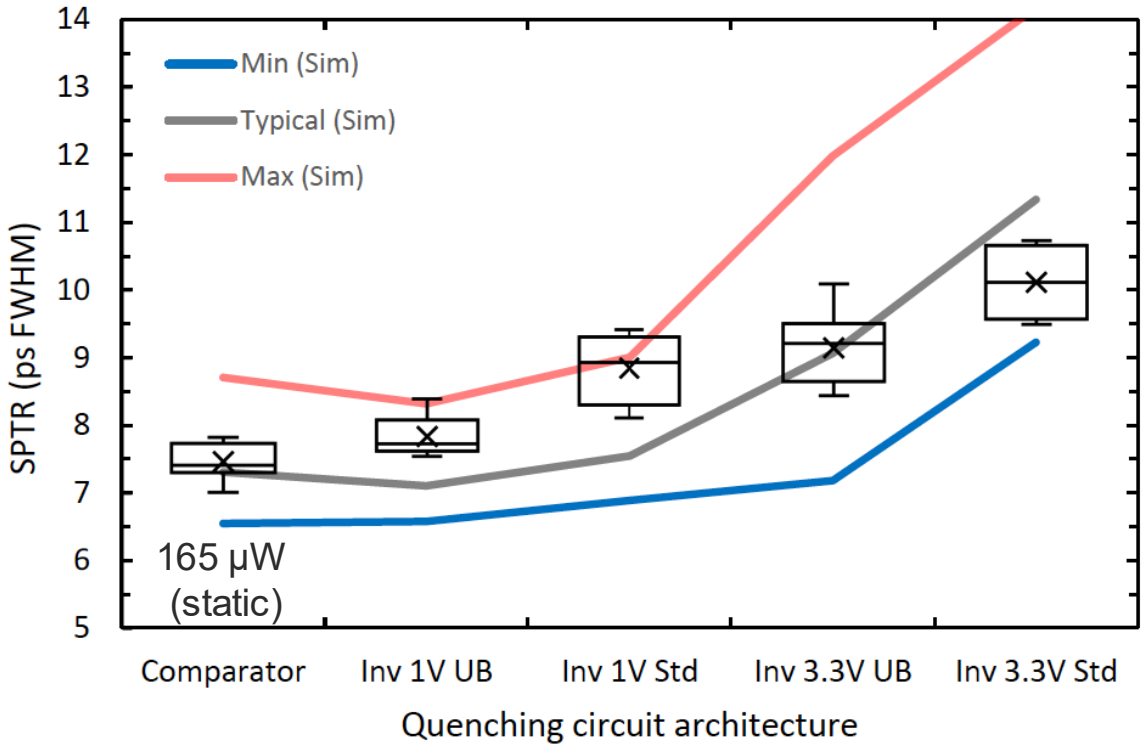
Quenching Circuit Discriminator Architecture Impact SPTR

UDS

- Exploring the impact of the discriminator design on the SPTR
  - TSMC 65 nm CMOS (general purpose)
- 6 designs
  - Also direct comparison between designs
  - Real SPAD signal
- All designs can provide < 10 ps SPTR (FWHM)

- Comparator (open-loop opamp)
- 1V unbalanced inverter 10:1
- 1V balanced inverter
- 3.3V unbalanced inverter 19:1
- 3.3V balanced inverter





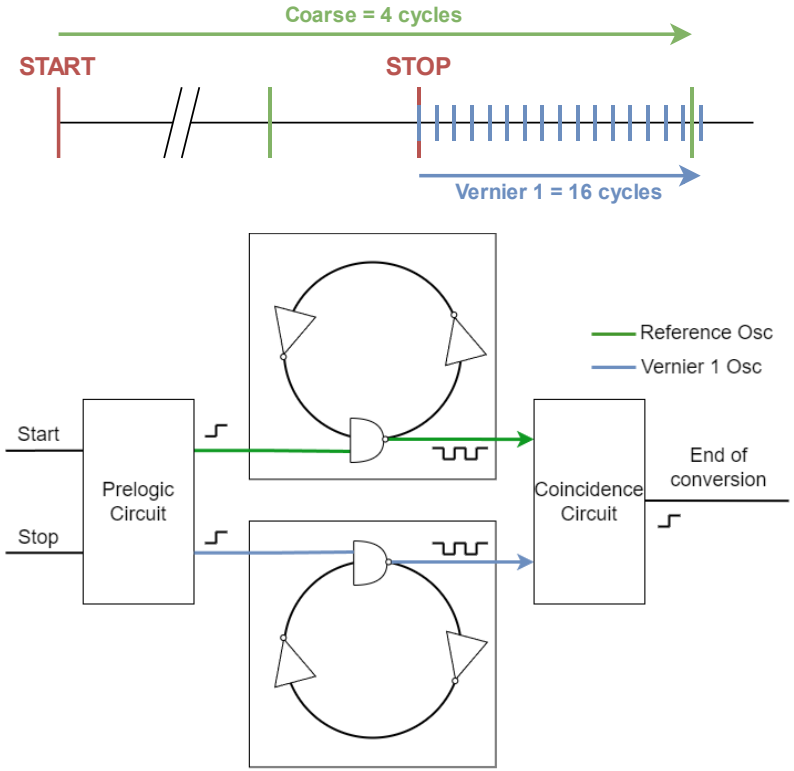
Nolet et al. Quenching Circuit Discriminator Architecture Impact on a Sub-10 ps FWHM Single-Photon Timing Resolution SPAD, Instruments 2023, 7, 16.

From single-vernier to multi-vernier TDC

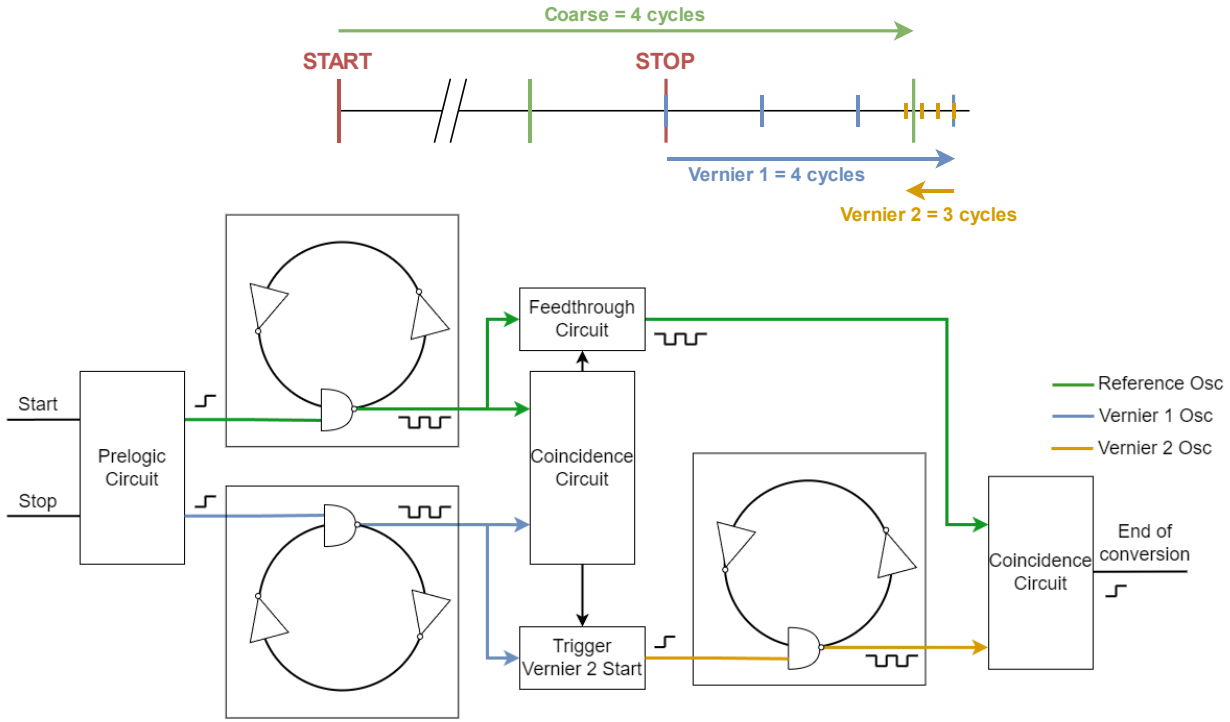
UDS

- To reduce conversion time (lower number of cycles for a given time interval)
- While improving (or at least maintaining) resolution and precision (jitter)

Single vernier TDC

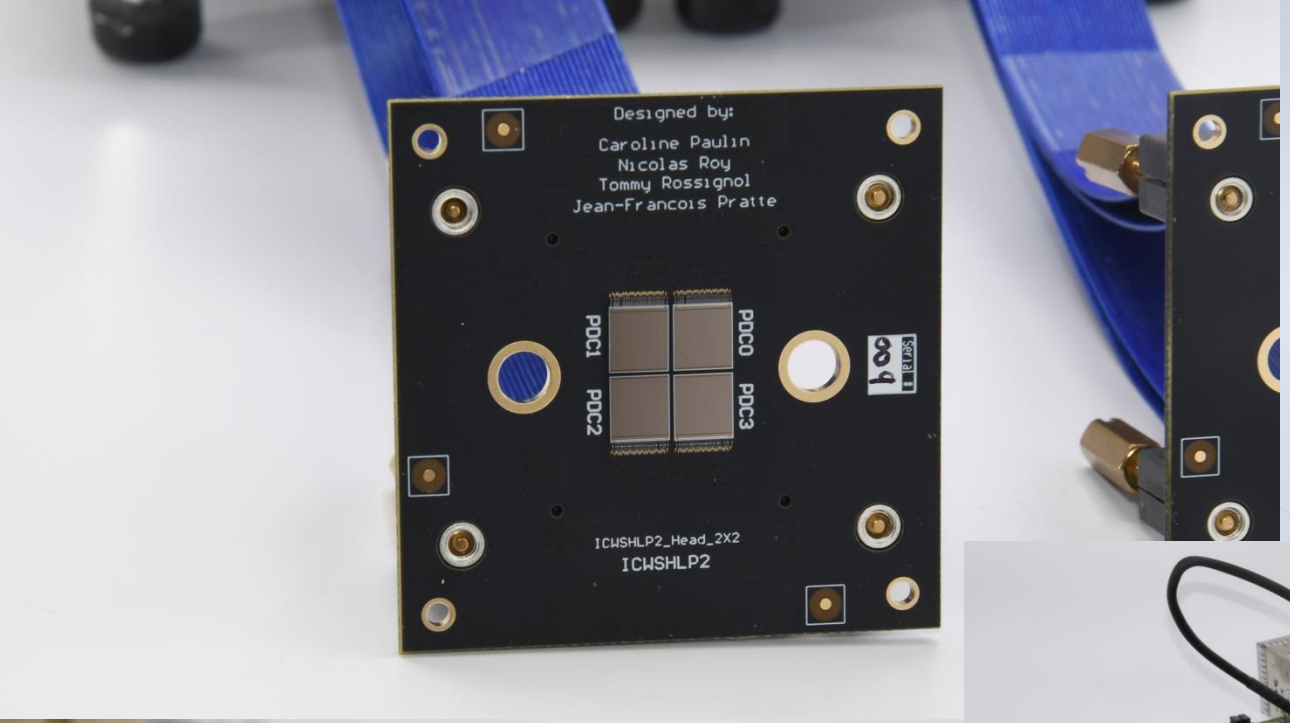


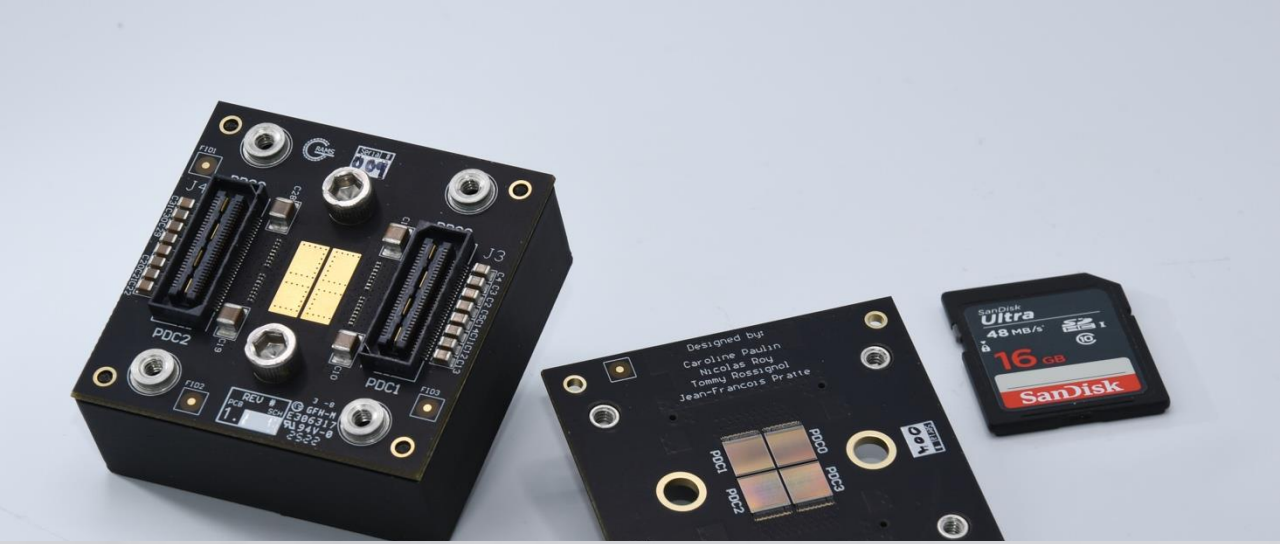
Multi-vernier TDC

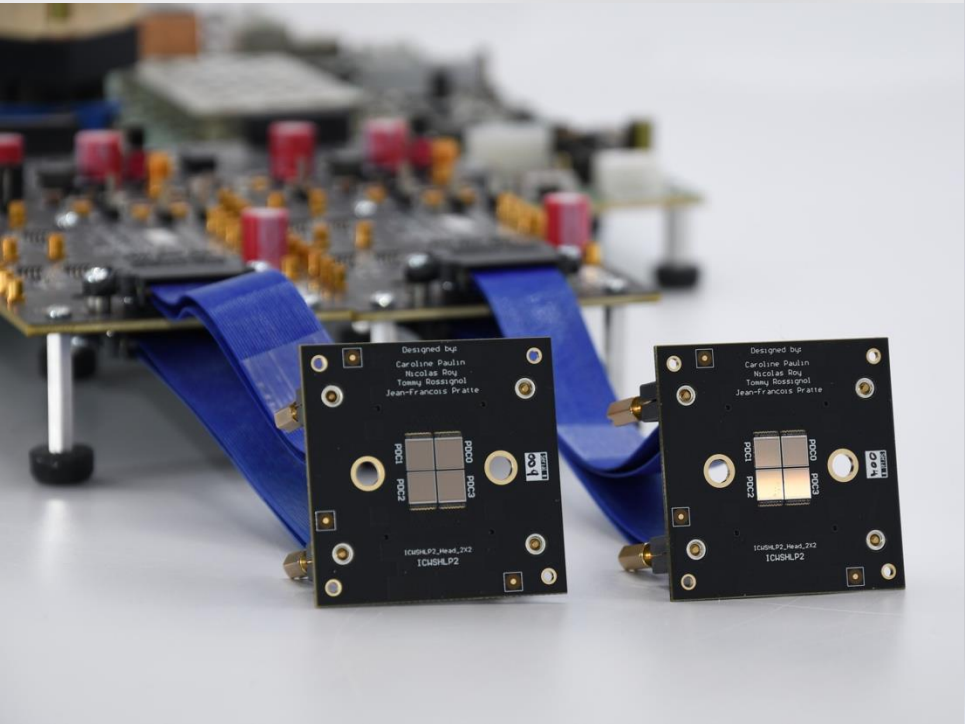


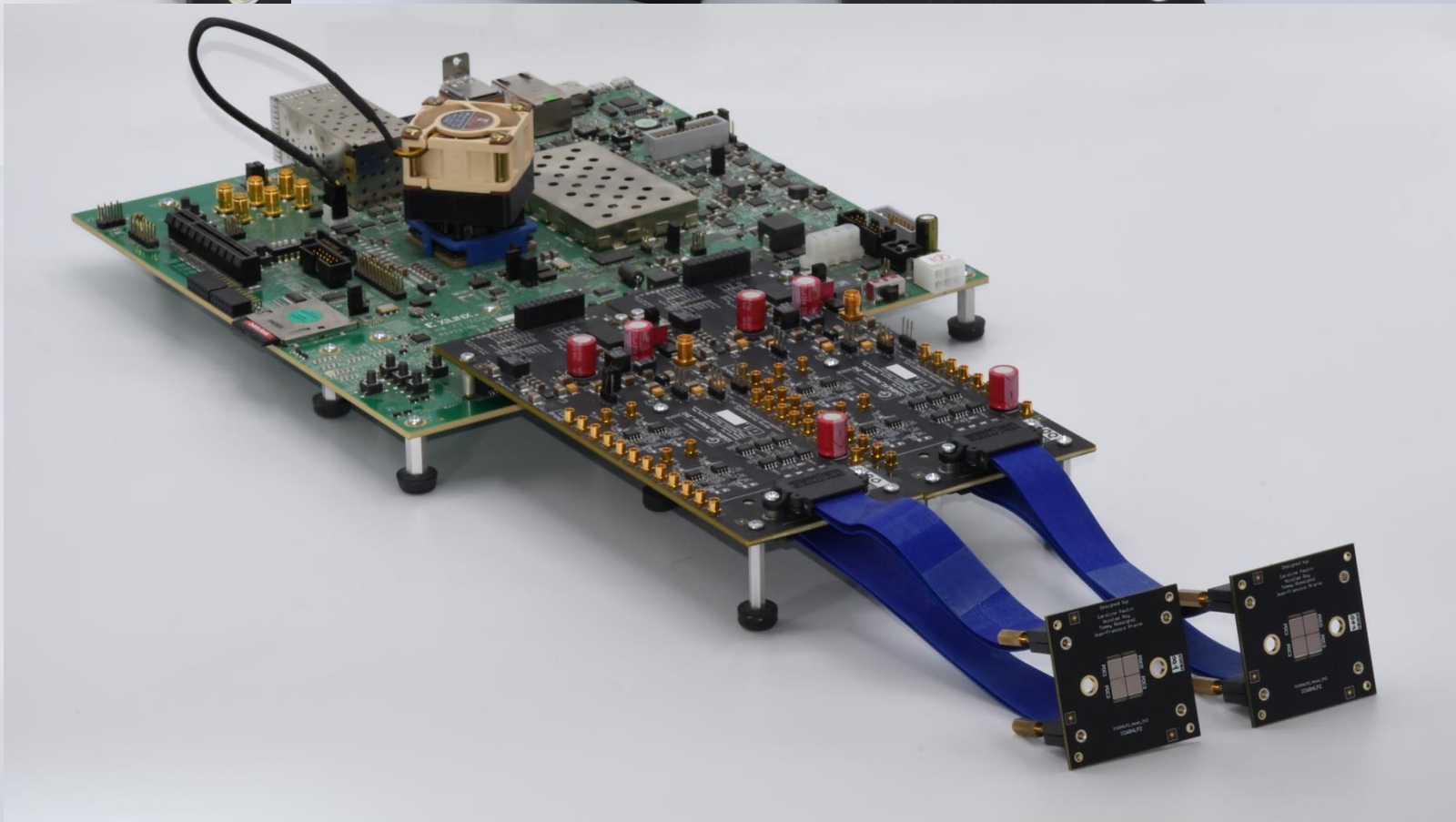
PDC technology dissemination:

Sharing a test platform
to allow collaborators
to explore the technology


Designed by:
Caroline Paulin
Nicolas Roy
Tommy Rossignol
Jean-Francois Pratte
PDC1
PDC0
PDC2
PDC3
ICWSHLP2_Head_2X2
ICWSHLP2

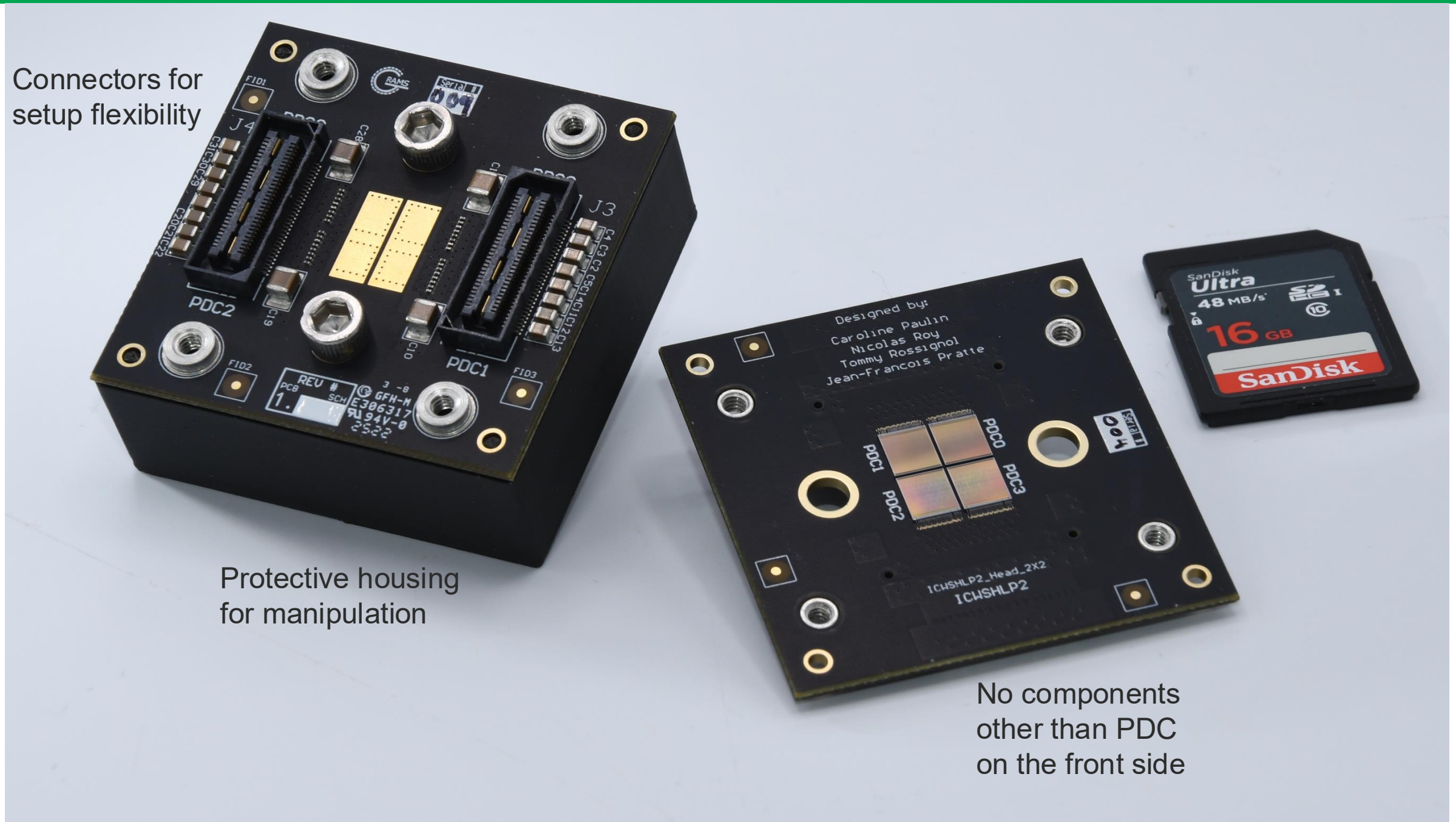

PDC2
PDC1
Designed by:
Caroline Paulin
Nicolas Roy
Tommy Rossignol
Jean-Francois Pratte
PDC1
PDC0
PDC2
PDC3
SanDisk
Ultra
48 MB/s
16 GB
SanDisk

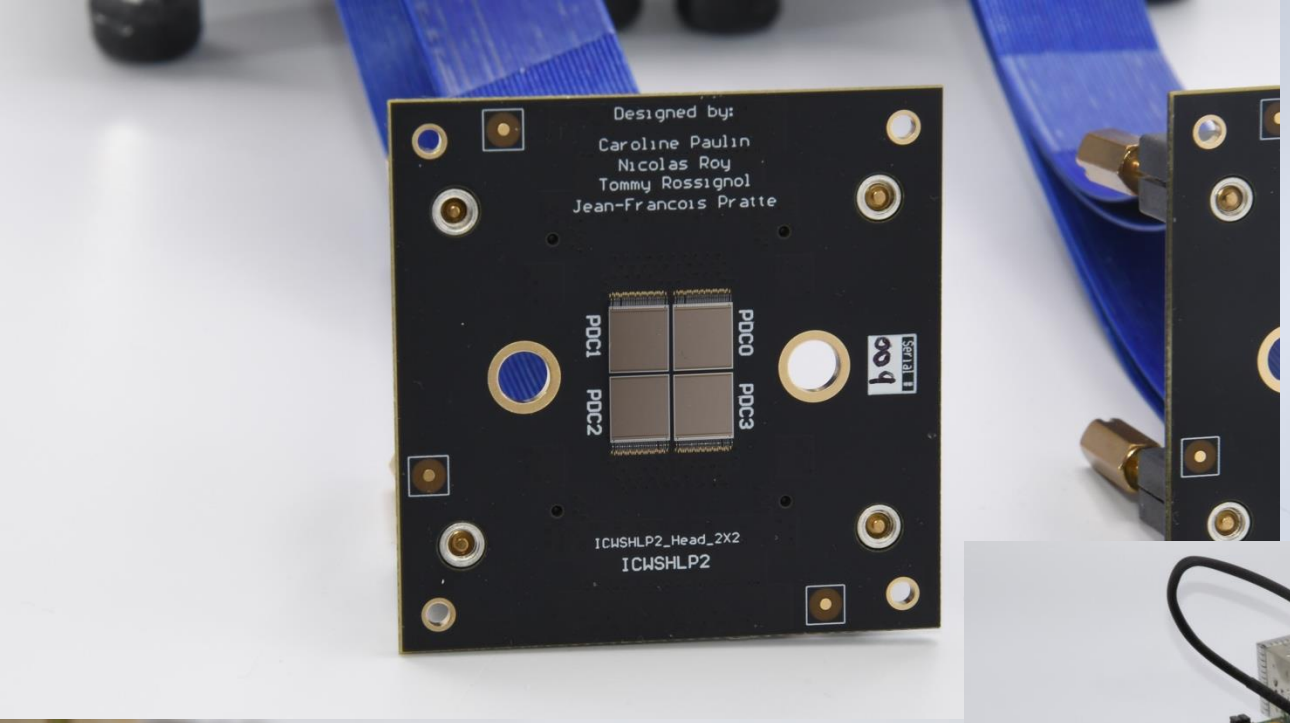

Designed by:
Caroline Paulin
Nicolas Roy
Tommy Rossignol
Jean-Francois Pratte
ICWSHLP2_Head_2X2
ICWSHLP2



Front and back side of the 2x2 PDC tile

UDS




Designed by:
Caroline Paulin
Nicolas Roy
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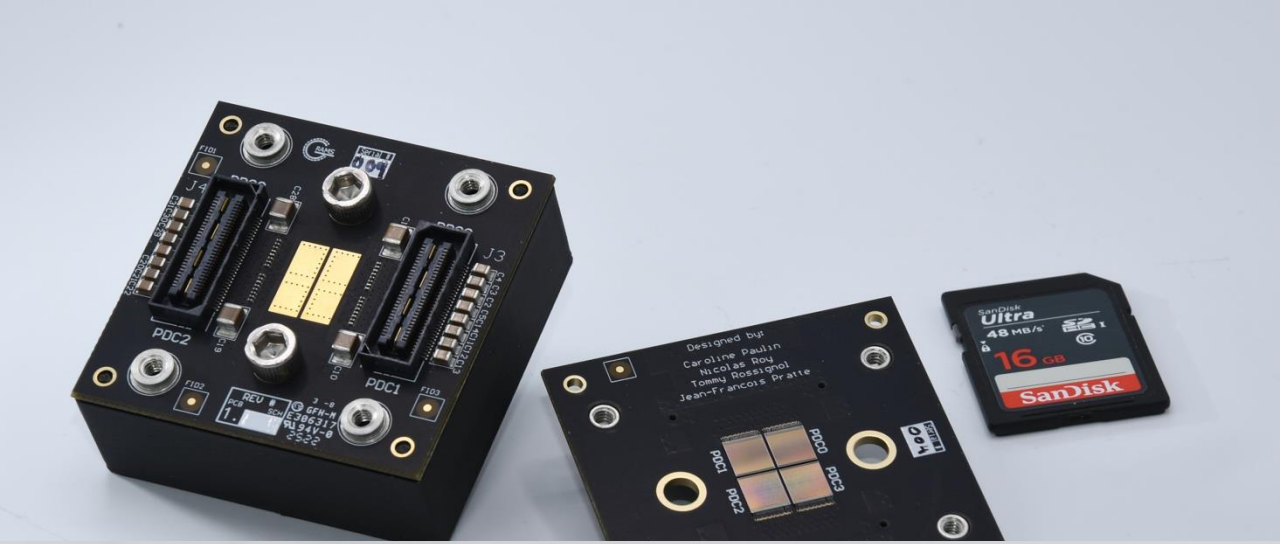
Jean-Francois Pratte
PDC1
PDC0
PDC2
PDC3
ICWSHLP2_Head_2X2
ICWSHLP2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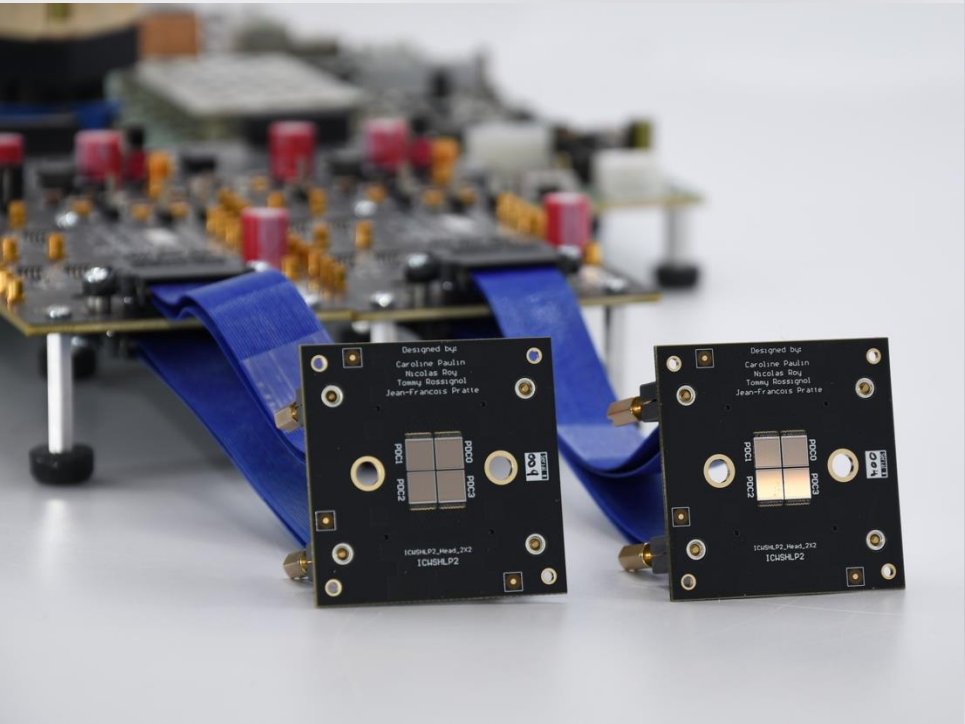
Designed by:
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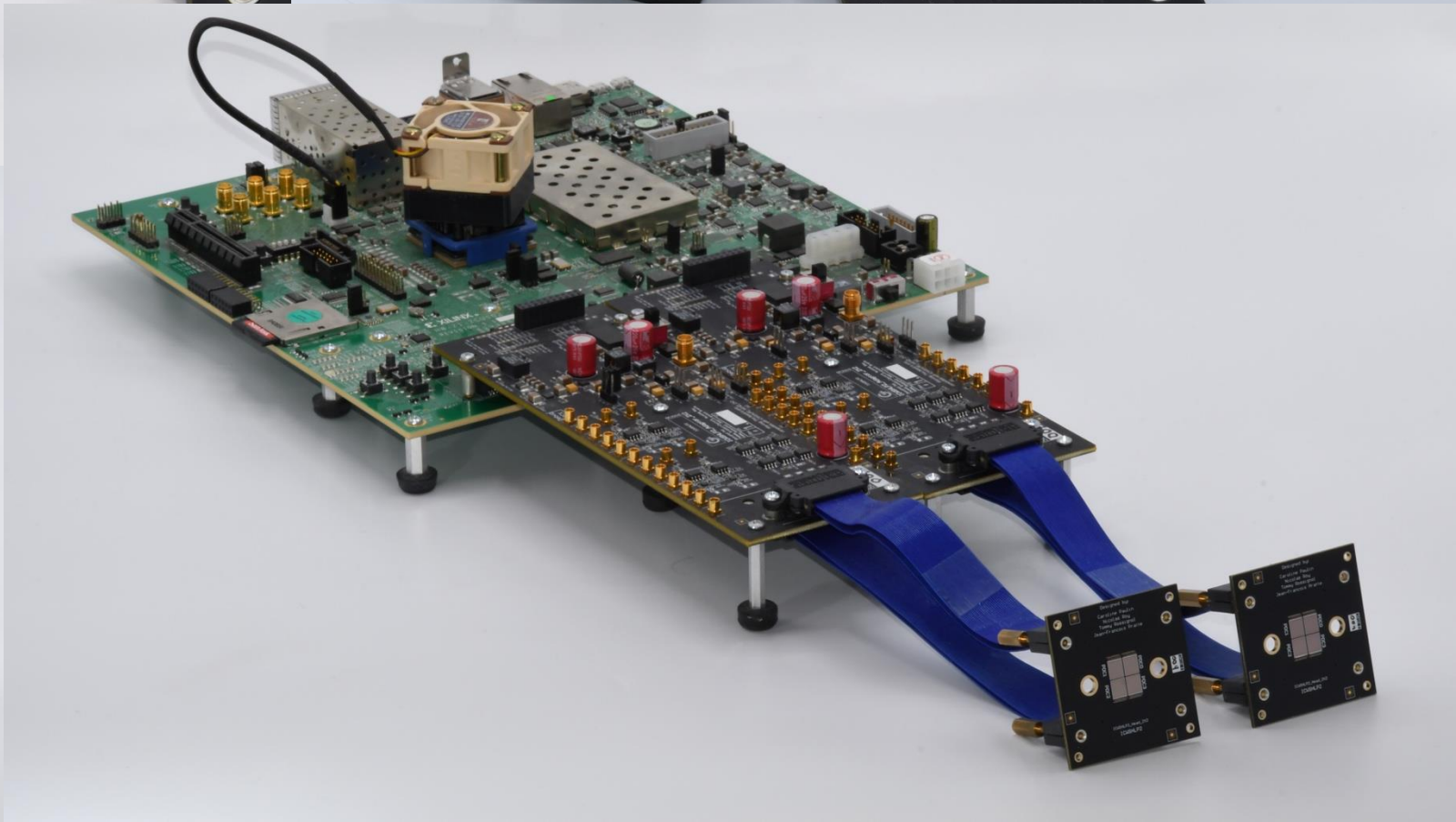
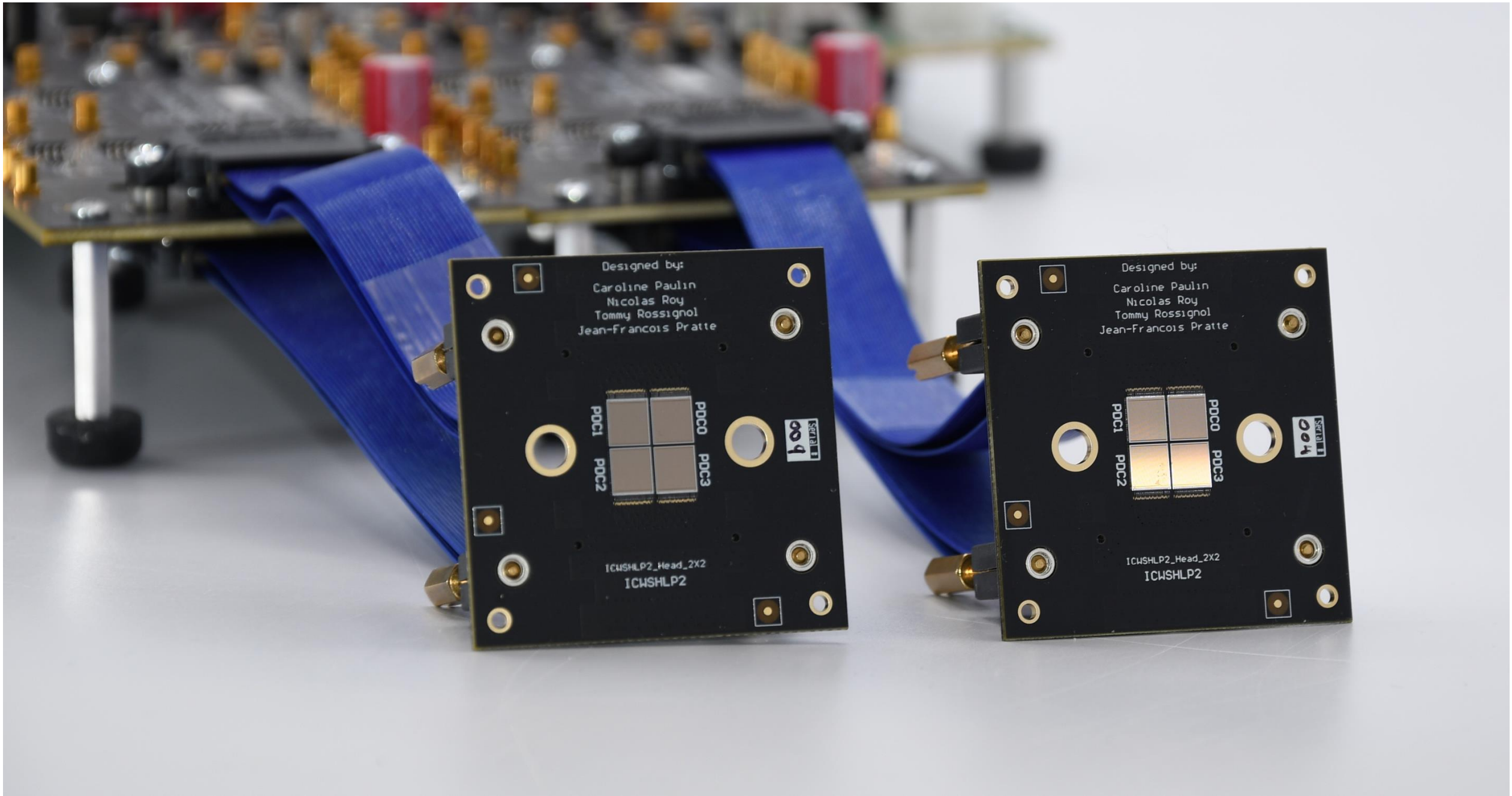
ICWSHLP2_Head_2X2
ICWSHLP2

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PDC0
PDC1
PDC2
PDC3
ICWSHLP2_Head_2X2
ICWSHLP2

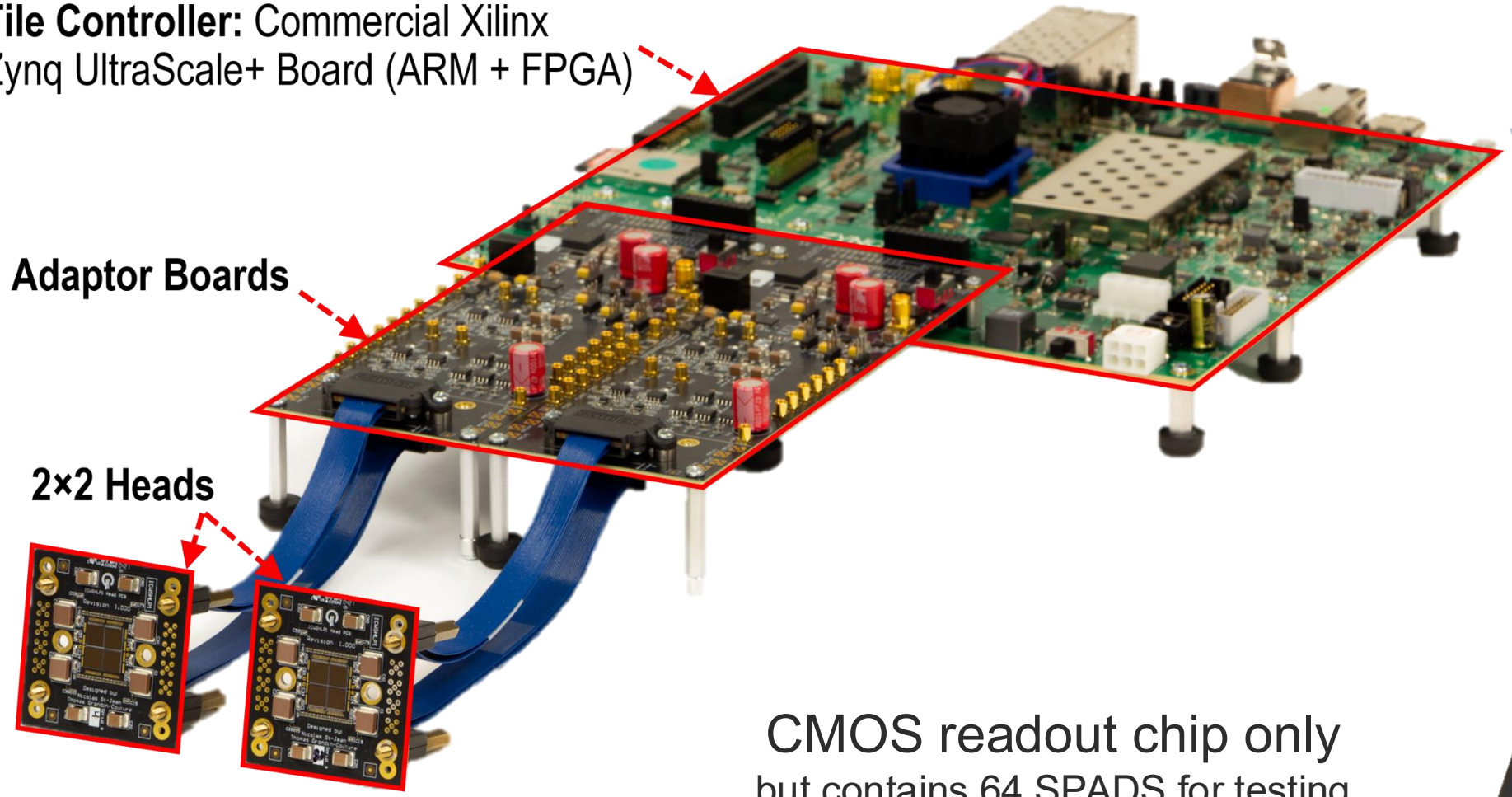
2×2 Photodetection Module

UDS

Tile Controller: Commercial Xilinx Zynq UltraScale+ Board (ARM + FPGA)

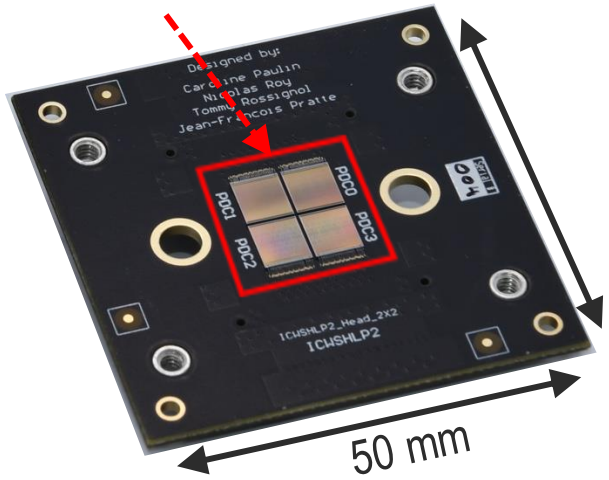
Adaptor Boards

2×2 Heads



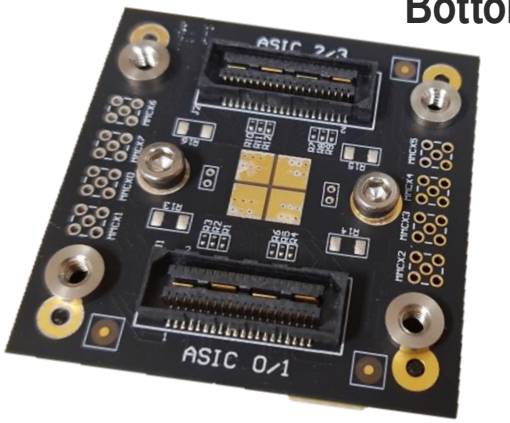
2×2 PDCs

Top



50 mm

Bottom



CMOS readout chip only

but contains 64 SPADS for testing

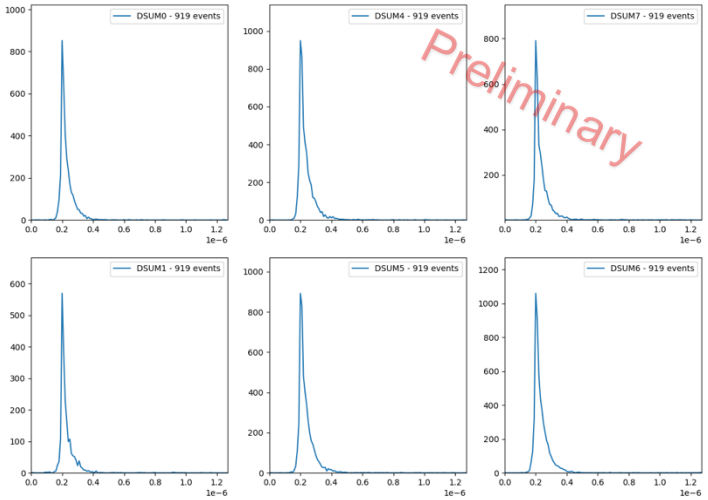
→ Its a « functional » detector

A simple coincidence measurement setup

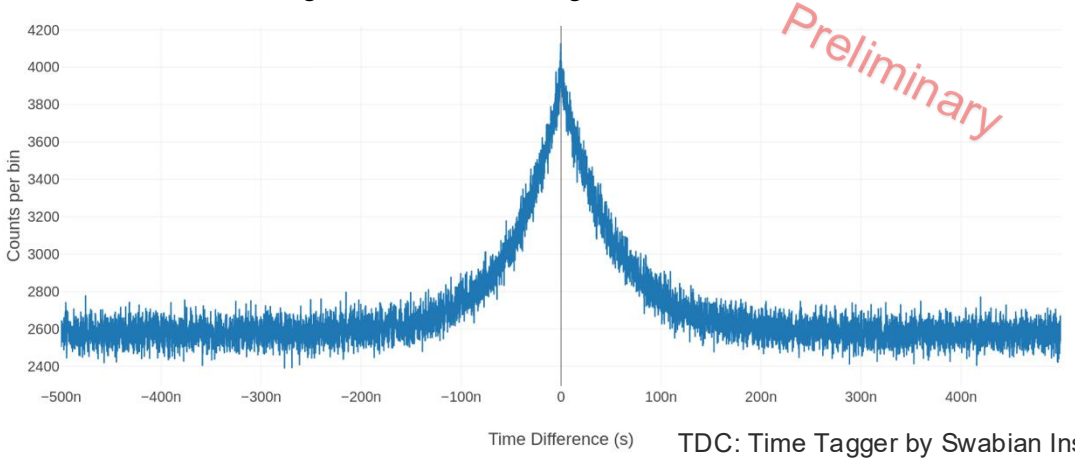
UDS

Demonstrating two modes of operation

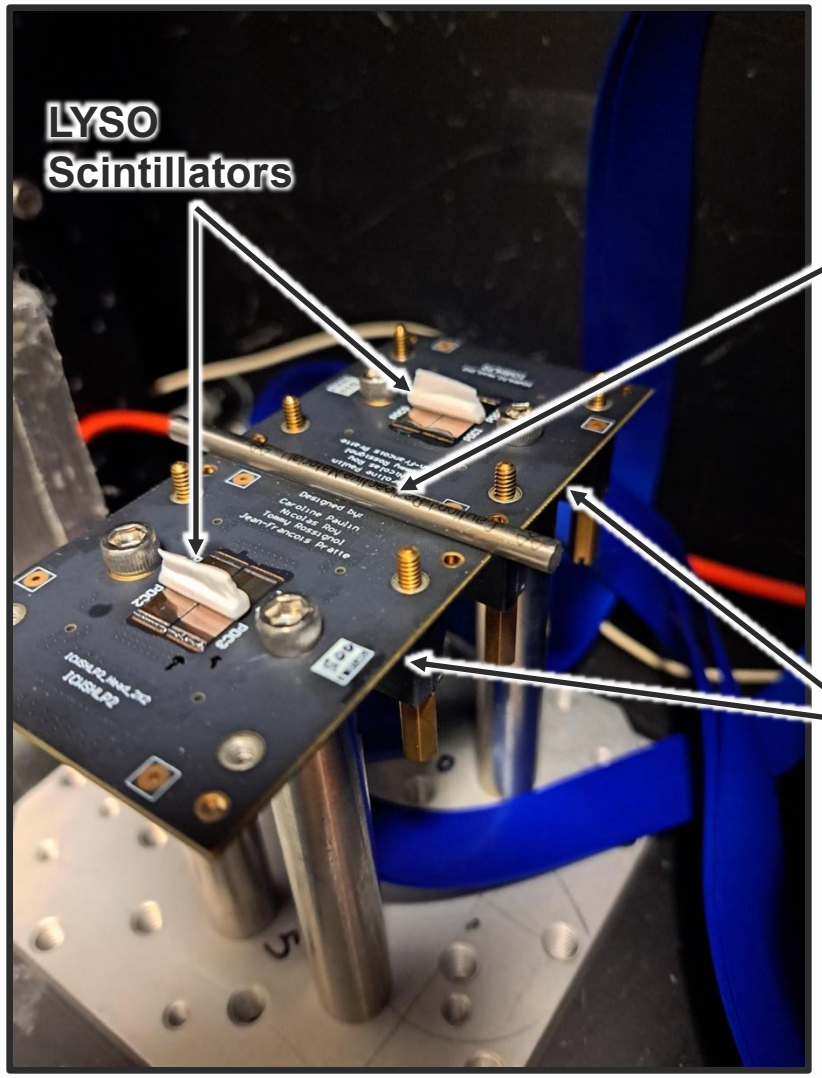
- Digital sum
  - once a trigger is detected
  - for 6 PDCs on 2 heads



- Time interval with external TDC
  - Correlation histogram between flags from 2 PDCs



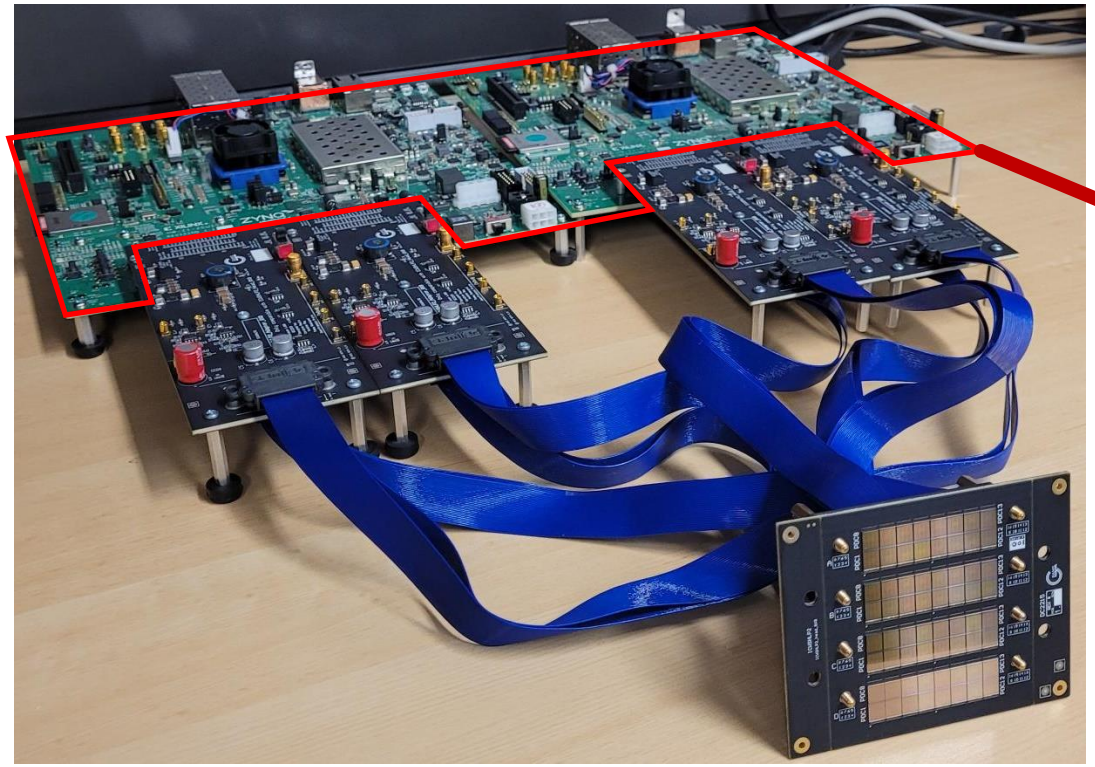
TDC: Time Tagger by Swabian Inst.



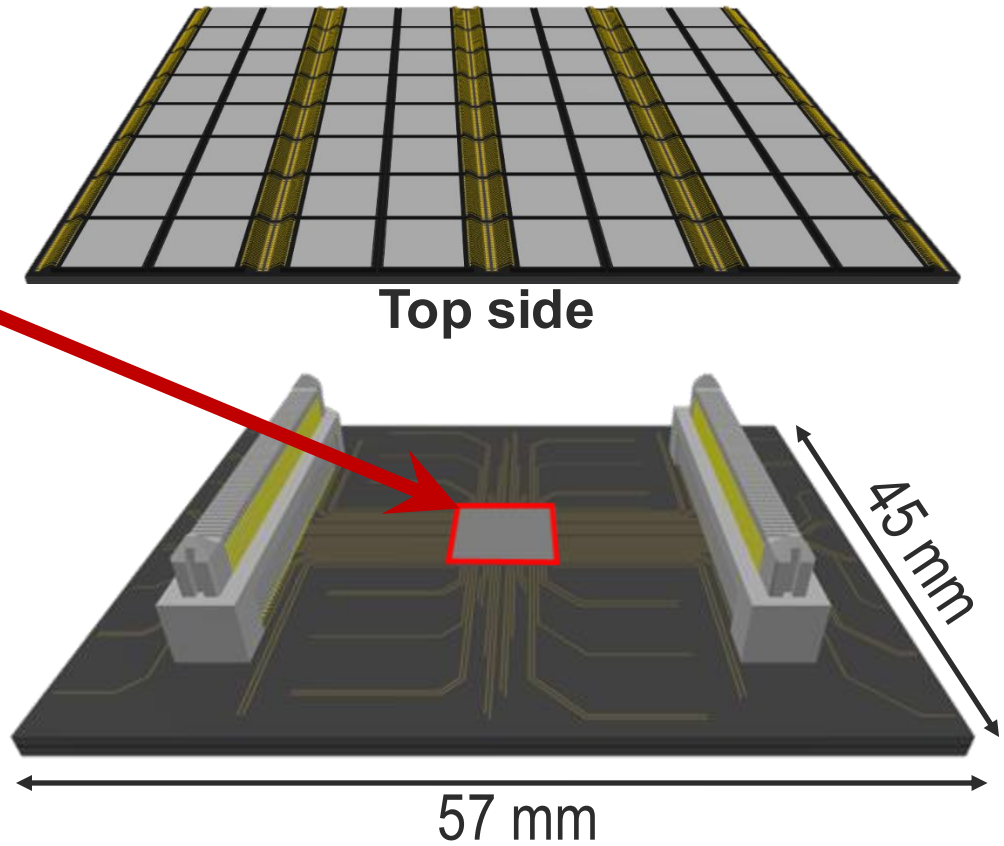
Next Step: FPGA board to a Tile controller

UDS

FPGA-based Controller



ASIC-based Controller



With support from OAK RIDGE National Laboratory