High-bandwidth and Low-latency Data Transfer Tests for the new ATLAS Liquid Argon Calorimeter Readout

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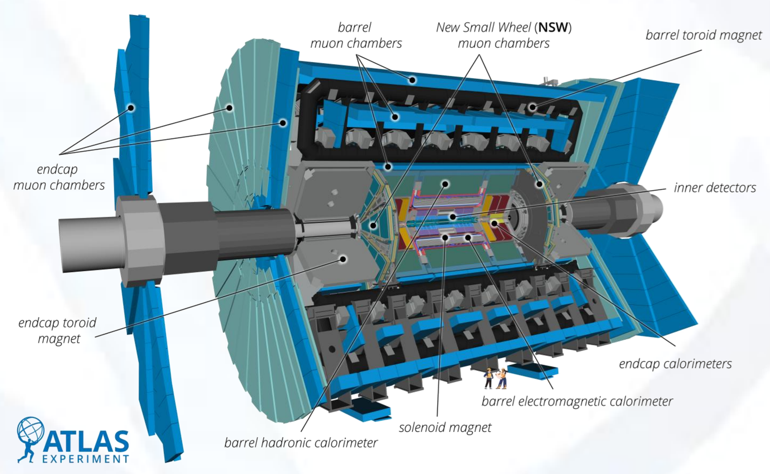
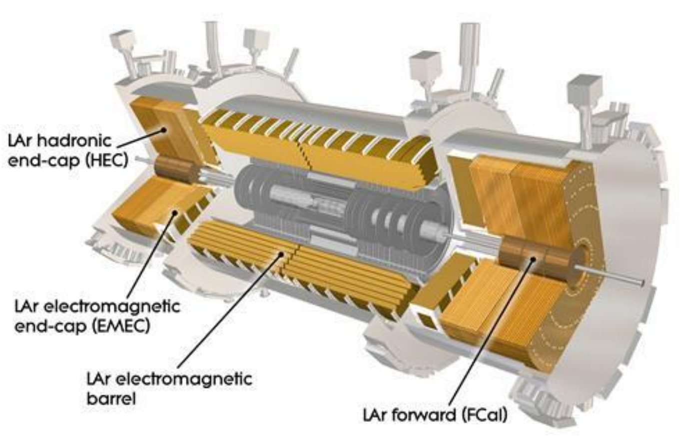


ATLAS is a general-purpose detector at the **Large Hadron Collider** (LHC) designed to detect a wide range of particle physics phenomena

1. Liquid Argon Calorimeter



- Liquid Argon (LAr) based sampling calorimeter with metal absorbers
- Incoming electrons, photons, and hadrons shower in the absorber and ionize the liquid argon

2. High-Luminosity LHC

What is it?
LHC upgrade to achieve instantaneous luminosities a factor of 5 to 7.5 its nominal value, enabling experiments to enlarge their data sample by one order of magnitude compared to the LHC baseline programme

Physics Goals: Extend sensitivity of searches for new physics and improve precision measurements

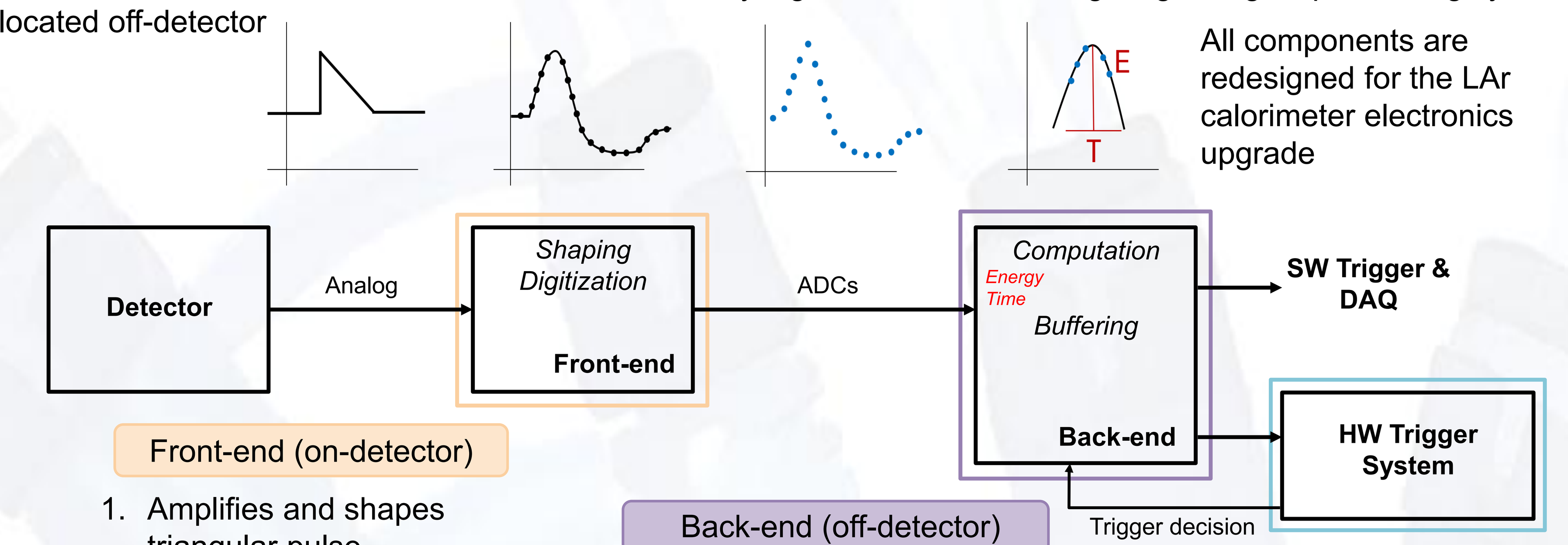
LAr Calorimeter at the HL-LHC:
- Radiation limits of current readout electronics will be exceeded
- Current readout is incompatible with the planned upgrade of the Trigger/DAQ systems

New requirements lead to the design of a completely **novel** LAr Calorimeter readout for the HL-LHC

3. New LAr Calorimeter Readout

Raw data from all calorimeter cells will be continuously digitized and sent to large digital signal processing system located off-detector

All components are redesigned for the LAr calorimeter electronics upgrade



Front-end (on-detector)
1. Amplifies and shapes triangular pulse
2. Samples and digitizes signals at 40 MHz
3. Serializes ADC outputs and sends off-detector via optical links

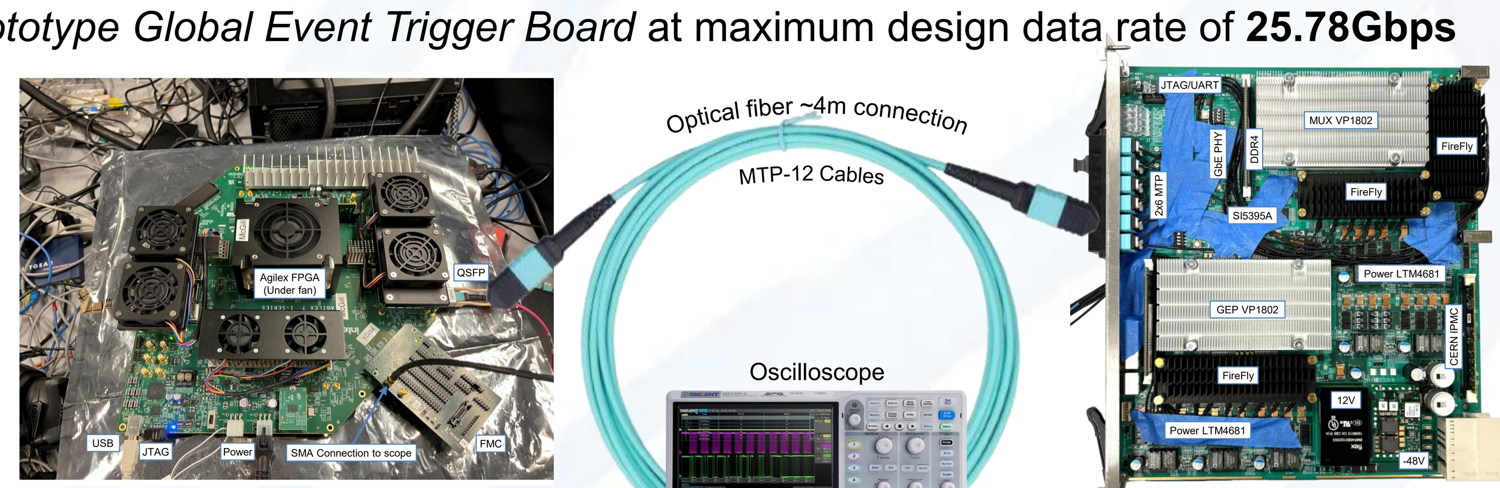
Back-end (off-detector)
1. Processes ADC values to extract energy and time of signal
2. Sends information to trigger system at 40MHz
3. Buffers values while waiting for trigger decision
4. Sends full data stream to DAQ

Global Event Trigger Processor (GETP)
- Receive energies from cells which pass a 2σ above-noise-ratio threshold
- Consist of:
  - Feature extraction modules
  - Global Event Processor Trigger

LAr Signal Processor (LASP)
- Monolithic custom-designed ATCA blade with two Field-Programmable Gate Array (FPGA) processing units
  - Use high-performance Intel FPGAs
- Each board receives digitized waveform from 768 calorimeter cells
  - ~1.35 Tbps of data!
- **Send reconstructed energy and time to Global Trigger at 25.78Gbps**

4. Hardware Setup

Goal: First demonstration and test of **data transfer** between *LASP-like device* and *prototype Global Event Trigger Board* at maximum design data rate of **25.78Gbps**

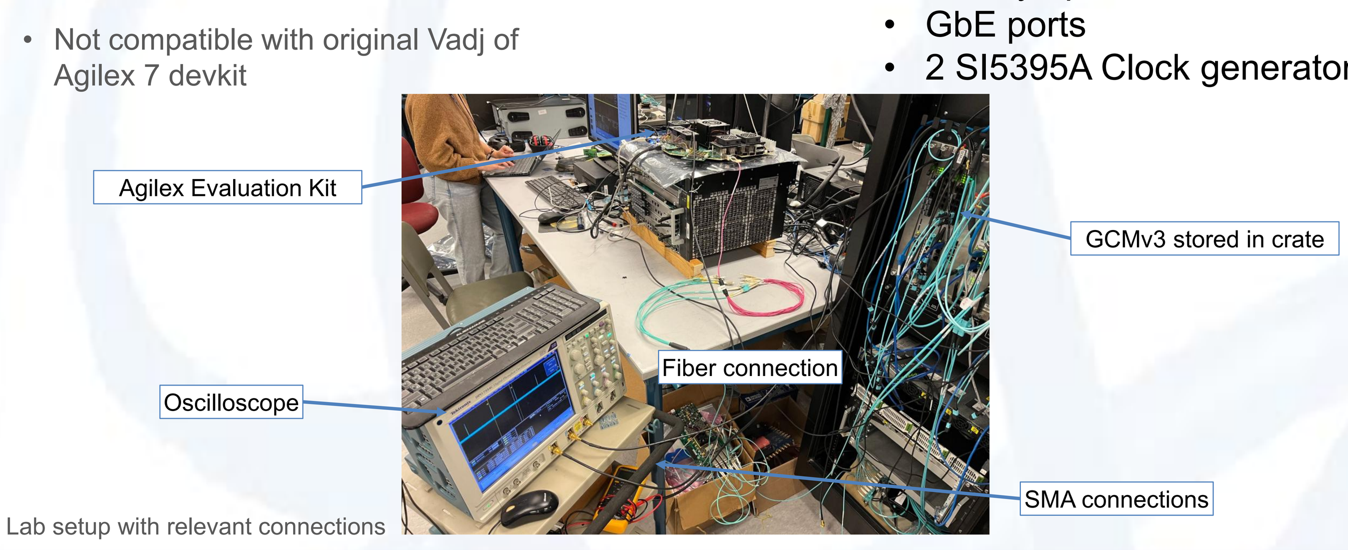


LASP-like device
Transmitting (TX)
Altera Intel Agilex7 FPGA Evaluation Kit

- I-series Transceiver Development Kit
  - DK-SI-AGI040FES
  - (6x F Tile) transceiver capabilities
- QSFP Modules
  - QSFP-100G-SR4-S
- TX Optical Power OMA: -6 to 3 dBm
- Customized Xilinx XM105 FMC
  - Not compatible with original Vadj of Agilex 7 devkit

Global Trigger Prototype Board
Receiving (RX)
GCMv3 Hardware

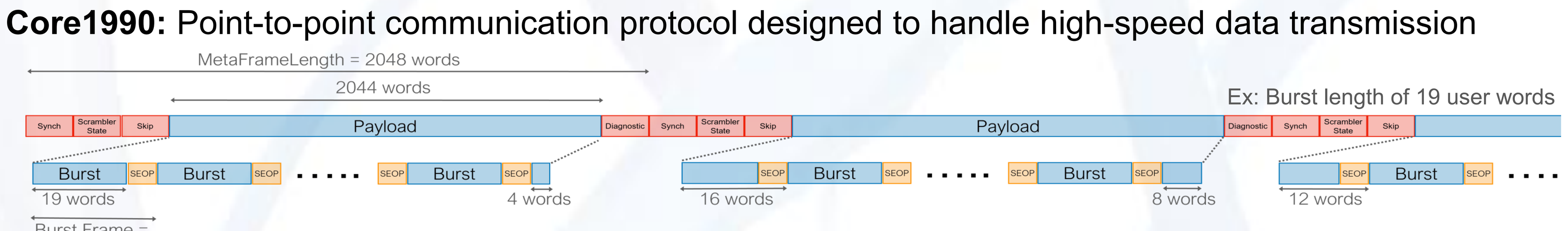
- Featuring Xilinx Versal Premium VP1802 System-on-Chip
  - 1 VP1802 for MUX (multiplexing logic)
  - 1 VP1802 for GEP/gCTPi (Global Event Processor / Global Common Trigger Processor interfaces
- FireFly optical interfaces
- GbE ports
- 2 SI5395A Clock generators



Lab setup with relevant connections

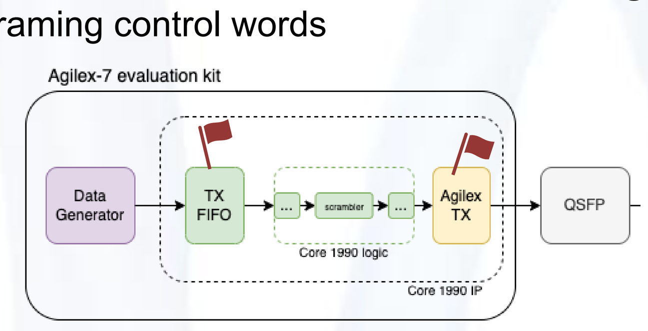
5. Firmware Implementation

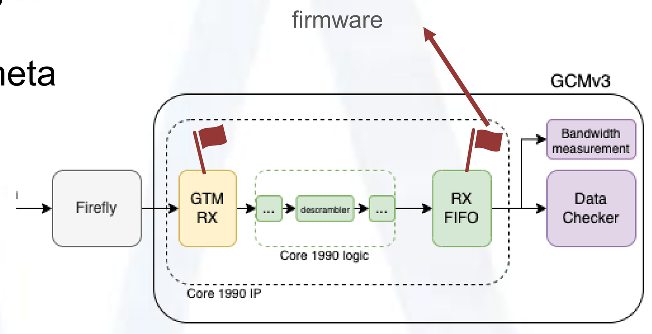
Core1990: Point-to-point communication protocol designed to handle high-speed data transmission



Implementation for LAr:
- Implementation uses Start/End of Packet (SEOP) words
- User data is packed into *Burst Frames* of size **Burst Length** + SEOP word
- A *Meta Frame* has size **'MetaFrameLength'** including 4 meta framing control words

Firmware raises flags before and after Core1990 IP core
- Seen using an oscilloscope
- Monitor behaviour of firmware





- Core1990 IP Core
  - Adapted for Intel FPGAs
- Single clock domain at 402.83 MHz
- Configurable data rate from Data Generator to **TX (Transmitting)** FIFO
- Configurable Core1990 Burst Lenght
  - Number of data words per burst

- Core1990 IP Core
- Single clock domain at 402.83 MHz
- Data checker reports data integrity based on the transmitted data pattern
- Two synchronous accumulators
  - First increases every clock cycle and acts as a time reference
  - Second increases every valid **RX (Receiving)** data

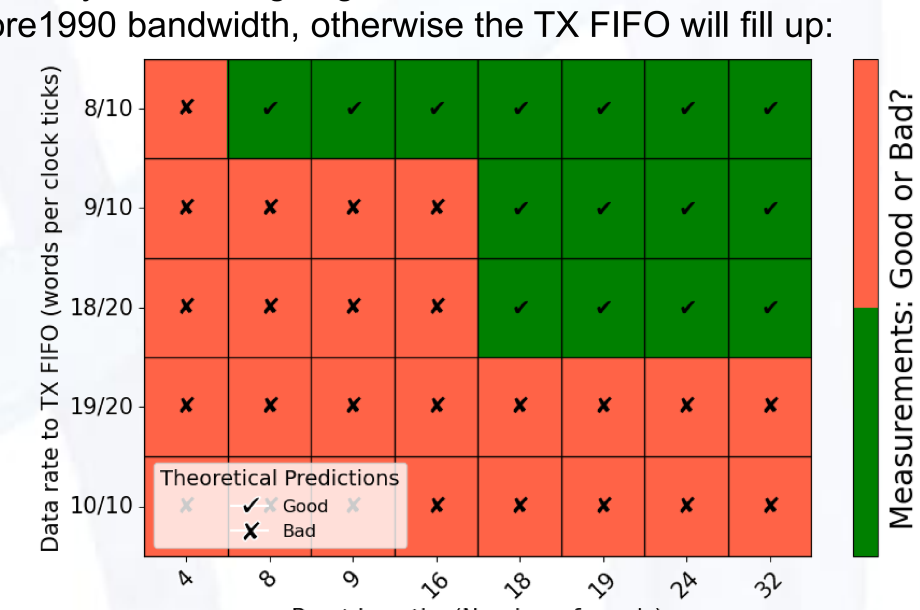
6. Results: Bandwidth and Latency Measurements

Theoretical Bandwidth Measurements

Core1990 bandwidth:
- Start with maximum bandwidth = 25.78125 Gbps (402.83 MHz x 64-bits)
  - × 64/67: Due to 64/67-bit encoding (64-bit payload + 3-bit header)
  - × N/(N+1): Burst Length of N words followed by a SEOP word
  - × 2044/2048: Meta framing overhead (4 meta words every 2044 words)
- For example, for N=19, the bandwidth is 23.35 Gbps

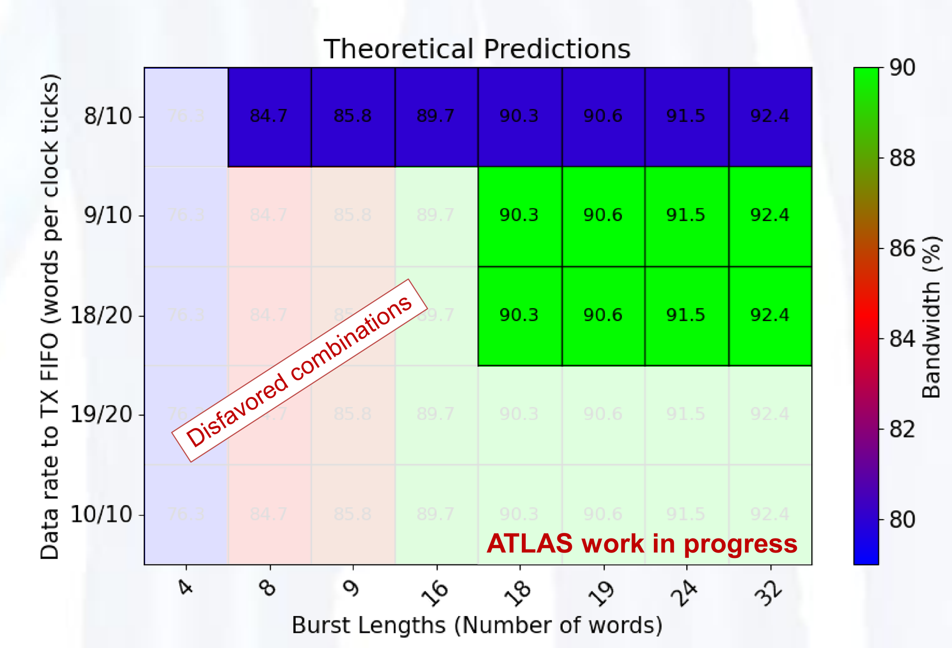
Data rate into TX FIFO from Data Generator:
- For example, data rate of 8 words every 10 clock ticks corresponds to a bandwidth of 25.78 Gbps × 8/10 = 20.63 Gbps

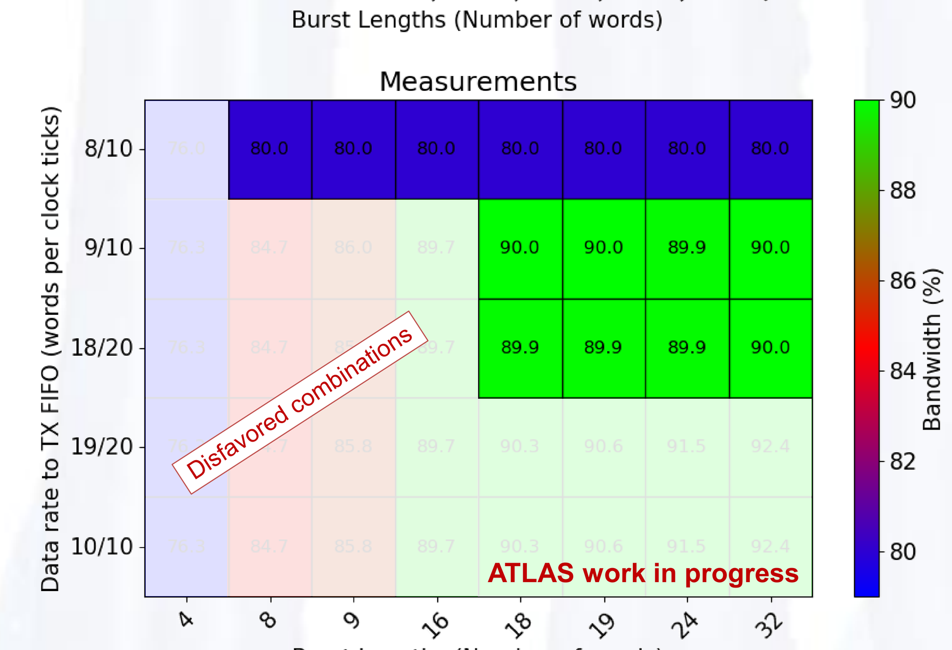
In theory, data rate going into FIFO must match or exceed the Core1990 bandwidth, otherwise the TX FIFO will fill up:



- Yes ✓: TX FIFO does not fill up
  - Good combination of parameters!
- No ✗: TX FIFO fills up

Theory and measurements match perfectly.



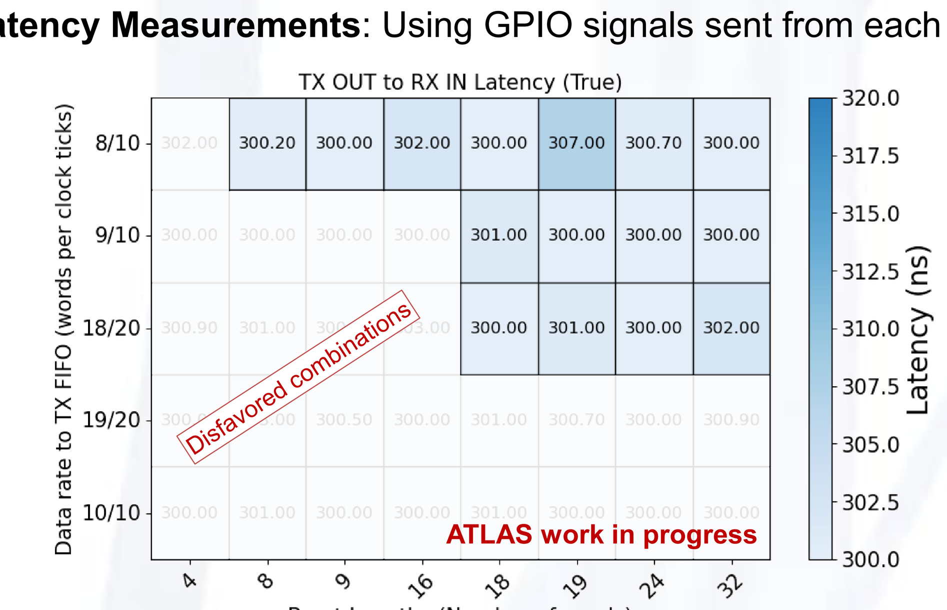


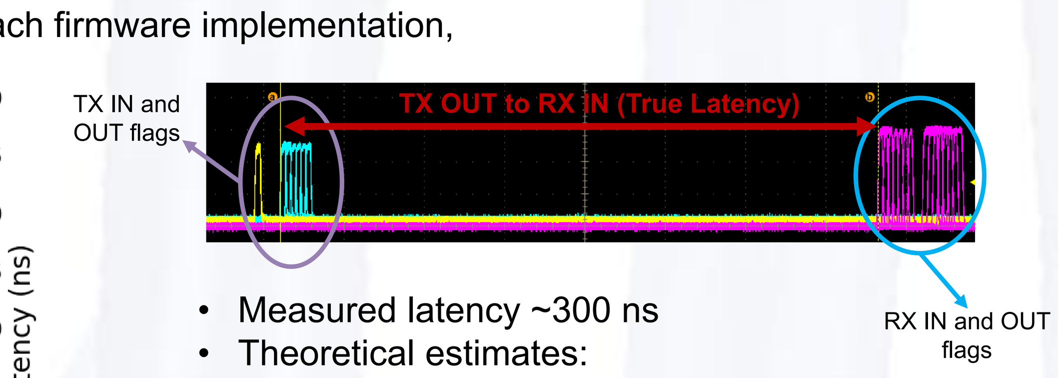
Measurements are expressed as fraction of total available bandwidth (25 Gbps).

Measurements differ from theoretical predictions by at most 13%

Viable combination of parameters found at **90% total bandwidth**

Latency Measurements: Using GPIO signals sent from each firmware implementation,





- Measured latency ~300 ns
- Theoretical estimates:
  - 313-329 ns
  - Match measurements
- Constant latency within measurement uncertainties
- Full understanding of contributions to latency value

7. Conclusion

Successful demonstration of data transfer between *LASP-like device* and prototype *Global Event Trigger Board*

- LASP Agilex to GCMv3 data transfer on 4 optical links
- Updated Core1990 protocol specifically for LAr
- No bit errors found on overnight run

Found desirable data rate and burst length combinations based on **excellent agreement** between measurements and theoretical predictions

- Exploited whole parameter space
- Optimize data amount and transfer rate