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Efficacy of Radiation Hardening by Design Techniques on an ASIC 32-bit RISC-V Microcontroller

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A 32-bit RISC-V microcontroller is designed and fabricated at a 22-nm FD SOI node using Radiation Hardening by Design Techniques. The device features 512 KB of on-board memory and can run at a clock speed of ~300 MHz. The device also supports a rich set of interface options. Using both architectural changes as well as more complex standard cell replacements, the device shows strong reliability against SEE induced faults in broad-beam testing. The device is also functional after 100 kRad of testing using high-energy protons. Results from irradiation experiments suggest that the core and peripherals are extremely robust, with SEFIs originating from accumulated memory errors. With proper software design, the device can be SEFI immune up to an LET of 96.30 MeV·cm2/mg.

Keyword-1

Singe Event Upset

Keyword-2

Radiation

Keyword-3

Semiconductor

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