

# Efficacy of Radiation Hardening by Design Techniques on an ASIC 32-bit RISC-V Microcontroller

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**Abstract:** A 32-bit RISC-V microcontroller is designed and fabricated at a 22-nm FD SOI node using Radiation Hardening by Design Techniques. The device features 512 KB of on-board memory and can run at a clock speed of ~300 MHz. The device also supports a rich set of interface options. Using both architectural changes as well as more complex standard cell replacements, the device shows strong reliability against SEE induced faults in broad-beam testing. The device is also functional after 100 kRad of testing using high-energy protons. Results from irradiation experiments suggest that the core and peripherals are extremely robust, with SEFIs originating from accumulated memory errors. With proper software design, the device can be SEFI immune up to an LET of 96.30 MeV·cm<sup>2</sup>/mg.

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## I. INTRODUCTION

Radiation induced upsets in digital systems, such as memories, processors, or complete system-on-chips is one of the leading concerns for device reliability [1, 2, 3]. As engineers and designers of space systems continue to require higher performance and more power efficiency, smaller feature sizes and increased memory density must be utilized, which often results in systems becoming even more prone to radiation-induced faults [4].

In recent years, the RISC-V Instruction Set Architecture (ISA) has become increasingly popular for usage in the space industry [5, 6]. In many prior works, forms of triplicated lock-stop devices have been proposed and tested for RISC-V microcontrollers, with varying levels of hardness assurance [7, 8]. However, these types of approaches are often costly to implement. Furthermore, many prior works have investigated soft-cores synthesized on SRAM or flashed based FPGAs, as opposed to custom-designed ASICs [9, 10, 11]. Therefore, there is a lack of information for the performance of custom-fabricated devices.

In this work, a 32-bit RISC-V microcontroller is designed, fabricated, and tested with broad-beam radiation sources to evaluate its soft error rate (SER). The device, named StarRISC, utilizes several architectural and layout-based techniques to significantly improve the reliability of the device. It is shown that with proper knowledge of the radiation environment and strong understanding of software design, the device can be SEFI immune up to an LET of 96.30 MeV·cm<sup>2</sup>/mg.

## II. RISC-V MICROCONTROLLER OVERVIEW

StarRISC is an adaptation of the CORE-V-MCU project by Open Hardware group. It features a small and efficient open-source RISC-V core, the CV32E40P [12, 13]. The ISA of the core has been extended to support both common RISC-V instruction set extensions, as well as a handful of custom instructions related to the PULP architecture. Additionally, the core supports a rich set of peripherals which includes UART, SPI, I2C, QSPI, and 32 GPIO ports. An onboard JTAG module is also present, which allows users to program the device and debug it through a supported eclipse-based Software Development Kit (SDK). Shown in Figure 1 is the architectural block diagram of the device.

The device has 512 KB of on-board SRAM memory, as well as a small read-only-memory for booting. All the on-chip memory is accessible to the core. The device also has an on-board Phase-Lock-Loop (PLL) CLK generator to drive the entire device with an operating speed of up to ~300 MHz. Table 1 provides a brief comparison of the device with comparable other rad-tolerant microcontroller devices commonly used.

## III. RADIATION HARDENING TECHNIQUES

StarRISC features a variety of hardening techniques to improve it's overall reliability in radiation rich environments. Firstly, the 512 KB SRAM was extended from 32-bit words to 39-bit words to store additional parity bits for a Single Error Correcting Double Error detecting (SECDED) hamming code. The direct

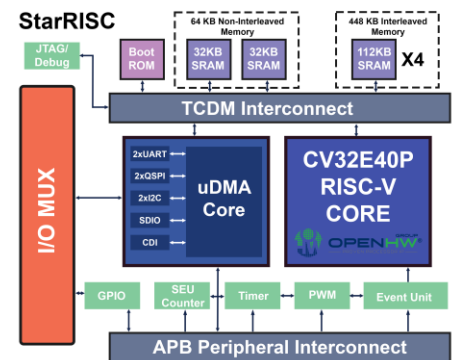


Figure 1: StarRISC architectural block

TABLE I  
SINGLE CORE RAD-TOLERANT DEVICE COMPARISON

| Device          | CLK Speed (MHz) | RAM Size | Interfaces                               |
|-----------------|-----------------|----------|--|
| <i>StarRISC</i> | ~300            | 512 KB   | I2C, UART, SPI, QSPI, JTAG, SDIO         |
| VA41630         | 100             | 320 KB   | I2C, ADC, CAN, SpaceWire                 |
| SAM3X8ERT       | 84              | 512 KB   | Ethernet, CAN, SDIO, UART, SPI           |
| GR716B          | 100             | 192 KB   | SpaceWire, Ethernet, CAN, UART, I2C, SPI |

memory core of the device was modified, such that reads of memory addresses containing single bit errors then became read-modify-write processes. From the perspective of a user, device memory reads also counted as memory scrubs. Additionally, flags to indicate single bit and double bit errors were connected to counters within the device so real-time monitoring of memory Single Bit Upsets (SBUs) and Double Bit Upsets (DBUs) could be implemented within the testing software.

Furthermore, all registers, whether they be flip-flops (FFs) or latches, within the core of the device and the supporting peripherals were replaced from their standard cell versions to custom-design radiation-hardened cells. All FFs or latches made use of the “stacked-transistor” hardening technique, which has been demonstrated in prior works to be an extremely effective hardening technique for FDSOI technologies [14, 15 16]. Shown in Figure 2 is an example schematic of the flip-flops used. Various layout-based techniques were used to separate sensitive nodes, induce the pulse-quenching effect, and separate active diffusion layers to make the cells as robust as possible [17]. Many different cells were made of varying drive strengths, sizes, and functionality in order to integrate the hardened cells into the design as seamlessly as possible. All cells underwent extensive TCAD simulations, showing no upsets for all device states up to a Linear Energy Transfer (LET) of 128 MeV·cm<sup>2</sup>/mg. Similar flip-flops were also beamline tested on a prior test-chip, showing no upsets up to an LET of ~90 MeV·cm<sup>2</sup>/mg, which was the largest value available at the beamline. These cells were also implemented into the divider and phase-frequency detector of the on-chip PLL, among other radiation hardening techniques for the charge pump and low pass filter.

Lastly, all buffer cells within the chip were set to higher drive strengths than required to assist with increased timing slack to aid with device TID degradation, as well as to make perturbations on CLK and reset lines as minimal as possible.

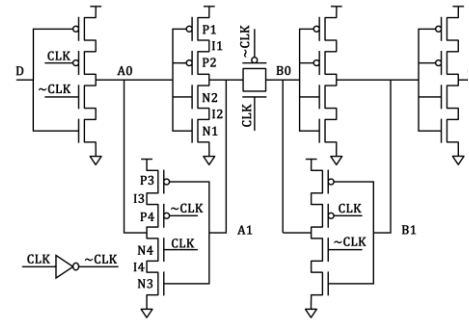


Figure 2: Example stacked-transistor flip-flop schematic used in the design of StarRISC.

## IV. EXPERIMENTAL SETUP & RESULTS

### A. Software & Device Setup

For all irradiation experiments the same setup and software configurations were used to keep all results comparable to one another. The StarRISC device was mounted on a development kit board, which allowed access to all device functionality and peripherals. A HS2 JTAG programmer was used to initiate the device and to dump any relevant information off the device during testing. The board was powered via a 9V barrel connector, such that board current could be monitored. The USB connector was also utilized so that real-time information from the device could be saved and monitored in the event of failures or crashes from the UART port.

The overall software suite is shown in Figure 3. The testing software used had two different modes, a *non-looped mode* in which all tests run only once before eventually repeating, and another *looped mode* in which each unit test ran multiple times before proceeding to the next. The reasoning for the two modes was to have a large amount of variation in the special and temporal access rates of the device memory to better mimic device usage in a realistic space environment.

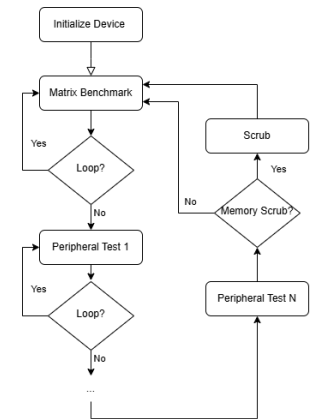


Figure 3: Example flowchart of software testing suite used during experiments

## B. Alpha Particle Testing

Alpha particle experiments were conducted at the University of Saskatchewan using an Americium-241 source with 2.5  $\mu\text{Ci}$  of activity and  $4.61\text{E}+7$   $\text{a}/\text{cm}^2/\text{hr}$  emissivity. The chip was de-lidded and the source was placed approximately 2 mm away from the surface of the die. Shown in Figure 3 is the device mounted on the development board undergoing alpha particle testing, along with a testing block diagram.

Initial experiments ran the non-looped suite with memory scrubbing occurring after all tests had completed. After 48 hours of testing the device was still operational, showing an average SRAM error rate of 80 SBUs per minute. Additional testing was run with no scrubbing, with a resulting SBU rate of around 50 per minute. This shows that the testing suite alone utilizes a little more than half of the memory space. No DBUs were observed during these tests. However, if memory scrubs occurred after a considerable time, double bit errors could be detected in unused memory regions of the device. This suggests that individual alpha particles are not capable of causing DBUs in device memory, but rather that these DBUs originate from accumulated SBUs within the same data word.

## C. Proton Irradiation

Proton testing was performed at TRIUMF in Vancouver British Columbia using 105 MeV protons, as shown in Figure 5. Experiments included both looped and non-looped tests. For all scenarios tested no device failures or crashes were observed. Devices were tested up to a fluence of  $1\text{E}12$  particles/ $\text{cm}^2$ , and up to a total dose rate of  $\sim 100$  kRad. There were no measurable differences in the operating current, and the average SBU rate was  $\sim 7$  per minute.

## D. Heavy Ion Irradiation

Heavy ion experiments were conducted at the Texas A&M Cyclotron facility using Cu, Kr, Ag, and Pr ions in the 15 MeV cocktail with respective LETs of 18.4, 30.1, 43.5, and 64.1. The flux rate used for testing was  $1\text{E}4$  particles/ $\text{cm}^2/\text{second}$ .

During testing of the non-looped tests, no errors or SEFIs were observed up to an effective LET of 96.30 MeV·cm<sup>2</sup>/mg. However, for looped tests both non-critical and device crashes were observed at all tested LET values. Figure 6 shows the SRAM cross-section per bit as found by non-looped testing with scrubbing. Shown in Figure 7 are the device SEFI and total memory DBU cross-sections for nominal LET values. Shown in Figure 8 are the device

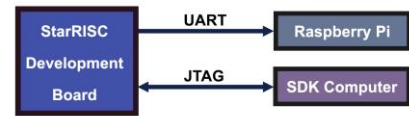


Figure 4: The StarRISC development board and testing block diagram.

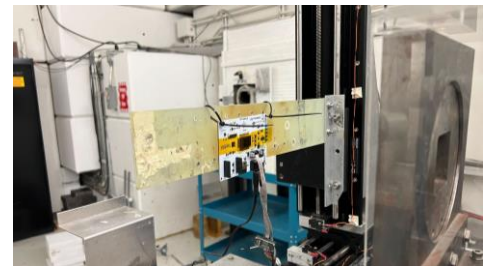


Figure 5: Proton irradiation of StarRISC at TRIUMF. The beam was collimated to be focused only on the microcontroller.

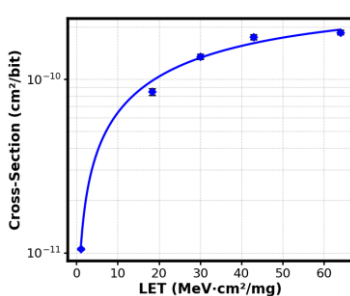


Figure 6: Device SRAM SBU cross-section per bit.

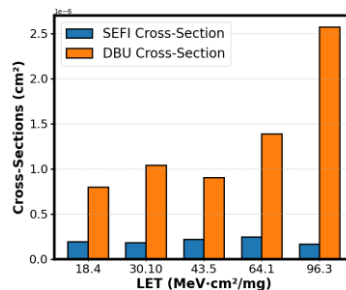


Figure 7: SEFI & DBU cross-section during "looped" testing.

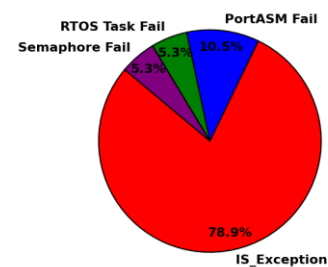


Figure 8: Percentage of error codes seen during looped testing.

crash error codes seen during testing and their percentage of all errors seen. SEFI cross-sections did not increase with LET. Similarly, DBUs did not generally increase until exposed to particles with very high LETs. As well, for all device failures the “IS\_Exception” fault was by far the most common occurrence during device failure.

Table II documents all observed device error codes, their number of occurrences and at what LET, as well as a brief description and probable cause of the error.

TABLE II  
DEVICE FAILURE CODES DURING HEAVY ION IRRADIATION

| DEVICE ERROR CODE    | PARTICLE LETS DURING FAILURE  | NUMBER OF OCCURRENCES | DESCRIPTION & LIKELY CAUSE   |
|----------------------|-------------------------------|-----------------------|--|
| IS_EXCEPTION         | 18, 30, 43, 46*, 61*, 64, 96* | 15                    | GLOBAL EXCEPTION HAS BEEN RAISED. MACHINE PROGRAM COUNTER, OR INSTRUCTION CODE IS UNDEFINED OR NULL.       |
| PORTASM FAILURE      | 43, 61*                       | 2                     | ERROR DURING CONTEXT SWITCHING OR REGISTER SERVICE ROUTINES. LOADED REGISTER VALUES ARE NULL OR UNDEFINED. |
| TASK CONTROL FAILURE | 64                            | 1                     | PRIORITY VALUES FOR TASKS WITHIN FREERTOS ARE IN UNDEFINED OR NULL STATE                                   |
| SEMAPHORE FAILURE    | 96*                           | 1                     | QUEUE POINTER IN FREERTOS IS IN A UNDEFINED OR NULL STATE.   |

\* Indicates an LET value achieved via angled device testing

## V. CONCLUSION

During proton testing no device test failures or entire device SEFIs occurred, despite a total testing fluence of 1E12 particles/cm<sup>2</sup>. These results show that the device is remarkably resilient to faults from protons. During proton testing the rate of SBUs collected was low, which also suggests that the rate of memory errors most likely contributes to the overall device reliability.

Charged particle testing did yield device crashes, but only for the looped testing suite. During non-looped testing all the actively used device memory is frequently passed over, thus repeatedly scrubbing the sensitive memory regions. For looped tests, only a small portion of the used memory is repeatedly accessed at any given time. As such, it is expected that the device SEFI cross-section rate is closely related not only to particle LET, but also the rate at which memory upsets are collected and scrubbed. For the error codes recorded during testing, all can be explained by corrupted memory being loaded into the core and thus raising global exceptions in the device.

In summary, the device shows strong reliability to radiation-induced faults. Results suggest that the applied radiation hardening techniques are effective at preventing faults in the core and peripherals, and that any remaining failures are the results of accumulated memory upsets.

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