Radiation damage investigation of epitaxial p-type silicon using Schottky and pn-junction diodes

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Schottky Project description and goals

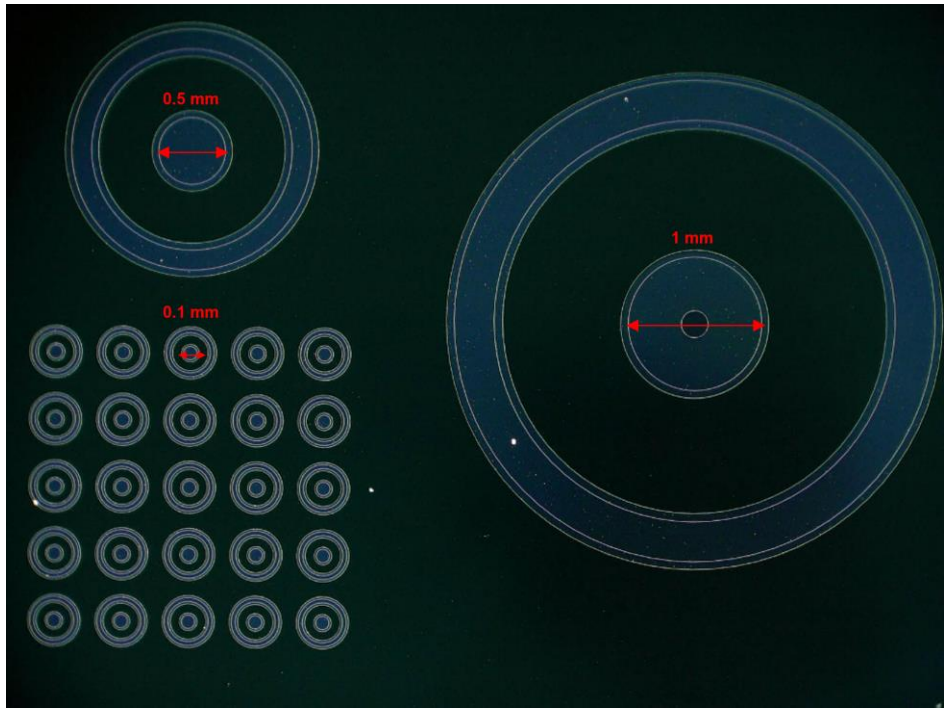
part of RD50 - Radiation hard semiconductor devices for very high luminosity colliders

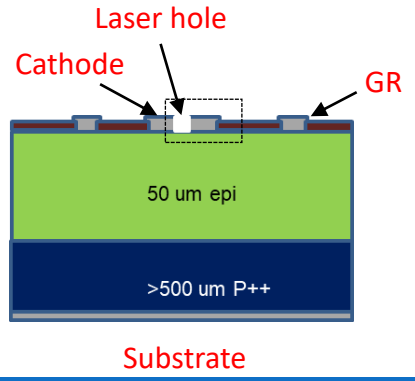
- **What:**
  - fabricate Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers
  - doping concentrations as they are normally found in CMOS MAPS devices
- **Why:**
  - investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors
  - develop reliable damage models that can be implemented in TCAD device simulators
- **How:**
  - 6-inch wafers at five B-doped epitaxial levels (10^{13} to 10^{17} cm^{-3}) 25x each, total **125 wafers**
  - fabrication process at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF)
  - measurements will be carried out at RAL, Carleton, Birmingham, JSI, IHEP

Design and layout of devices

5 type of devices proposed:

- #1: 2 mm Ø cathode with 0.4 mm Ø central hole, 10 x 10 mm^2 area
- #2: 1 mm Ø cathode, 0.2 mm Ø central hole, 5 x 5 mm^2
- #3: 0.5 mm Ø cathode, no central hole, 2.5 x 2.5 mm^2
- #4: 0.1 mm Ø cathode, no central hole, 0.5 x 0.5 mm^2
- ‘cell’ with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)
- detailed description during the 35th RD50 workshop





Fabrication details & comparison

RAL-ITAC

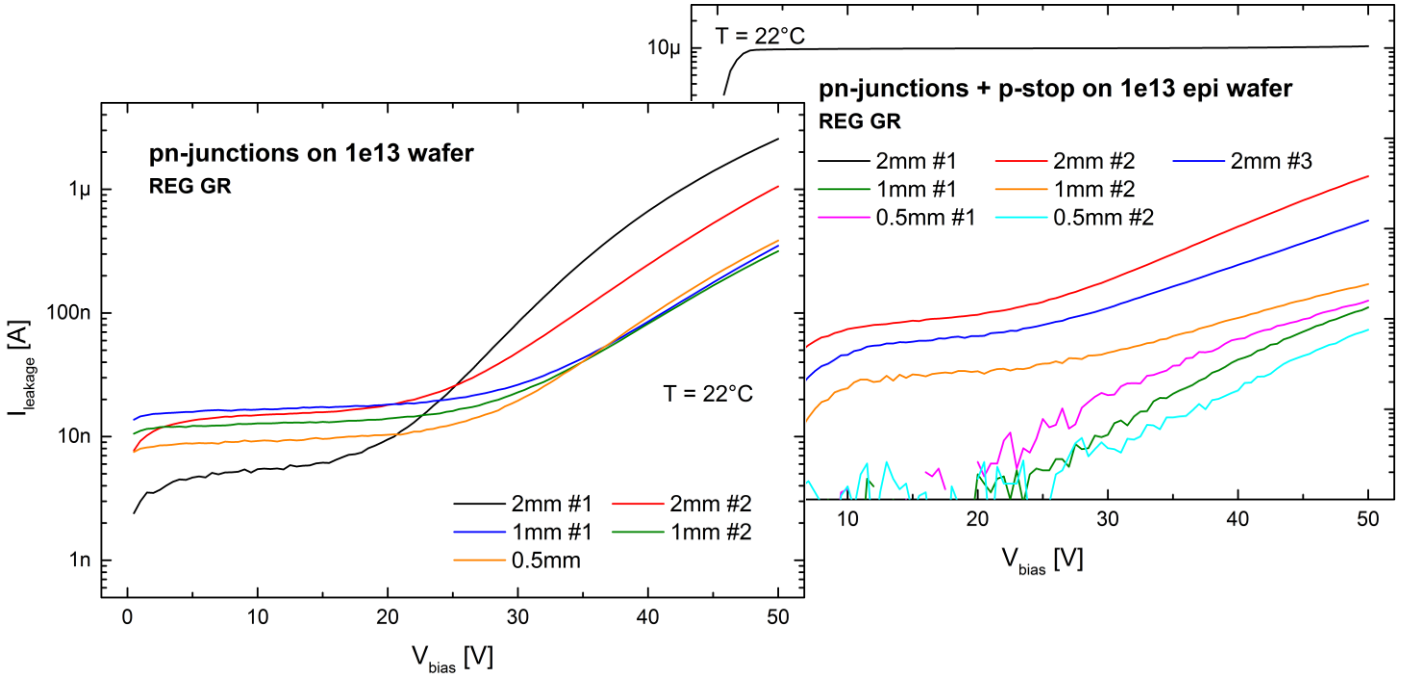
- Schottky fabrication process only, optimised on test wafers
- oxide deposition @150°C
- Al sputtering immediately after etching (no thin SiO2 layer)
- Al lift-off in Acetone ultrasonic tank

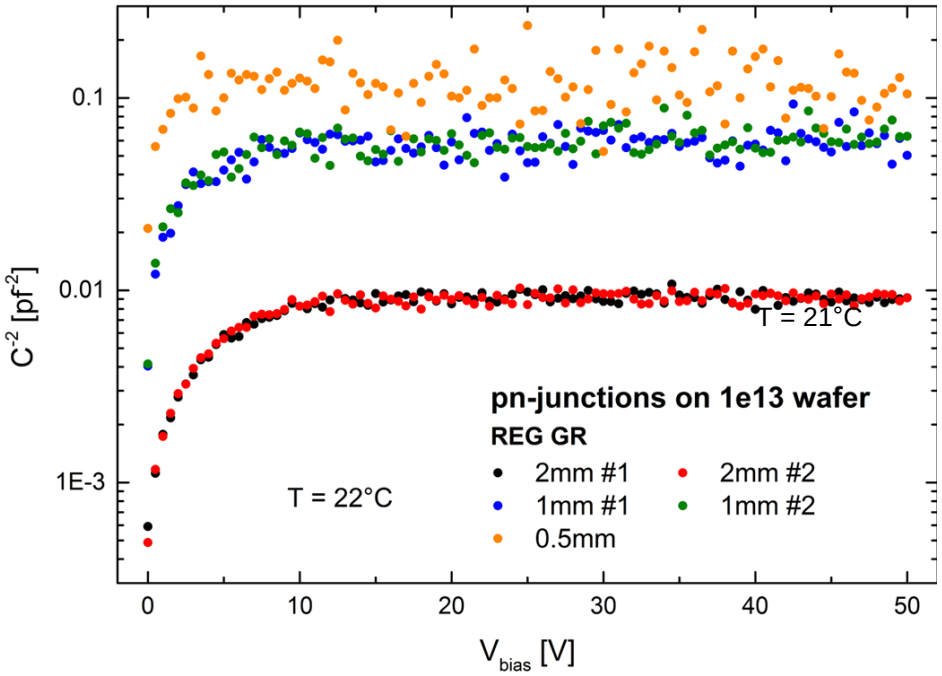
CUMFF

- pn-junction and Schottky processes, optimised on test wafers
- 6” substrate wafers laser cut into 4” or 6” wafer pieces
- high temperature thermal oxidation
- Al front metal thermal deposition, back Al via e-beam evaporation
- front metal patterning + etching

full details of fabrication processes in E.G. Villani’s talk from the 36th RD50 Workshop

IV + CV measurements: CUMFF pn-junctions (1e13 vs. 1e16)





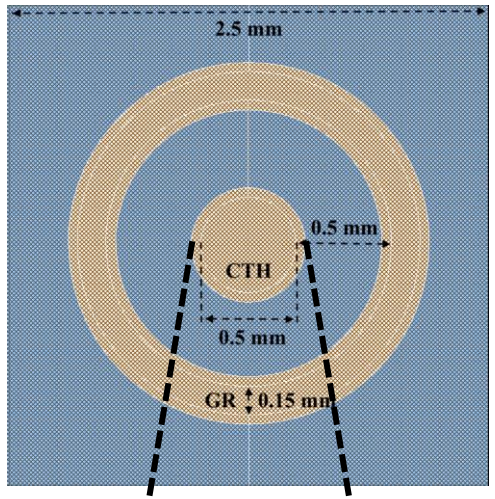
- current can vary by large margin on same wafer
- very low initial current often seen
- no hard breakdowns observed; gradual increase in current
- ➢ leakage current at much lower levels compared to first fabrication iterations

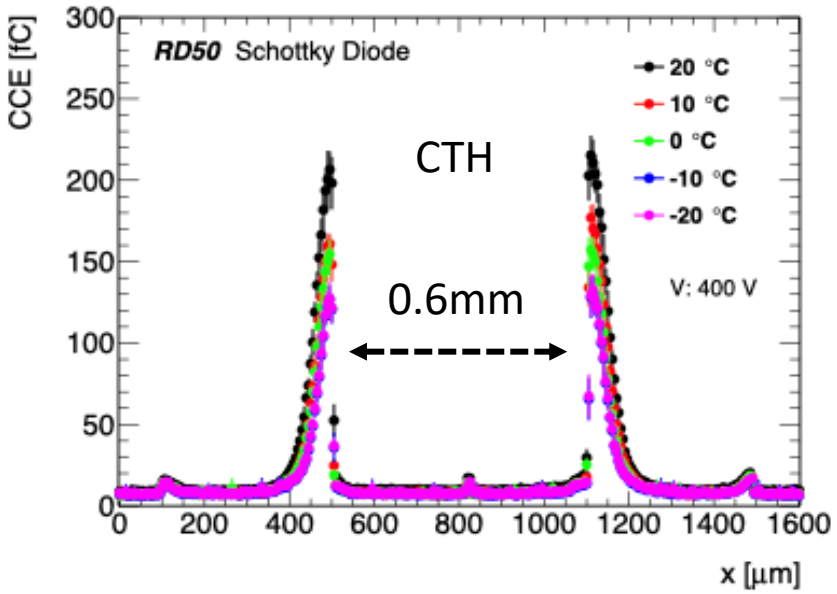
- depletion of epi layer at low voltages
  - small differences for different structure flavours
  - agrees with back-of-the-envelope calculation for high-resistivity 50um epi layer
- capacitance scales nicely with structure size

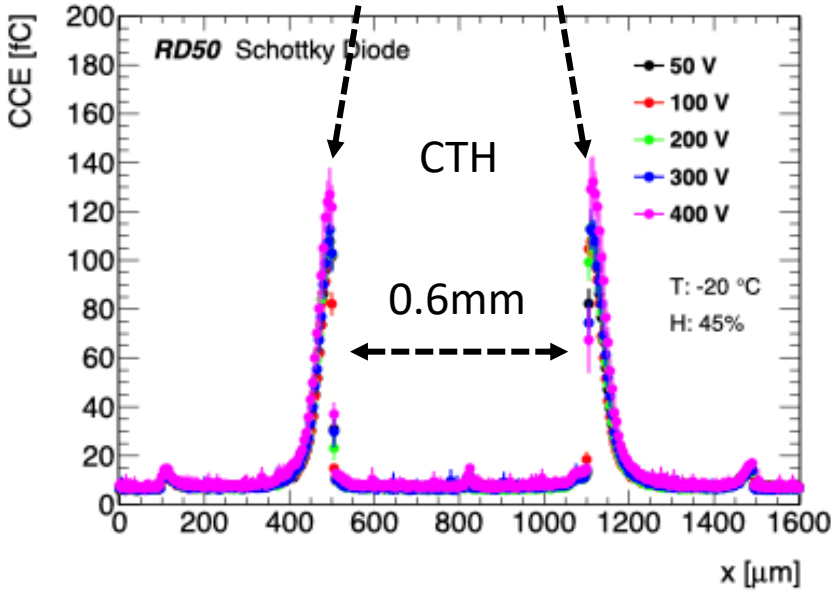
more basic electrical measurements in backup

Charge Collection Efficiency: RAL Schottky (unirrad.)

- Schottky diode with no central laser hole
- Bias Voltages: 50, 100, 200, 300, 400 V
- Temperatures: 20, 10, 0, -10, -20°C

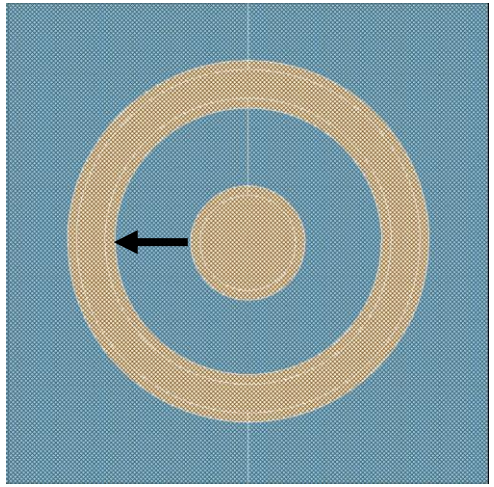


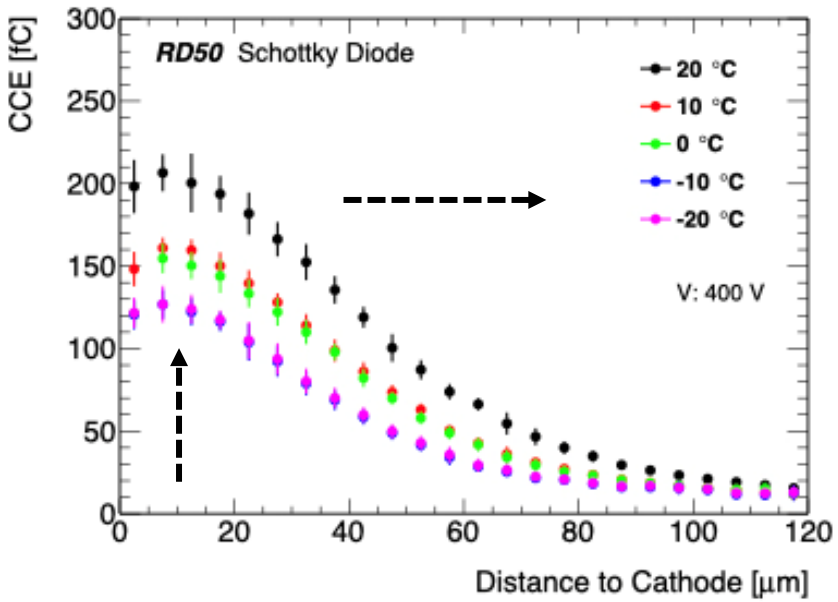


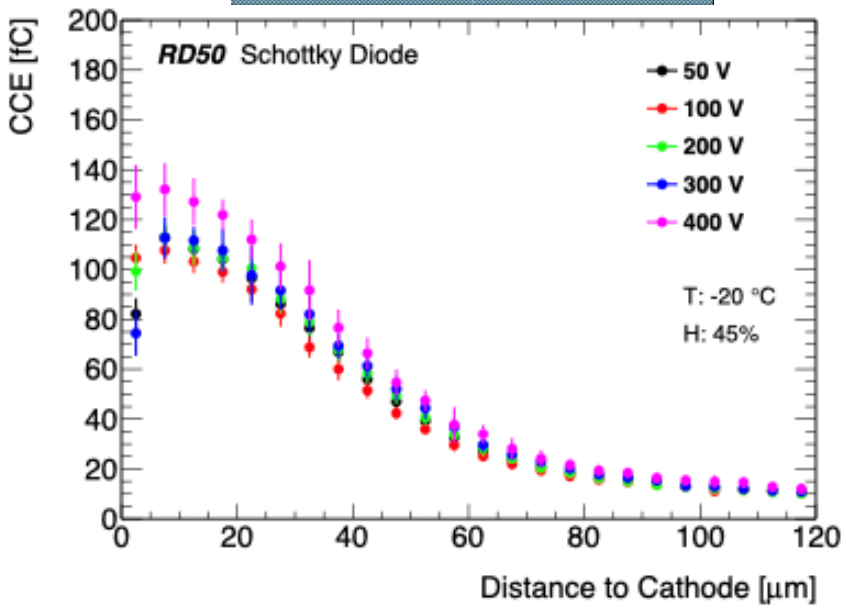


Charge Collection Efficiency: RAL Schottky (unirrad.)

- depleted thickness decreases with increased distance from the cathode edge
- at fixed bias voltage, the higher the temperature, the larger the CCE; still under investigation
- at low temperature, no significant improvement on CCE for various bias voltages

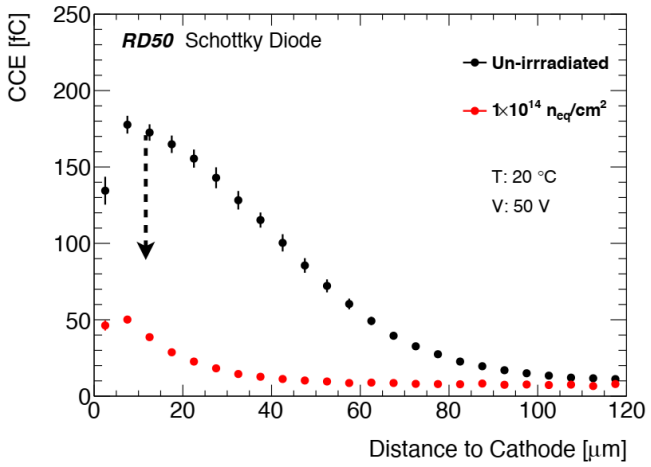


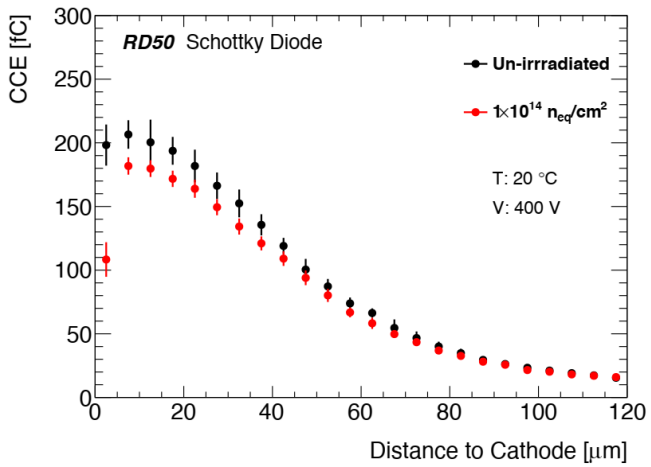




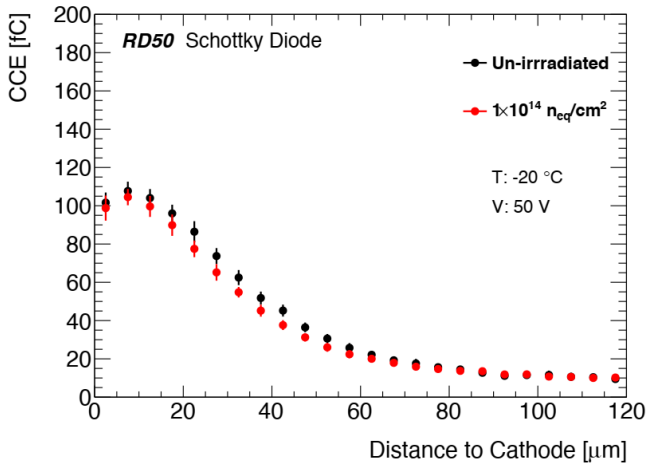
Charge Collection Efficiency: irrad. RAL Schottky

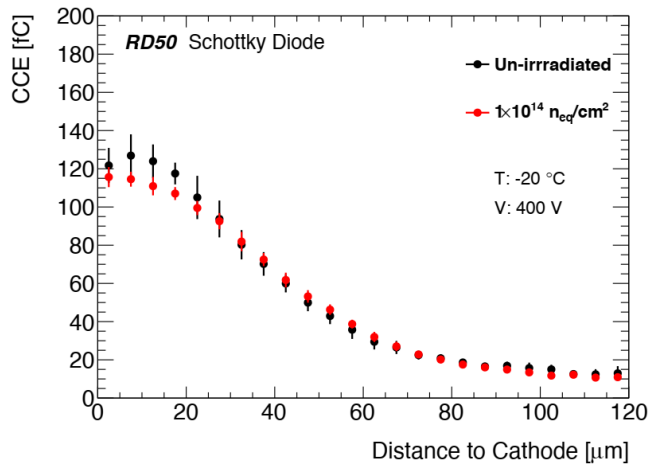
- CCEs of Schottky diodes before/after neutron irradiation ($1x10^{14}$ n_{eq}/cm^2)
- charge trapping effects reduced at higher bias voltage or low temperature





+20°C





-20°C

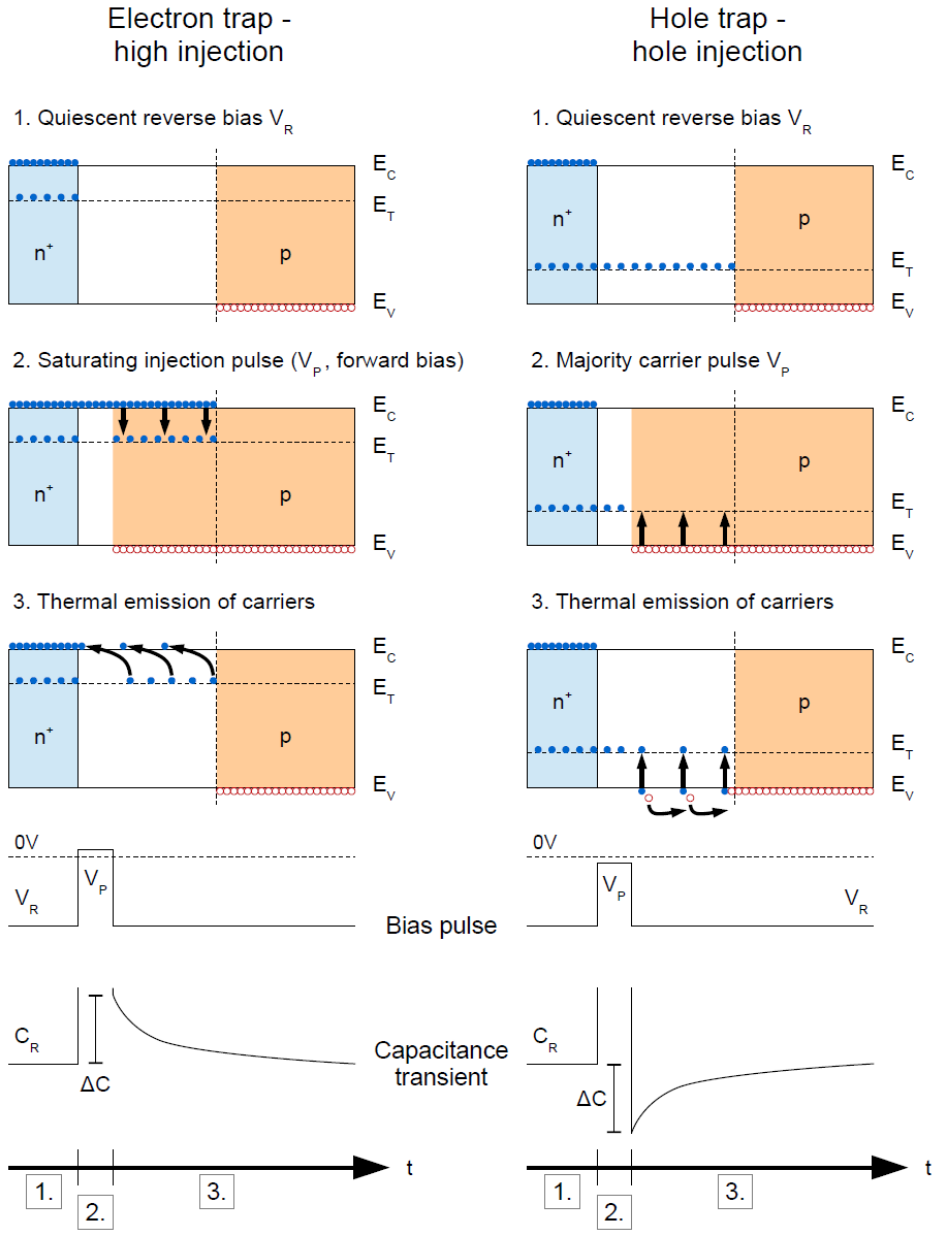
50V

400V

DLTS: basics

1. DUT is under constant reverse bias
2. filling pulse with specific voltage V_P and duration is applied
   - pulse settings need to be adjusted to trap states of interest
   - V_P as reduced reverse bias → majority carrier traps (holes)
   - V_P slight forward bias → minority carrier traps (electrons), if capture rate much larger than competing majority traps
3. bias back to prior level, measure capacitance transients

- usually average O(100) transients per temperature point to reduce noise
- plot $\Delta C = C(t_2) - C(t_1)$ vs. temperature for fixed times
- analyse peaks/valleys in spectrum by varying Rate Window $[t_1; t_2]$

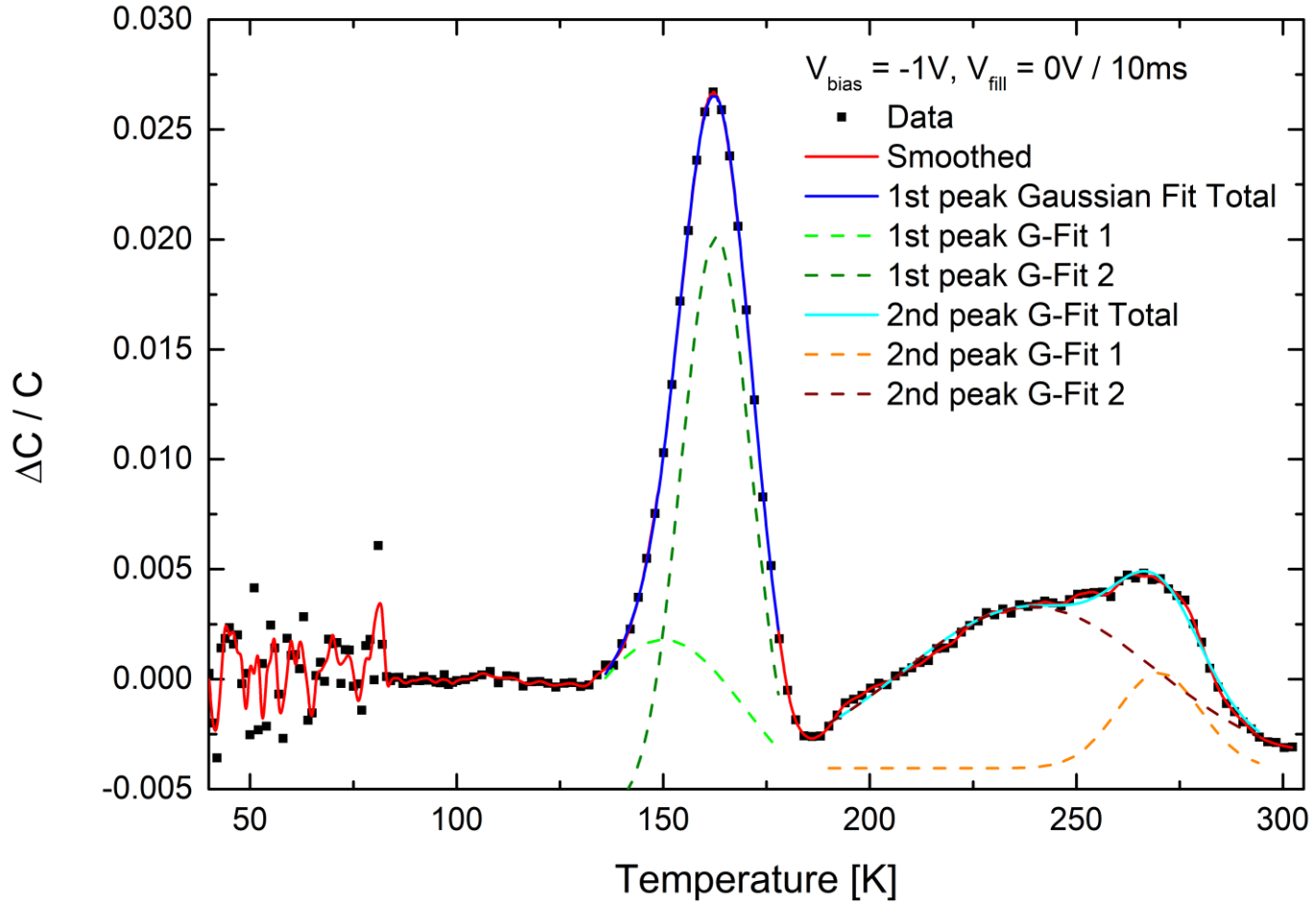


DLTS: Rate Window plot – pn diode (unirrad.)

- multiple DLTS measurements performed for diode samples
  - different bias voltage + filling pulse settings used

Example: pn-diode with p-stop

- 2 peaks (≙ hole traps) with one clearly a convolution of 2 trap states
  - analysis of narrow peak at ~165K also shows 2 trap states
  - example of RW analysis shown
- more results in backup slides



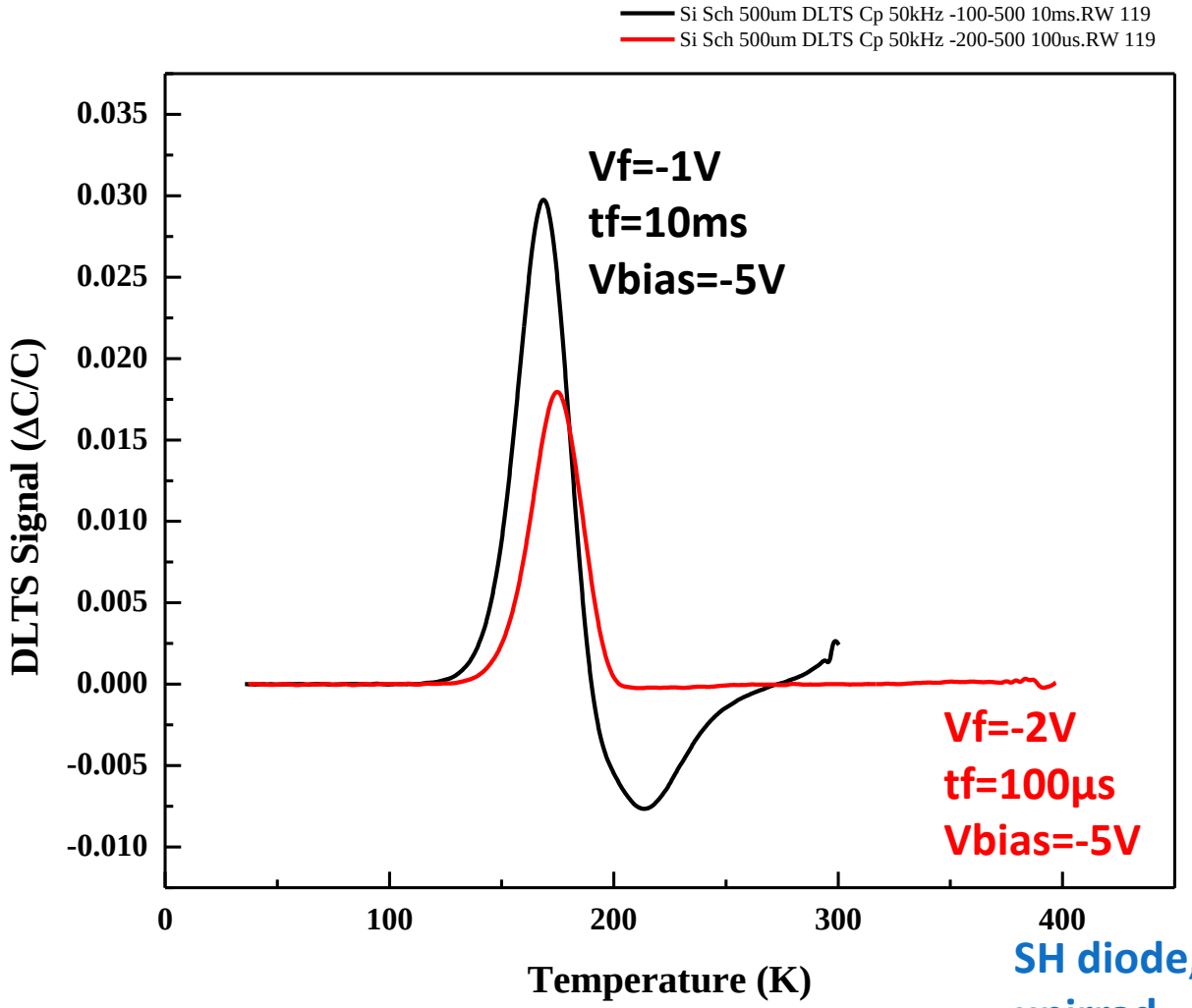
pn diode, with p-stop

DLTS: RAL Schottky diode (unirrad.)

DLTS spectrum:

- 1 peak with 2 majority carrier traps
- ‘minority’ carrier trap
  ⇒ vanishes for reduced + shorter filling pulse
  ⇒ surface/interface states likely
- large majority carrier trap for larger filling pulses at room temperature

T_{median} [K]	E_{trap} [eV]	σ [cm²]
170	0.312	5.5E-15
180	0.294	3.3E-16

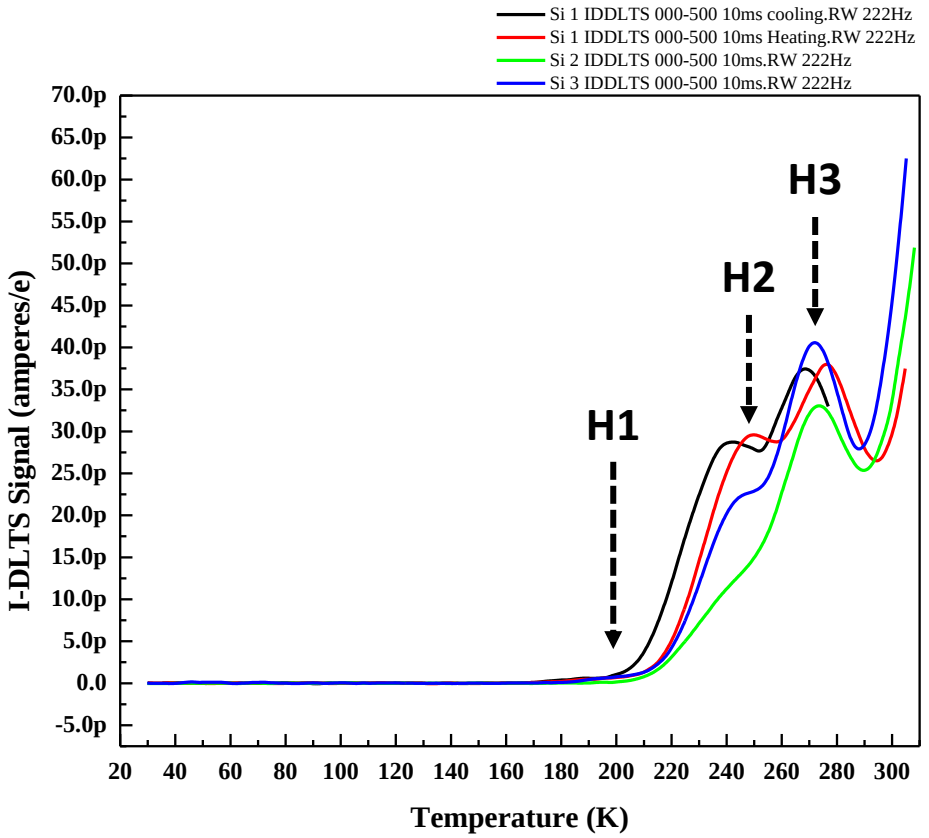


SH diode, unirrad.

I-DLTS: irrad. RAL Schottky

- regular DLTS difficult due to high leakage current
- similar to capacitance DLTS, but no AC test signal, measures current transients
  - double-pulse variant for increased sensitivity
- filling pulse 0V/10ms at -5V
- trap signals at 200K, 240K, 270K, and possibly >300K
  - signal at > 300K may be due to increasing current

	T_{median} [K]	E_{trap} [eV]	σ [cm²]
H1	200		
H2	250	0.46 ± 0.009	2.4E-15 ± 1.5X
H3	275	0.58 ± 0.014	4.5E-14 ± 1.8X

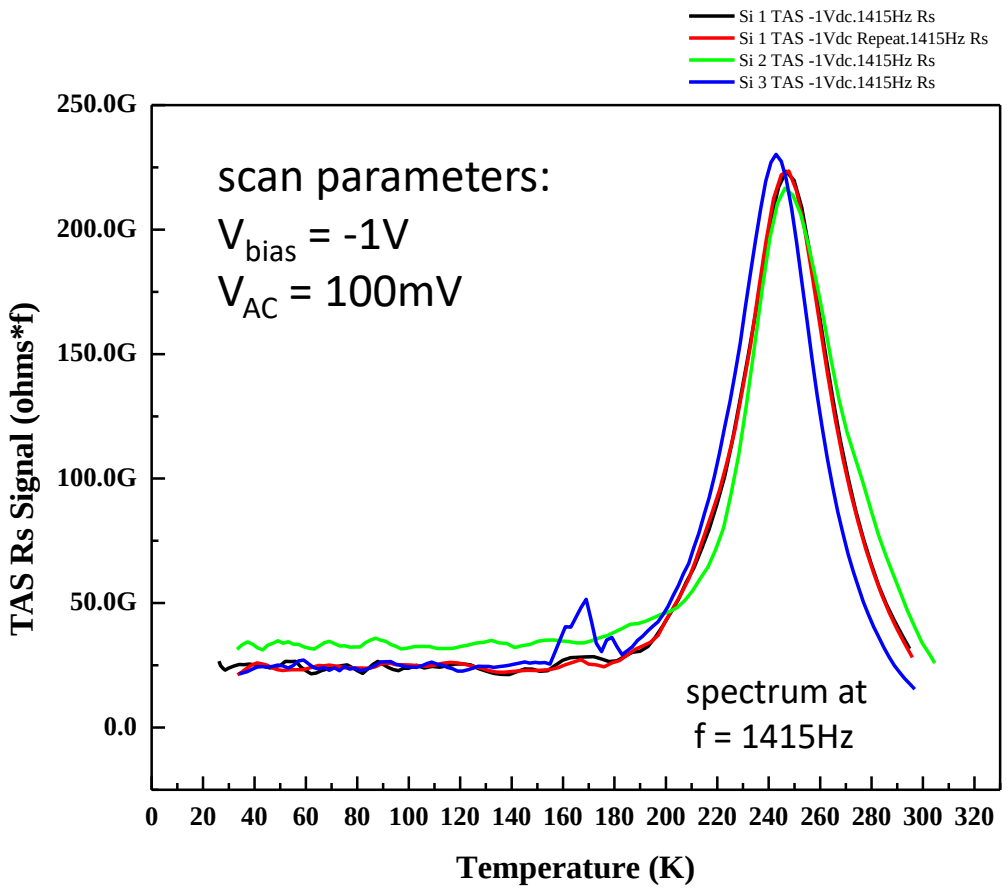


SH diode, 1x10^{15} irrad.

Thermal Admittance Spectroscopy (TAS): irrad. RAL Schottky

- measure capacitance, resistance, and conductance as function of frequency and temperature
  - steps/peaks in temperature dependence indicate thresholds for new traps contributing
- applicable for low-doped or high-resistivity materials
  - complements DLTS
  - useful for irradiated devices with high fluences
- trap energy is 0.4-0.5 eV above the valence band
  - consistent with I-DLTS results

sample	E_{trap} [eV]	σ [cm^2]
Si 1	0.433 ± 0.006	$3.6x10^{-14}$ ± 1.3X
Si 1 (repeat)	0.422 ± 0.008	$2.2x10^{-14}$ ± 1.5X
Si 2	0.486 ± 0.008	$4.0x10^{-13}$ ± 1.5X
Si 3	0.445 ± 0.009	$9.3x10^{-14}$ ± 1.5X



SH diode, $1x10^{15}$ irrad.

Summary & outlook

- fabrication efforts at RAL and CUMFF has ramped up
  - new mask design at CUMFF proves adaptability of fabrication process to findings
- RAL Schottky diodes underwent neutron irradiation at Ljubljana
  - post-irradiation results from DLTS and CCE measurements

Outlook:

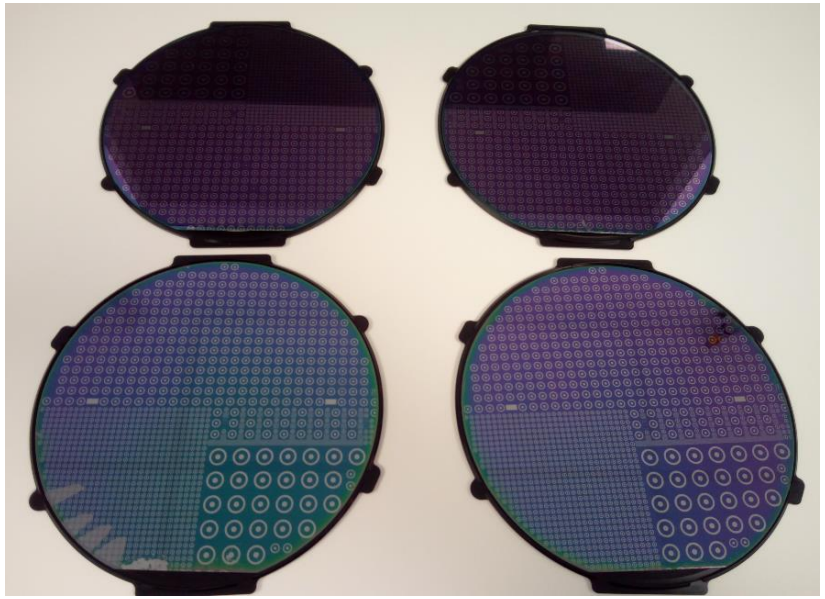
- TCAD simulations of Schottky diodes ongoing
  - need to improve breakdown voltage simulation
- ongoing charge collection measurements at RAL and DLTS + TAS at Carleton
  - comparison of pre/post-irradiation, input for TCAD simulation
- CUMFF pn-junction diodes sent out for irradiation

Backup

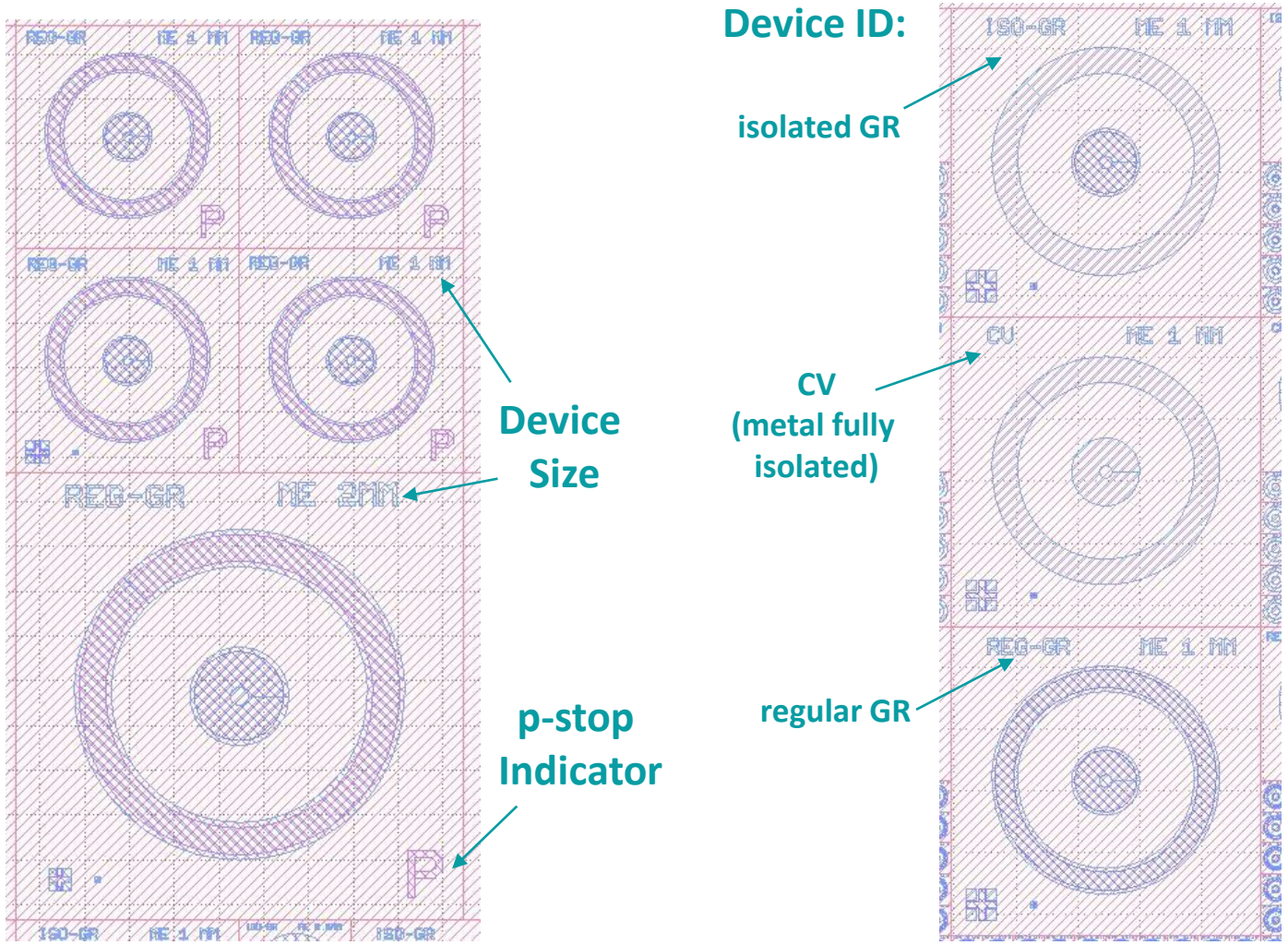
Fabrication details

CUMFF

- new masks made, including isolated MOS gate GR variation for all device types + optional p-stop



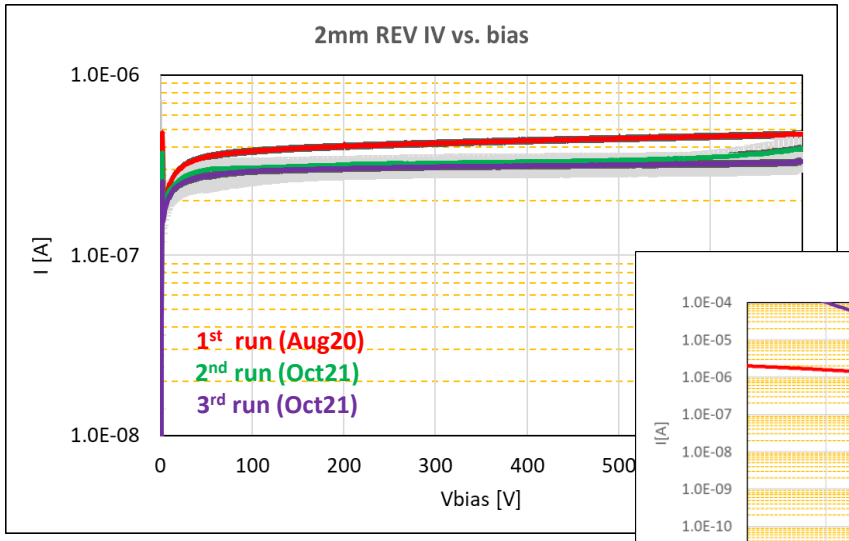
full 6” Schottky wafers @RAL



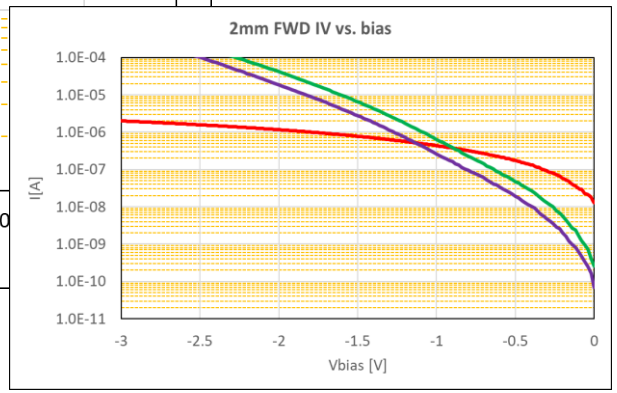
new masks with different structure flavours @CUMFF

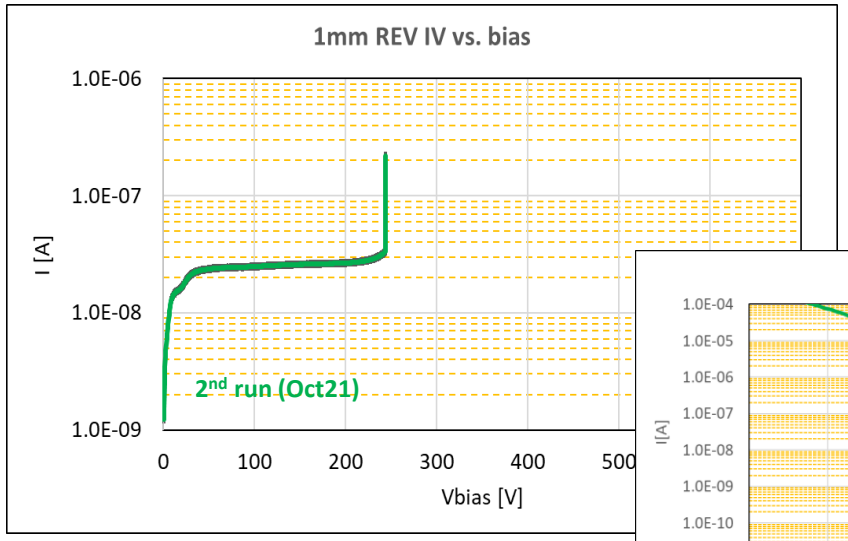
T = 21°C

IV measurements: RAL Schottky (1e13 vs. 1e15)

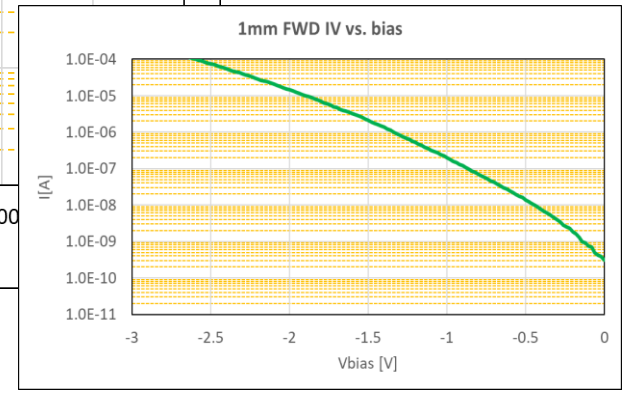


1e13 wafer





1e15 wafer

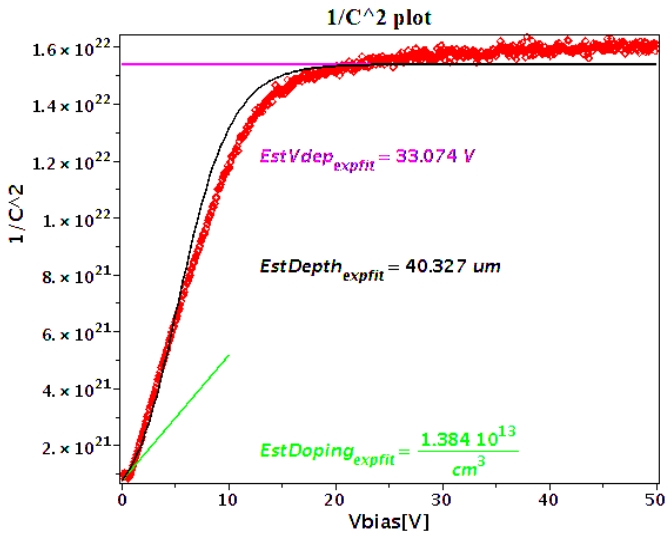


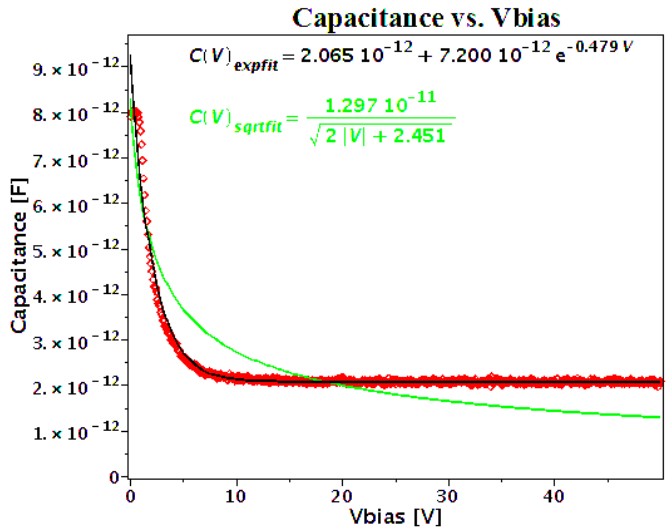
- reverse bias IV similar in all runs, slightly lower leakage in the two latest runs
  - breakdown voltage > 700V
- forward bias shows very different characteristics

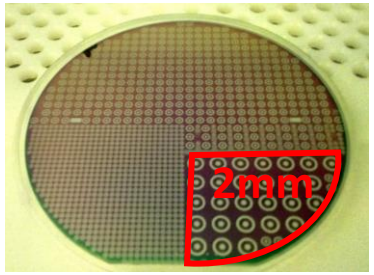
- expected lower leakage in reverse bias, with lower BV
- measured BV is high for this doping
- forward bias ~linear

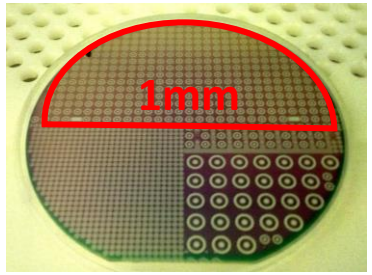
CV measurements: RAL 1e13 Schottky

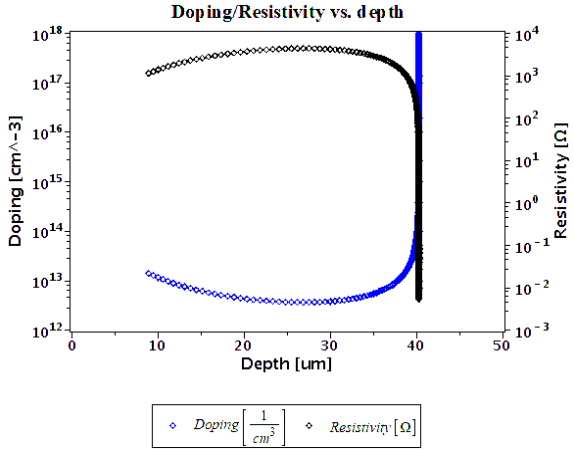
T = 21°C
f = 100kHz
V_{AC} = 30mV









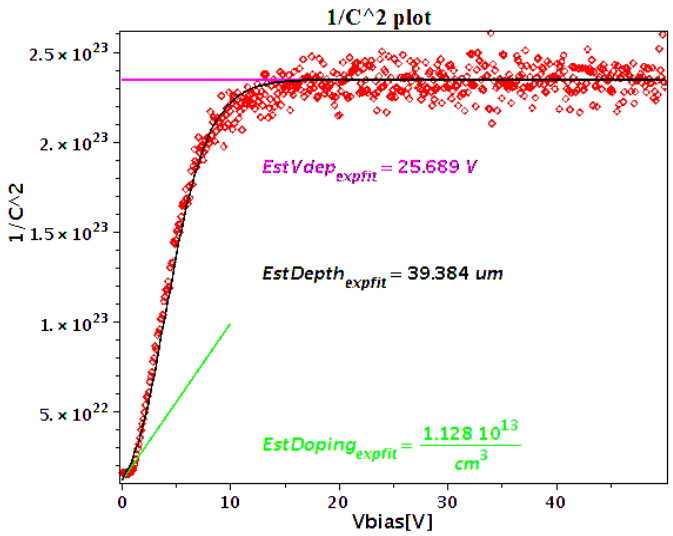


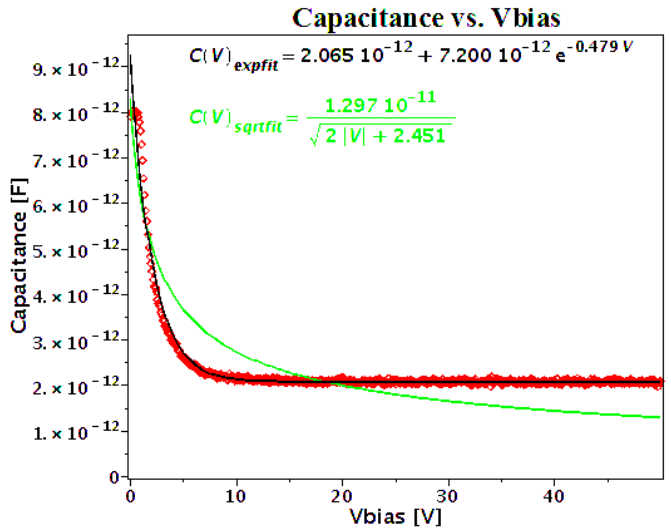
V_d	1.716
φ_b	2.134

V_d	1.343
φ_b	1.739

Φ(Al) = 4.1 [eV]
χ(Si) = 4.05 [eV]

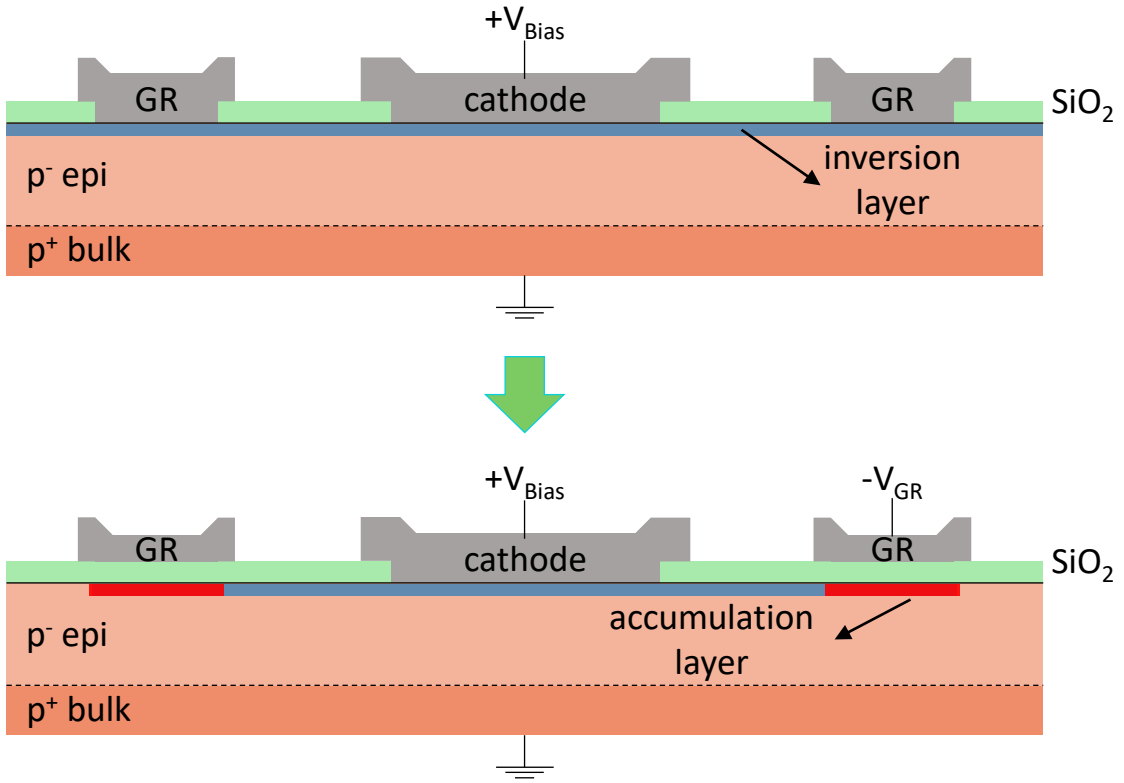
φ_b = 1.16 - (4.1 - 4.05)
= 1.11 (ideal case)
φ_b from CV too high – needs further investigation (TCAD)





Reducing leakage current: MOS gate guard ring structure

- some Schottky diodes on 1e13 cm^{-3} wafer had high leakage currents
- tests showed that cause was formation of electron inversion layer
- expected typical behaviour after radiation damage in oxide
  - outlook to actual behaviour after irradiation
- mitigate by modifying the masks to isolate GR on oxide
- apply low negative V to gated GR
  - accumulation layer formation in interface
  - limit inversion layer



solve this issue **now**

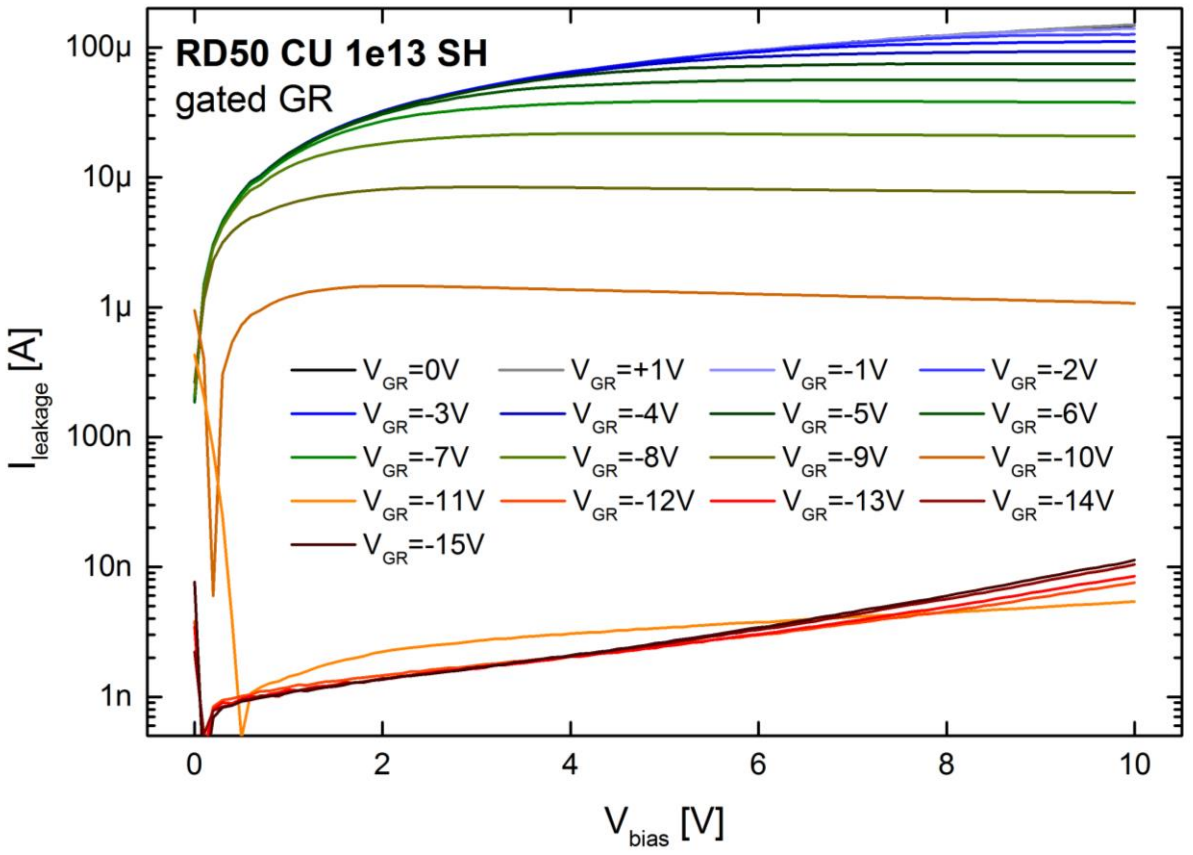
⇒ improve performance of irradiated devices **later**

Reducing leakage current with ISO-GR structure

- isolated GR works as gated MOS structure
  - reduces surface current by limiting inversion layer
- high leakage fully mitigated for V_{GR} <-10V
  - depending on oxide thickness
- devices even showed ‘memory effect’
  - stable-ish charge traps in interface
  - improvements during repeated scans

➢ p-stop for provides more consistent performance
  ➢ better definition of active volume

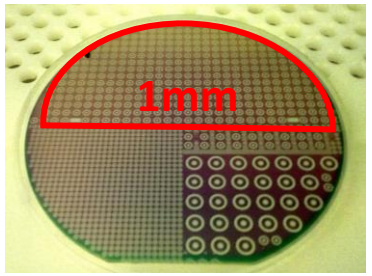
➢ looking forward to effects on irradiated devices

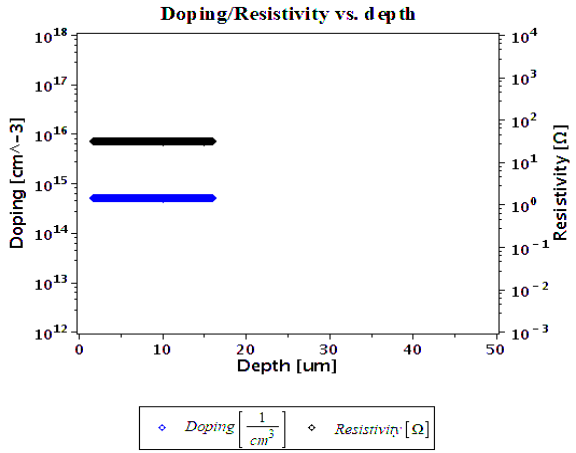


CV measurements: RAL 1e15 Schottky

T = 21°C
f = 100kHz
V_{AC} = 30mV

- 2 HR wafers show doping as expected
  - CV plot not really well described by 1/√V fit
  - barrier height estimate from CV too high
  - estimate from IV in progress
- devices on 1e15 wafer so far show very good 1/√V Cap dependence
  - doping as expected
  - barrier height clearly too high





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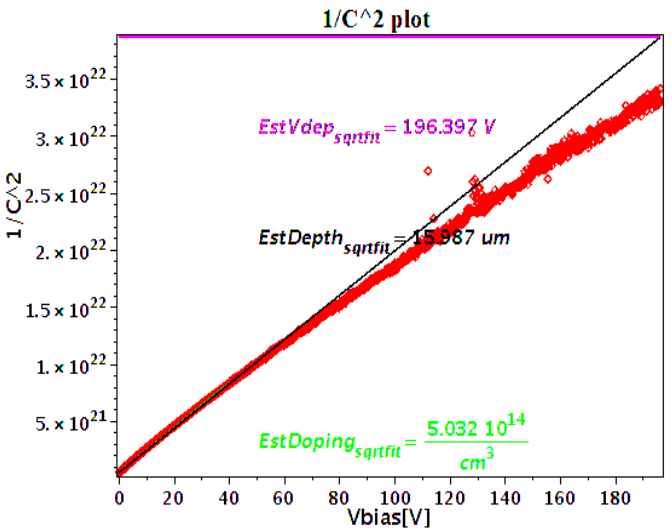
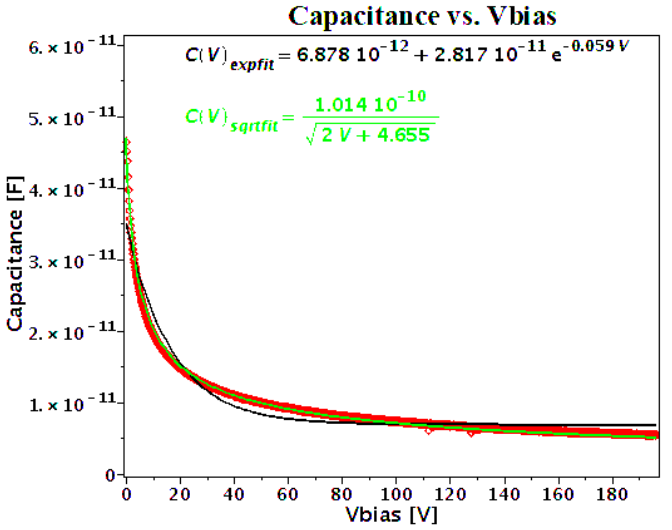
= 1.11 (ideal case)
φ_b from CV too high – needs further investigation (TCAD)

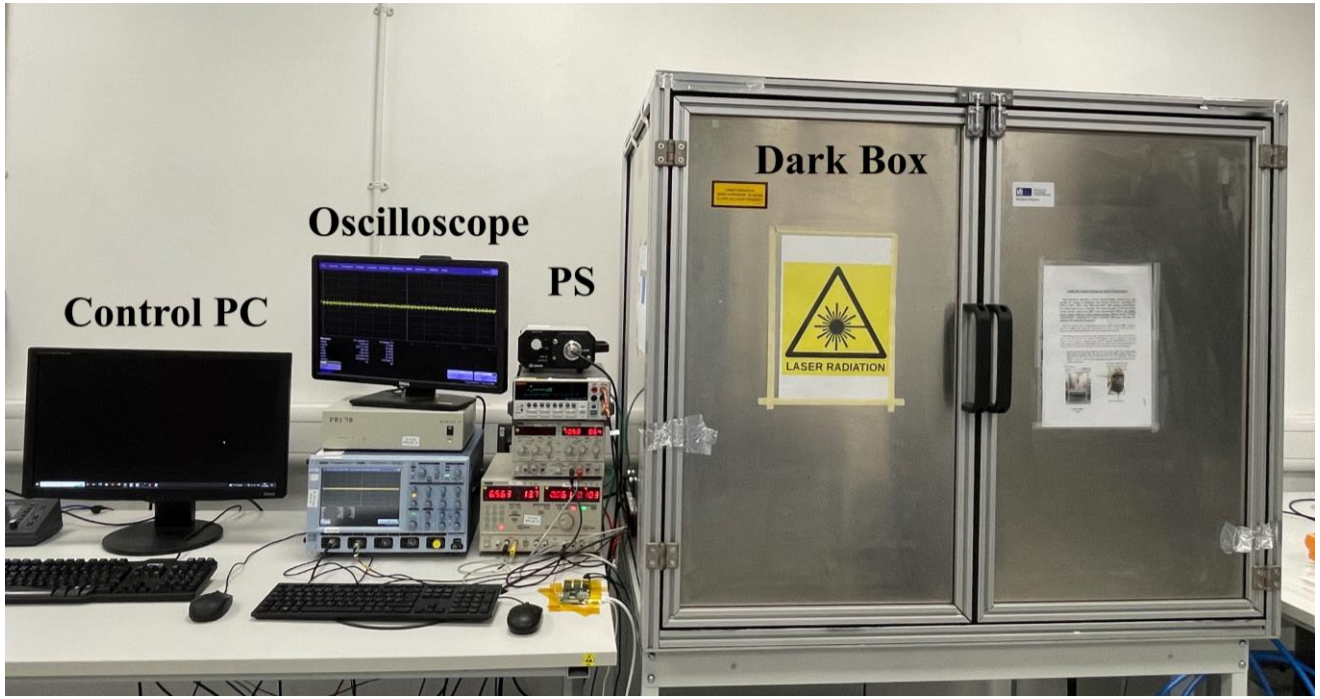


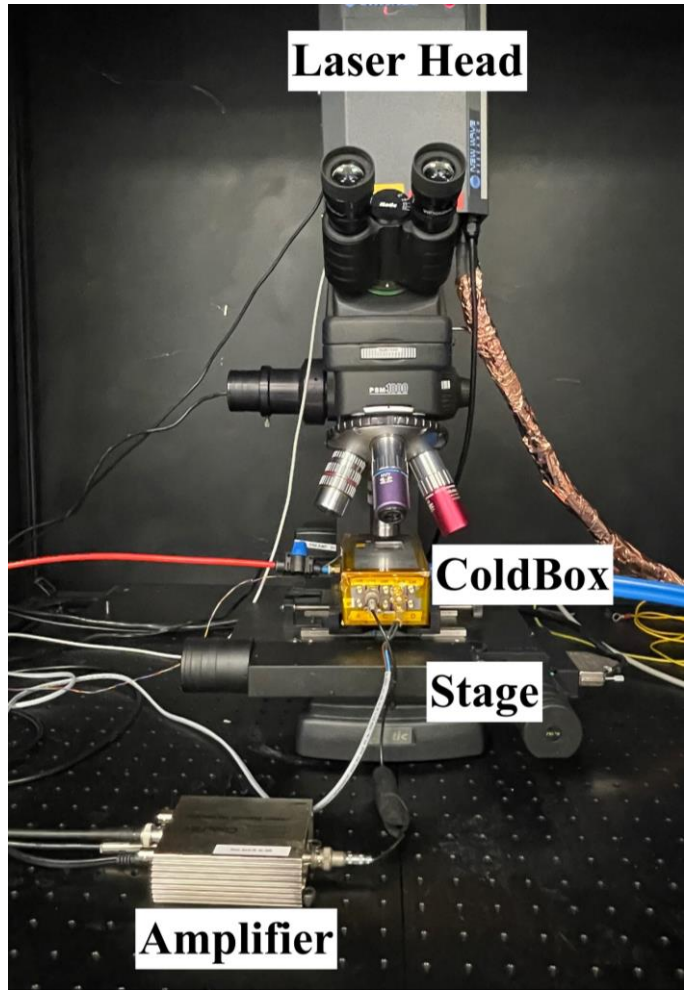


V_d	2.328
φ_b	2.646

Charge Collection Efficiency: Setup

- Laser: IR(1064 nm), 5µm x 50µm, 23.44 ± 0.2 pJ
- Stage: move step of 5µm
- Temperature: -20℃ … +20 ℃





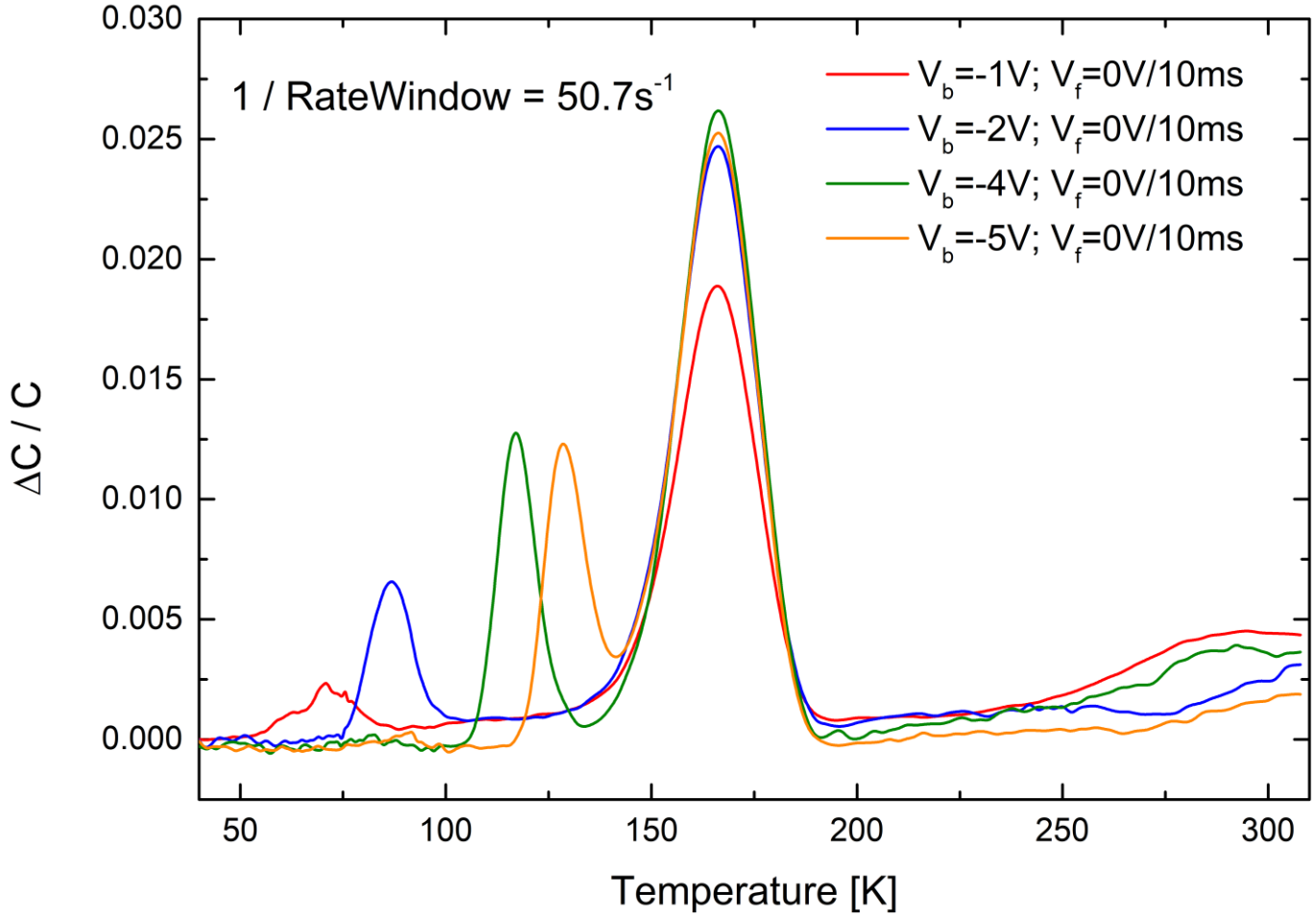
DLTS: Rate Window plots

- multiple DLTS measurements performed for diode sample with/without p-stop
  - different bias voltage + filling pulse settings used

<u>pn-diode:</u>

- Rate Window plots with same Rate Window parameters shown for different scans
- 2 peaks (≙ hole traps) at low T and onset of another peak at room temperature
  - low-T peak shifts for different bias voltage

⇒ **surface/interface traps**

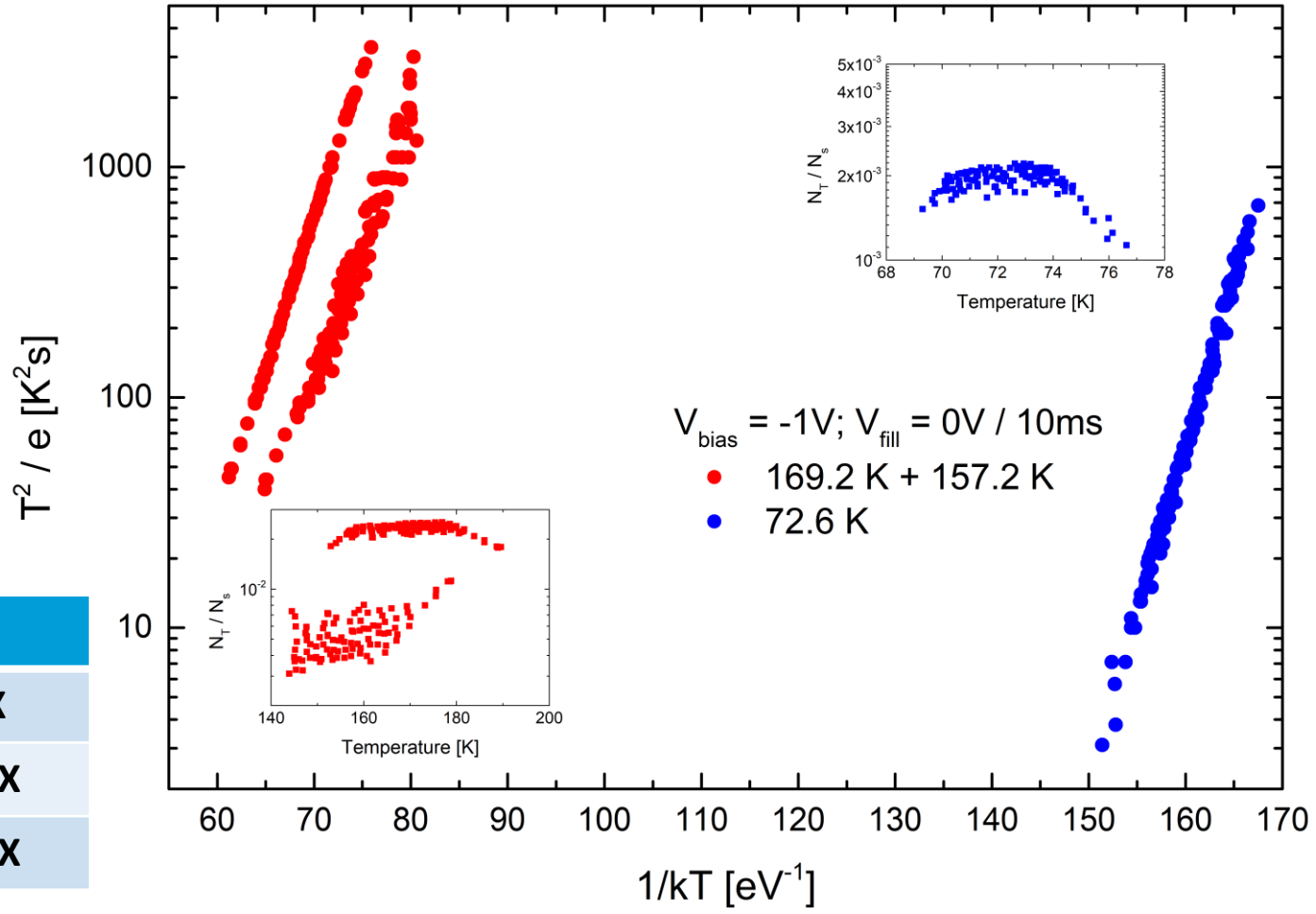


pn diode, no p-stop

DLTS: Arrhenius plots

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels

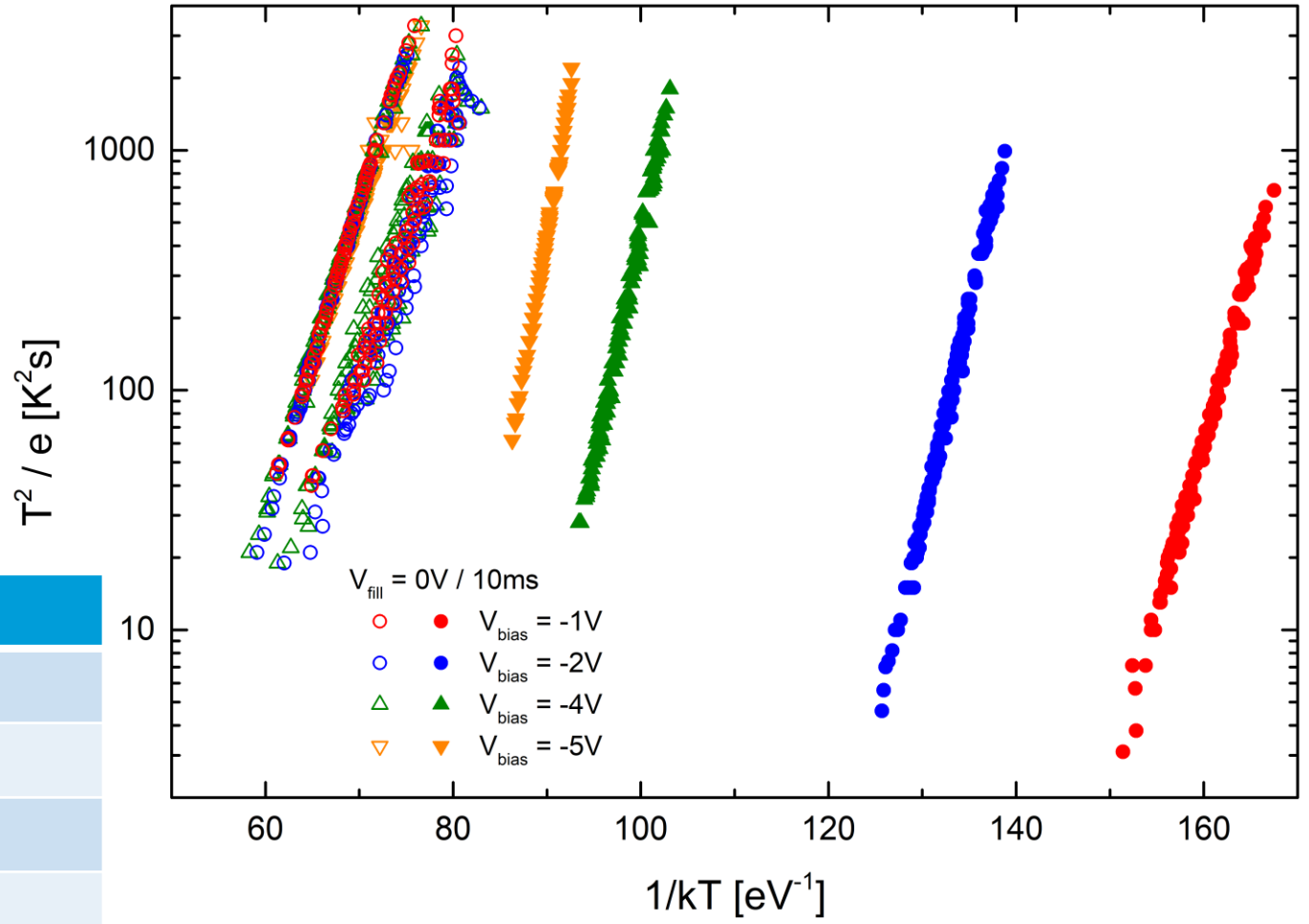
T_{median} [K]	E_{trap} [eV]	σ [cm²]
72.6	0.330 ± 0.007	$4.1x10^{-1}$ ± 3.1X
157.2	0.260 ± 0.011	$1.9x10^{-16}$ ± 2.3X
169.2	0.298 ± 0.002	$5.8x10^{-16}$ ± 1.1X



pn diode, no p-stop

DLTS: Arrhenius plots

- good agreement of common 165K peak
  ⇒ peak contains 2 traps each
- surface/interface states make up low-T peak



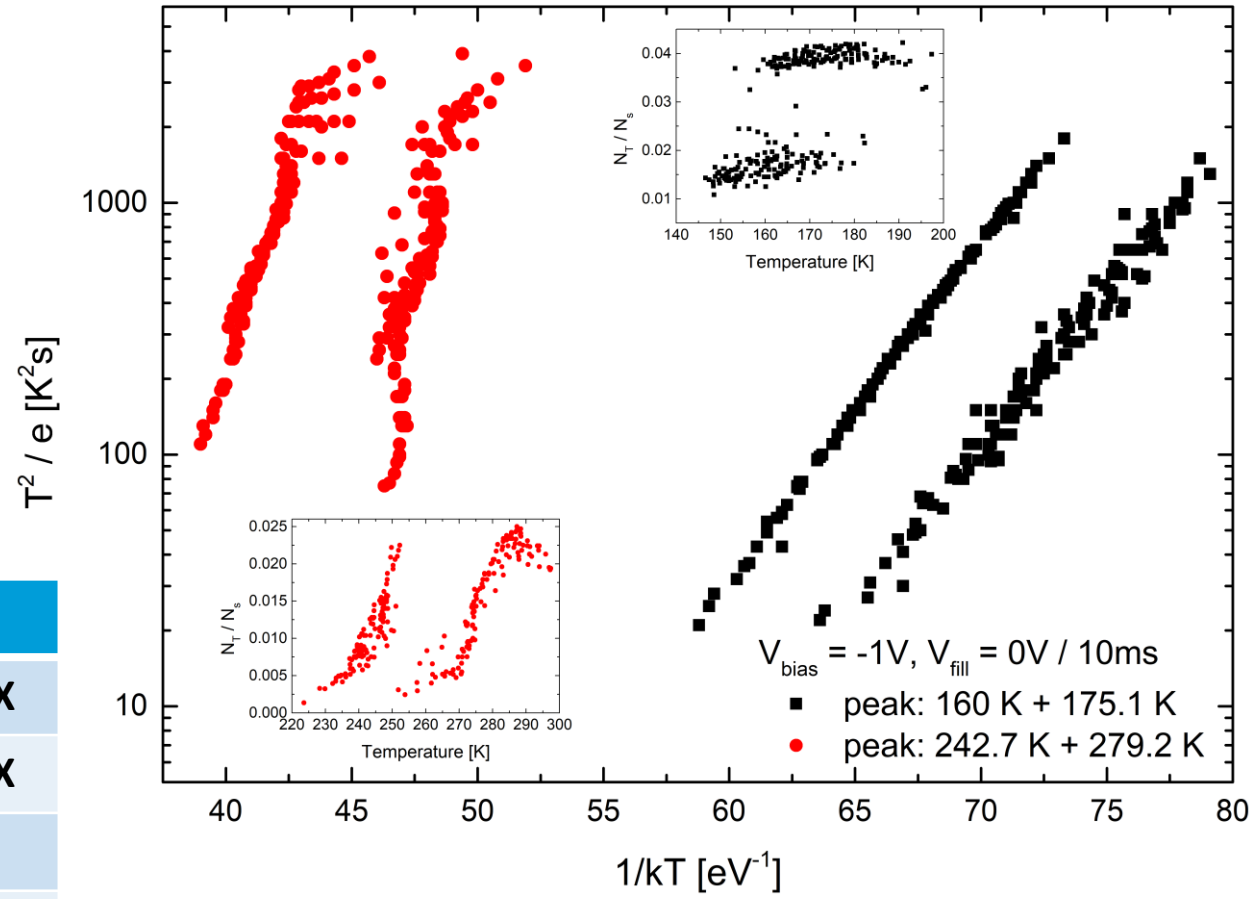
T_{median} [K]	E_{trap} [eV]	σ [cm^2]
72.6 (-1V)	0.330 ± 0.007	$4.1x10^{-1}$ ± 3.1X
87.4 (-2V)	0.407 ± 0.005	$9.4x10^{-1}$ ± 2.0X
118.6 (-4V)	0.442 ± 0.005	$9.9x10^{-6}$ ± 1.6X
129.2 (-5V)	0.545 ± 0.007	$1x10^{-3}$ ± 1.9X

pn diode, no p-stop

DLTS: Arrhenius plots – pn diode (unirrad.)

- plateau in trap concentration indicates that trap state was saturated with filling pulse
  - positive slope indicates insufficient saturation, negative slope competing trap levels
- filling pulse for peaks at higher T not optimal, fitting results not very precise

T_{median} [K]	E_{trap} [eV]	σ [cm²]
160.0	**0.268 ± 0.014**	**3.0×10^{-16} ± 2.7X**
175.1	**0.309 ± 0.005**	**1.0×10^{-15} ± 1.4X**
242.7		
276.2	**0.59 ± 0.04**	**2.4×10^{-14} ± 5.4X**

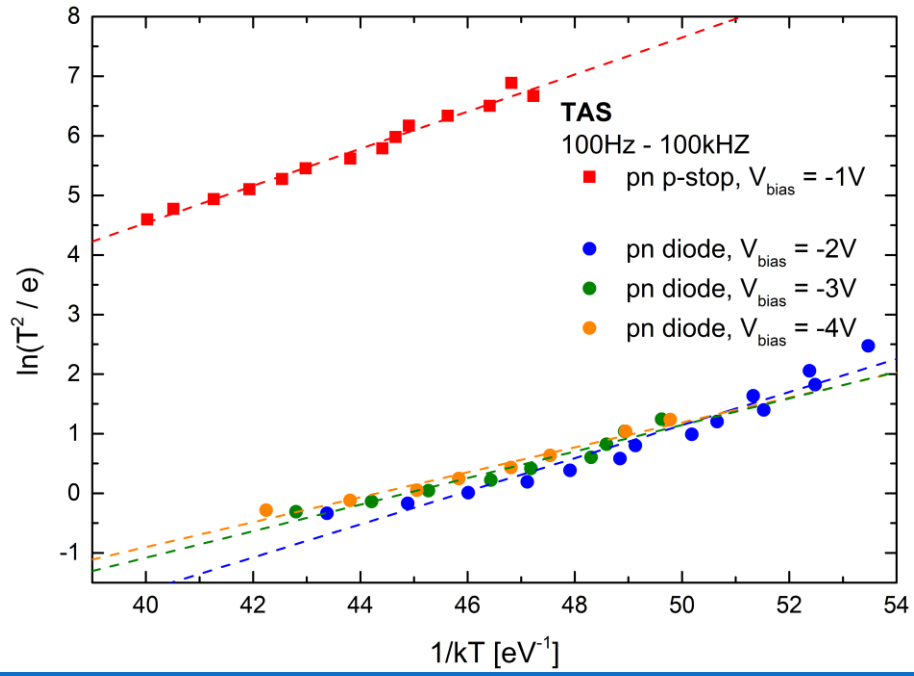


pn diode, with p-stop

Thermal Admittance Spectroscopy (TAS)

- steady-state measurement
- measure capacitance C, resistance R, and conductance G as function of frequency and temperature
- defect contribution to C/R/G depending on test signal frequency and temperature
- steps/peaks in temperature dependence indicate thresholds for new traps contributing
- applicable for low-doped or high-resistivity materials, complements DLTS
- useful for irradiated devices with high fluences
  - standard DLTS might fail due to leakage current

scan	E_{trap} [eV]	σ [cm²]
-1V pstop	0.311 ± 0.026	8.4×10^{-19} ± 3.1X
-2V pn	0.277 ± 0.043	1.0×10^{-16} ± 8.3X
-3V pn	0.168 ± 0.040	4.9×10^{-19} ± 6.2X
-4V pn	0.209 ± 0.037	3.3×10^{-18} ± 5.5X

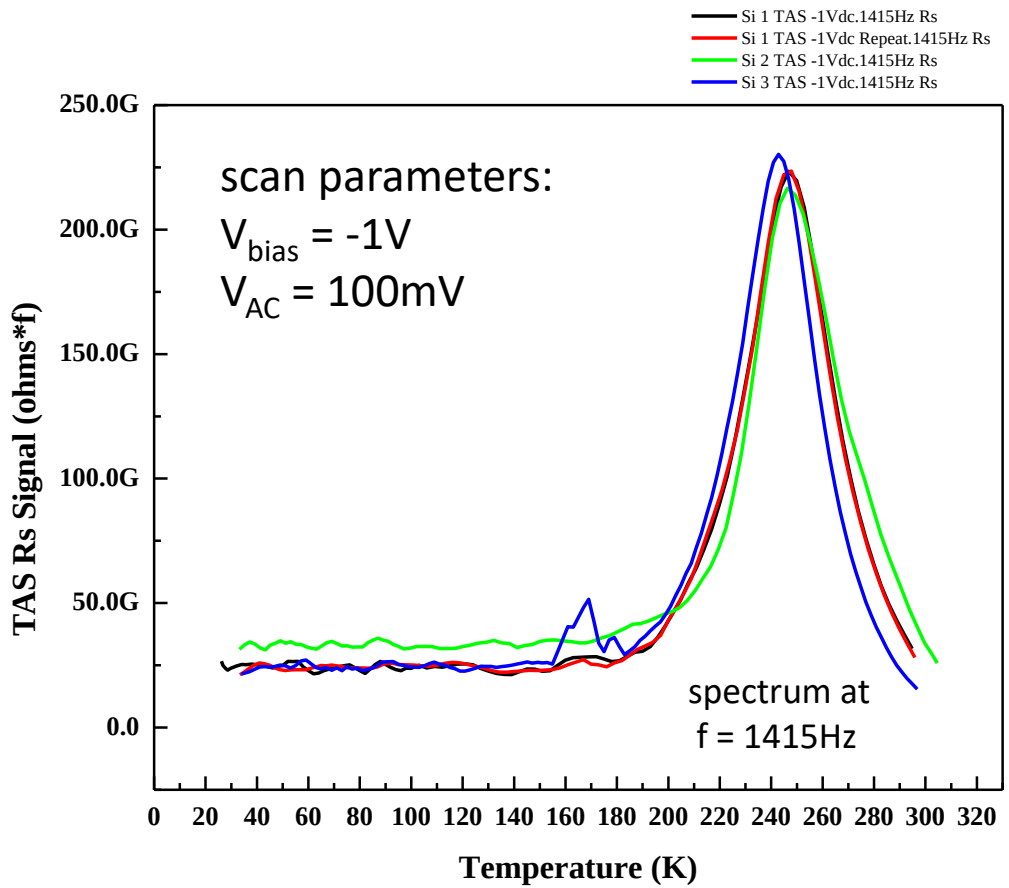


pn diodes, unirradiated

TAS: irrad. RAL Schottky

- good signal from Rs(f,T); not from any of the other properties (Cs, Cp, Gp)
  - measured from 20Hz to 100kHz
  - spectra for multiple device samples shown
  - noise at 160 K for device sample #3
- trap energy is 0.4-0.5 eV above the valence band with the scattering of ~ 60 meV
  - consistent with I-DLTS results

sample	E_{trap} [eV]	σ [cm^2]
Si 1	0.433 ± 0.006	$3.6x10^{-14}$ ± 1.3X
Si 1 (repeat)	0.422 ± 0.008	$2.2x10^{-14}$ ± 1.5X
Si 2	0.486 ± 0.008	$4.0x10^{-13}$ ± 1.5X
Si 3	0.445 ± 0.009	$9.3x10^{-14}$ ± 1.5X



SH diode, $1x10^{15}$ irrad.