Measuring Single Event Upset Cross Sections and Other Radiation Effects in Readout Electronics for the ATLAS Inner Tracker Upgrade

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R1-8 Test Facility II (PPD) Session – June 10, 2021

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(Indico page link)

UNIVERSITY OF TORONTO

ATLAS EXPERIMENT

NSERC CRSNG

Introduction

- For the High-Luminosity Upgrade of the LHC (HL-LHC) [1], ATLAS is upgrading its silicon tracking detector as part of the Inner Tracker (ITk) Upgrade [2, 3]
  - Tracker will have improved granularity to handle increased hit occupancy
  - Tracker will be radiation hard to operate in the harsh HL-LHC conditions
    - O(10) Mrad dose over the lifetime of the ITk
- This talk will describe the performance of the ITk's readout ASICs in testbeams performed at TRIUMF's Proton Irradiation Facility (PIF)
  - Performed in August and December 2020, each with 480 MeV protons – approximately 48 hours worth of runtime data

ABCStar ASICs

- ATLAS Binary Chip (ABCs) are the front end readout ASICs for ITk strip modules [4]
  - Takes analog signals and digitizes them (256 channels)
  - ABCStar ASICs are the most recent “major” revision and the version to be used in production
    - Prototype version: **V0** (worked well)
    - Newly available (production) version: **V1**

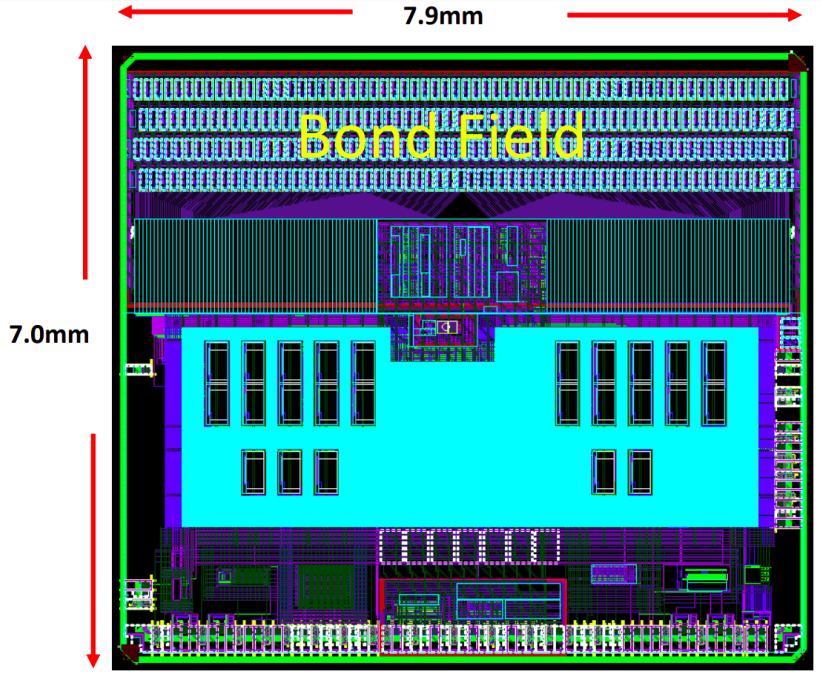


Image taken from Slide 7 of Mitch Newcomer’s presentation at FE Electronics 2018 [5]

Radiation Effects in ASICs

- ASICs are generally radiation hard, but can experience single event effects (SEEs – upsets, latches, ...) or digital current enhancement (increased load on power supplies)
- **Single event upsets (SEUs)**: ASICs store digital values (0/1) – instances of radiation can “flip” bits from 0➔1 or 1➔0
  - Recoverable – however, these bit flips can still break internal machinery (e.g., send chip into low-power mode) or result in wrong outputs (e.g., fake or masked hits)
  - Number of SEUs measured ∝ total dose received
    - We want to quantify the **SEU cross section** in ABCstar ASICs

ABCStar Registers and Triplication

- A key difference between V0 and V1 ABCStar ASICs is the **triplication** of all 32-bit registers
  - Store configuration, counters, etc.
- Triplication replicates the logic for each register 3 times, and the 3 replicates vote for the value of each register [6]
  - **Protects** the register from SEUs in one of the replicates – we want to verify this
  - See pictorial representation in Backup
- Front-end buffer is **not** triplicated for either
  - Stores hit information

Register type	Number of registers
SCReg	1
ADCS	3 (6)
MaskInput	8
CREG	2 (7)
STAT	7 (5)
HPR	1
TrimDAC	40
CalREG	8
HitCountREG	64

Un-bracketed numbers correspond to V1 chips, bracketed numbers correspond to V0 chips – see Backup for descriptions

ASICs Tested @ TRIUMF

Chips tested in August 2020

Chip	Generation	Distance [cm]	Dose [Mrad]	Fluence [p/cm^2]
261	V1	18.8	4.30	1.18×10^{14}
002	V0	31.0	3.34	9.17×10^{13}
259	V1	44.0	2.67	7.33×10^{13}
267	V1	56.3	2.23	6.13×10^{13}

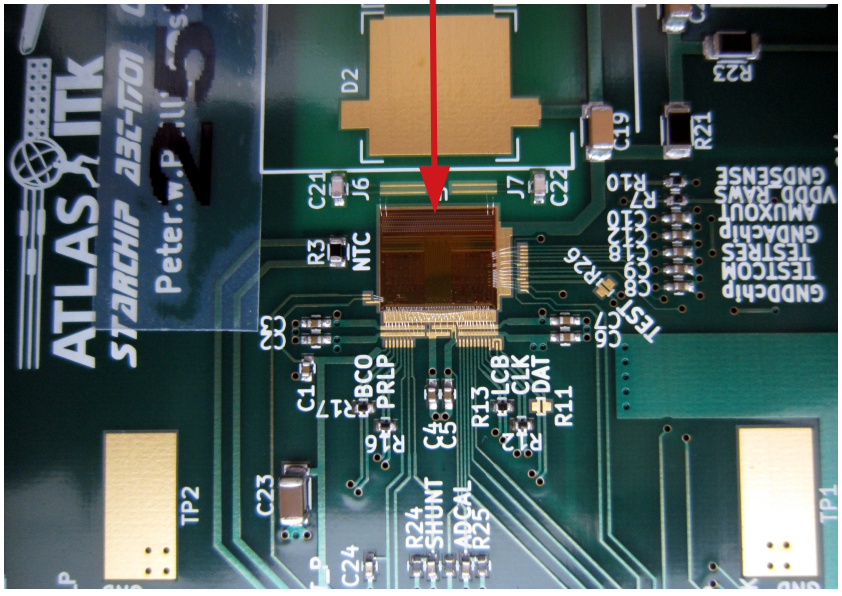
Chips tested in December 2020

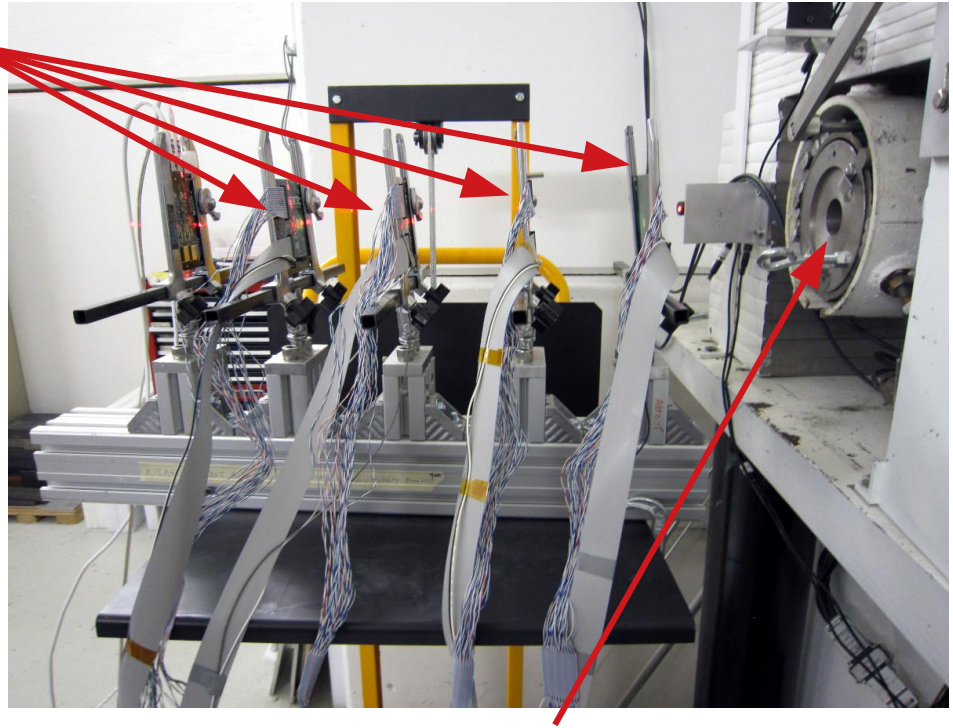
Chip	Generation	Distance [cm]	Dose [Mrad]	Fluence [p/cm^2]
259	V1	43.5	2.48	6.80×10^{13}
273	V1	46.0	2.38	6.55×10^{13}
267	V1	56.0	2.07	5.67×10^{13}
274	V1	58.5	2.00	5.49×10^{13}

- Two testbeams: August (***needed*** to test V0 vs. V1) and December 2020 (***opportunity***: more statistics)
- Measured digital/analog currents pulled by the ASICs
  - Chips 259+267 **common** to both: useful for testing the effect of pre-irradiation on digital currents
- SEU measurement: registers for all chips filled in predictable ways and repeatedly read out
  - By comparing expected payloads to what's measured, we can identify SEUs (examples in Backup)

Testbeam Setup @ TRIUMF PIF

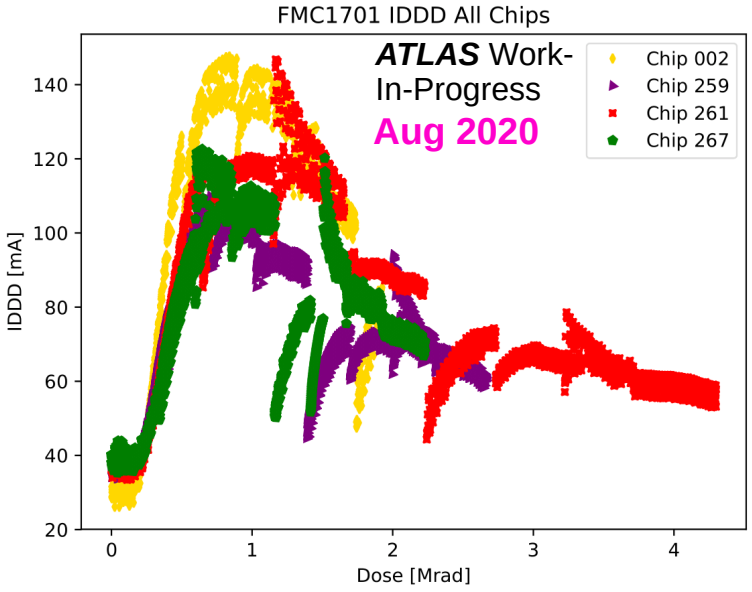
Single chip boards (SCBs) with mounted ASICs

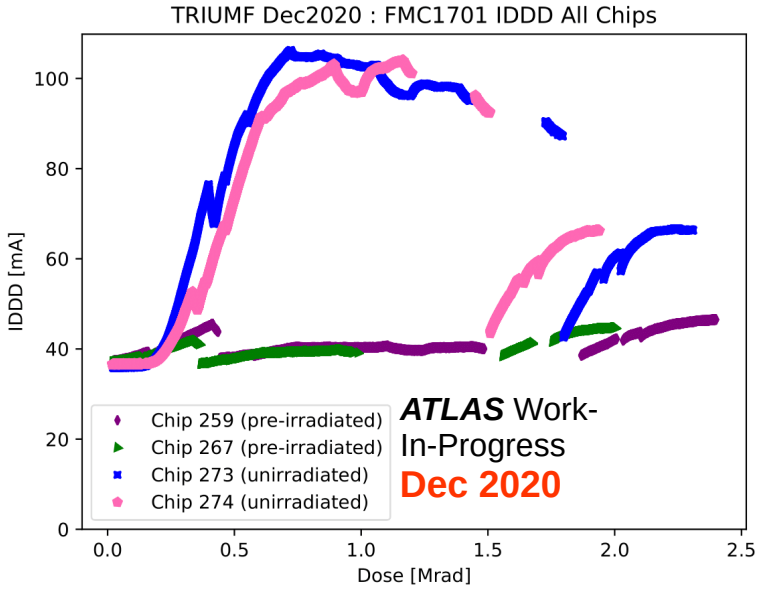




Beamline

Digital Currents with Protons: August vs. December 2020





Consistent with ABC130 results (Sec. 4.10 of [4]): Total Ionizing Dose (TID) bump in digital current near 1 Mrad (**~100% increase** in current – major **problem** for detector cooling)

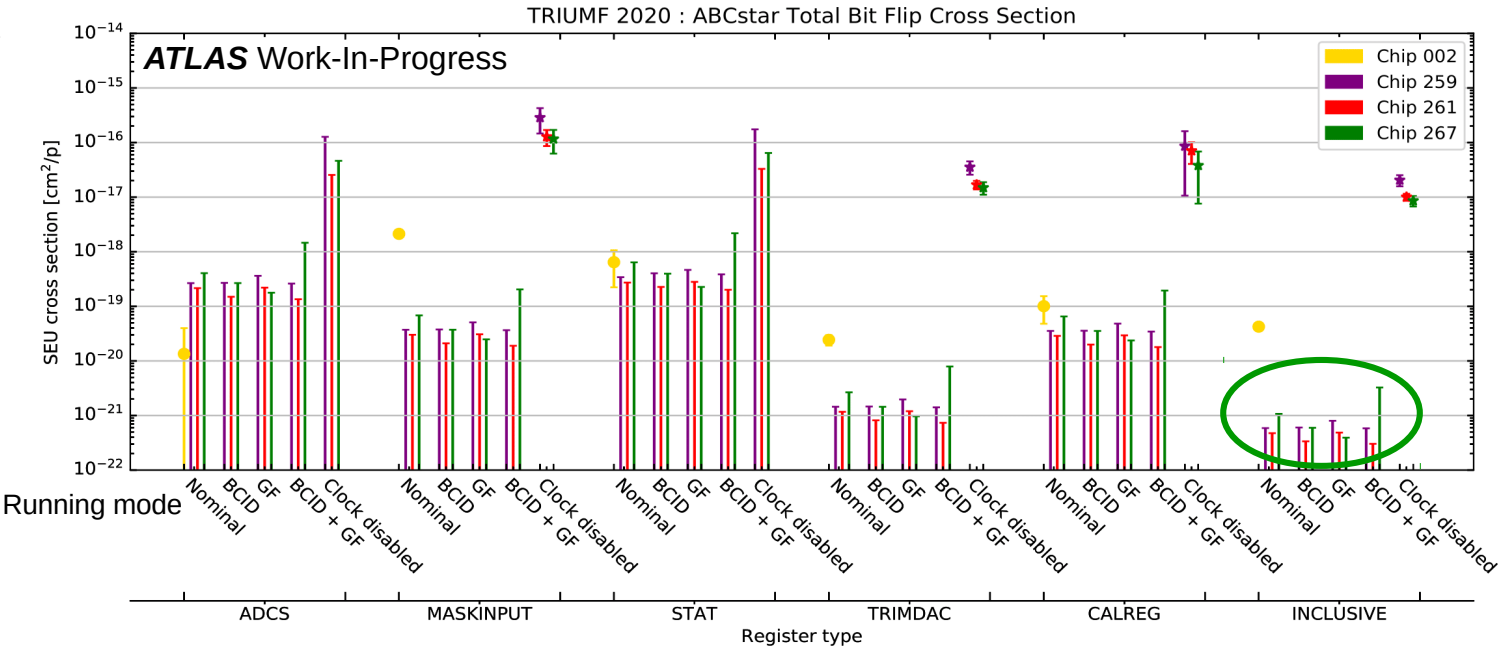
➔ **Mitigated by pre-irradiation** (i.e., Chips 259+267 in right plot)

August 2020 Register Cross Sections

*Bars **without** data points correspond to **upper limits** assuming **1 SEU** (more details on calculation in Backup)*

*Clock disabled running mode **enhances** SEU cross section (effectively switches off triplication)*

Cross section normalized to total fluence (protons/cm^2)



V1 chips saw **0 SEUs** out of ~20M bits, upper limit assuming 1 SEU: **3.90 x 10^{-24} cm^2/p**
V0 chip saw **389 SEUs** out of ~3M bits, cross section: **(4.24 ± 0.07) x 10^{-20} cm^2/p**

Summary

- Presented an overview of the ABCStar testbeams in August and December 2020 at TRIUMF
  - Pre-irradiating ASICs **mitigates** the increase in digital current with TID
  - Triplication of registers works as expected: **no SEUs** measured for V1 chips in triplicated registers
- Analysis of front-end (physics) packets is ongoing (considerable amount of raw FPGA data: ~300 GB)
- Parallel analysis of testbeam data for ABCStars acquired from Louvain, Belgium with heavy ions
  - Examines the response of the ASICs to different energy transfers

References

[1] I. Béjar Alonso *et al.*, *High-Luminosity Large Hadron Collider (HL-LHC): Technical design report*, tech. rep. CERN-2020-010, CERN, Geneva (2020).

[2] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Pixel Detector,* tech. rep. CERN-LHCC-2017-021, ATLAS-TDR-030, CERN, Geneva (2017).

[3] ATLAS Collaboration, *Technical Design Report for the ATLAS Inner Tracker Strip Detector*, tech. rep. CERN-LHCC-2017-005, ATLAS-TDR-025, CERN, Geneva (2017).

[4] L. Poley, C. Sawyer, *et al.*, *The ABC130 barrel module prototyping programme for the ATLAS strip tracker*, J. Instrum. **15** (2020) P09004.

[5] M. Newcomer, *Front-end chips for ATLAS ITK upgrade*, Front End Electronics 2018, Orford, Québec, Canada (2018).

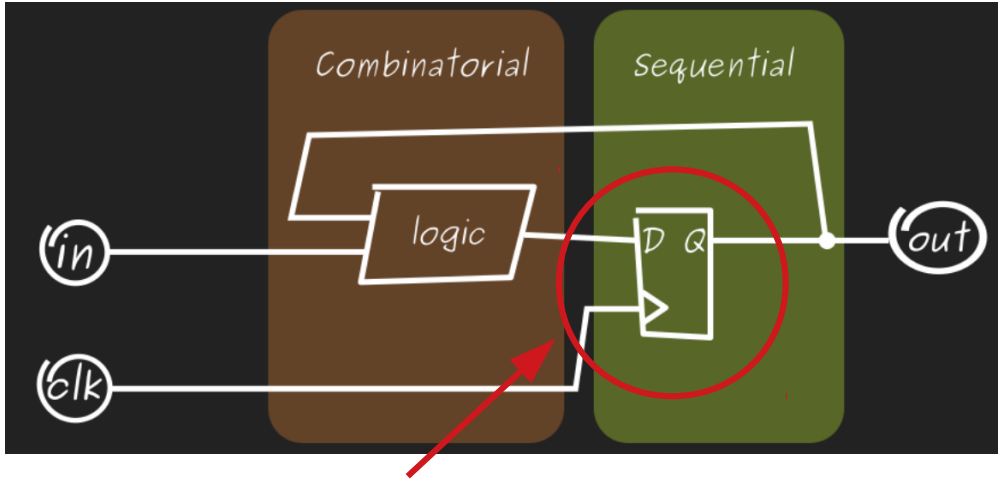
[6] S. Kulis, *Single Event Effects mitigation with TMRG tool*, J. Instrum. **12** (2017) C01082.

Questions?

Backup

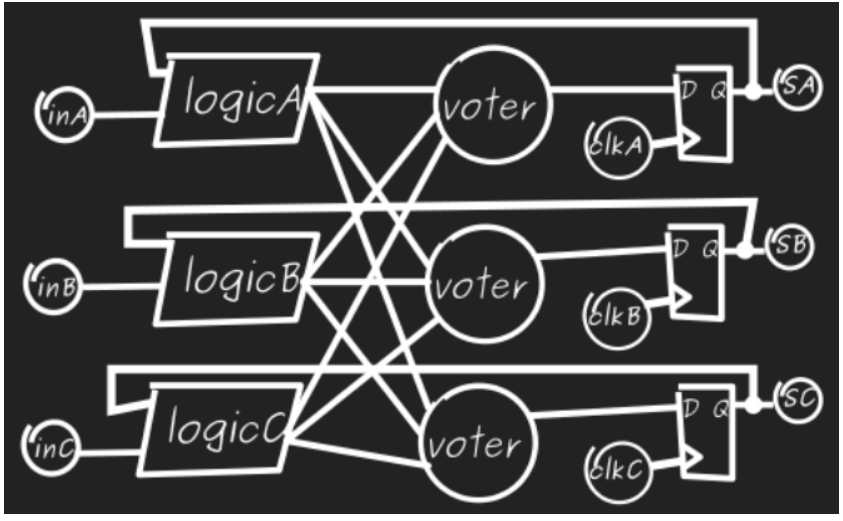
Register Triplication: Pictorially

Untriplicated register



Flip-flop reads D on rising clock edge, outputs at Q on falling clock edge

Triplicated register



Voter takes majority (e.g., [1, 0, 1] ➔ 1)

Images obtained from Slide 12 and Slide 32 of Stefan Biereigel's and Szymon Kulis' presentation on TMRG (December 2019, Leipzig – also see the TMRG webpage with CERN Microelectronics)

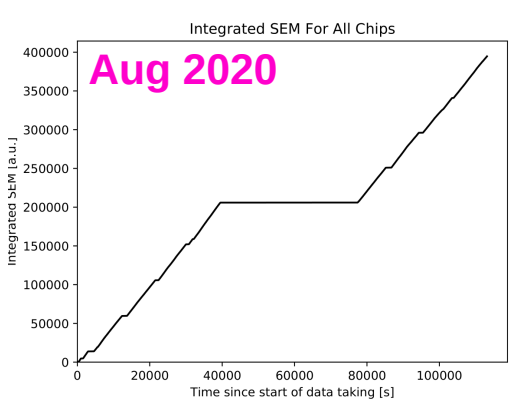
Examples of SEUs in a Register

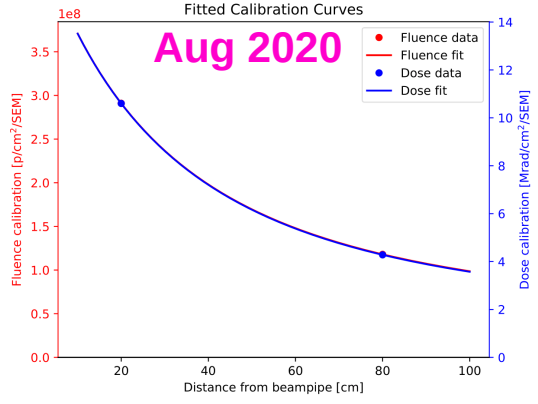
Register type	Description	Number of registers
SCReg	Special/control	1
ADCS	ADC monitoring	3 (6)
MaskInput	Mask for each channel	8
CREG	Digital config	2 (7)
STAT	Runtime statistics/counters	7 (5)
HPR	High priority status codes	1
TrimDAC	Trim for each channel	40
CalREG	Calibration mask	8
HitCountREG	Cluster info for each channel	64

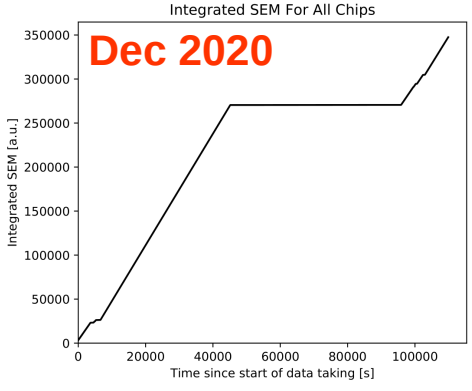
Un-bracketed numbers correspond to V1 chips, bracketed numbers correspond to V0 chips

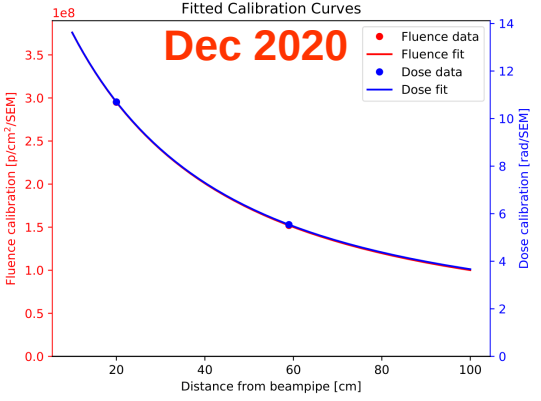
Dose and Fluence Calculation

- PIF @ TRIUMF provides SEM (i.e., particle) counts – all chips see the same integrated SEM
- Linear fit fluence/SEM and dose/SEM vs. $1/R^2$ where R is the radial distance from the beamline
- calibration(R = chip position) * SEM(time) = dose/fluence(time)



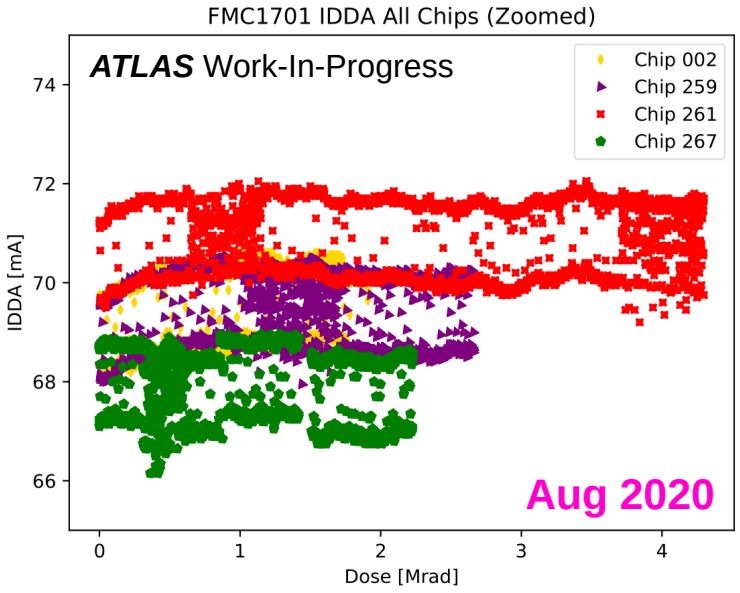


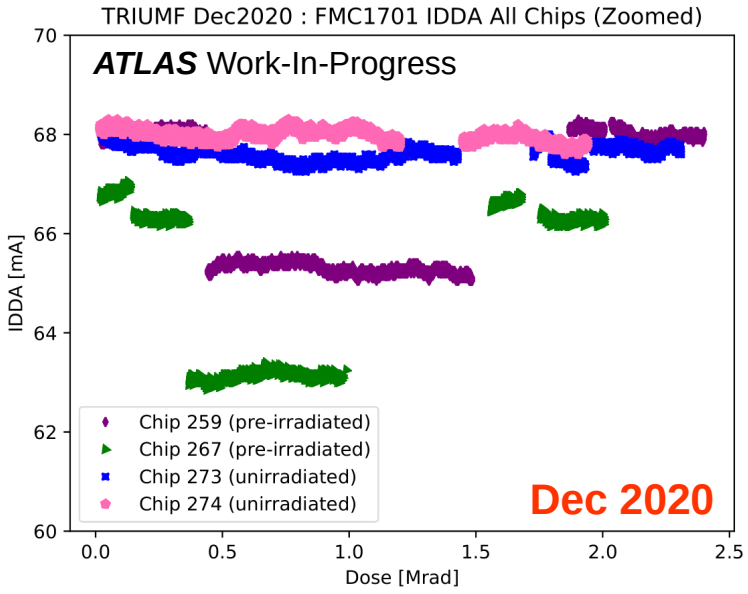




Red/blue curves lie on top of one another

Analog Currents with Protons: August vs. December 2020

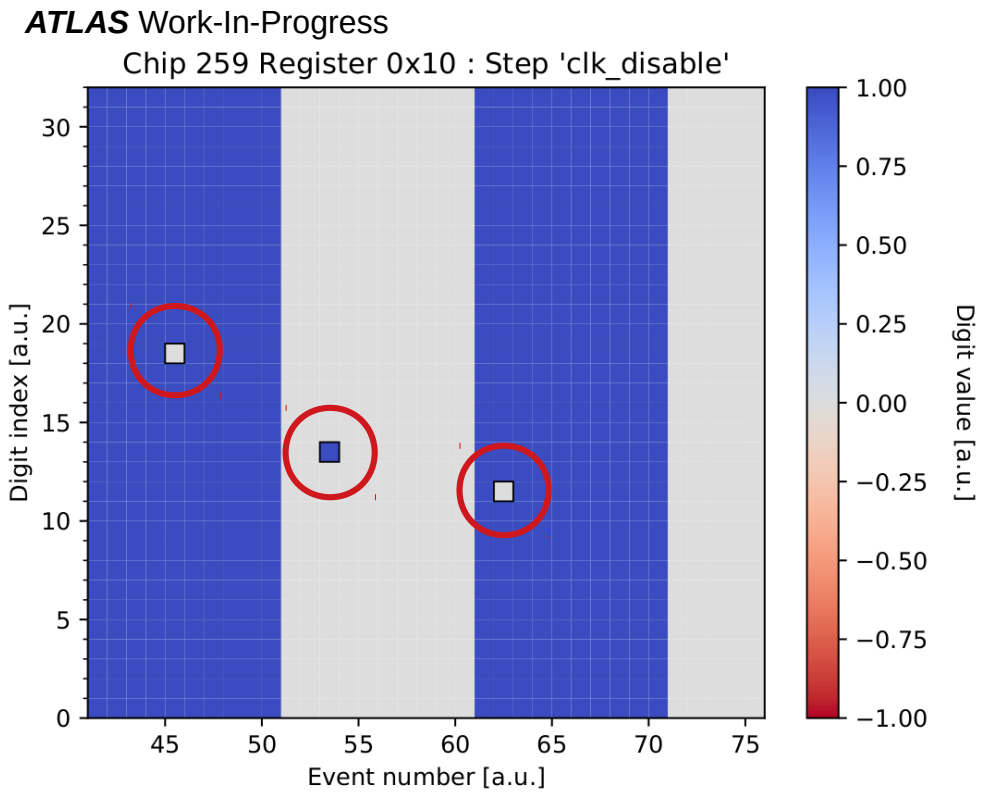




Consistent with ABC130 results (Sec. 4.10 of [4]) – 70 mA analog current (flat in dose) – drops in current for Chips 259+267 for December likely due to communication timeouts

Examples of SEUs in a Register

SEUs are circled in red



SEU Cross Section Calculation

- If we have $n_{0\to1}$ 0➔1 bit flips and $n_{1\to0}$ 1➔0 bit flips and measure a total of $N_{packets}$ 32-bit registers, then the SEU cross section is calculated as:

$$\sigma_{\mathrm{SEU}} = \frac{1}{\phi} \times \frac{n_{0\to1} + n_{1\to0}}{32 \times N_{\mathrm{packets}}}$$

Integrated fluence ϕ is counted ***only*** between the **write** and **read** times of each register

- We can also calculate a 95% confidence interval:

$$\Delta_{\sigma_{\mathrm{SEU}}} = \frac{1.96}{\phi} \times \sqrt{\frac{R \times (1-R)}{32 \times N_{\mathrm{packets}}}} \text{ where } R = \frac{n_{0\to1} + n_{1\to0}}{32 \times N_{\mathrm{packets}}}$$

August 2020 Register Cross Sections: In Numbers

ATLAS Work-In-Progress

Chip	Running mode	$n_{0\to1}$	$n_{1\to0}$	$32 \times N_{\text{packets}}$	ϕ [p/cm^2]	$\sigma_{\text{SEU}} \pm \Delta_{\sigma_{\text{SEU}}}$ [cm^2/p]
002	Nominal	12	377	3166816	2.90×10^{15}	$(4.24 \pm 0.07) \times 10^{-20}$
259	Nominal	0	0	1687328	1.01×10^{15}	$*5.88 \times 10^{-22}$
	BCID	0	0	1634624	1.02×10^{15}	$*6.03 \times 10^{-22}$
	GF	0	0	1428352	8.74×10^{14}	$*8.01 \times 10^{-22}$
	BCID + GF	0	0	1642048	1.05×10^{15}	$*5.82 \times 10^{-22}$
	Clock disabled	3	69	67008	5.24×10^{13}	$(2.05 \pm 0.10) \times 10^{-17}$
261	Nominal	0	0	1434336	1.47×10^{15}	$*4.75 \times 10^{-22}$
	BCID	0	0	1707328	1.74×10^{15}	$*3.37 \times 10^{-22}$
	GF	0	0	1453536	1.41×10^{15}	$*4.86 \times 10^{-22}$
	BCID + GF	0	0	1857024	1.78×10^{15}	$*3.03 \times 10^{-22}$
	Clock disabled	12	166	124544	1.42×10^{14}	$(1.00 \pm 0.04) \times 10^{-17}$
267	Nominal	0	0	1189056	7.85×10^{14}	$*1.07 \times 10^{-21}$
	BCID	0	0	1853312	9.05×10^{14}	$*5.96 \times 10^{-22}$
	GF	0	0	2227296	1.14×10^{15}	$*3.93 \times 10^{-22}$
	BCID + GF	0	0	713600	4.30×10^{14}	$*3.26 \times 10^{-21}$
	Clock disabled	3	79	122816	7.76×10^{13}	$(8.60 \pm 0.36) \times 10^{-18}$

Inclusive in registers, asterisks refer to upper limits **assuming 1 SEU**