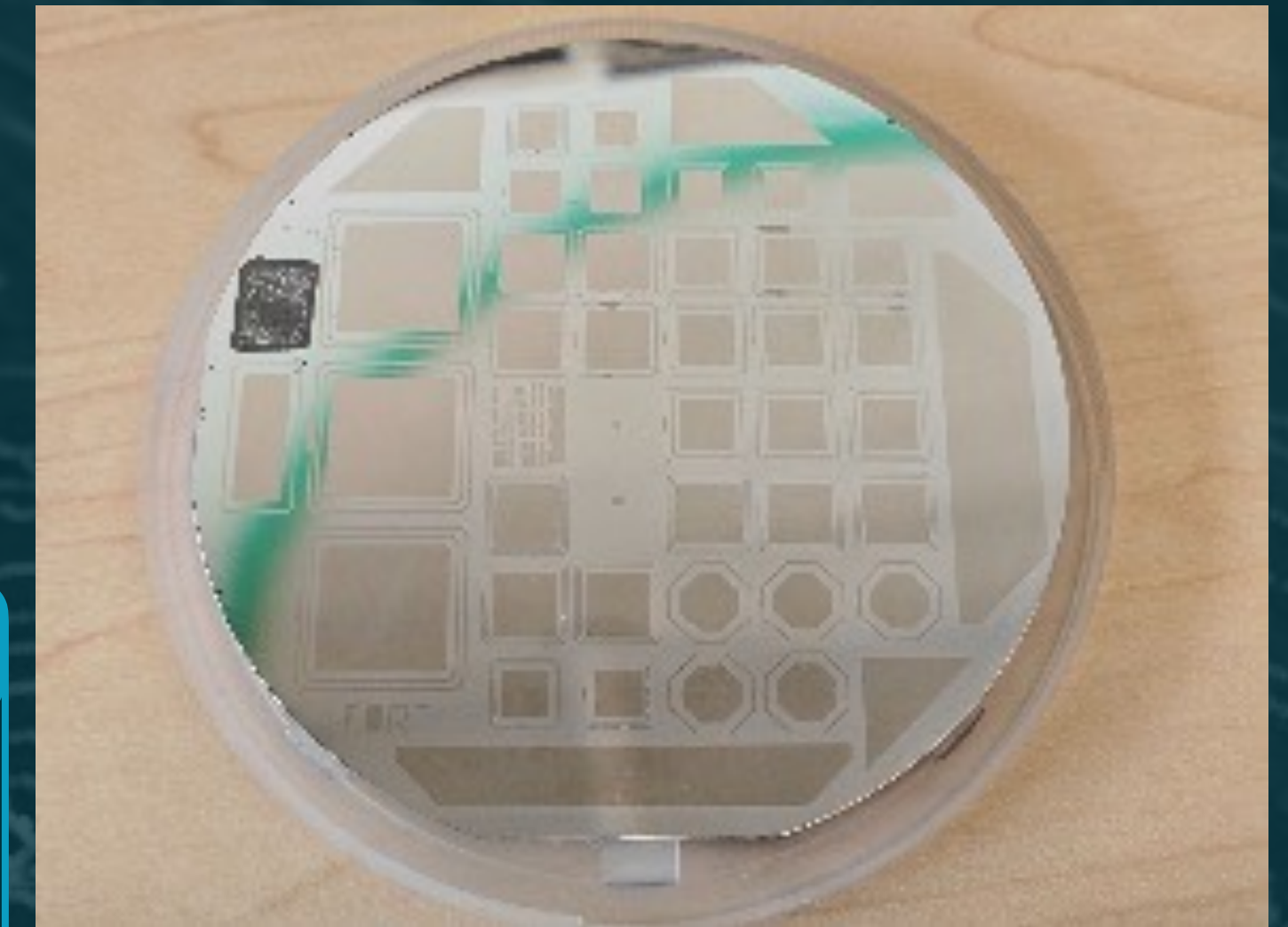
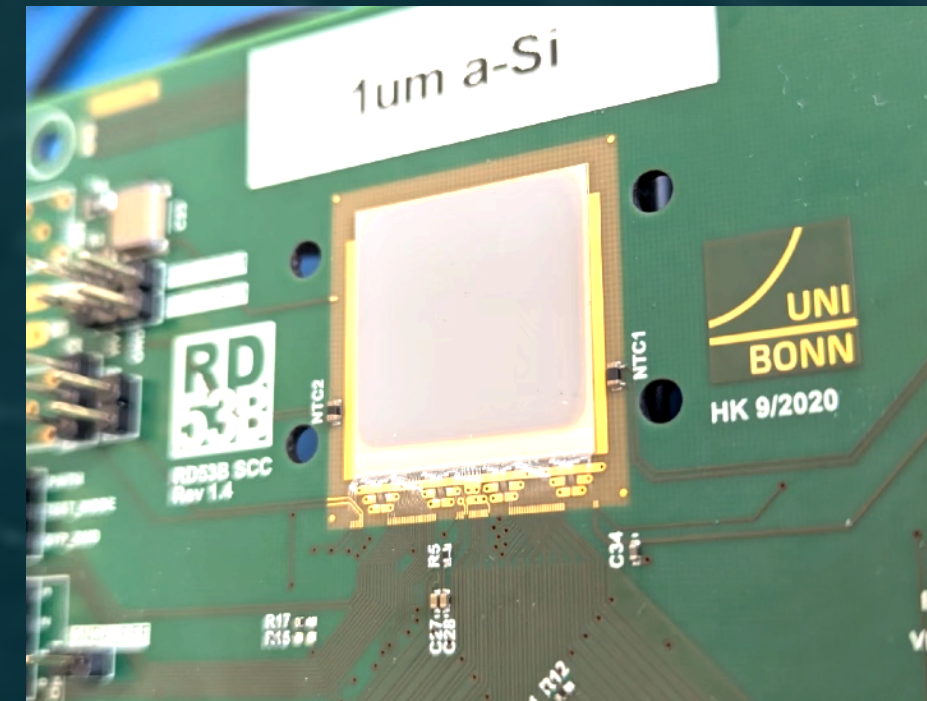
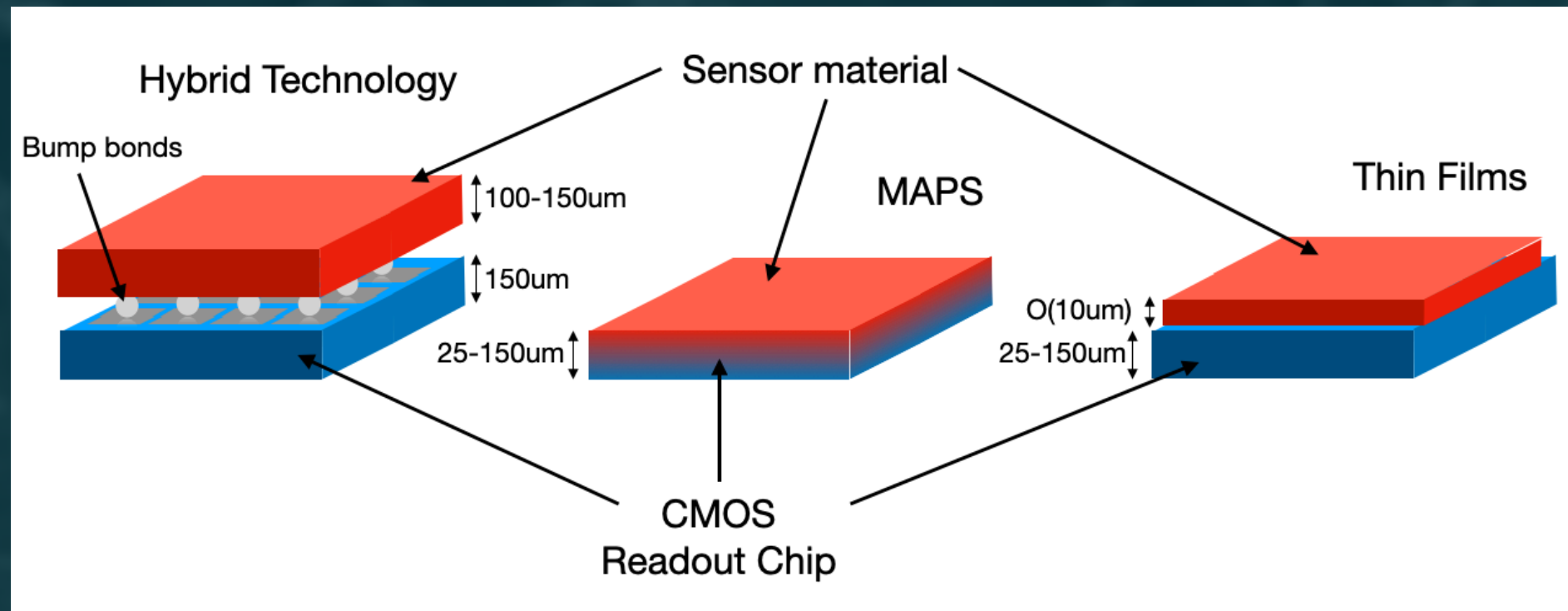


FORC: Film on Readout Chip

US Thin Film Sensor Enthusiasts - 02.10.26

Timon Heim - LBNL

Film on Readout Chip

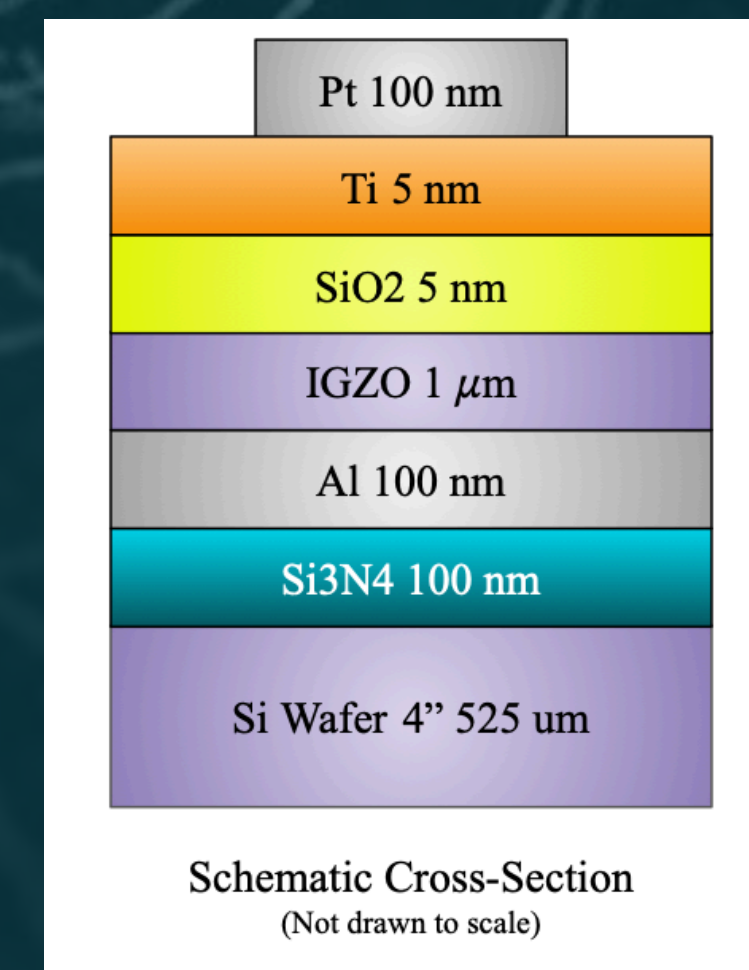


Film on Readout Chip (FORC)

- Goal: deposit sensor material directly onto CMOS Pixel readout chip to enable low mass and highly scalable Pixel detectors
- Allows independent readout chip and sensors development
- LDRD in FY24/25 to investigate thin film sensors using facilities available at LBNL:
 - Semiconductor Detector Lab (SDL)
 - Molecular Foundry
 - UC Berkeley Nanolab
- Primary sensor materials investigated:
 - a-Si: known caveats but should yield functioning detector
 - IGZO (Indium Gallium Zinc Oxide): very high electron mobility and can theoretically yield equivalent amount of electron/hole pairs than crystalline silicon

Status

- Three prong investigation:
 - 1. Identify suitable materials and understand required processing/stackup
 - 2. Understand and test constraints of direct deposition on CMOS chips
 - 3. Test industrialization and scalability of process
- Do currently not have functioning prototype
- Had to learn a lot of material science, many of steps we want to do are unorthodox ($\geq 1\mu\text{m}$ thick layers, substrates, deposition constraints)
- Very close to hopefully first working a-Si prototype
- Some more work needed for IGZO due to more complicated material stackup/processing



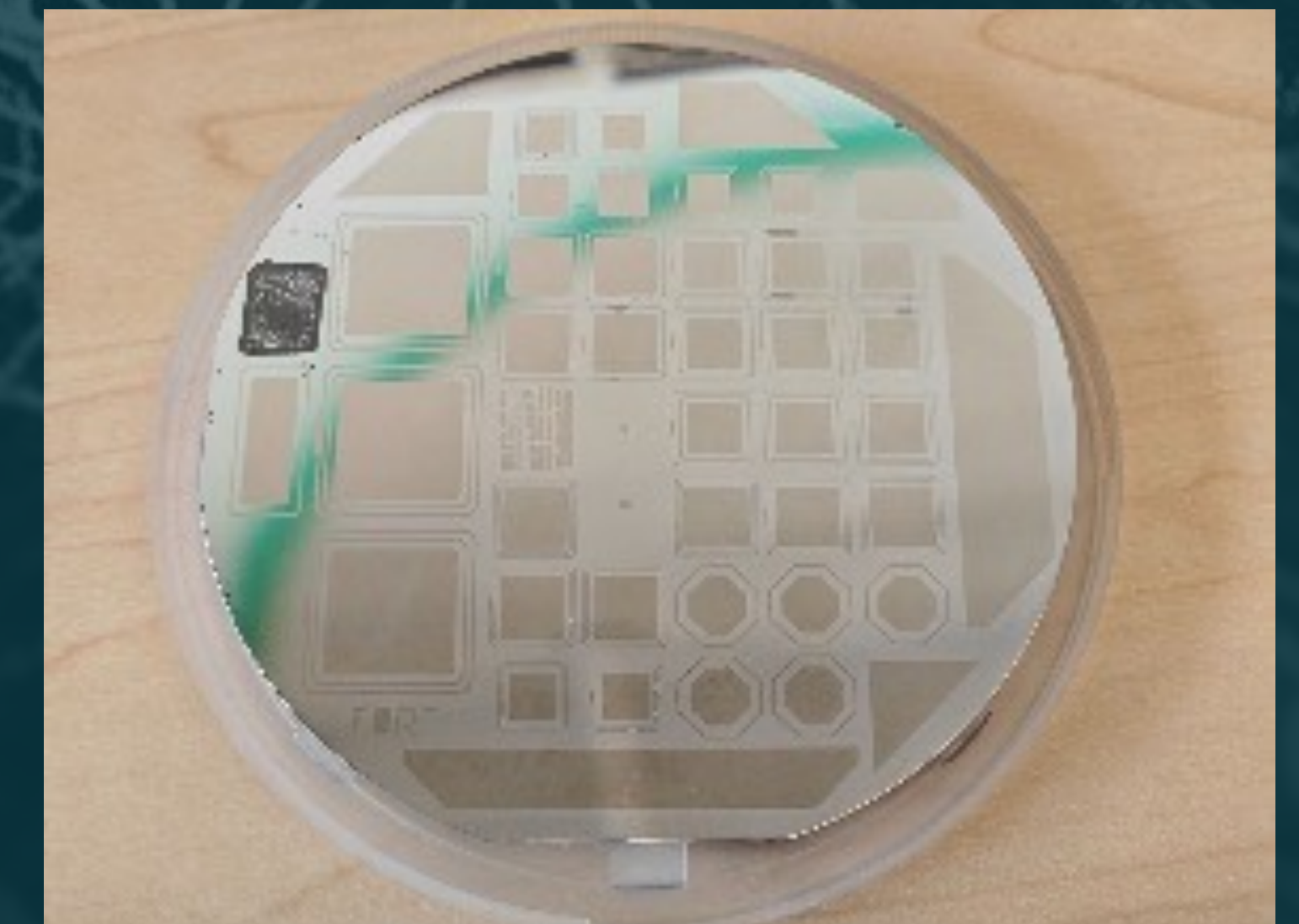
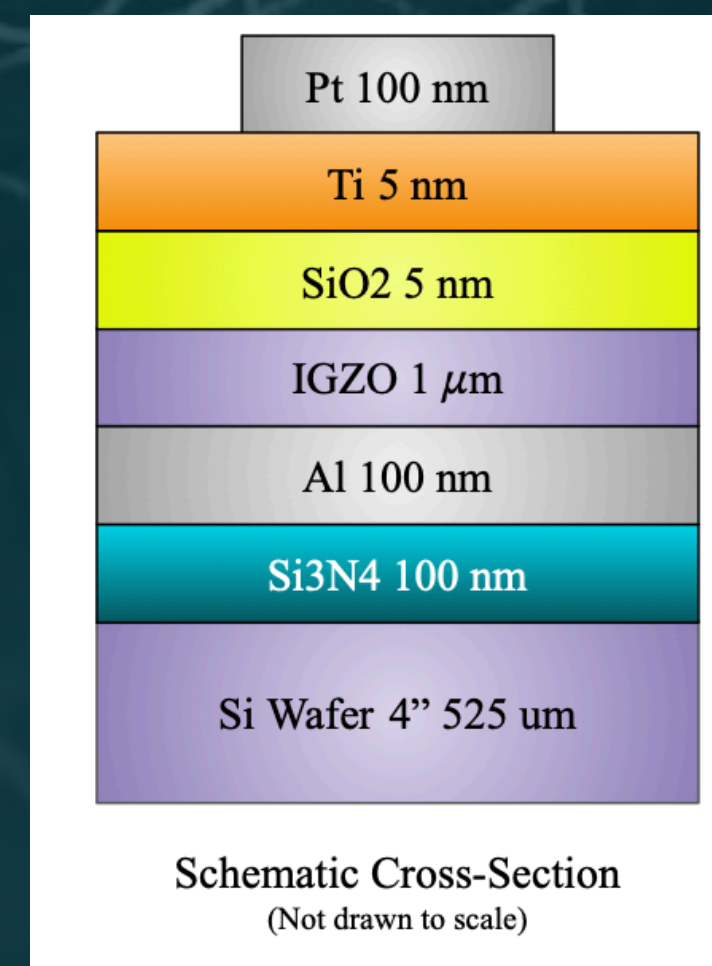
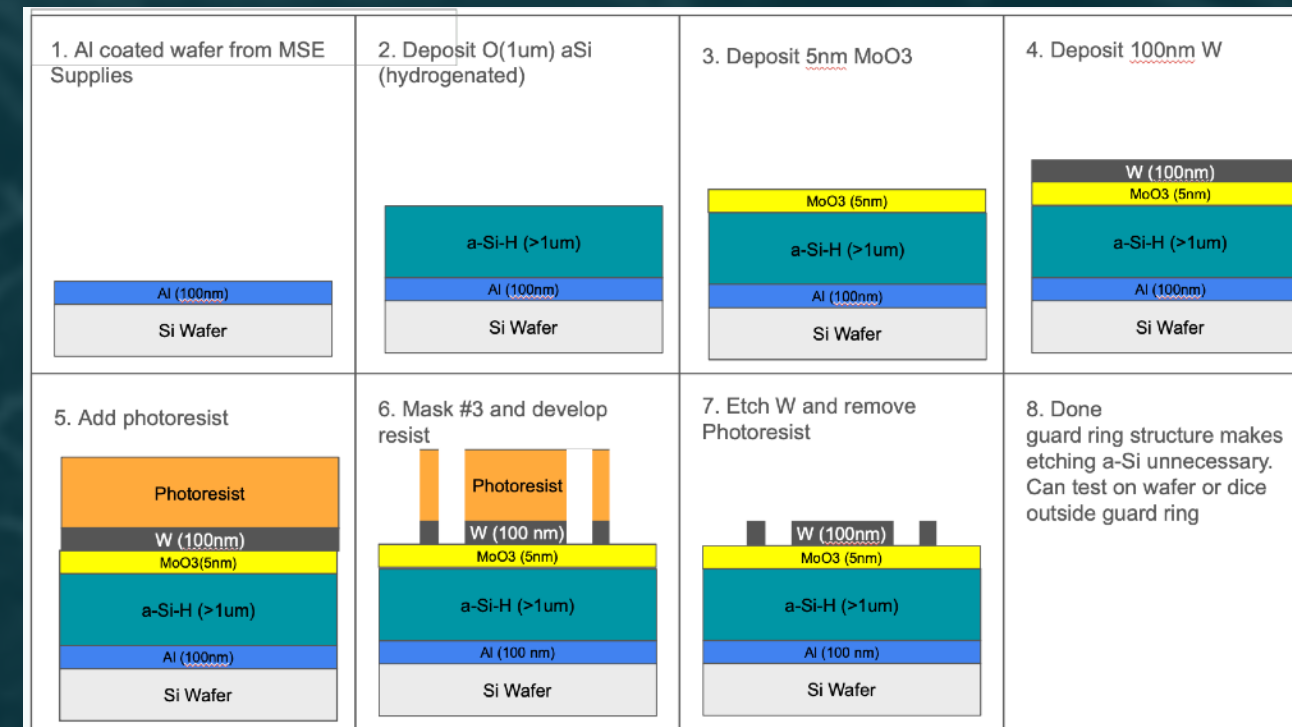
a-Si:H

- Cannot dope -> cannot make PIN diode
- Relying on Schottky diode with metal to achieve depletion in intrinsic layer
- Are aware that pad capacitance likely too large for 1μm thick layer to observe any MIPs
- Observed low-ohmic contact between front-side electrodes -> long goose chase of suspected pin holes
- Eventually figured out Si wafer substrate might be the issue -> now passivating it with SiN before depositing backside electrode (Al)
- Revisiting wafer mask to make smaller pads (less capacitance) and easier access to backside electrode

IGZO

- IGZO resistivity heavily dependent on O vacancy density (vacancies increase carrier density) -> O₂ added during sputtering & annealing -> can potentially use this in place of doping to create carrier density profiles
- Due to high electron mobility need different metal for Schottky contact, chose Platinum but less easily available
- Ran into issue of galvanic corrosion during wet etch, had to switch to dry etch
- Still having issues with low-ohmic contacts
- IGZO has very low hole mobility, expecting to have issues with phase charge build up

Problems Encountered



Wafer Prototypes

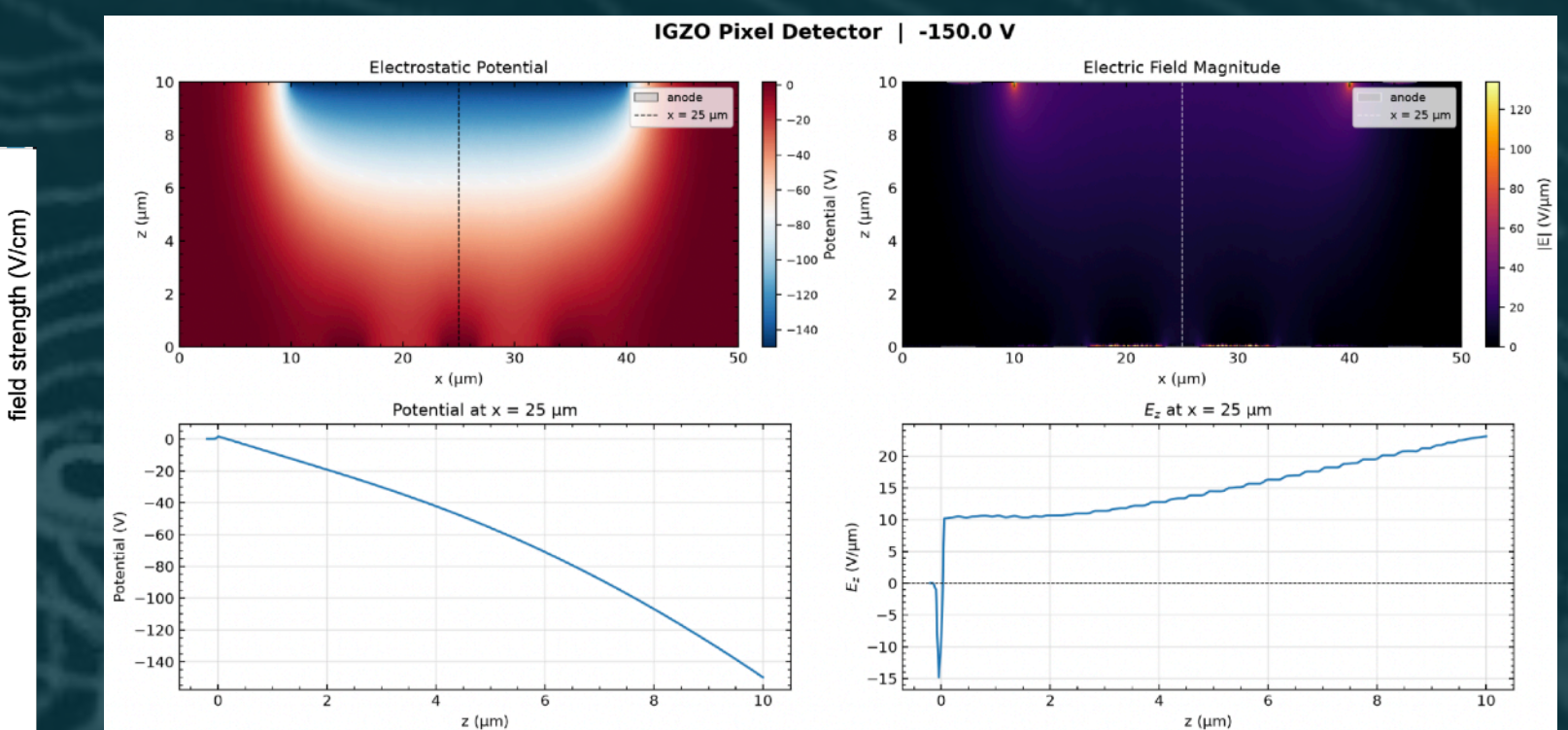
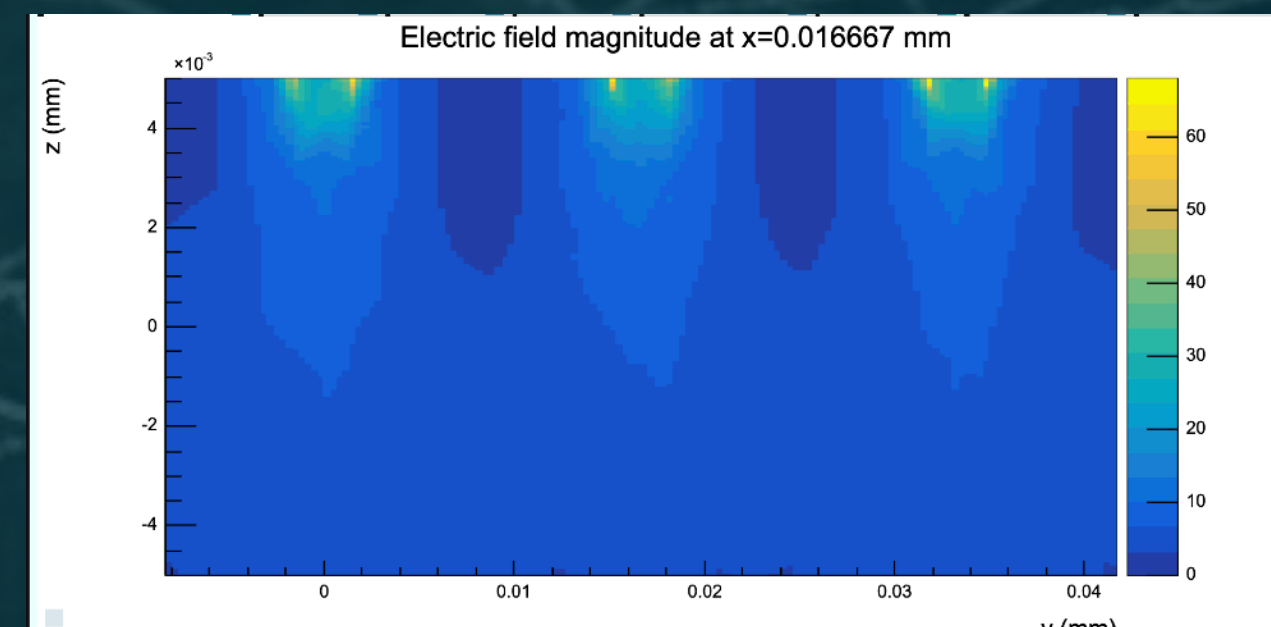
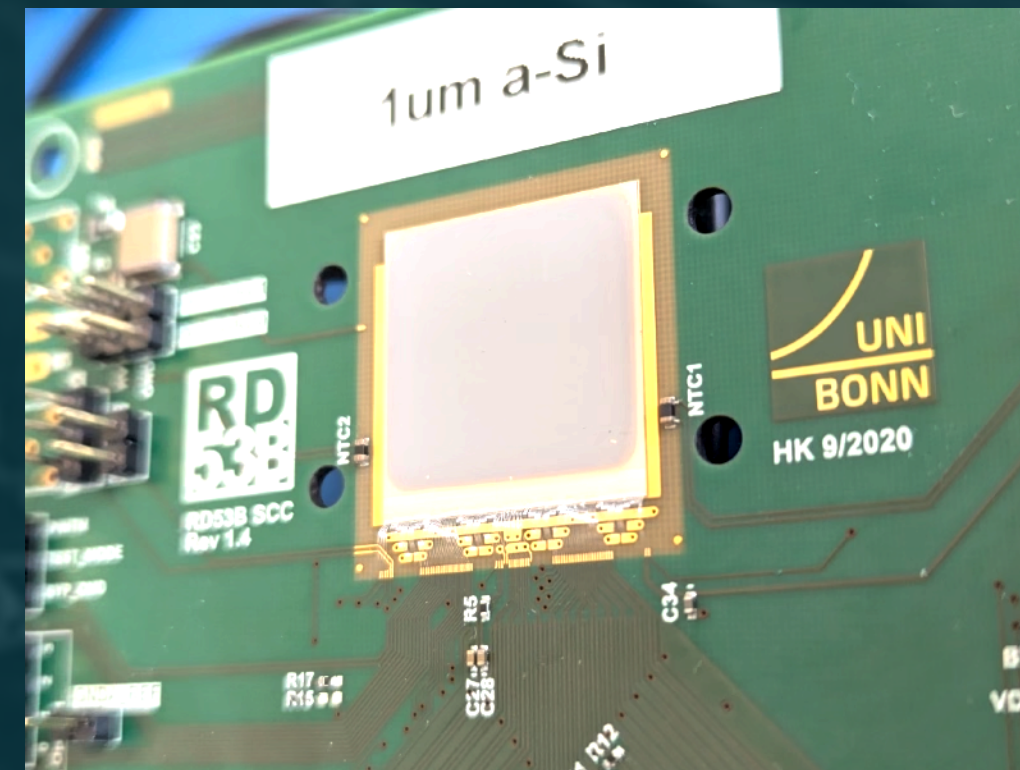
- Prototyping on wafers has been beneficial to figure out the most basic material interactions and processes
- But pad size with easily achievable feature size is limited -> large detector capacitance
- Looking into miniaturization and easier access to backside -> Likely requires more shadow masking
- Goal: establish processing pipeline for test diodes
- Stuck with 1 μ m films for now -> 1 μ m = 8hr deposition

Deposition on ITkPixV2

- Very limited number of ITkPixV2 chips -> need to find time to perform political work to buy R&D wafer lot with in community to get more
- Successfully performed number of tests with a-Si:H (shadow masking, ESD safety, etching) -> should be ready to make some prototypes
- Would really need more than 1 μ m to get enough charge deposition, but have not tested that on wafers

CMOS + X

- Was awarded CMOS + X shuttle run in 28nm CMOS
- Goal: develop readout chip platform for wafer scale sensor deposition testing -> 4D Fabric
- Culprit: don't have chip design ready, work in progress, tapeout planned for December
- Other culprit: do not have clear process yet that we want to test



Simulation

- Successfully established a simulation chain for IGZO with devsim and Allpix2
- Lots of parameters guessed, hoping to dial it in with prototype measurements
- Have some questions about the simulation flow

Outlook

