

ITAINNOVA activities for the CMS high luminosity upgrade and ECFA DRDs PID2023-148418NB-C43

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Project Main Data - Meeting - Zaragoza

- **Total Researchers:** 5+3
 - **Budget:** 182.000 €
 - **Key Words:** LHC, CMS, Particle Detectors, Physics Analysis, Dark Matter, Pixel Silicon Detectors, Power Distribution
- EDPs: 3,5
- Term:** 3 years

1. Introduction

- ITA contribution is focused on WP4, WP5, WP2
- **WP4 – R&D on detector electronics for 4D tracking and high data density detectors:**
 - Develop innovative power distribution schemes (GaN DC-DC, serial powering, supercapacitors) to improve efficiency and robustness of future high-density detectors.
 - Implement high-precision timing distribution techniques (White Rabbit) to achieve sub-nanosecond synchronization for 4D/5D detector systems.
 - **Alignment with DRD7** (Electronics Systems R&D collaboration):
 - Contributes to Theme DRDT7.1 → Advanced technologies for higher data density & power efficiency.
 - Contributes to Theme DRDT7.3 → Development of high-precision timing distribution for 4D/5D techniques.
- **WP2 - Sensor production, module assembly, and hybrid testing for CMS ETL)**
 - Associate to ETL activities
- **WP5 - Advanced detector characterization techniques).**
 - **Alignment with DRD3**
- These activities has started 2.5 years ago – GANCAP4CMS, PC, AIDAINNOVA & EUROLABS

1. Introduction

- **ITA leads Work Package 4 (WP4)** – R&D on detector electronics for 4D tracking and high-data-density detectors (DRD7 collaboration).
 - **WP4.O1 – High-efficiency power distribution with GaN DC-DC converters.**
 - **Task WP4.T1: Development of a new GaN-based DC-DC converter for serial powering architectures.**
 - **WP4.O2 – High-precision and deterministic reference distribution with White Rabbit.**
 - **Task WP4.T2: Development of a distributed synchronization architecture based on WR for timing detectors.**
- **Collaborative contributions:**
 - WP2 (Sensor production, module assembly, and hybrid testing for CMS ETL).
 - **Task WP2.T2: Final qualification of LGAD+ETROC hybrids (support in grounding, EMC, noise characterization).**
 - WP5 (Advanced detector characterization techniques).
 - **Task WP5.T2: Upgrade and improvement of EMC test systems** (noise transfer function measurement, conducted emission in radiation environments).

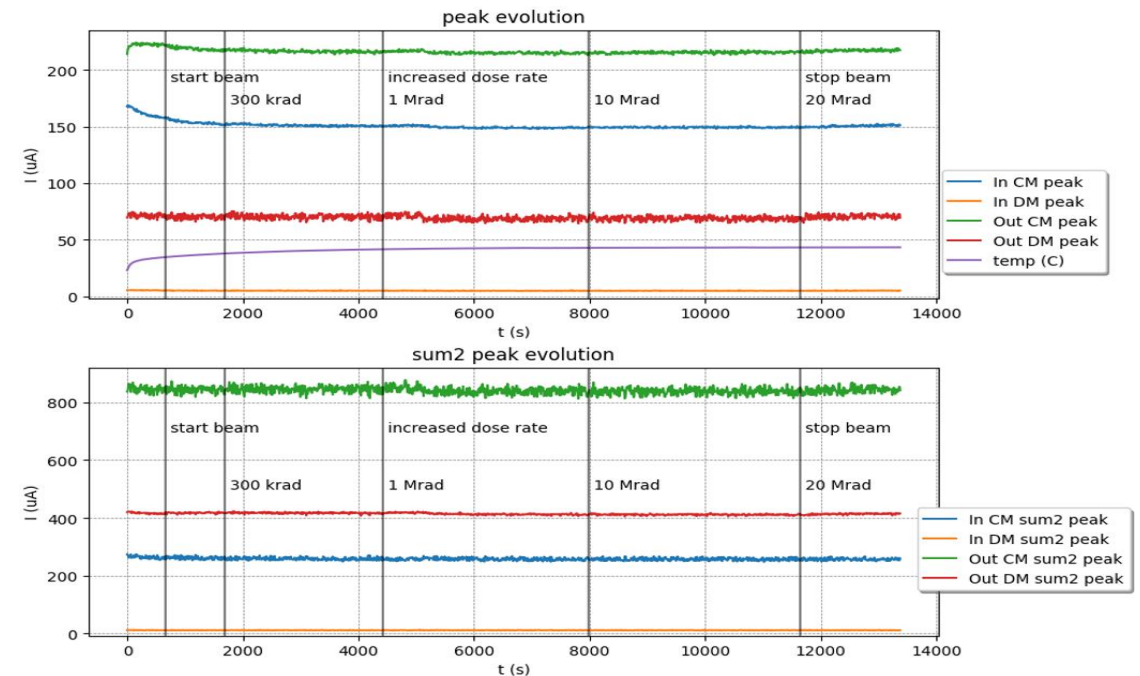
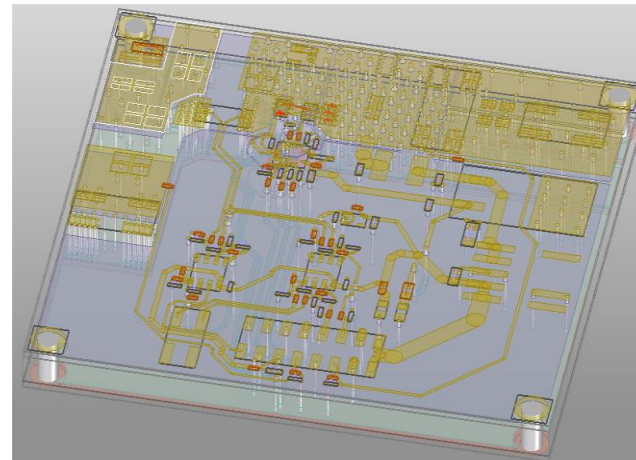
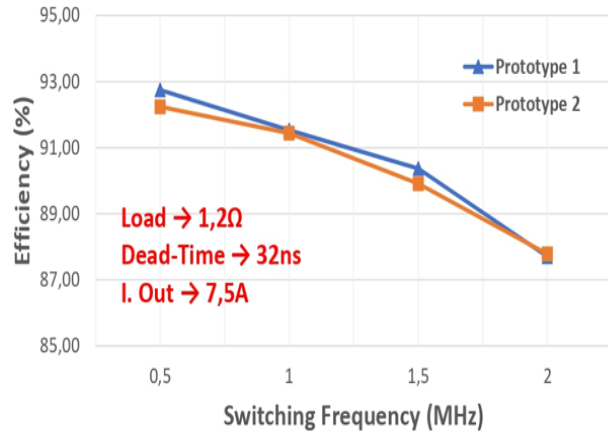
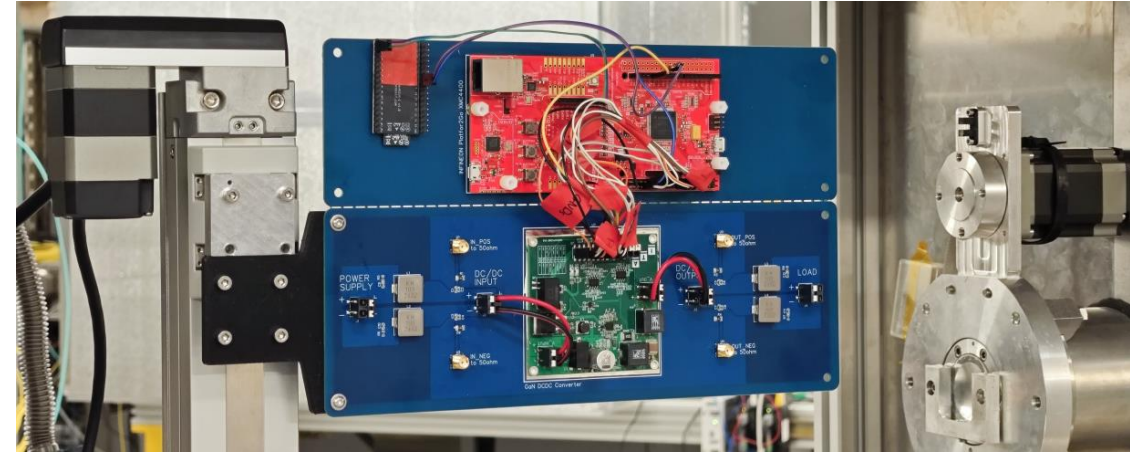
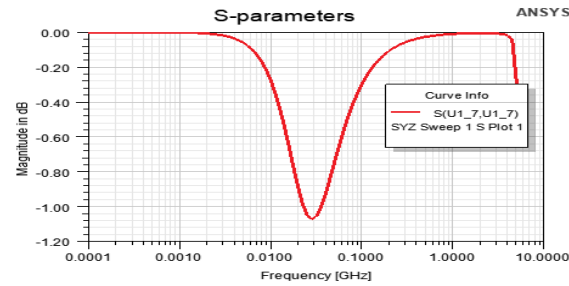
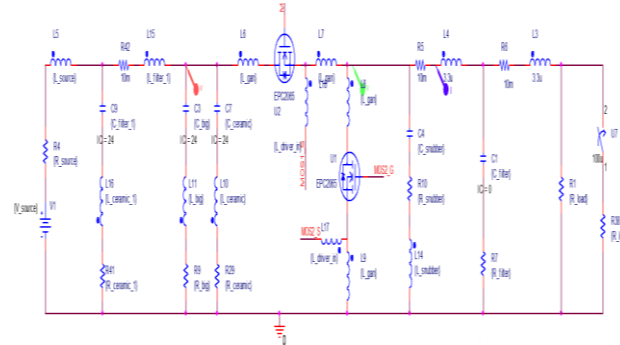
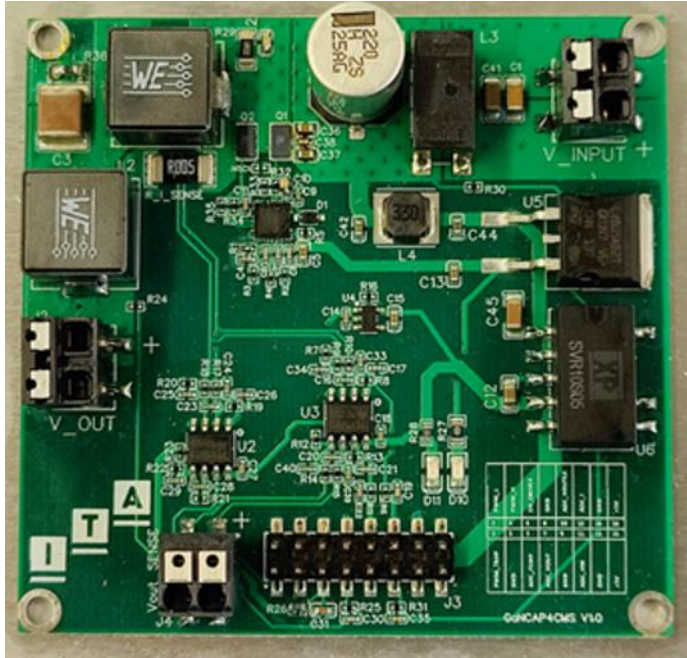
2. WP4 High-efficiency power distribution with GaN DC-DC converters

- The main goal of WP4 is to improve energy efficiency of next-generation detector systems.
 - Reduce material budget while ensuring robust and reliable power distribution.
 - Explore GaN-based DC-DC converters and supercapacitors for serial powering systems.
 - Address design challenges: radiation hardness, EMI filter sizing, PCB layout optimization..
- One task is planned (Task WP4.T1) focused on the development of a new GaN-based DC-DC converter
 - Define key parameters for detector power distribution.
 - Design and prototype an ultra-compact GaN converter.
 - Perform preliminary radiation hardness assessment.
 - Study PCB design strategies for robustness and EMI control.
 - Evaluate integration of supercapacitors in high-radiation environments

2. WP4 High-efficiency power distribution with GaN DC-DC converters

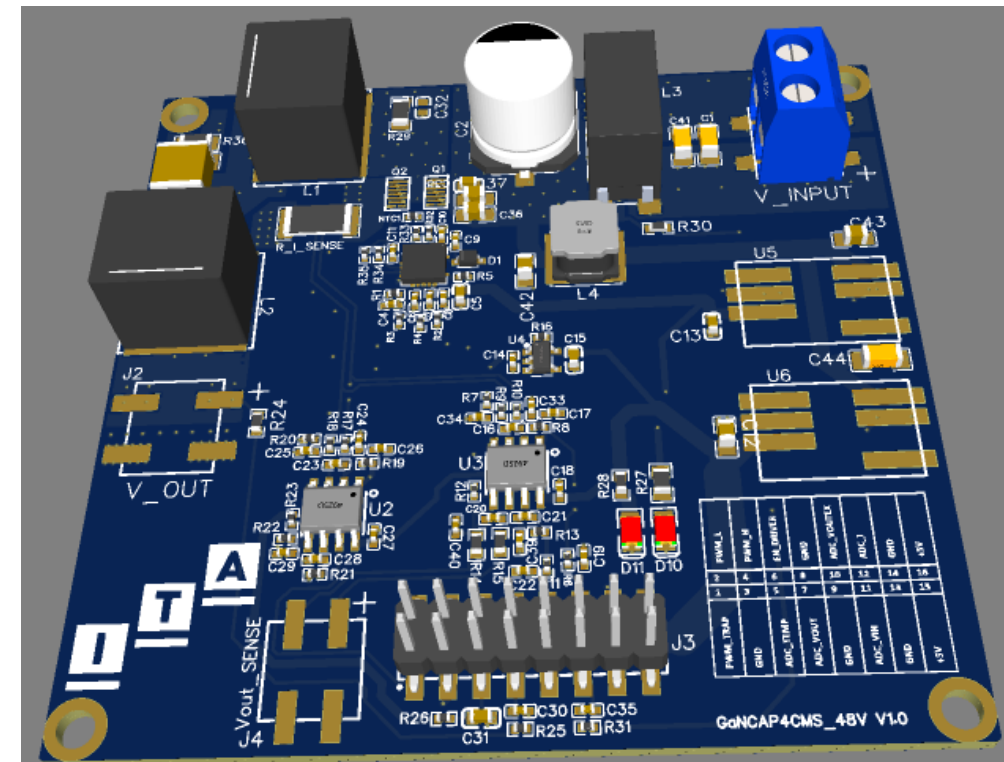
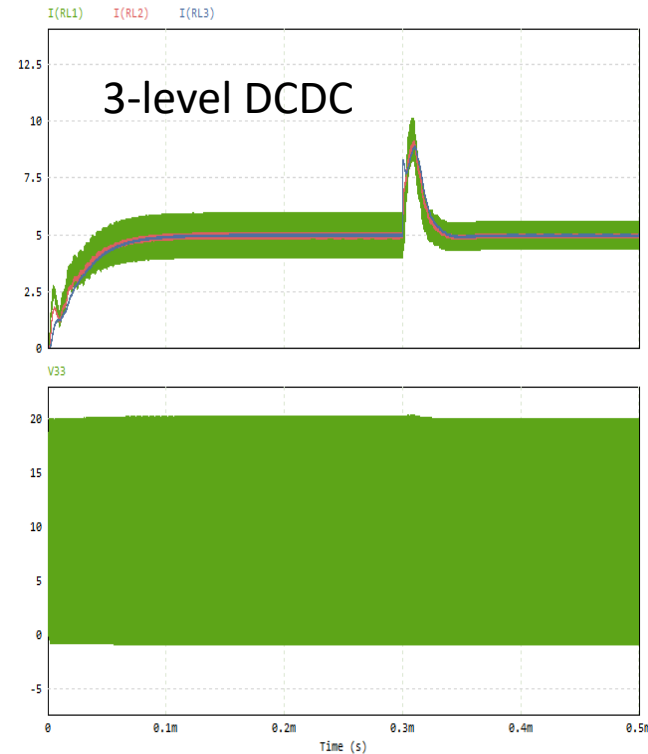
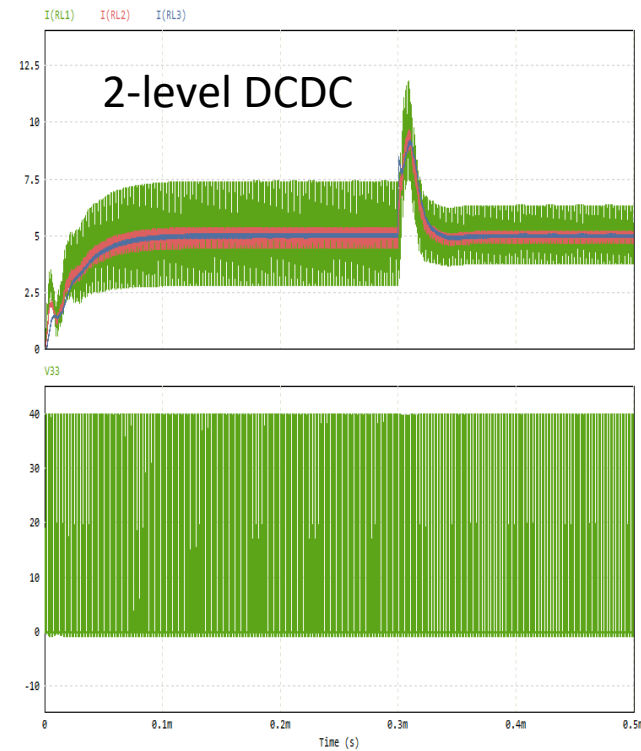
- First GaN-based DC-DC current-source prototype developed and tested.
- Prototype specifications: 12–24 V input, up to 10 A output, 200 W, 2 MHz switching frequency.
- Electrical and EMC modelling performed using HFSS-SiWave, PSIM and PSpice.
- Functional tests completed: efficiency, thermal behaviour, start-up, dead-time and ringing mitigation.
- Conducted EMI measurement setup developed and validated for time/frequency-domain characterization.
- Radiation campaign performed at IPHC-Strasbourg with 25 MeV protons up to 30 Mrad.
- No relevant degradation or clear EMI changes observed after irradiation.

2. WP4 High-efficiency power distribution with GaN DC-DC converters



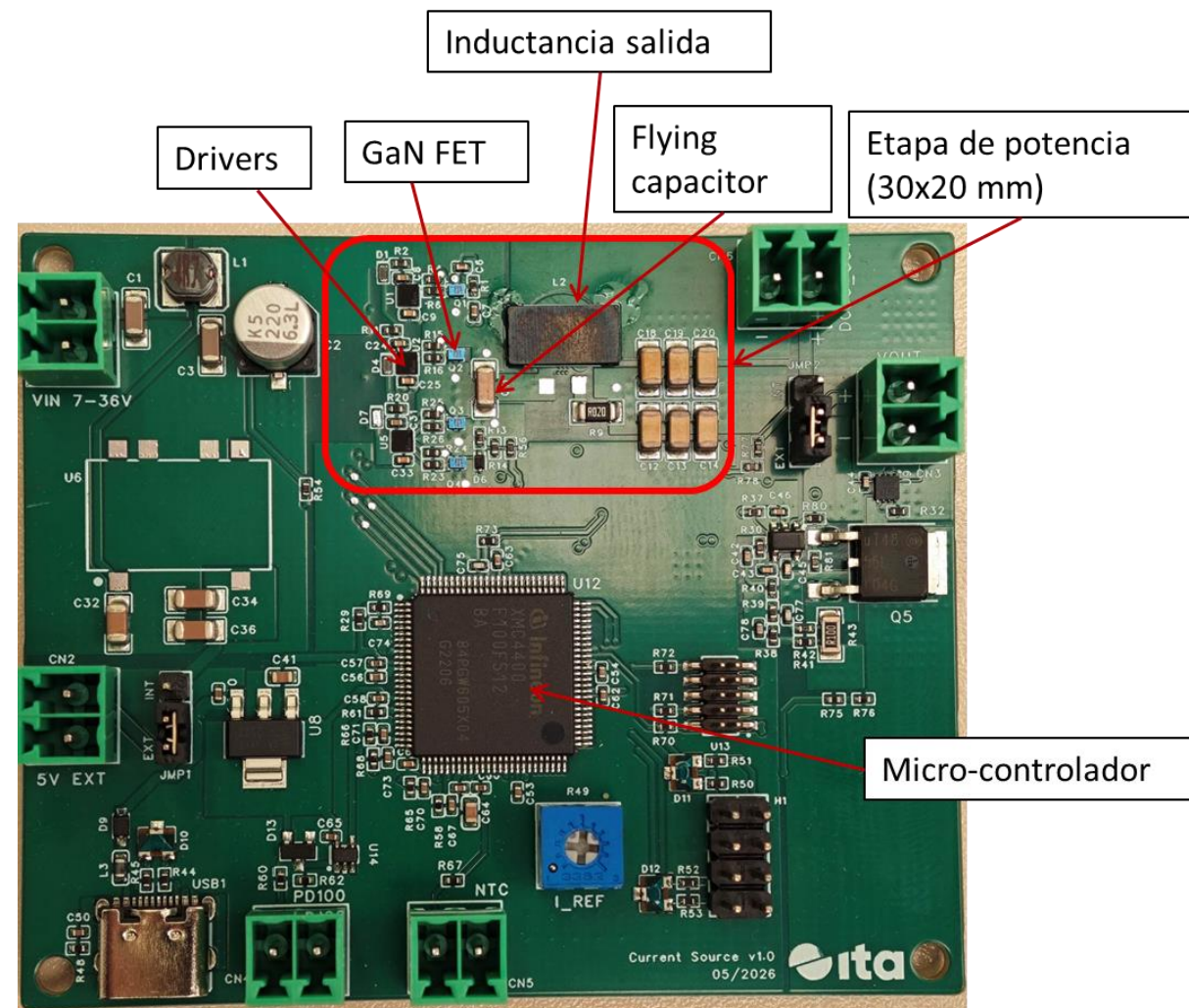
2. WP4 High-efficiency power distribution with GaN DC-DC converters

- New 48 V prototype has been developed, focused on compactness, filtering, COTS components and scalability.
 - Multilevel (2/3) topologies and modular/multiphase architectures



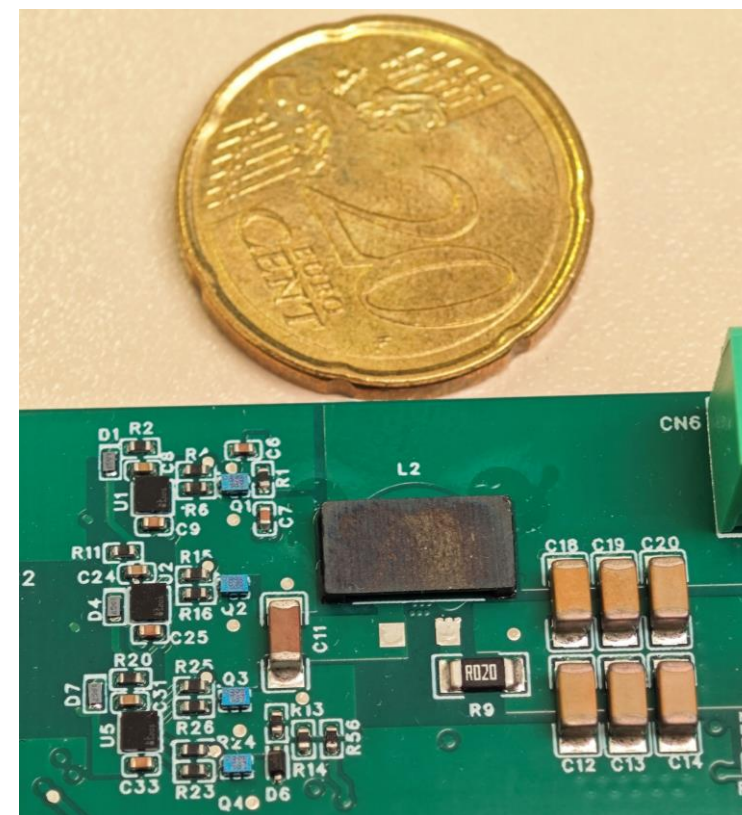
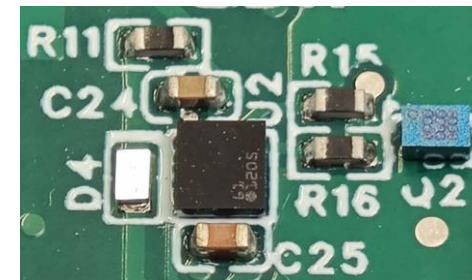
2. WP4 High-efficiency power distribution with GaN DC-DC converters

- The new GaN DC-DC current-source prototype characteristics – 3 Level topology validation
 - Three-level step-down multilevel flying-capacitor topology.
 - Input voltage range: 10–48 V.
 - Output current: up to 3 A, around 100 W.
 - Switching frequency: 1–5 MHz.
 - Effective output ripple frequency: $2 \times f_{sw}$.
 - Reduced transistor voltage stress: $V_{in}/2$.
 - Peak efficiency above 90%.
 - Fully based on COTS components.
 - Output filter inductance integrated in the PCB.



2. WP4 High-efficiency power distribution with GaN DC-DC converters

- Design upgrades for final prototype is planned for September
 - Radiation-tolerant GaN transistors and drivers.
 - Increased output capability:
 - Up to 10 A, 300–400 W.
 - Optimized layout to reduce parasitic inductance, EMI, overshoot and ringing.
 - More compact power stage by removing auxiliary elements.
 - Analog controller implementation.
 - Improved robustness against TID and single-event effects
 - Optimized input and output filtering



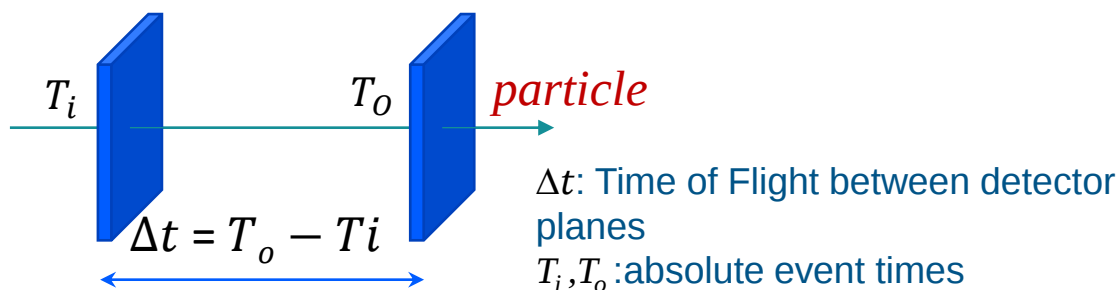
3. WP4.O2 – High-precision & deterministic reference distribution with WR

- Evaluate feasibility of the White Rabbit (WR) protocol for future 4D/5D detector reference.
 - Provide sub-nanosecond synchronization across distributed detector systems.
 - Address limitations of current WR COTS in terms of jitter, phase stability, and determinism.
 - Identify required hardware and component improvements for detector-grade performance.
- One task is planned (Task WP4.T2) focused on the development of a distributed synchronization architecture
 - **Define the architecture and implement a system demonstrator** using LGAD sensors + ETROC2 readout chip synchronized via WR.
 - **Perform functional tests to measure the reference performance for multiplane detectors systems synchronization.**
 - Identify performance bottlenecks and propose hardware/firmware improvements.
 - Validate applicability of WR to large-scale timing detector architectures.

3. WP4.O2 – High-precision & deterministic reference distribution with WR

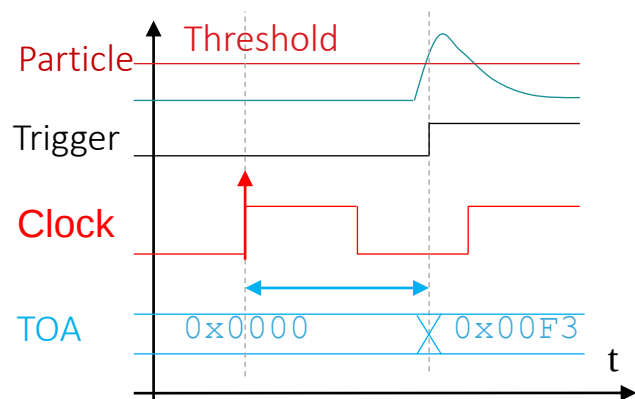
- Main activity aims to design and evaluate a prototype of a distributed clock network based on White Rabbit Technology to measure the time of flight of particles with accuracies in the sub-nanosecond range.

We want to measure Δt : Time of Flight (TOF) **We measure** 2 Time Of Arrival (TOA) w.r.t ref. clock



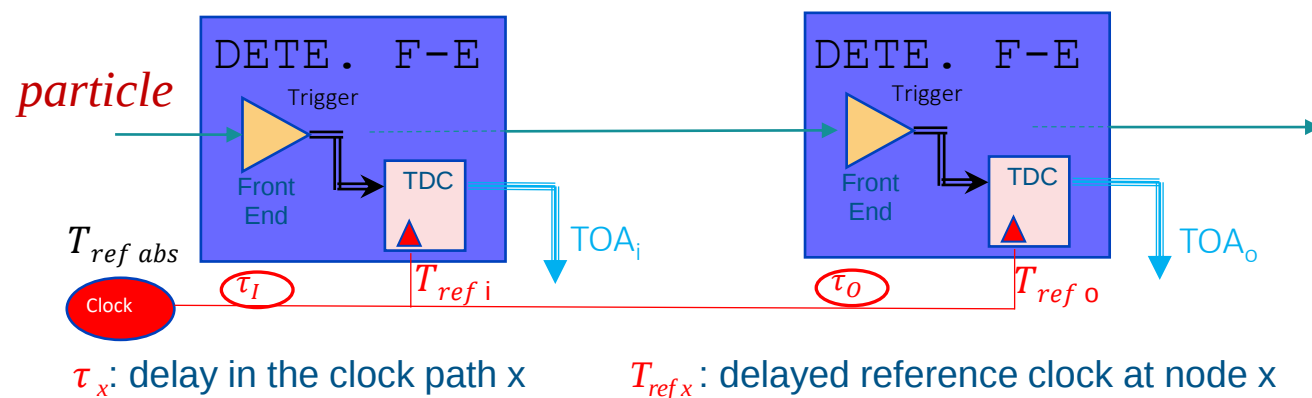
ToF MEASUREMENT

We use a local reference clock ($T_{ref x}$)



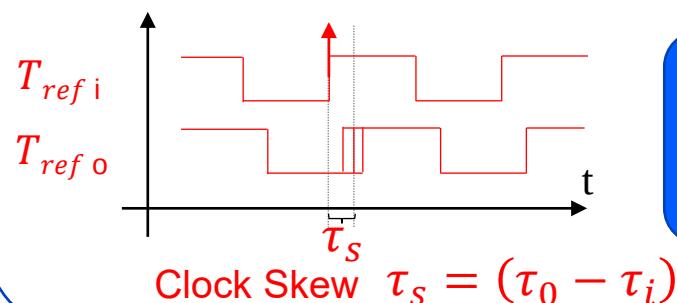
$$T_i = T_{ref i} + TOA_i$$

T_{ref} needs to be a common synchronized reference among all nodes



Synchronization: **We need a clock distribution** ensuring accuracy, precision and coping skew

Phase of the Ref clock at Detectors



High Accuracy profile

3. WP4.O2 – High-precision & deterministic reference distribution with WR

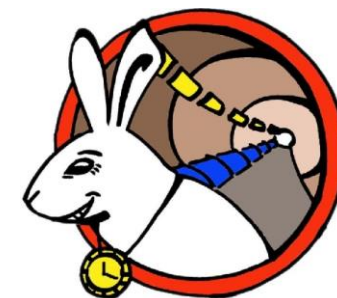
- The timing architecture aims to distributed a reference signal to synchronize different FEE (sensors +hybrids)
 - Simple open loop approach with regular coax cable / optical fibers
 - Study new timing solutions as IEEE1588 PTP (White Rabbit – Developed at CERN)

Standard - Non self-calibrating system



Traditional solutions require multiple coaxial cables or fibers calibrated and with temperature compensation to cope with jitter, wander... to achieve deterministic and synchronous clock/timing distribution

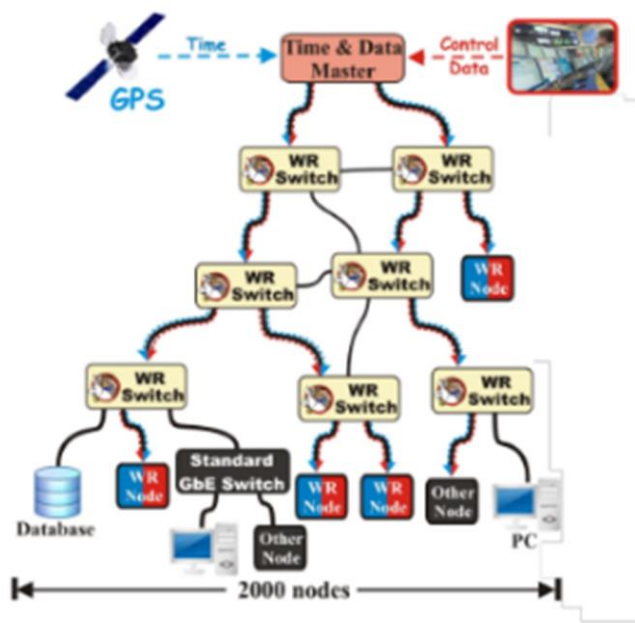
WR - Self-calibrating system



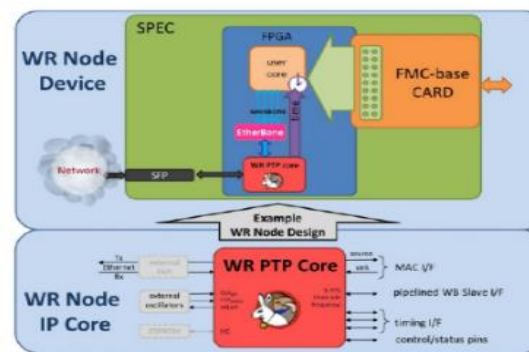
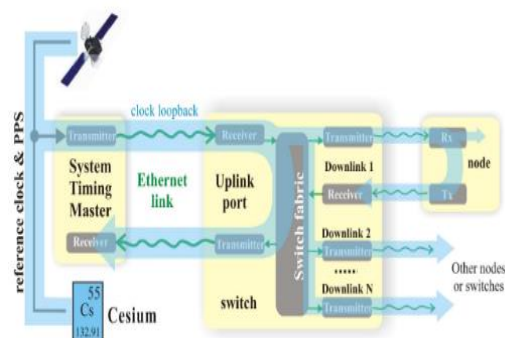
The White Rabbit Project originated the High Accuracy profile under the IEEE 1588 standard: Ethernet based technology for deterministic distribution of timing and data.

3. WP4.O2 – High-precision & deterministic reference distribution with WR

- White Rabbit is a synchronization system designed as an extension of PTP (Precision Time Protocol).
- It is able to achieve sub-nanosecond accuracy over a multi-level tree of nodes.



WR physical layer (clocks)



WR PTP Core

Hardware;

Carrier Board, application FMC, Computer, Cabling, Powering, Ref.

Gateway;

HDL for the FPGA (WR PTP Core)

Firmware;

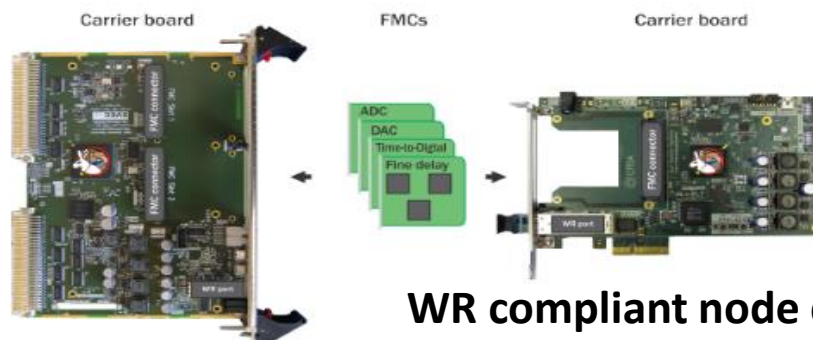
C code for the LM32 Softcore

Software;

Scripts and interpreter

IT/Infrastructure;

Computer(s) for FPGA programming, clocking and Python interpreter



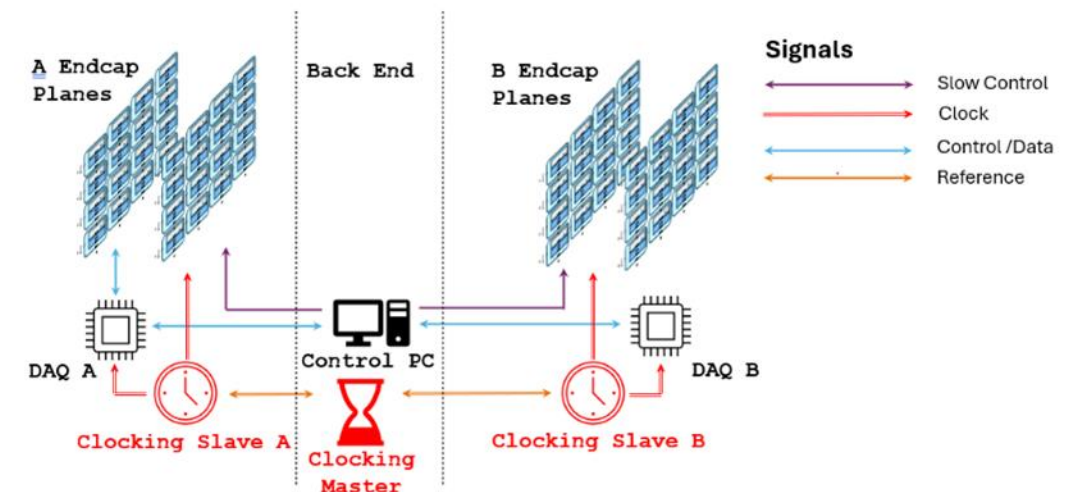
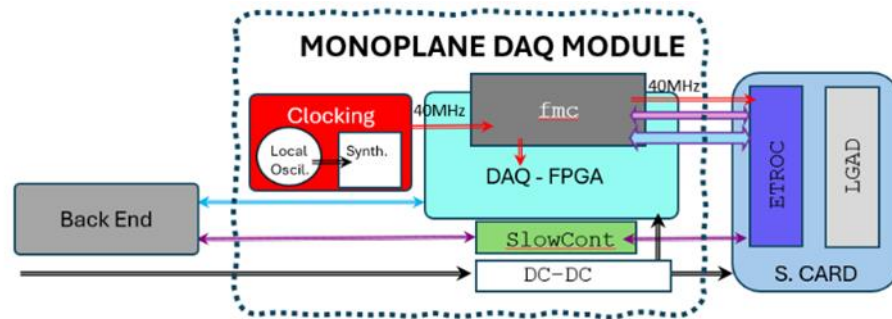
WR compliant node devices (hardware, firmware...)



Getting familiar with the WR technology,
nodes and flow

3. WP4.O2 – High-precision & deterministic reference distribution with WR

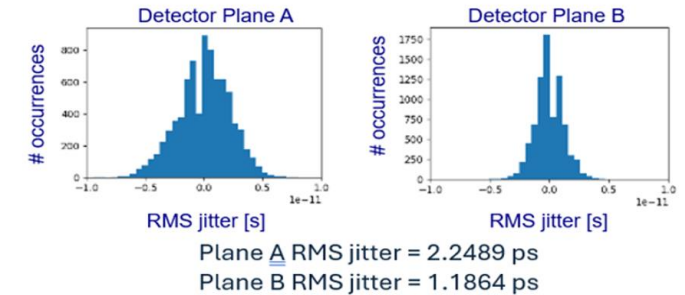
- White Rabbit test infrastructure implemented using CERN SPEC boards, WR switch, optical links, FMCs and the WR PTP Core.
- Incremental synchronization architecture developed and validated:
 - V1 – Single-plane, free-running: validation of the DAQ chain and local clock generation using HMC7044.
 - V2 – Multi-plane, open-loop: 40 MHz clock distribution over coaxial links using Si5338 PLL/jitter cleaners.
 - V3 – Multi-plane, closed-loop WR: 125 MHz distribution over optical fibre with local regeneration of 40 MHz for ETROC.



3. WP4.O2 – High-precision & deterministic reference distribution with WR

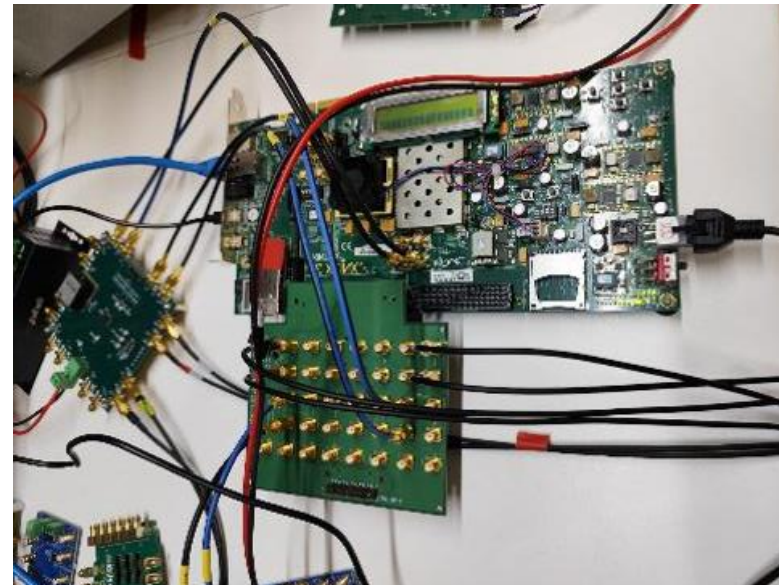
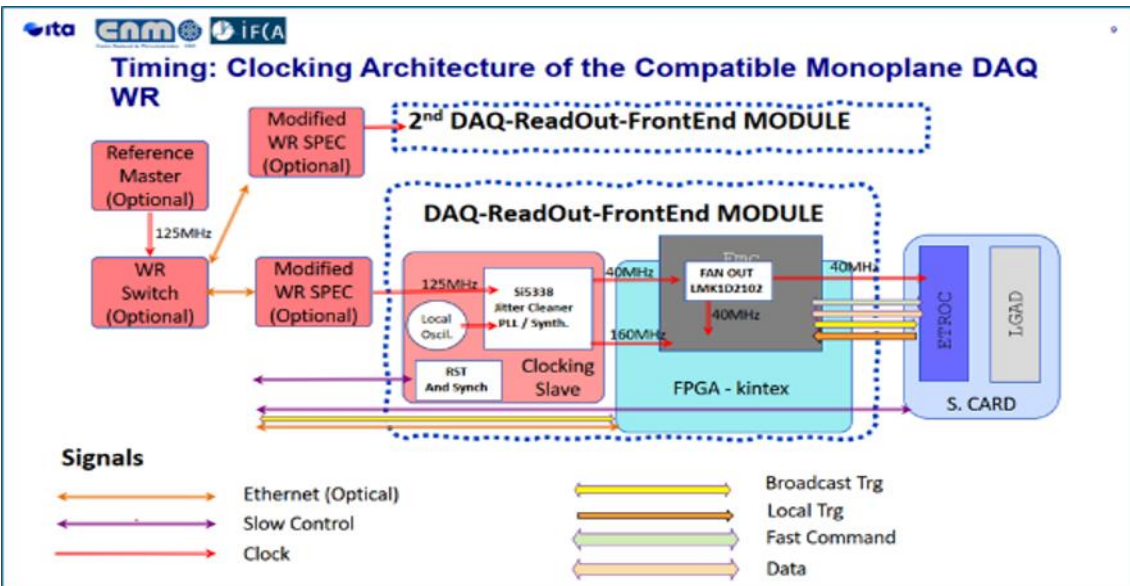
- Characterization of clock quality, phase stability, skew and Time Interval Error performed at different points of the reference path.
- Measured jitter (RMS-TIE) at the ETROC internal clock:
 - Approximately 1.5 ps RMS for the coaxial V2 configuration.
 - Approximately 1–2 ps RMS for the White Rabbit V3 configuration.
- Overall jitter below 10 ps RMS demonstrated at the ETROC frontend, confirming the feasibility of WR for sub-nanosecond detector synchronization.
- Main technical limitations identified: PLL phase-reset management, phase coherence, deterministic start-up and hardware/thermal dependence of residual skew.
- Next activities has been focused on complete integration with LGAD–ETROC detector planes and validation under representative operating conditions.

Phase 3 – Close-Loop WR Reference Distribution
40 MHz Internal ETROC Clock Test Point



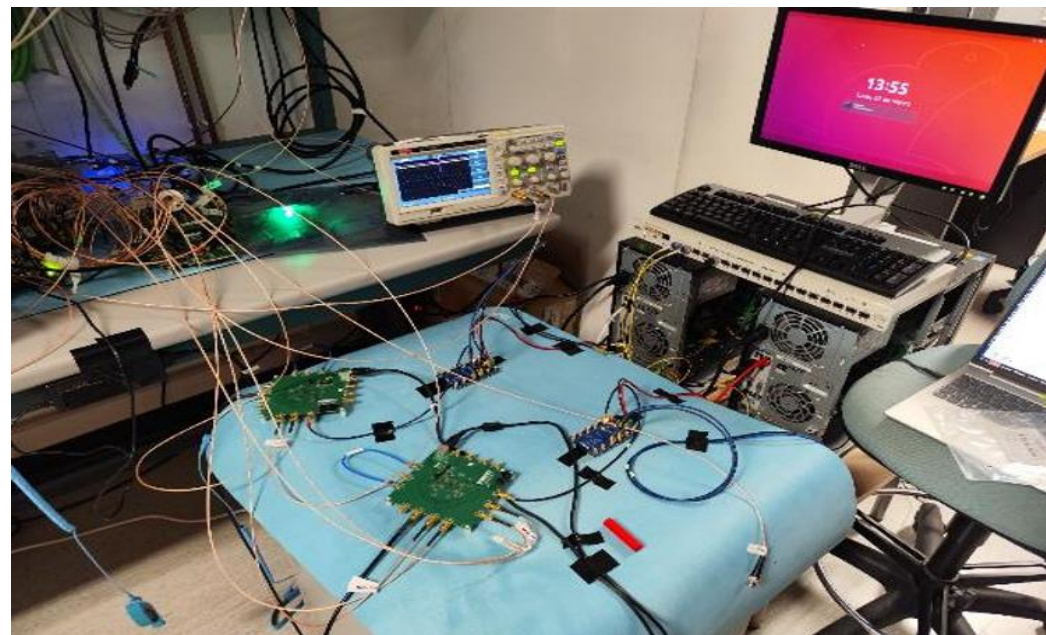
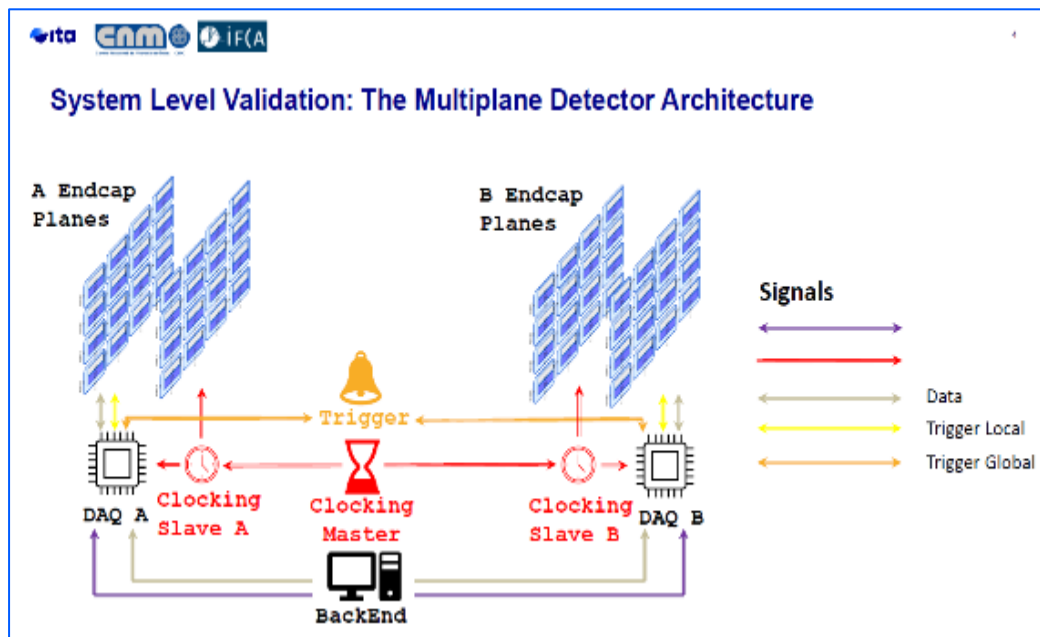
3. WP4.O2 – High-precision & deterministic reference distribution with WR

- The first set of activities of the final demonstrator preparation have been focused on Advanced DAQ and FEE architecture ETROC2-based
 - FPGA-based DAQ implemented on AMD Kintex-7 KC705.
 - Fast commands, serial data decoding, local trigger detection and Ethernet data transmission integrated.
 - Scalable architecture: up to 512 pixels per DAQ module, extendable with additional modules.
 - Auxiliary FMC, fan-out and ITA-SE-DIFF boards developed for system interoperability



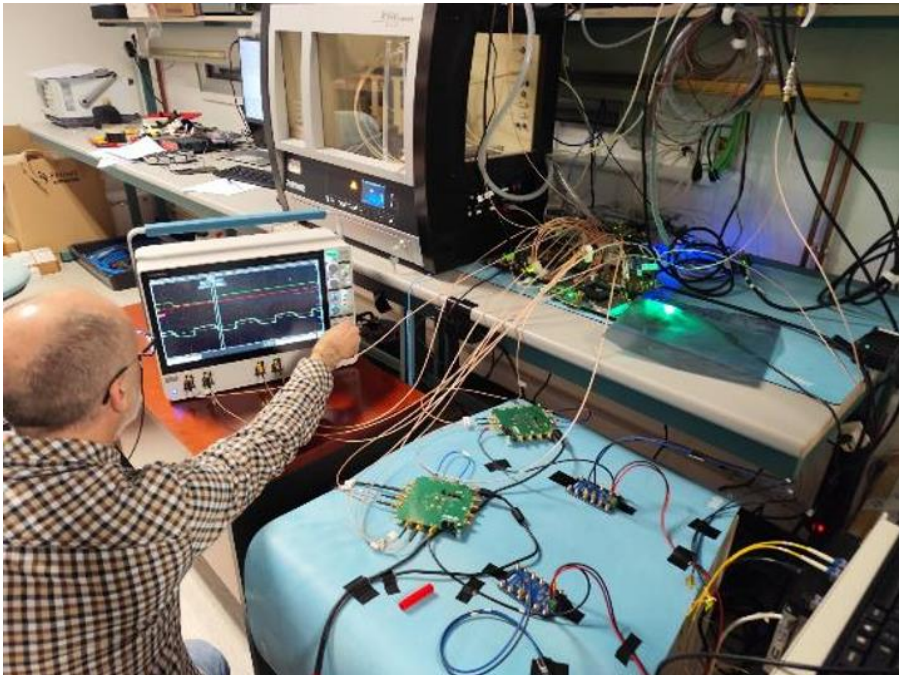
3. WP4.O2 – High-precision & deterministic reference distribution with WR

- Distributed timing architecture based on White Rabbit.
 - Closed-loop synchronization selected to improve jitter, skew and scalability.
 - SPEC-based WR implementation with local Si5338 clock generation.
 - TIE jitter below 10 ps rms experimentally demonstrated.
 - Global trigger logic implemented in FPGA with configurable coincidence, AND/OR and masking functions.

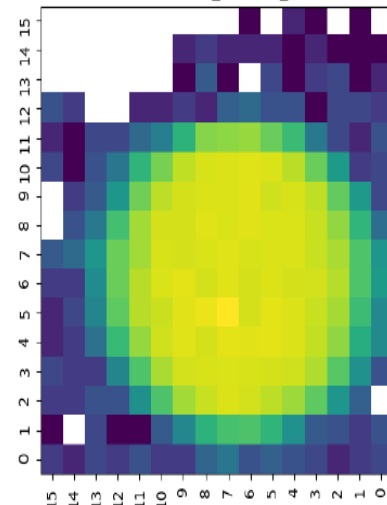


3. WP4.O2 – High-precision & deterministic reference distribution with WR

- Demonstrator integration and validation
 - Four-plane demonstrator architecture specified and integrated.
 - Electronics integrated with DAQ, trigger and WR timing subsystems.
 - Laboratory validation performed with X-ray setup at IFCA.
 - CERN test-beam support provided for DAQ, timing and trigger operation with LGAD/ETROC planes.

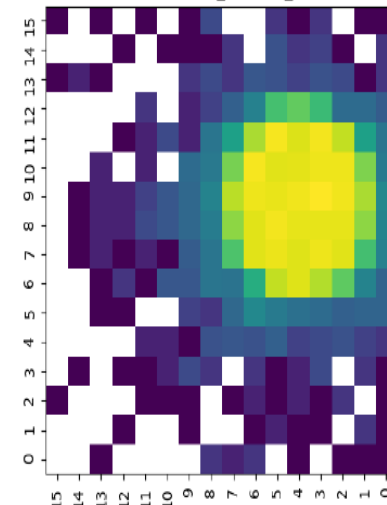


ToT for file:2Kintex/K2/run_708/file_5.sem [CHIP-ID:0]



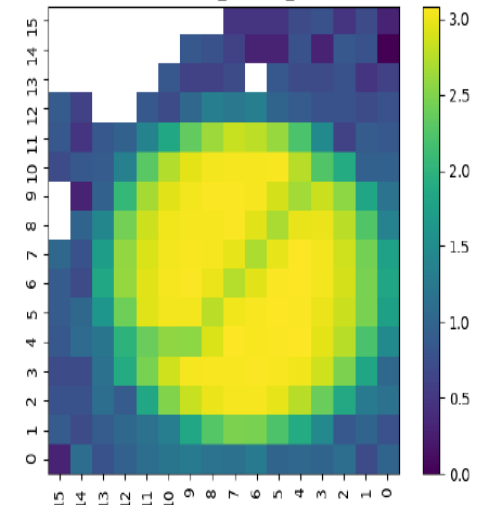
1st Plane

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2nd Plane

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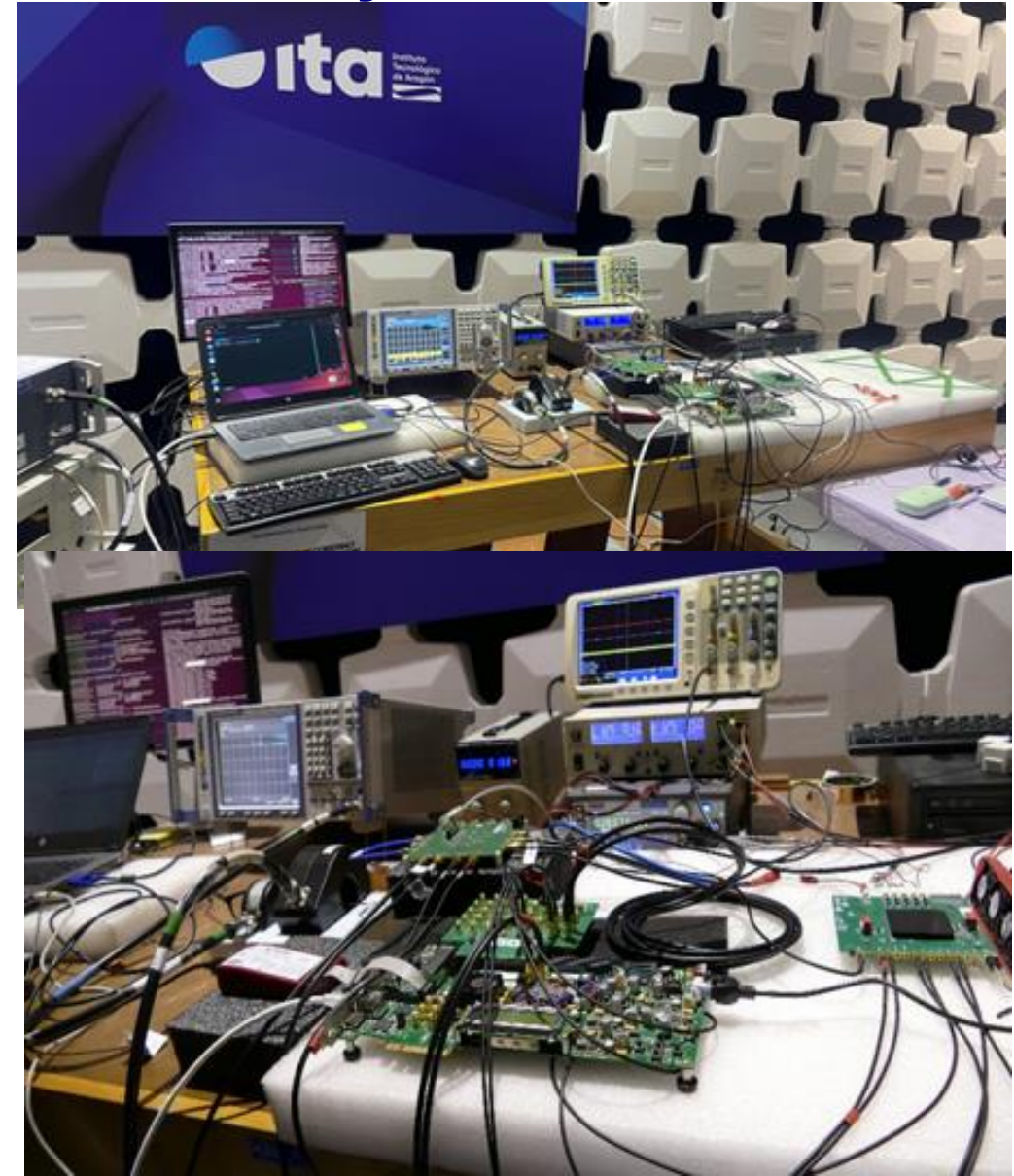
2nd Plane figure

4. WP2.O2 – Final qualification of LGAD+ETROC hybrids

- The main goal is to validate the performance of LGAD sensors + ETROC readout ASICs in final prototype form.
 - Ensure compliance with ETL technical specifications (timing resolution, radiation hardness, noise).
 - **Assess grounding, noise behavior, and overall system stability.**
 - Provide input for the transition to full module production.
- Task WP2.T2 – Qualification in test beams and irradiation campaigns
 - Test LGAD+ETROC hybrids in dedicated beam facilities (DESY, Fermilab, CERN).
 - Characterize noise, grounding, and timing performance under different radiation levels.
 - Perform irradiation campaigns before test beams to assess radiation tolerance.
 - Collaborate with ITA and CNA experts for EMC, grounding, and irradiation support.
- Activity linked to EUROLABS project - TA from FERMILAB / PORTUGAL

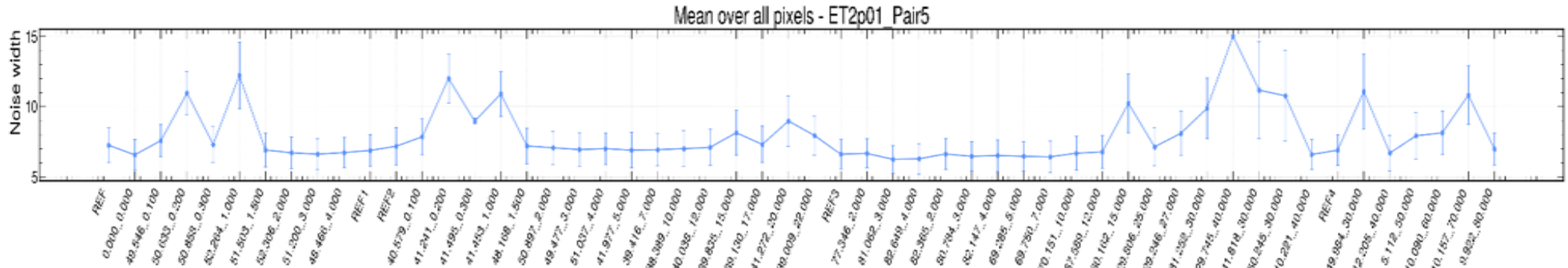
4. WP2.O2 – Final qualification of LGAD+ETROC hybrids

- EMC/noise susceptibility characterization of ETROC2 has been performed.
 - Focus on realistic operating conditions and picosecond-level timing constraints.
- Evaluation of EMI impact on:
 - Timing resolution.
 - Jitter.
 - Data integrity.
- Conducted noise injected into different ETROC test-board coupling ports.
 - Frequency range covered: 100 kHz – 100 MHz.
- Tests performed at the ITA EMC laboratory



4. WP2.O2 – Final qualification of LGAD+ETROC hybrids

- Preliminary results shows that the Noise response strongly depends on the injection point.
- Most critical coupling paths identified: VDDA and VDDD power lines & Clock inputs.
- Noise width and baseline fluctuations increase with injected noise amplitude and frequency.



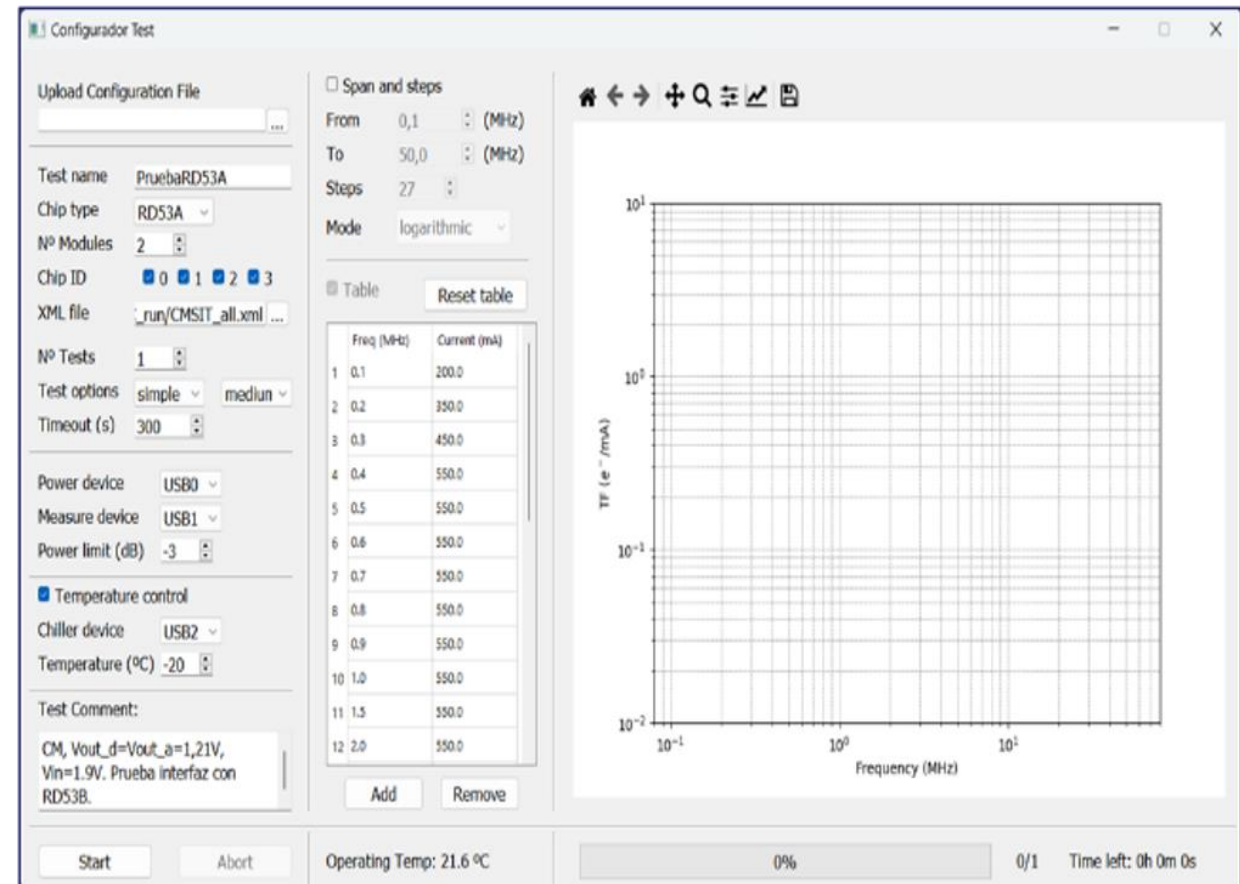
- The measurements confirm the sensitivity of the analog front-end to conducted noise.
- Measurable noise propagation has been observed through the power distribution network.
- These effects may compromise supply stability and the locking performance of the internal ETROC2 PLL.
- A detailed analysis of the complete dataset is still pending and has been assigned to Jordi.

5. WP5.O2 – Upgrade of the EMC laboratory for ECFA DRD activities

- The main goal is enhance EMC test capabilities to support detector electronics development.
- Improve automatic Transfer Function (TF) measurement system for detectors FEE
- Extend testing capacity for power supplies in radiation environments.
- Provide robust EMC support for DRD3 and DRD7 detector R&D.
- One task has been planned (WP5.T2) focused on the improvement of EMC test systems
 - Upgrade the automatic TF noise measurement system with improved GUI and cold box.
 - Refine the portable bench for conducted noise emission tests of power supplies in irradiation facilities.
 - Ensure compatibility with multiple radiation labs (CNA and others).
 - Collaboration between CNA and ITA to design and validate robust test setups.

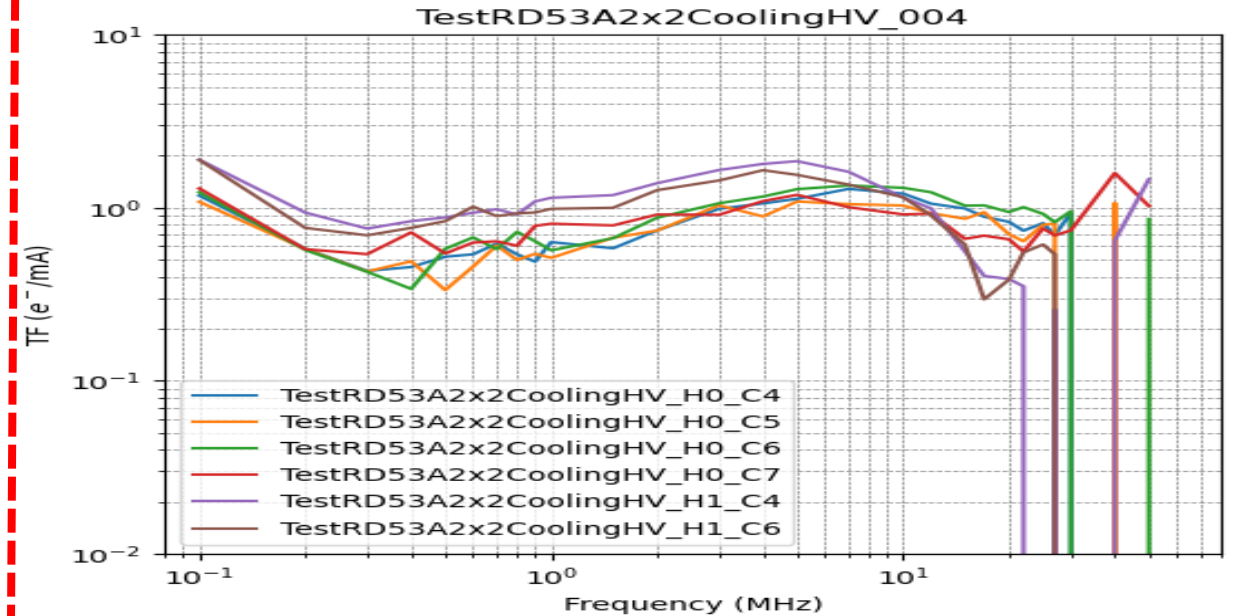
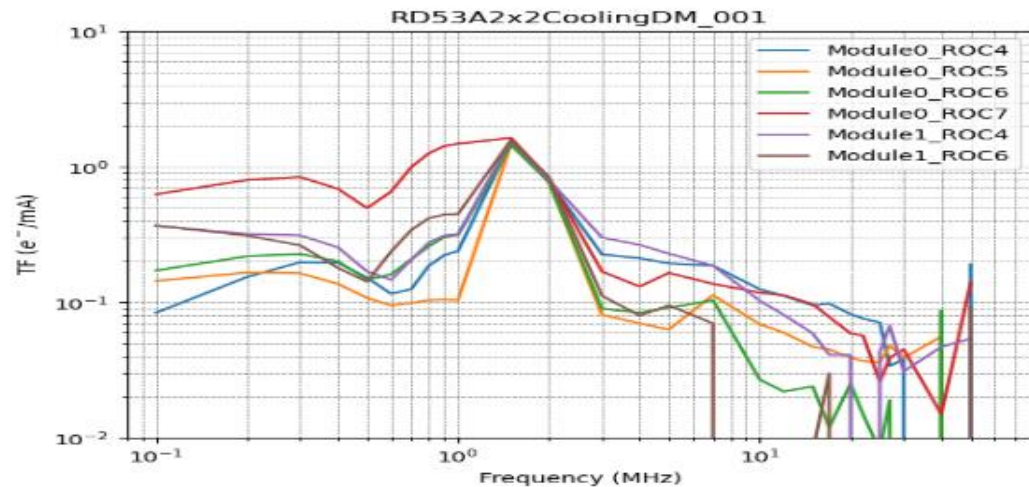
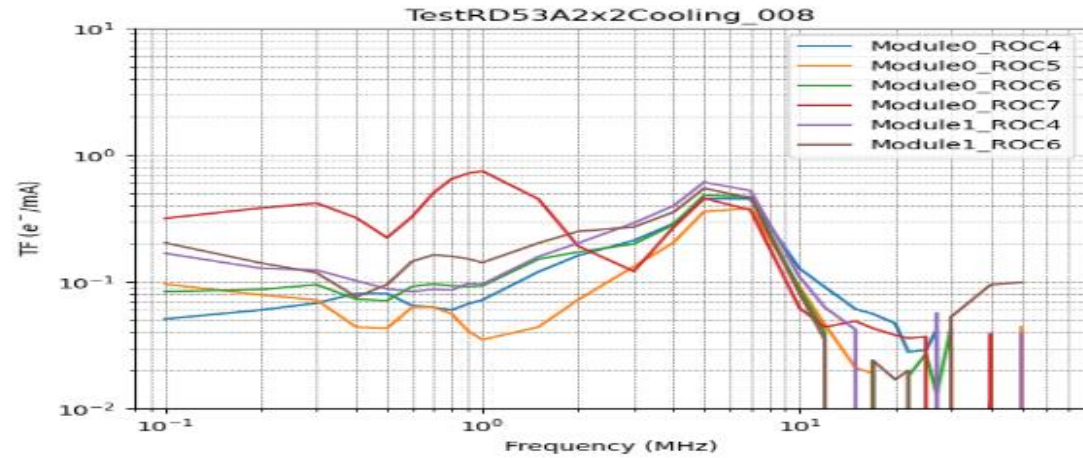
5. WP5.O2 – Upgrade of the EMC laboratory for ECFA DRD activities

- The first activity has been focused on the upgrade the automatic TF noise measurement system with improved GUI and cold box is totally operational



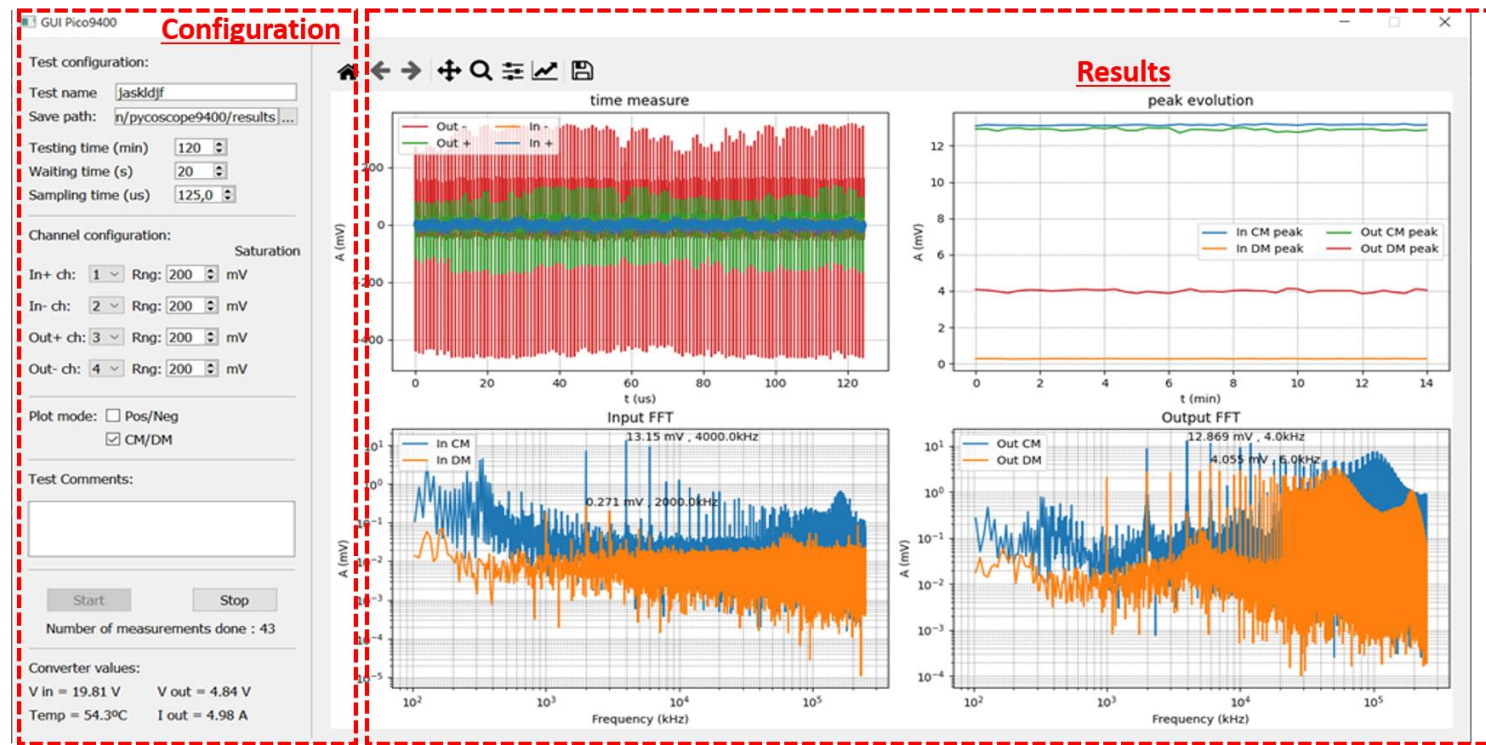
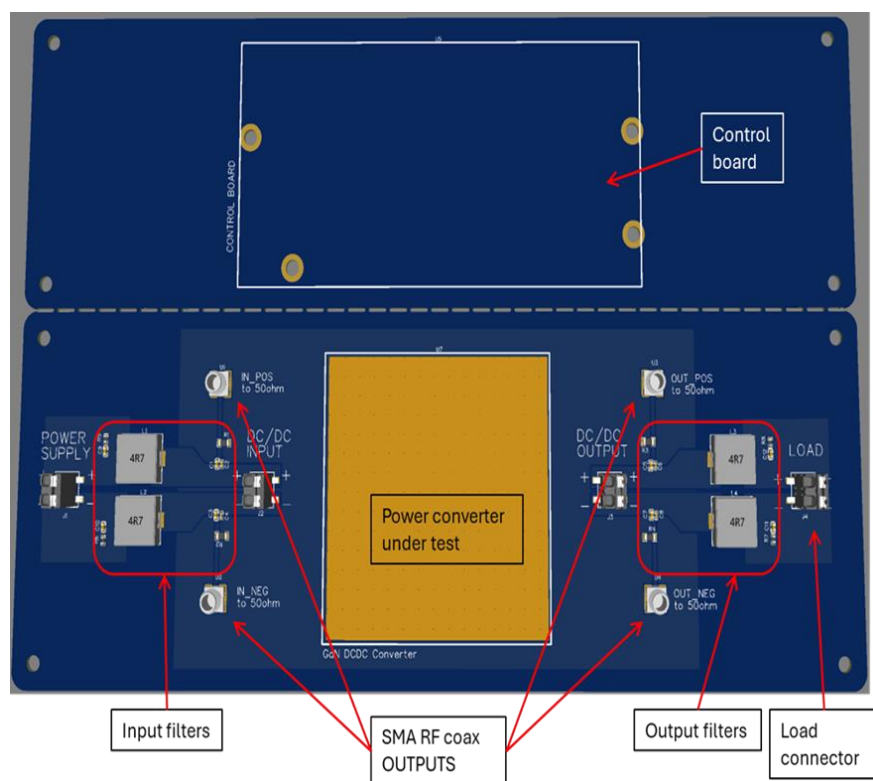
5. WP5.O2 – Upgrade of the EMC laboratory for ECFA DRD activities

- Both systems have been validated by testing a serial chain of two prototype of tracker barrel pixel modules with (2x2) RD53A readout chips (2x2 TBPX RD53A modules) with planar sensors



5. WP5.O2 – Upgrade of the EMC laboratory for ECFA DRD activities

- The second activity has been focused on the development of a customized portable test bench, designed to perform in-situ conducted EMC emission measurements of power supplies in IRRAD configurations.
- The system has been developed and tested. – IPHC – We will repeat the test at CNA



5. WP5.O2 – Upgrade of the EMC laboratory for ECFA DRD activities

- **Future Plans** – Two main activities within the project:
- Collaboration with CNA
 - Address noise issues at CNA facilities.
 - Test and validate the EMC irradiation test bench at CNA.
- Joint development with ITA, IFCA, and CNA
 - Design RF-compatible experimental platforms.
 - Focus on low-noise, high-speed electronics optimized for pulsed signal techniques (IBIC, TPA-TCT).
 - Coordinate this work with activities planned in the OTELLO 2 project.

6. Summary

- **ITA's activities within CMSUPG2**
 - Progressing rapidly and well aligned with DRD priorities.
 - Over 90% of planned work has already been achieved and justified.
 - Strong alignment with other European and national projects has been crucial for success.
- **Future plans**
 - Development of a new GaN-based DC-DC converter. (Rad – 3 level)
 - Design of RF-compatible experimental platforms with low-noise, high-speed electronics.
 - Strengthened collaboration with CNA on EMC and irradiation test activities.



¡Thank you!