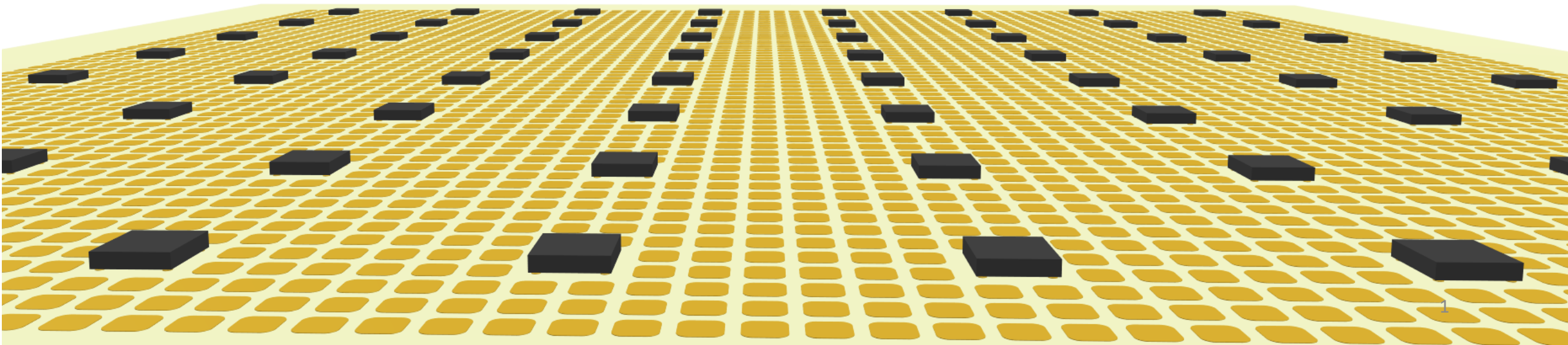
SoLAr dual light/charge anode readout

proposal for ProtoDUNE-III at CERN

Saba Parsa on behalf of the SoLAr project



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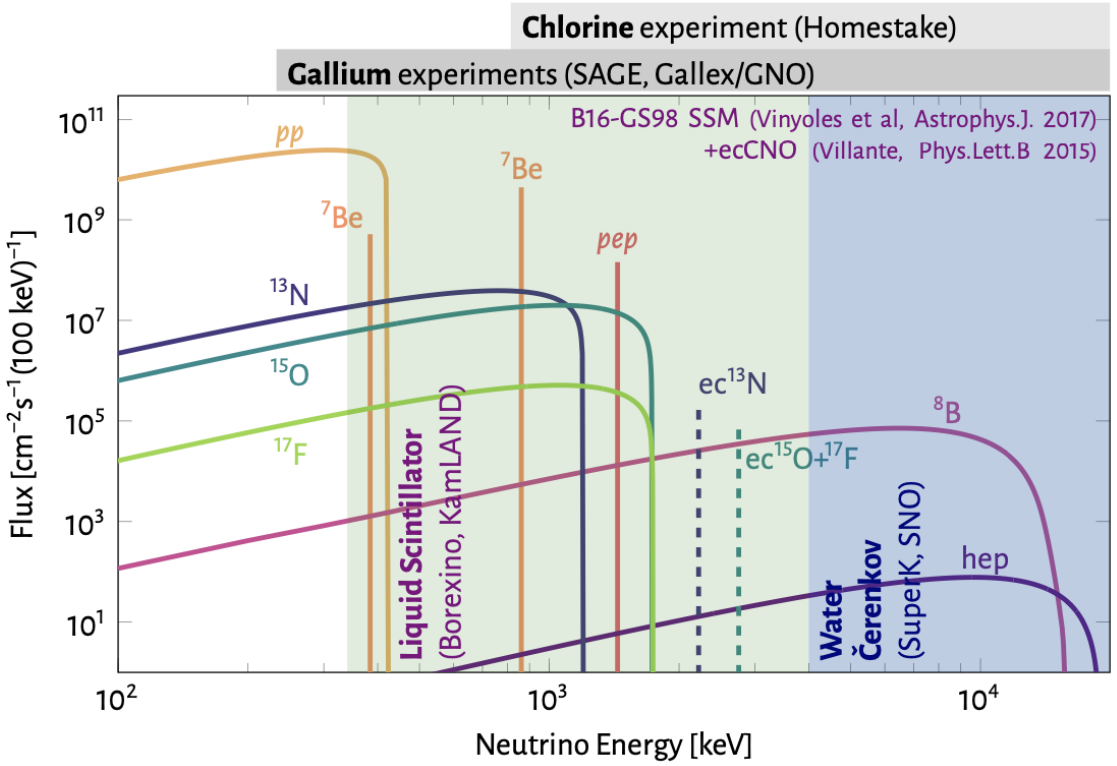
SoLAr Physics Motivation

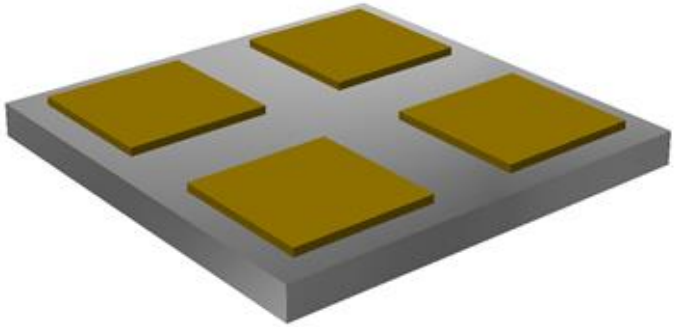
- Aim is to reach to the sensitivity for Solar hep neutrinos and other low energy physics at MeV energy scale
- Novel readout concept for LAr-TPC, to enhance the ability to identify "MeV-scale" events in space and time (online localized triggering)
- Improved calorimetry for O(MeV) signals using combined Charge/Light signals: Target $\Delta E/E \approx 7\%$

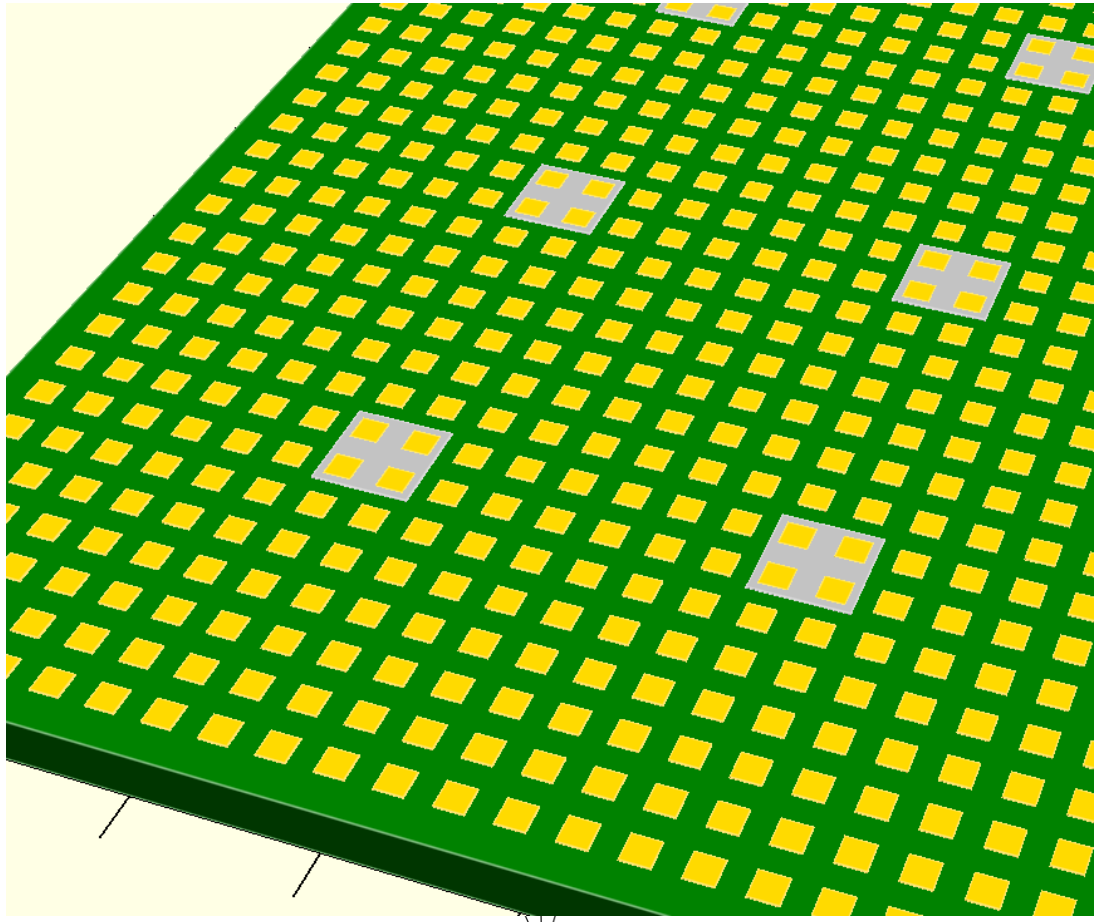


SoLAr concept

- Integration of charge/light readout on the same anode tile using pixelated charge readout and distributed array of VUV SiPMs among the charge pixel pads

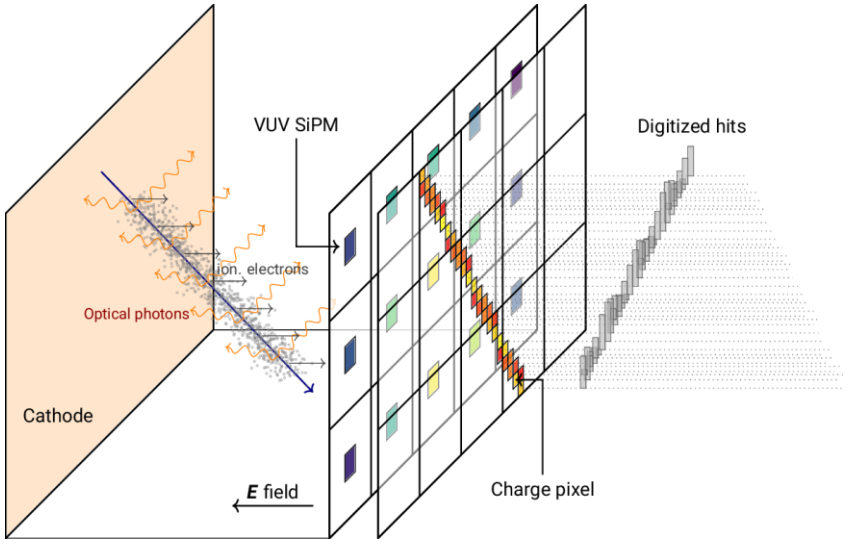
- SoLAr Cell: A modified VUV SiPM with 4 charge pads on top



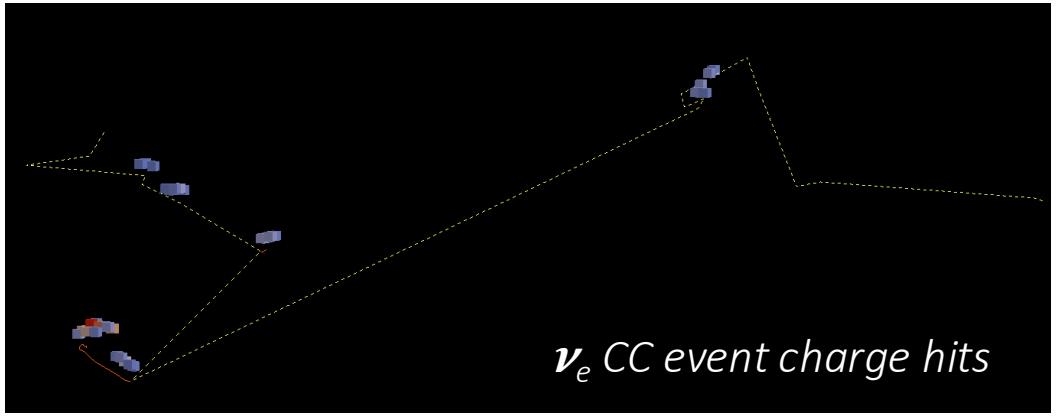


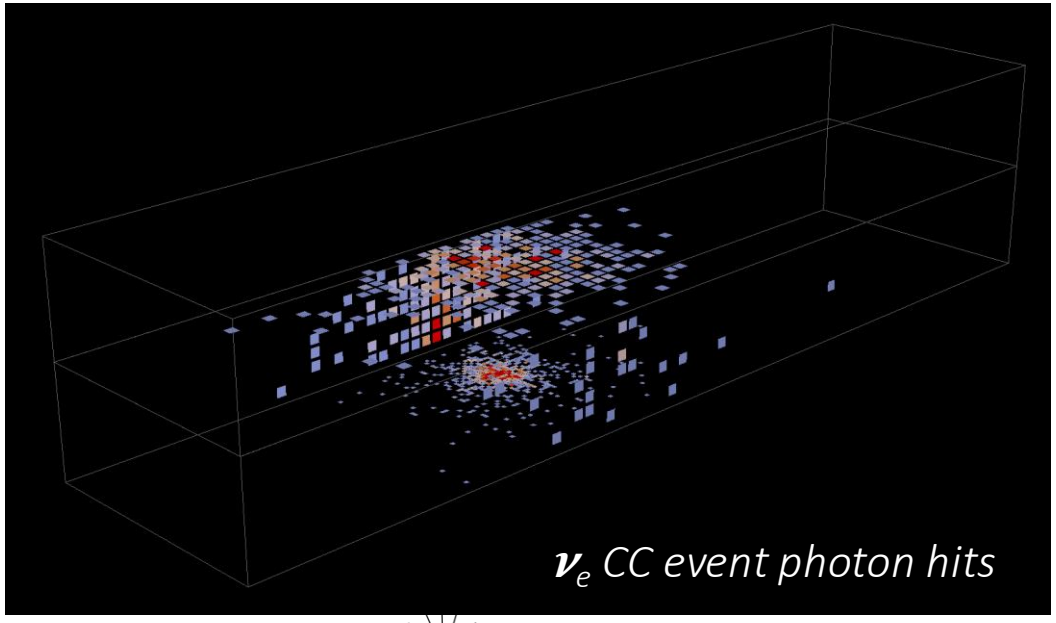
SoLAr Simulation

- Sensitivity studies for solar neutrinos in FD-4 with **solar-sim** Geant4-based simulation package
- Light-sensitive anode is particularly important for long drift TPC (VD ~ 6m)



In the context of Module of Opportunity

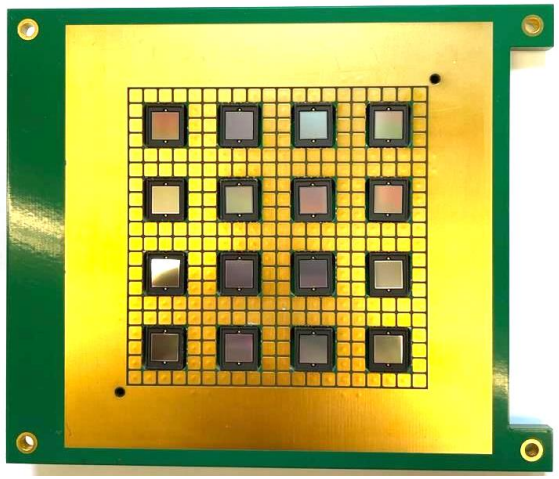


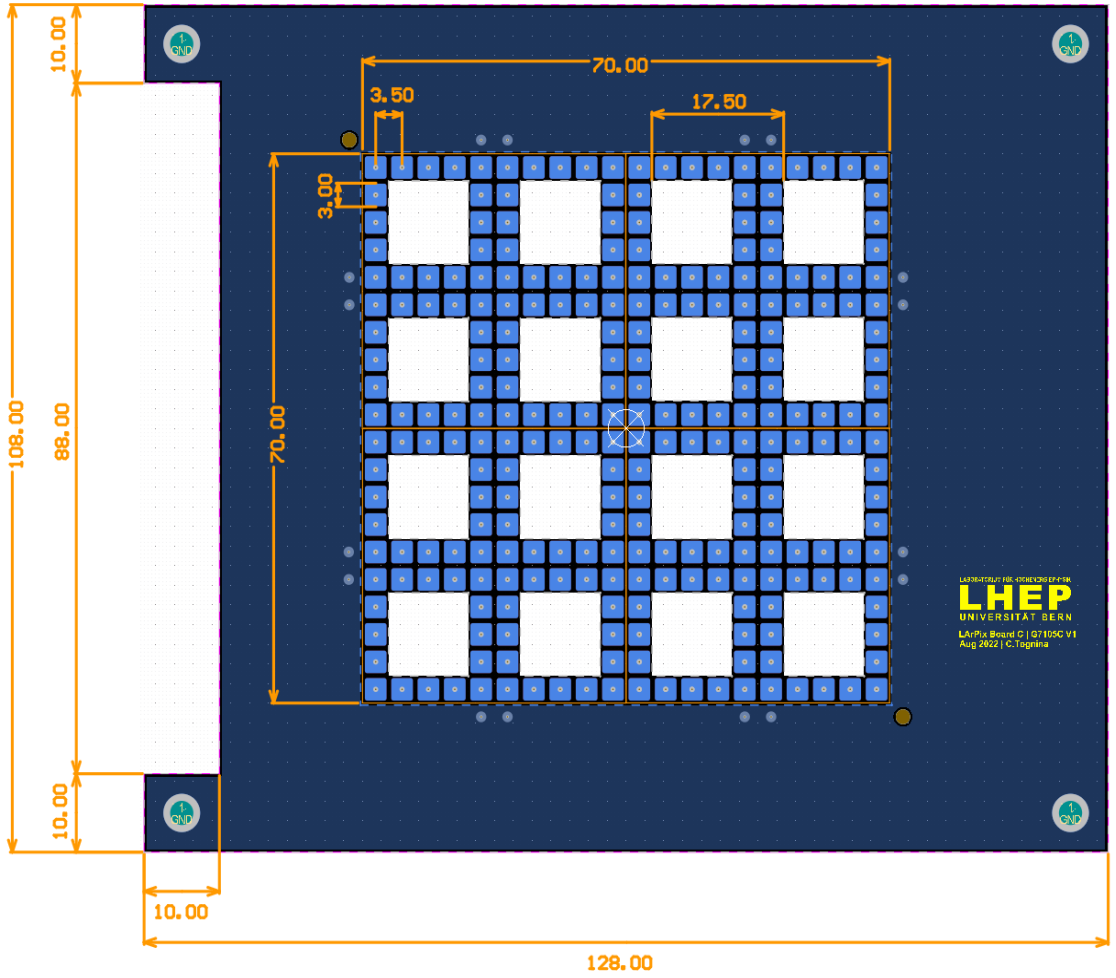


SoLAr Prototype-v1

Anode PCB design

- Charge pixel pads: 3mm
- Pixel pitch: 3.5mm
- SiPM sensitive area 6mm x 6mm
- SiPM pitch: 17.5mm
- Readout area: 70mm x 70mm





Based on LArPix-v2a

SoLAr

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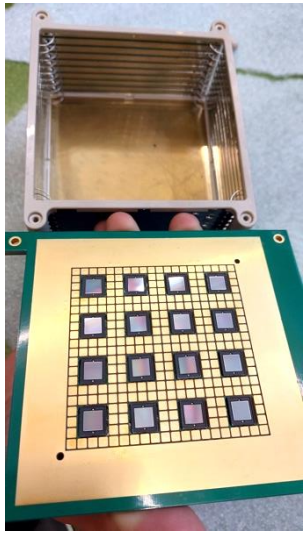
SoLAr Prototype-v1

Cosmics Test run @Bern

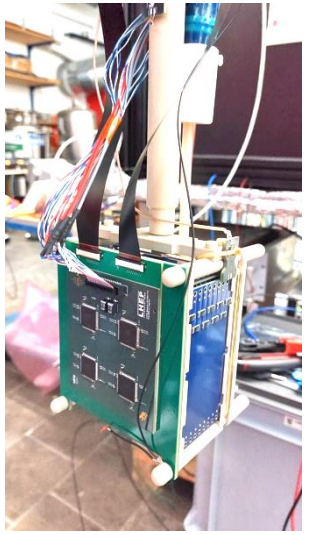
25-26 October 2022 (~24h operation)

- First demonstration of both light and charge on the same anode plane
- No interference was identified

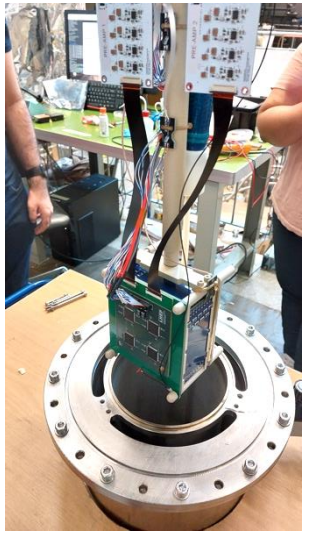
- SoLAr_v1 prototype demonstrator published in
  JINST 19 (2024) 11, P11010,
  e-Print: 2406.14121[physics.ins-det]



Inside the TPC



SoLAr-v1 TPC



Insertion into cryostat

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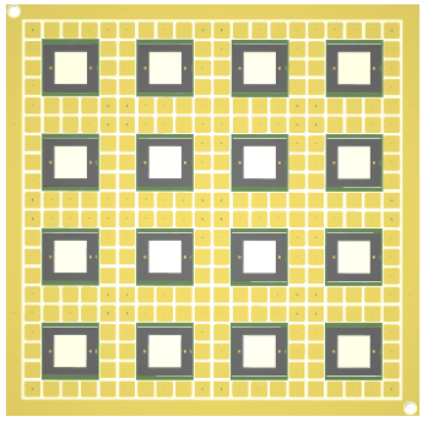
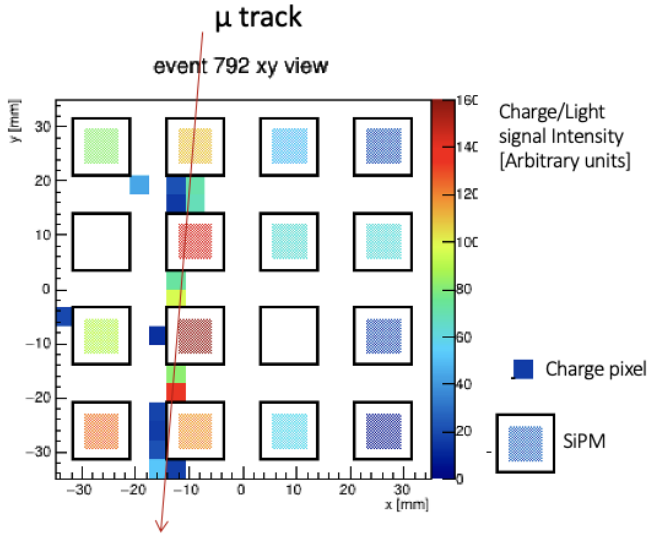
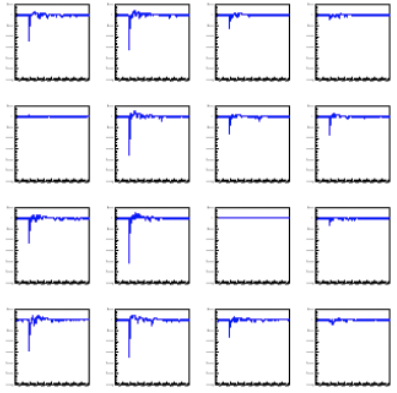
Anode plane visual guide





SiPM waveforms



JINST

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PUBLISHED: *November 13, 2024*

First demonstration of a combined light and charge pixel readout on the anode plane of a LArTPC

SoLAr

SoLAr

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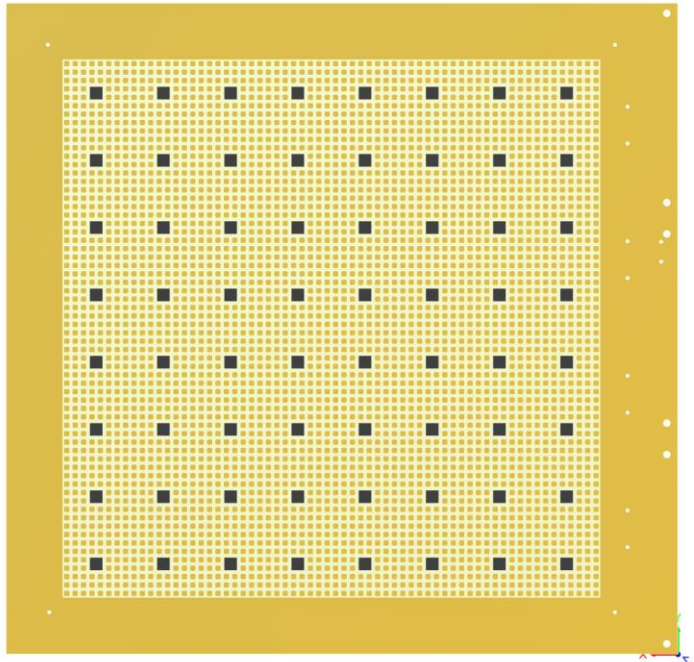
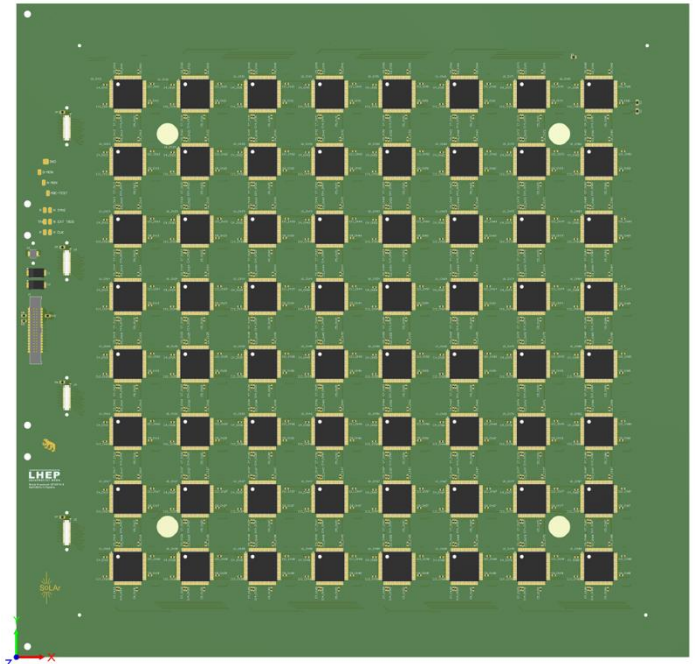
SoLAr Prototype-v2

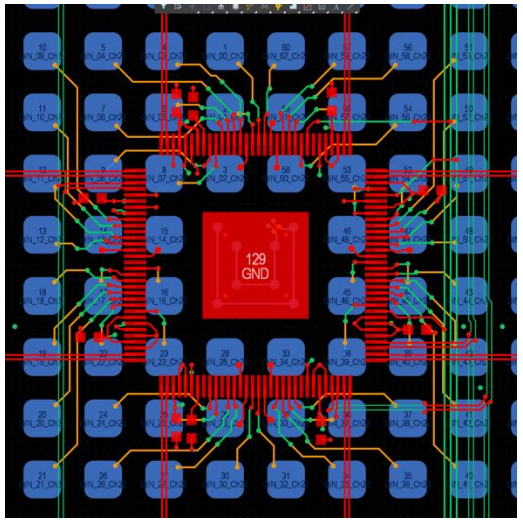
Anode PCB design

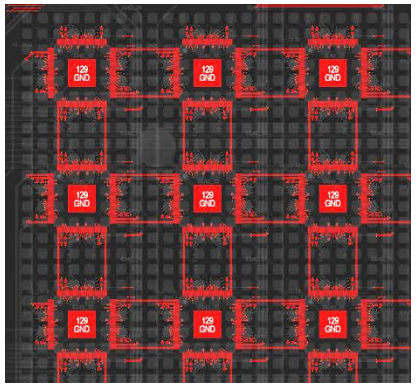
- 8-layer PCB, dimensions 31cm x 32 cm
- Divided into 8x8 regions
  - 1 region = 60 pixels + 1 SiPM
  - Pixel pitch: 4mm
- 64 LArPix (60 routed channels)
- 64 Hamamatsu VUV SiPMs
  - SMD type, 6mmx 6mm
  - SiPM pitch: 32 mm

Based on LArPix-v2b

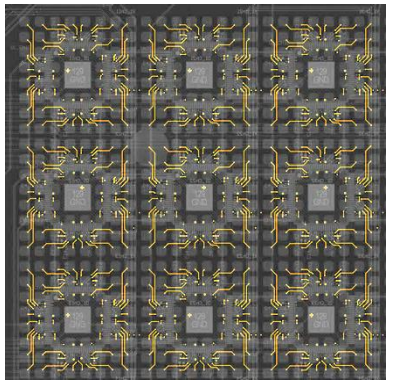




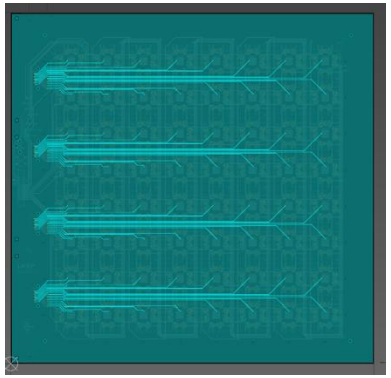




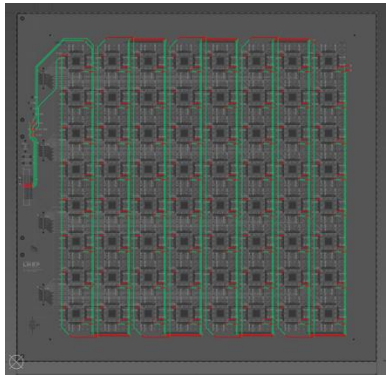
Hydra network



Pixel traces



SiPM traces



Digital traces

SoLAr

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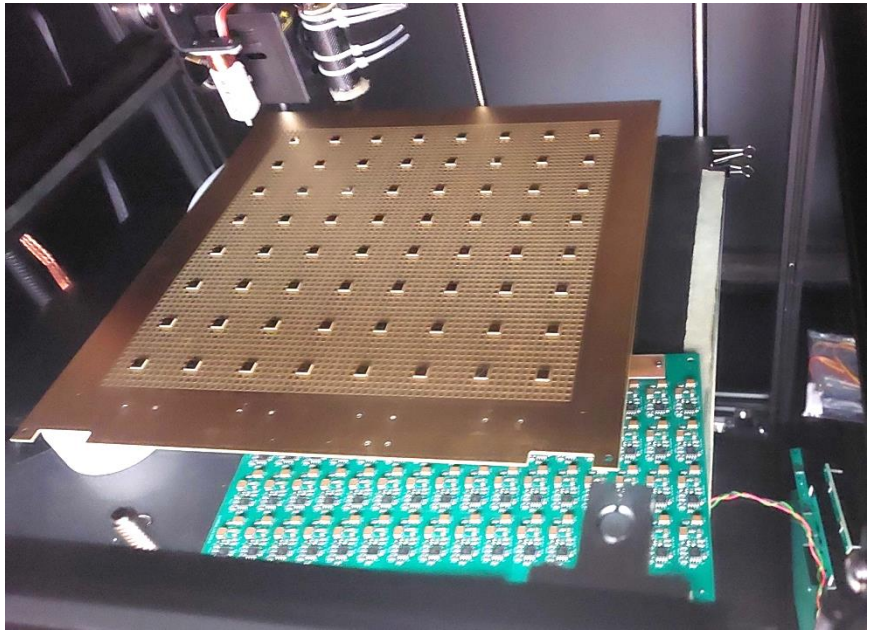
SoLAr Prototype-v2

Cosmics Test run @Bern

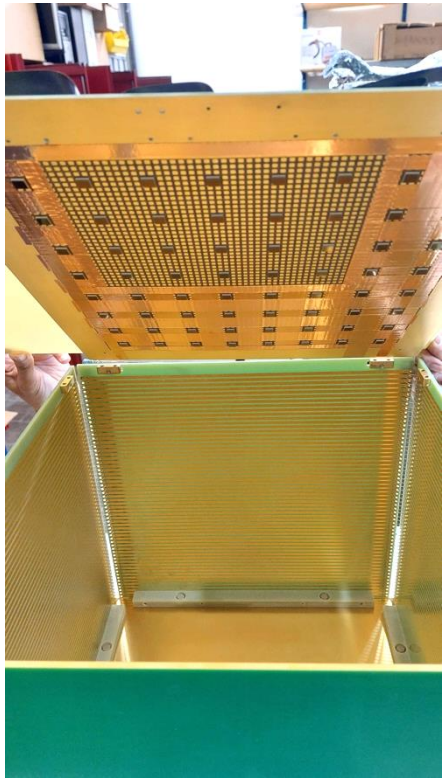
- Anode tile was populated with 64 SiPMs and 20 LArPix
- Un routed pixels were grounded with copper tape

3-10 July 2023

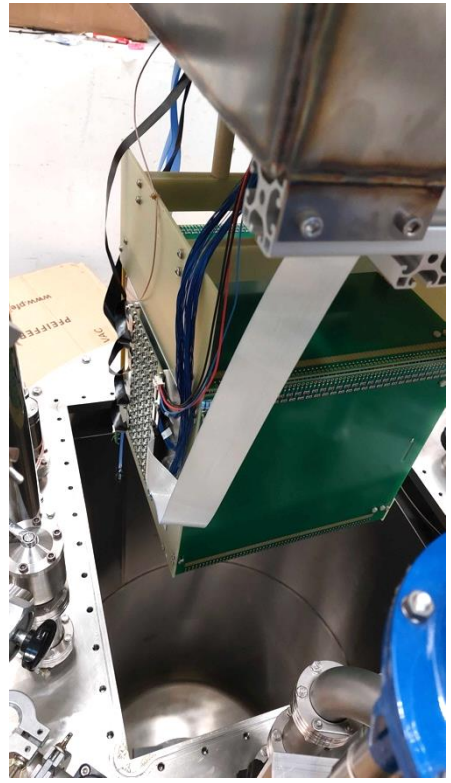
- Two days of cosmic run with nominal HV 15 kV
- Special Cobalt-60 source run



Warm SiPM test in a blackbox



Inner view of the TPC

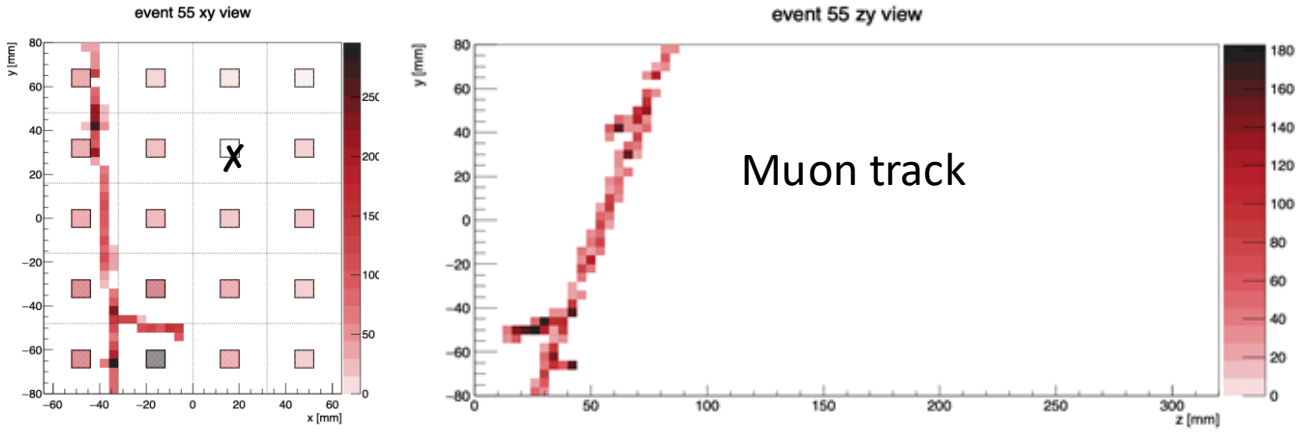


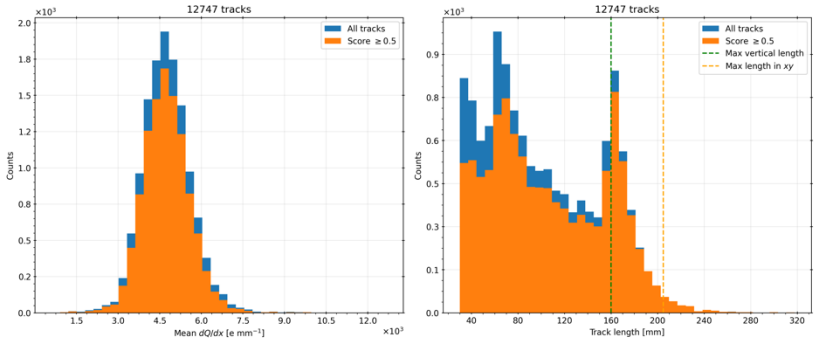
Insertion into cryostat

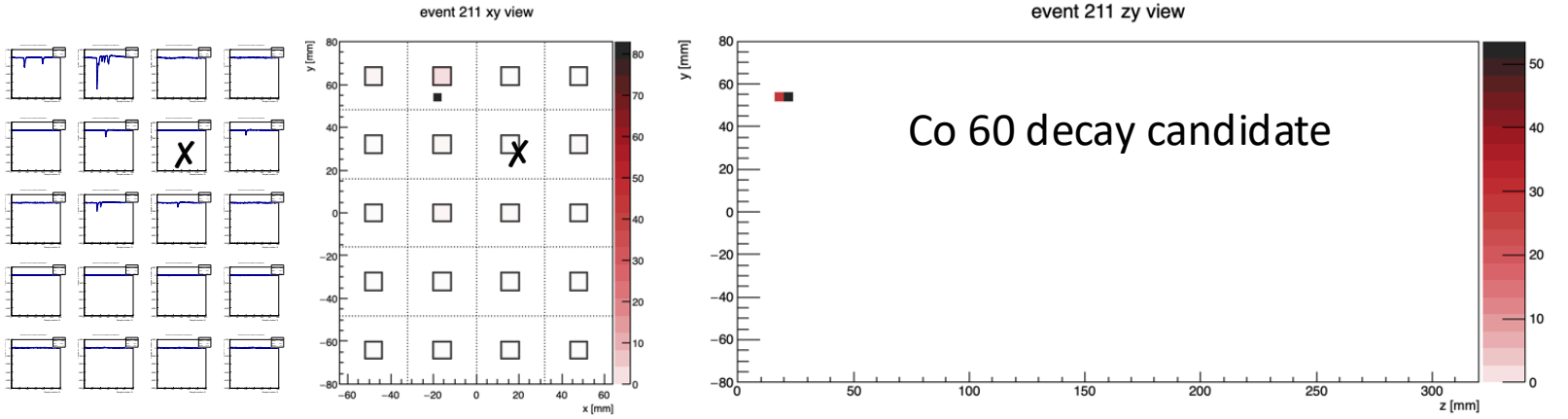
SoLAr Prototype-v2

Light and charge combined 3D display of a Cosmic muon track

- Raw event displays for a cosmic muon and a Co_{60} decay
- SoLAr-v2 paper in preparation for publication





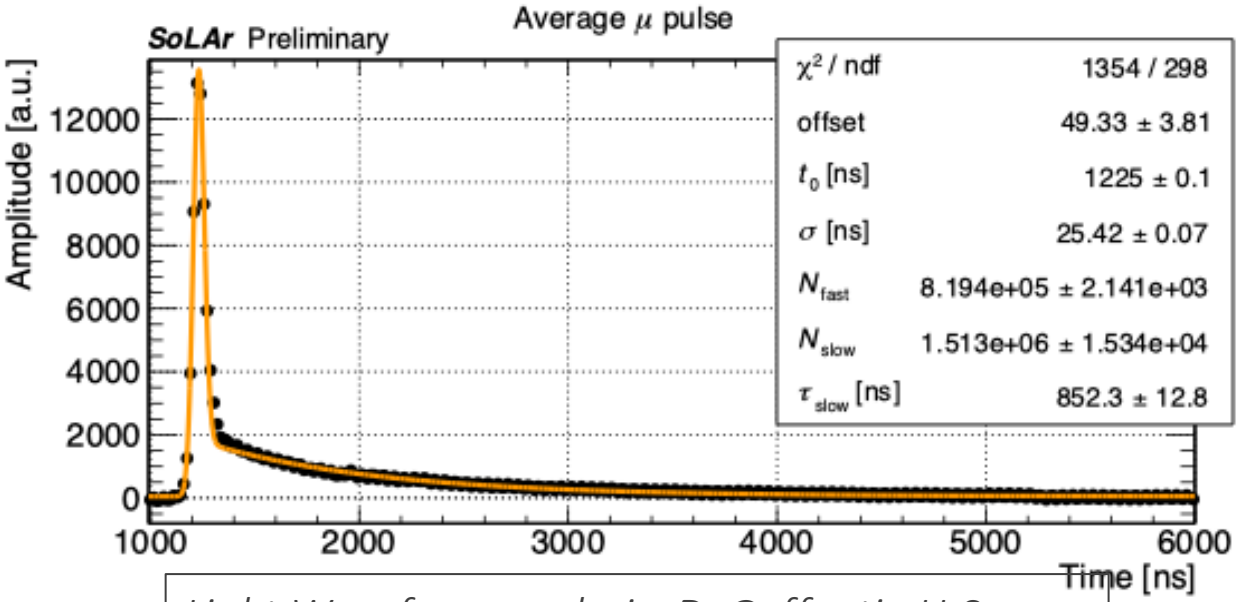


Charge analysis Guilherme Ferreira

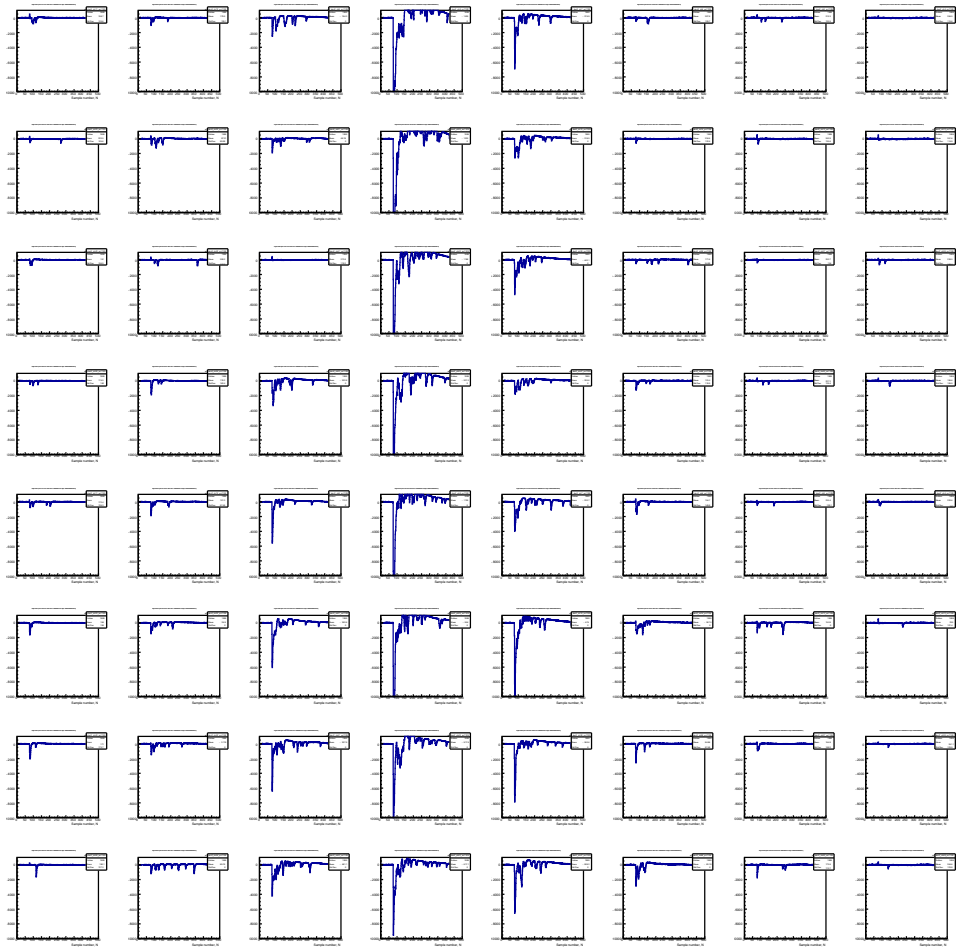
SoLAr Prototype-v2

Light waveforms

- Array of 64 SiPMs
- Full waveform readout with ADC-64 (JINR)
- Position reconstruction form light is viable
- Pulse shape discrimination is viable

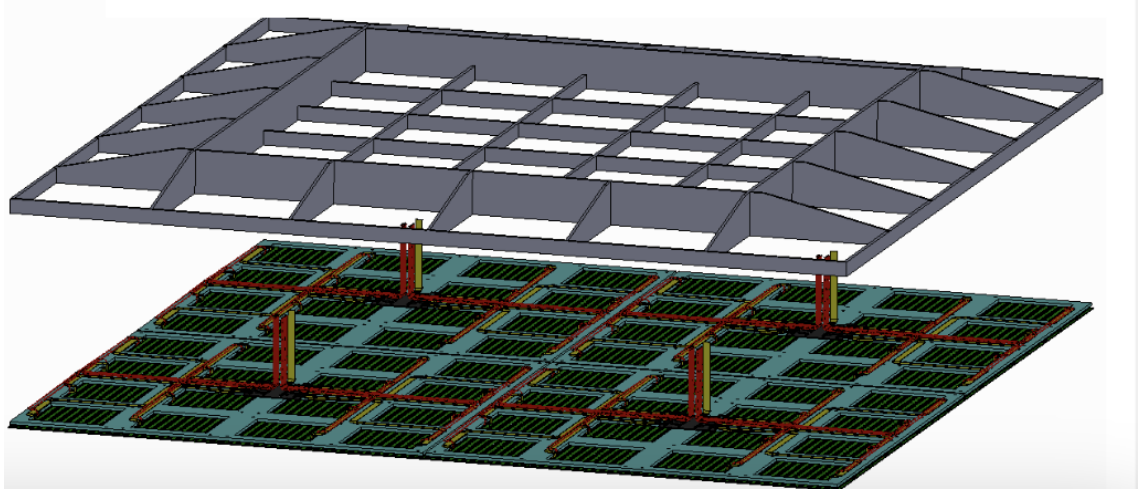


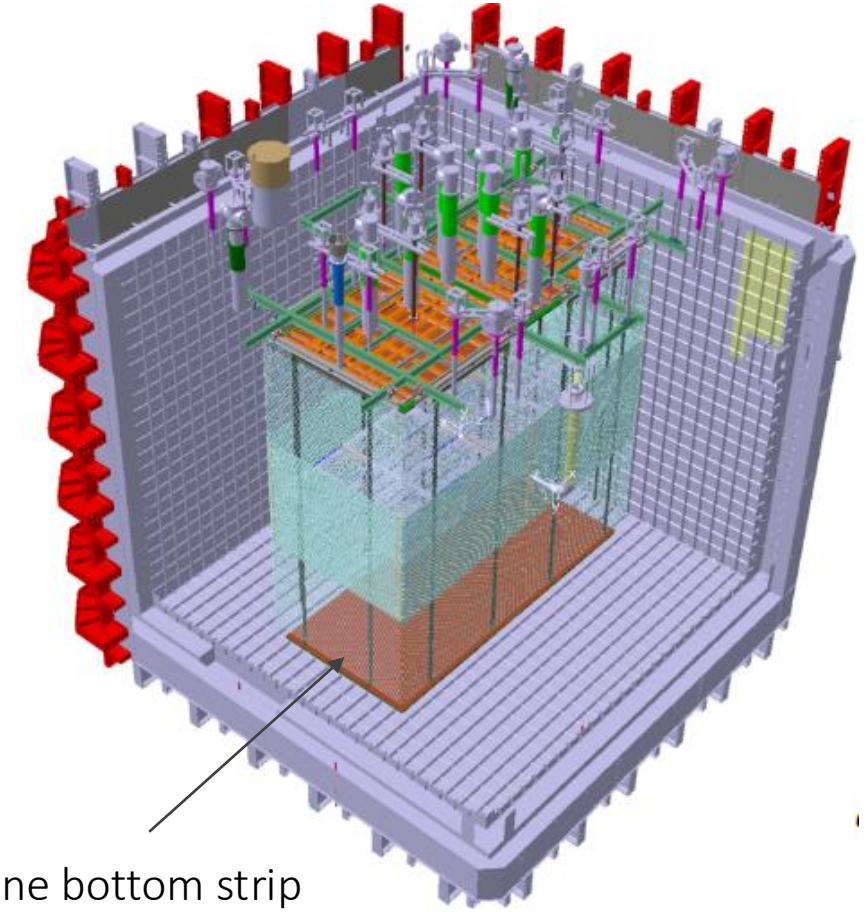
Light Waveform analysis D. Guffanti , H.Souza



Proposal for inclusion of SoLAr tiles in pixelated CRP

- Pixelated CRP is hosting 60 pixelated tiles
- Replace a few (2 to 5) of the LArPix tiles with SoLAr tiles in the planned pixelated CRP
- SoLAr tile is a modified version of a pure LArPix tile, so this is not a major alteration of the original plan
- It can be fully integrated through the same data acquisition chain.





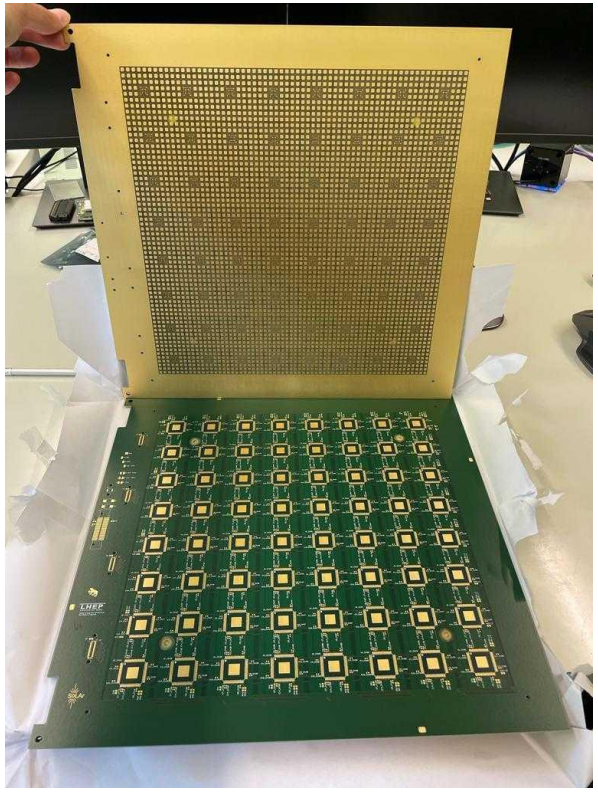
Replace one bottom strip CRP with a pixel CRP

Link to Brooke Russel talk yesterday

Redesign of SoLAr tile

- Produce larger SoLAr tiles to match the ND-LAr charge tiles: 30x48 cm
- Bern Electronics workshop can carryout the redesign with guidance from LBL
- Charge pixel readout: LArPix
- (New option) LightPix for the SiPM readout
- (Fall-back plan) Waveform digitizing, similar to SoLAr-v2 (additional feedthrough)

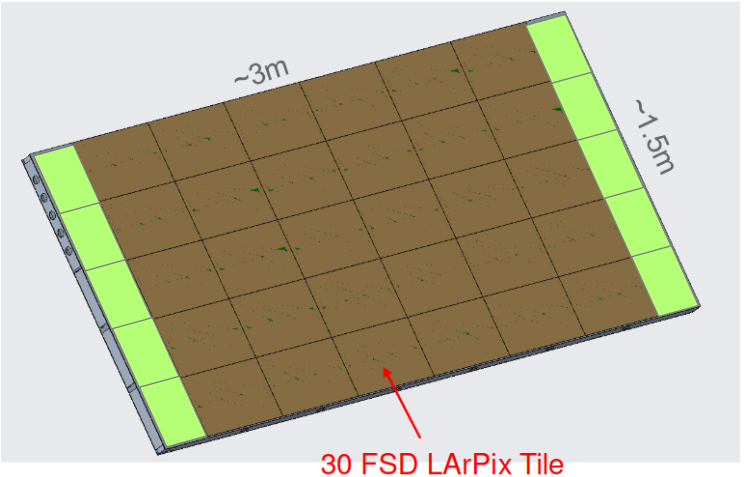
- 8-layer PCB
- Divided into 10x16 regions
  - 1 region = 60 pixels + 1 SiPM
  - Pixel pitch: 3.72 mm
- 160 LArPix (60 routed channels)
- 160 Hamamatsu VUV SiPMs
  - SMD type, 6mmx 6mm
  - SiPM pitch: 30 mm

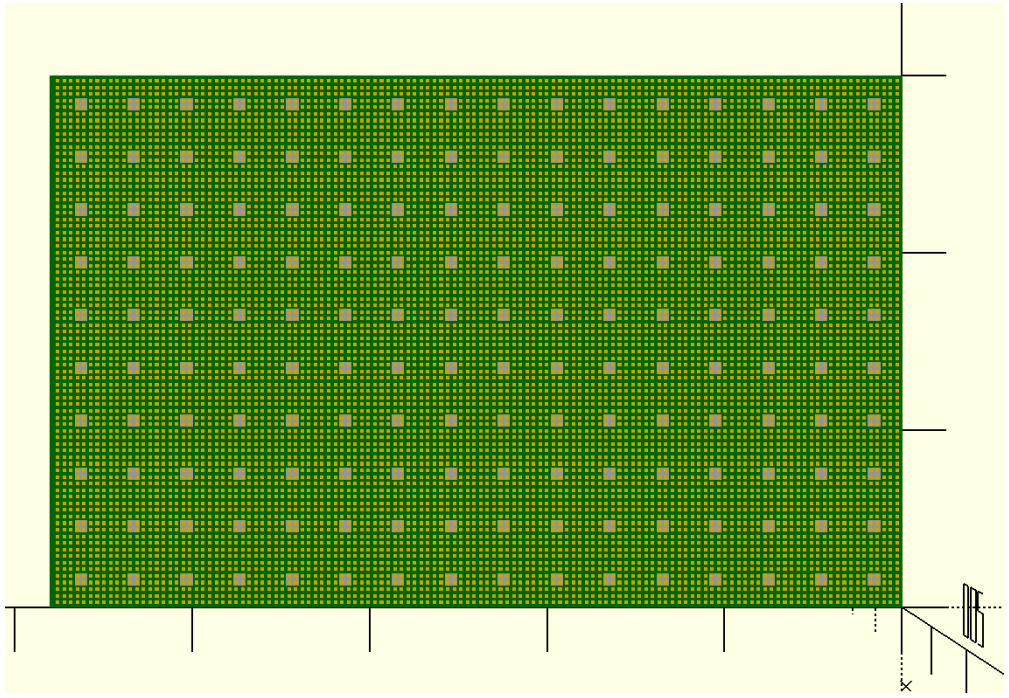


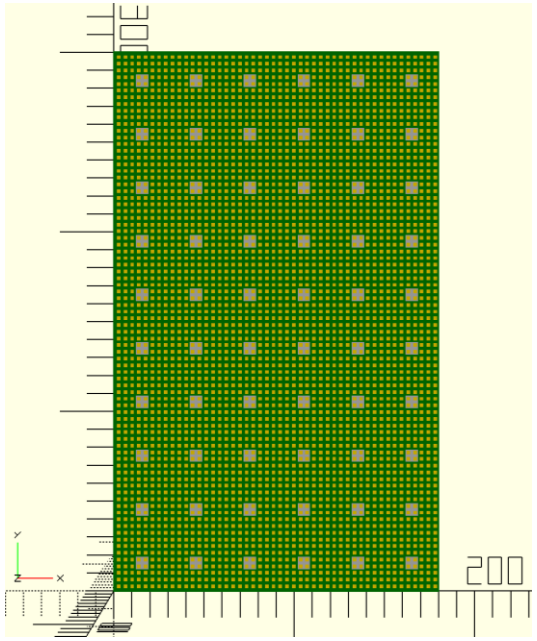
- With LightPix we can have digitized light intensity, but we won't be able to record the entire waveform

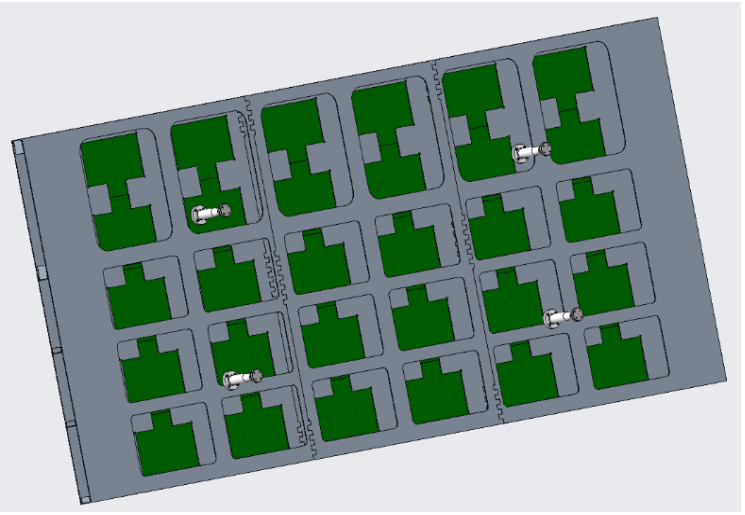
Tile Layout scheme

- Option 1: Replacing a few of the LArPix tiles: 30cmx48cm
- Option 2: Covering the side edges of the pixelated CRP panel: 30cmx18cm (20 slots available)
  - Concerns about uniformity of the E field
  - Concerns about proximity to the APEX modules and PTP re-emission





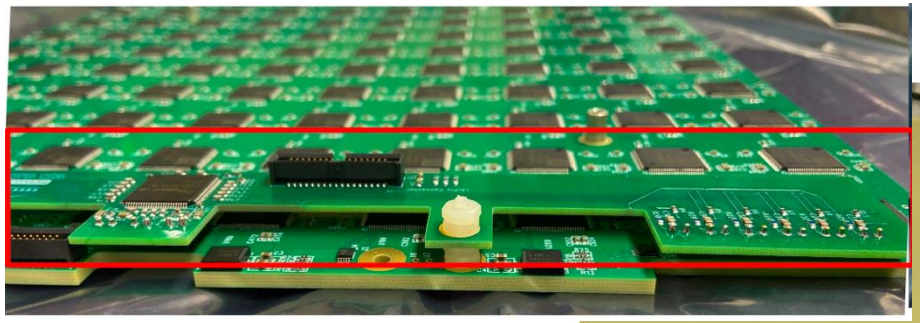


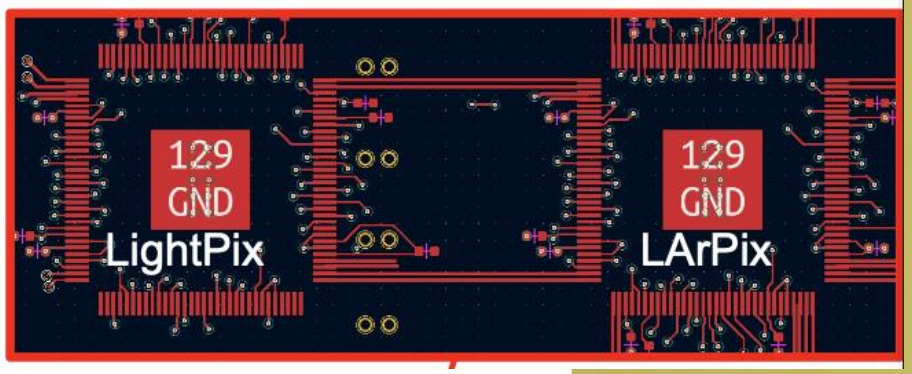


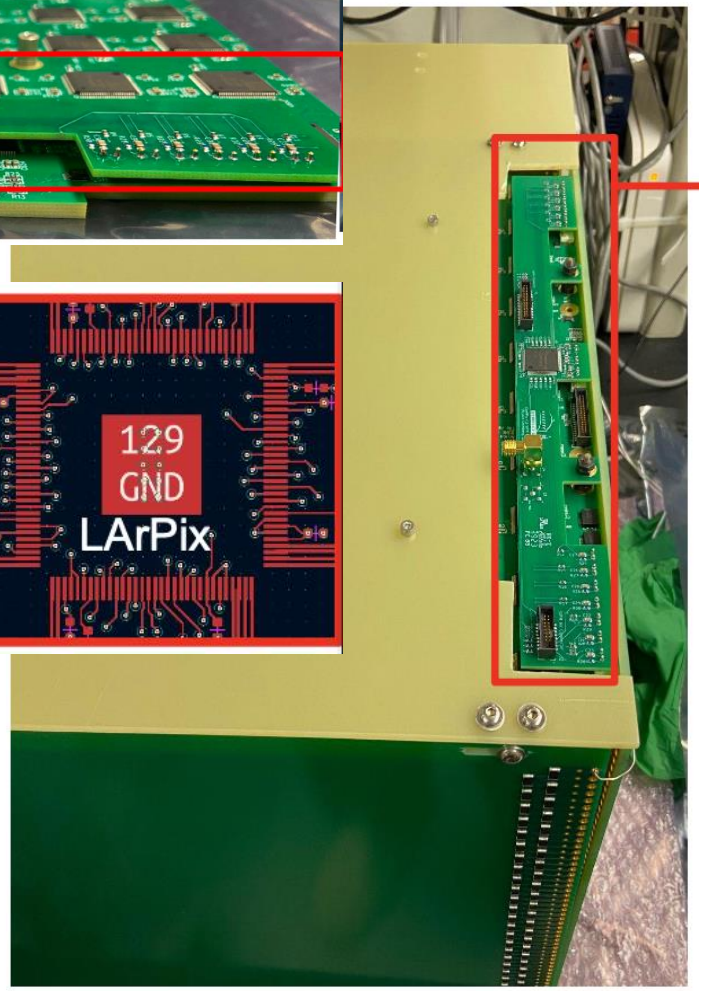
LightPix for SiPM readout

Stephen Greenberg

- Cryo compatible ASIC, digitize SiPM signal in cold
- Suitable for high channel counts, 32 channel per chip
- TDC with ns precision
- LArPix+LightPix: shared power/IO/single cable
- LightPix-v3 received Nov 2024







Setup at LBL with LightPix-v1

[Link](#) to Stephen Greenberg LightPix talk in pixel workshop

SoLAr Prototype-v3

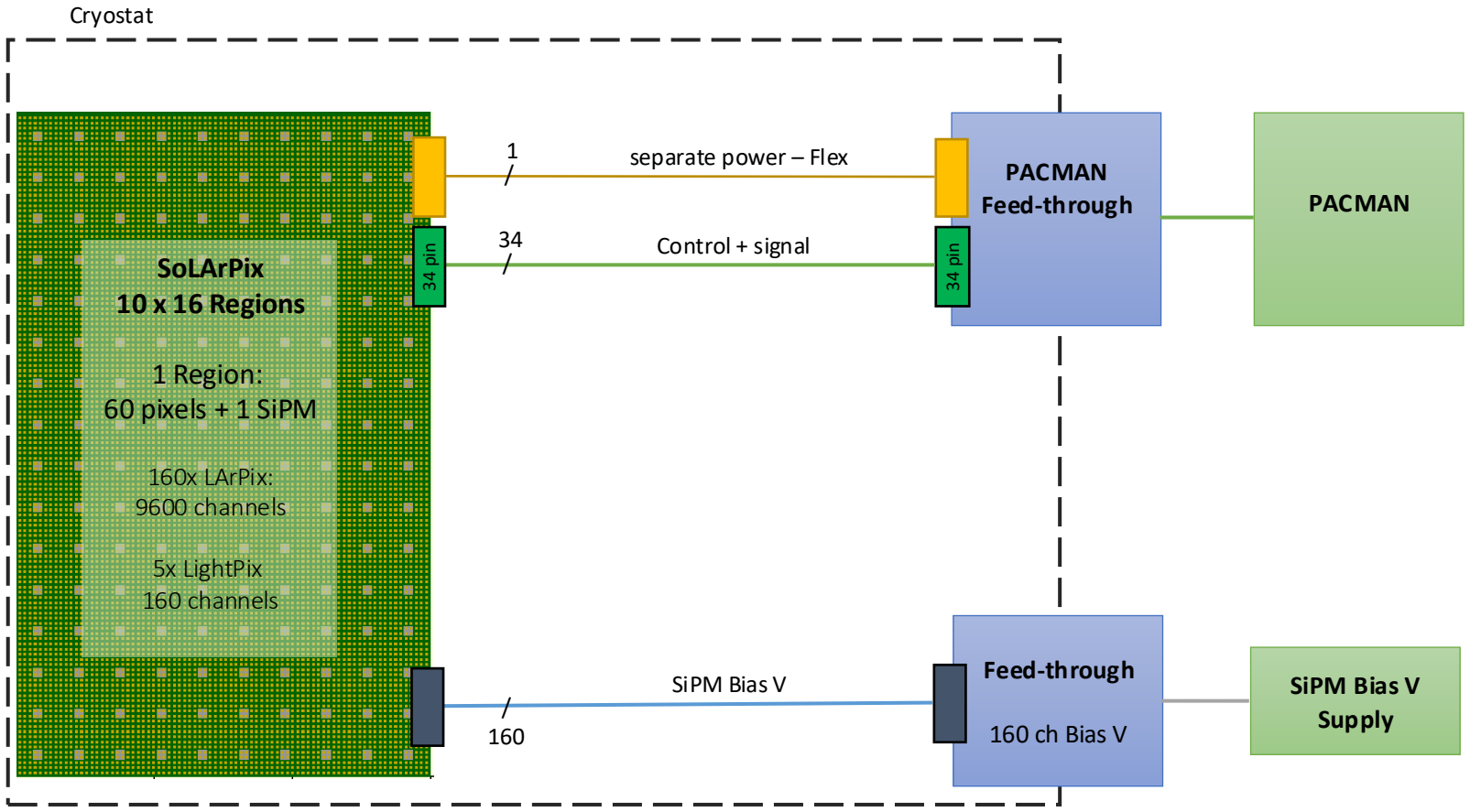
Readout scheme

Charge readout: LArPix-v3

Light readout: VUV SiPM+ LightPix-v3

- Daisy chain LightPix to LArPix
- Shared data and power cable
- Readout with one PACMAN

- Continuous Self-triggering ~ 100% live
- Low power, low noise



What is the goal of the test in ProtoDUNE-III

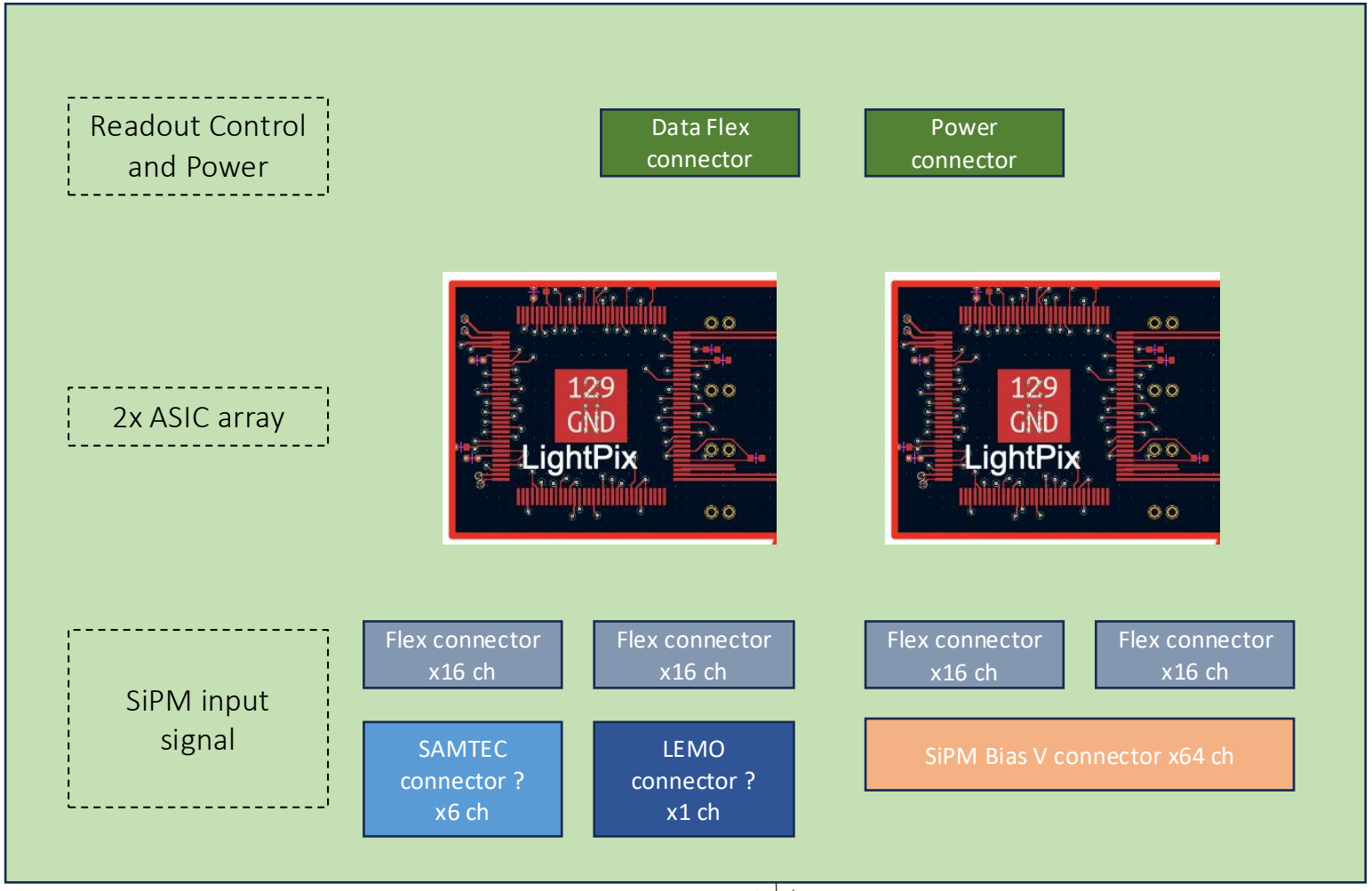
- The original goals for a technical demonstration of pixelated CRP [Brooke Russel talk]

- Test LArPix/LightPix combined readout on the SoLAr tile (A step forward from SoLAr-v2)
- Compare tracking performance of the SoLAr tile with purely LArPix tiles in the same setup
- Assess the optical gain from the SiPMs on the Anode vs depth (max tested depth was 30 cm)
- Testing the "cohabitation" of VUV SiPMs and other optical detectors using pTP or other shifters

Test PCB for LightPix ASIC

Which connectors do we need on the PCB for SiPM input signal?

- Single VUV SiPM board without preamplification? For initial development of control scripts at MIT
- SoLAr-v2 VUV SiPMs x64 For full test of all channels in warm and cold characteristic studies



Input from Stephen

Hi Stephen,
We are planing to produce a LightPix test PCB for SoLAr purposes. Brooke suggested that I check with you about PCB design features, probe points, trace to SiPM input, analog monitor access, digital monitor access, charge injection circuit, etc.
Any suggestions that you might have.
I thought to have a minimum of two LightPix to also verify chip to chip links.
And a single sipm board for early checks. How did you inject signal in first test? was you SiPM mounted on the same PCB as the LightPix?

Hey Saba, we have done this a few different ways. We have made seperate ASIC/SiPM boards in the past, and we have also mounted the SiPMs directly on the same board. I think this mostly comes down to geometric constraints.

I think digital monitor access is very important, the analog monitor is not quite as useful on this version of the chip because it doesn't actually monitor the signal that the front end sees

The ability to inject charge directly into some channels will be very useful understanding timing, I think. We have done this already with this version of the chip, but it may also be something you are interested in doing.

Note that for this version of the ASIC, we have already:

1.Shown that the TDC is very linear and is capable of <0.5ns timing resolution with a charge injection input

2.Shown that the ADC has O(~10 PE) range, and we can do very well in resolving individual PE peaks and spectra.

I think the biggest outstanding thing that still needs to be done is combining these measurements, and showing what the timing resolution is for a real SiPM signal. I am not sure what the best way to do this is--presumably a very fast LED pulsing circuit and several SiPMs would suffice for that.

Let me know if there are any other specific questions about any of this!

we hooked up the sipms in the same way, with the AC coupling capacitor C2=150pF. But there is no in-line resistor (i.e. R7=0), and we use R11=500 Ohms

SoLAr Prototype-v2 + LightPix

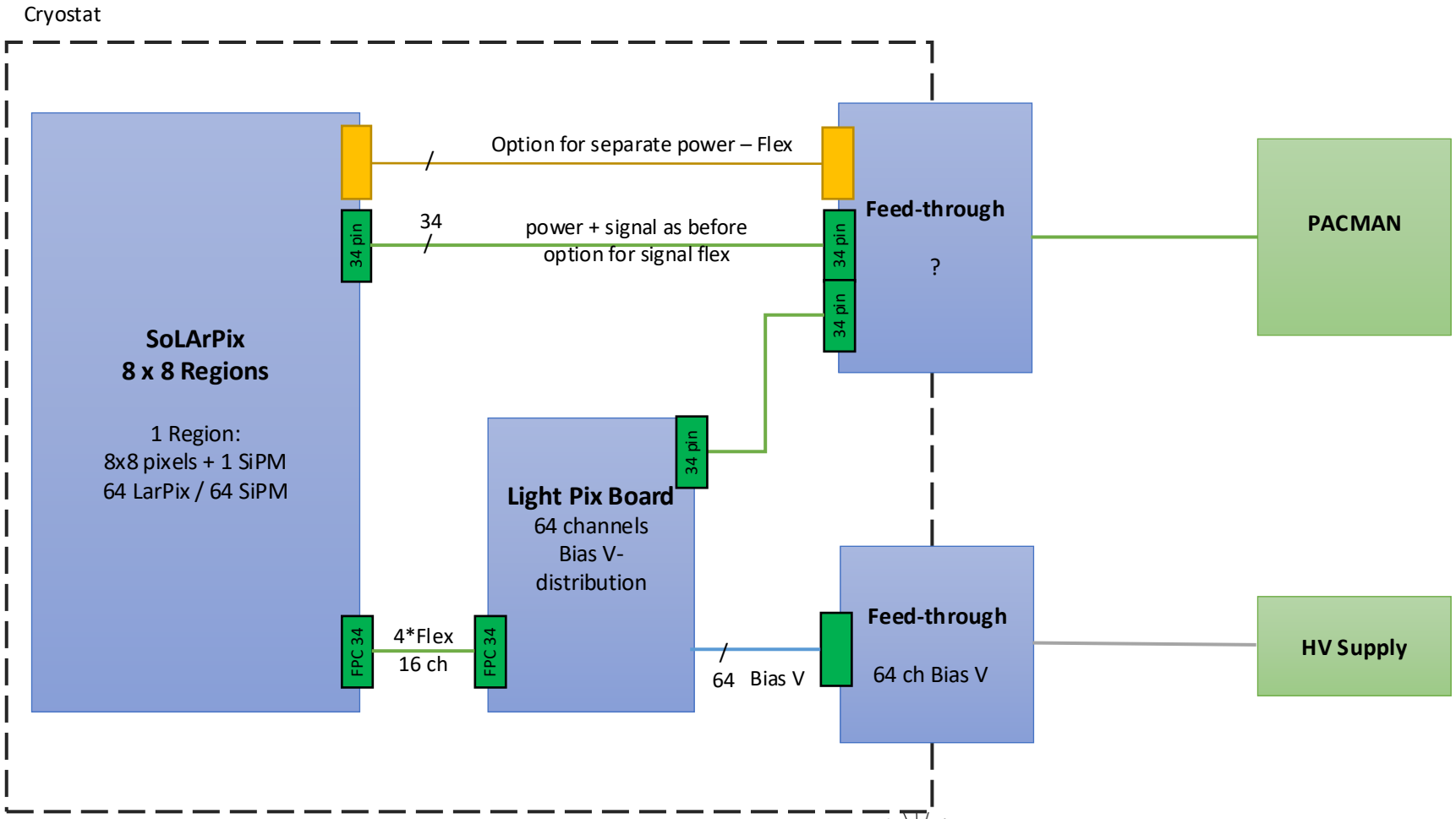
Readout scheme

Charge readout: LArPix-v2b + PACMAN

Light readout: VUV SiPM+ LightPix-v3 + PACMAN

SiPM Bias scheme:

- Continuous Self-triggering ~ 100% live
- Low power, low noise
- Modest data volume ~ 1MB/s per m^2 anode for charge

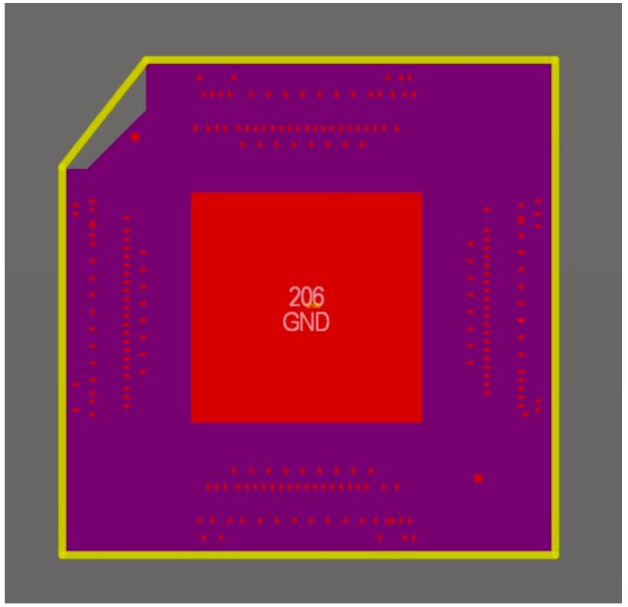


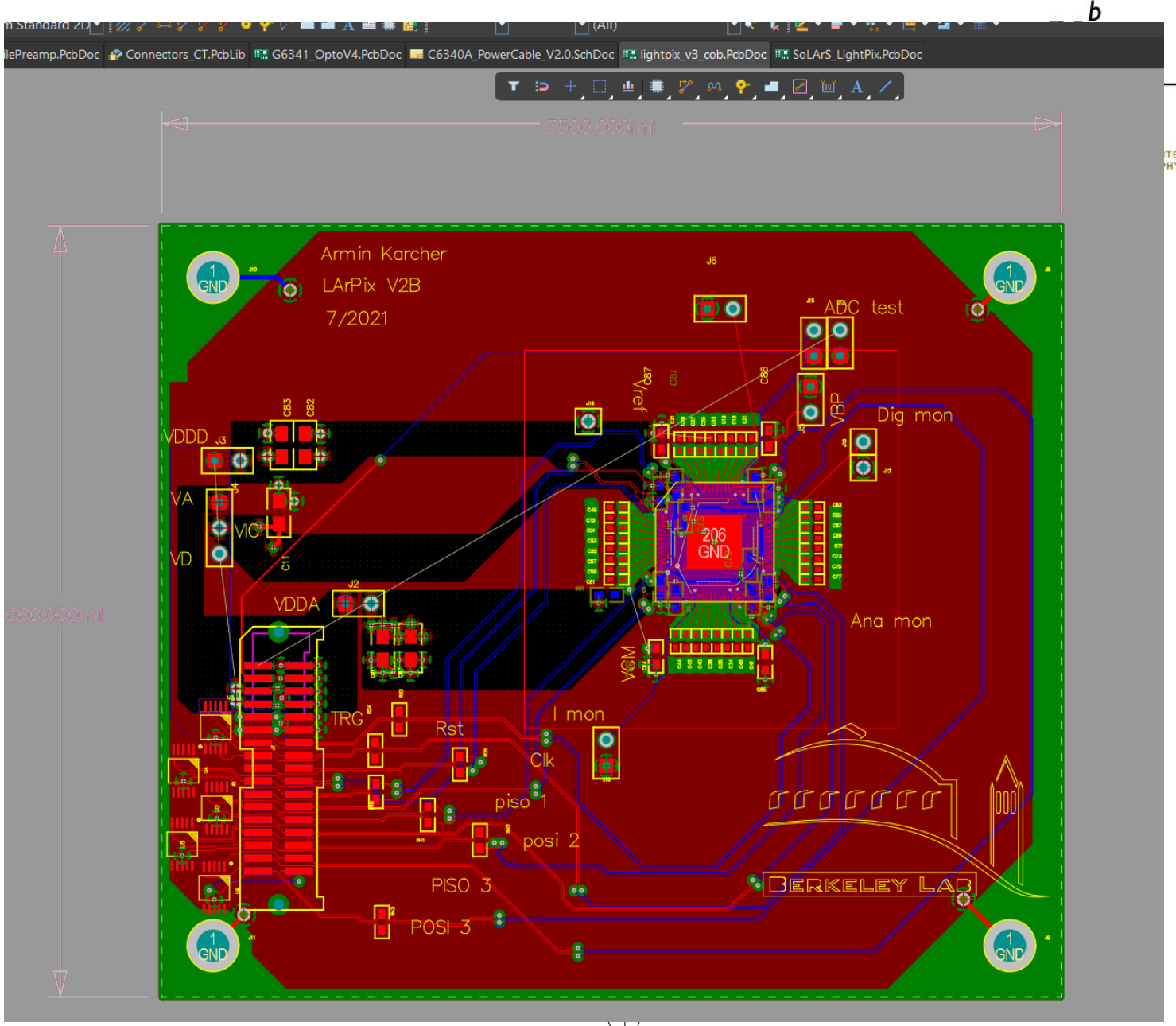
Pinout and wirebonding

From Armin Karcher

LightPix-v3_cob.PcbDoc

* Inside the file it says LArPix V2B. Double check it with Armin

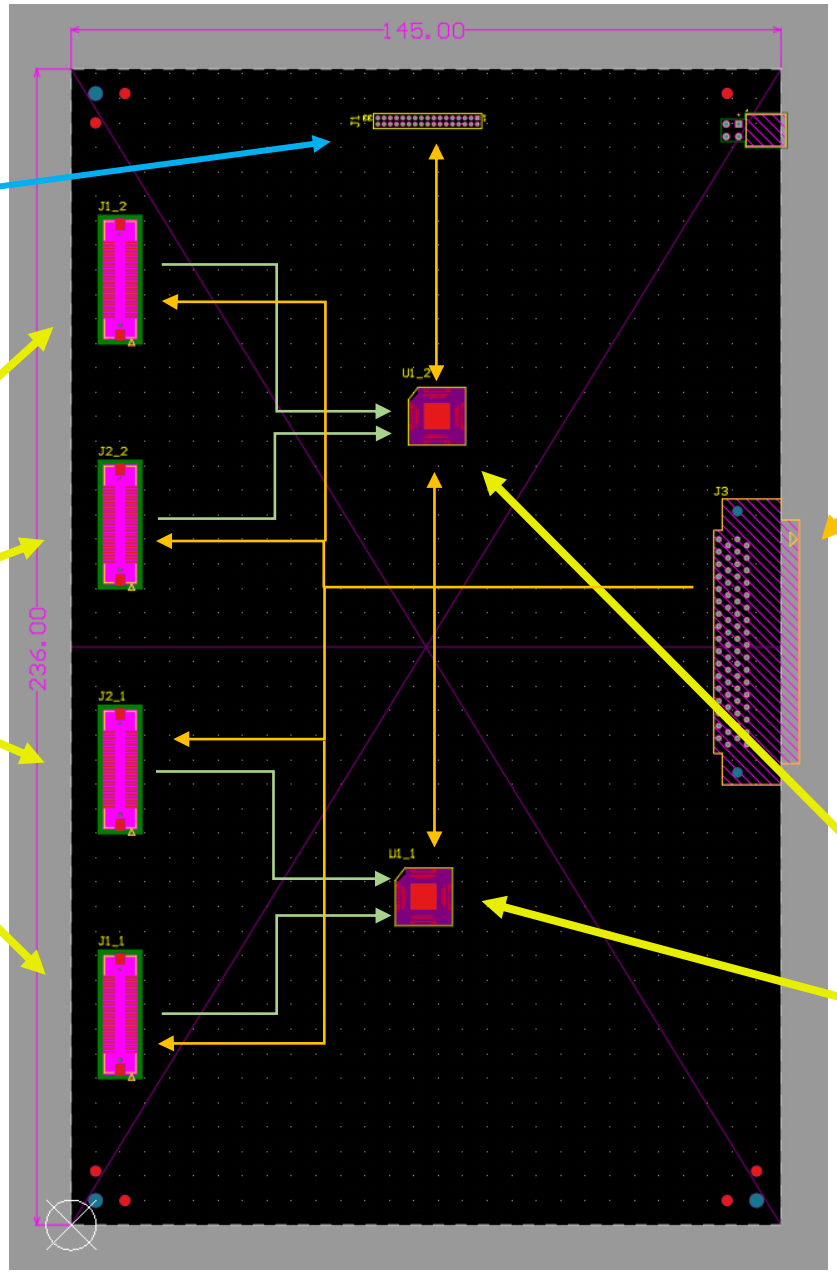




Board design

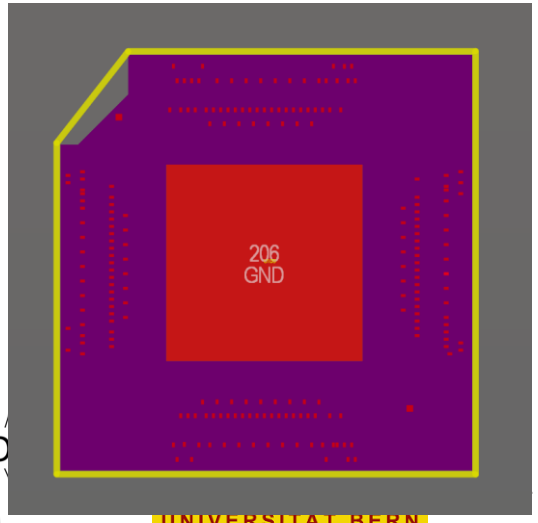
Connector to PACMAN

Molex connector to SiPMs
4 * 16 channels

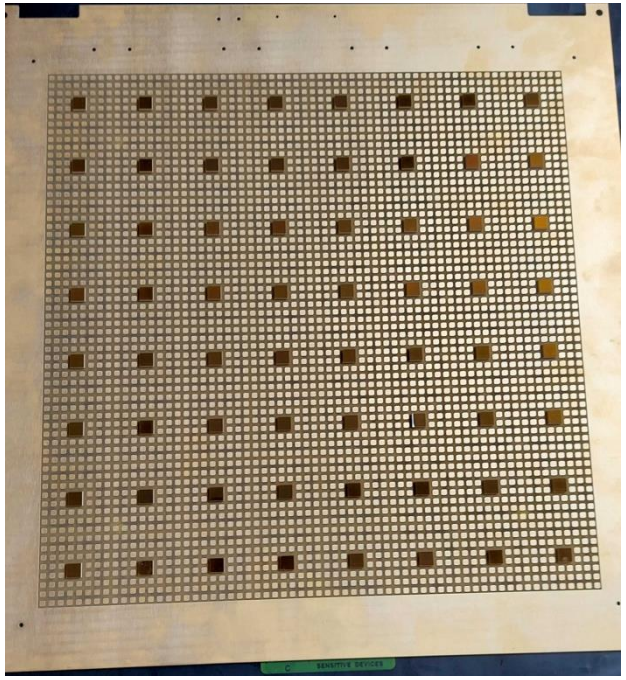


HV Connection (64 channels)

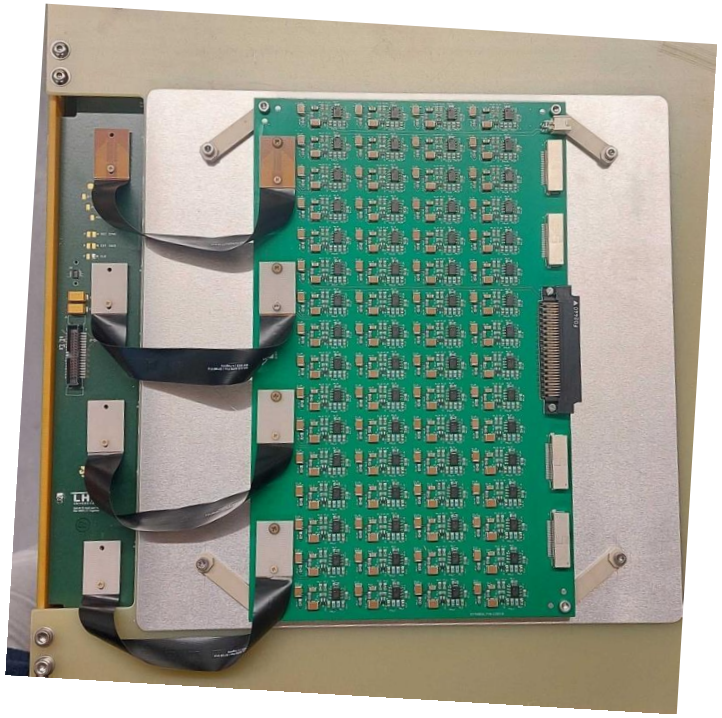
Wirebonding footprint



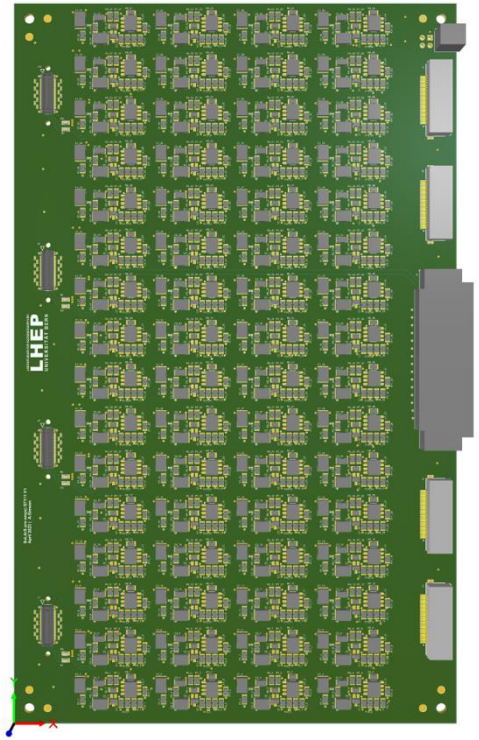
Same dimensions as Preamp-PCB



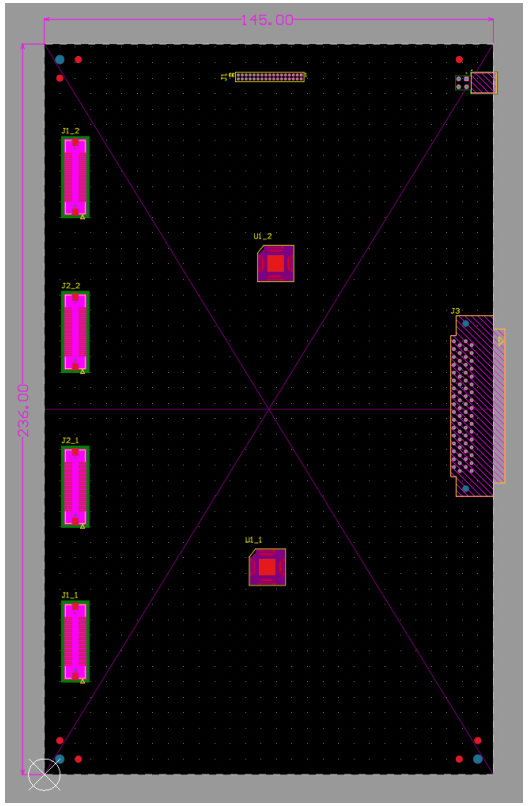
64 VUV SiPMs on SoLAr-v2



SoLAr-v2 cabled to preamp-PCB



Preamp-PCB (SoLAr-v2)

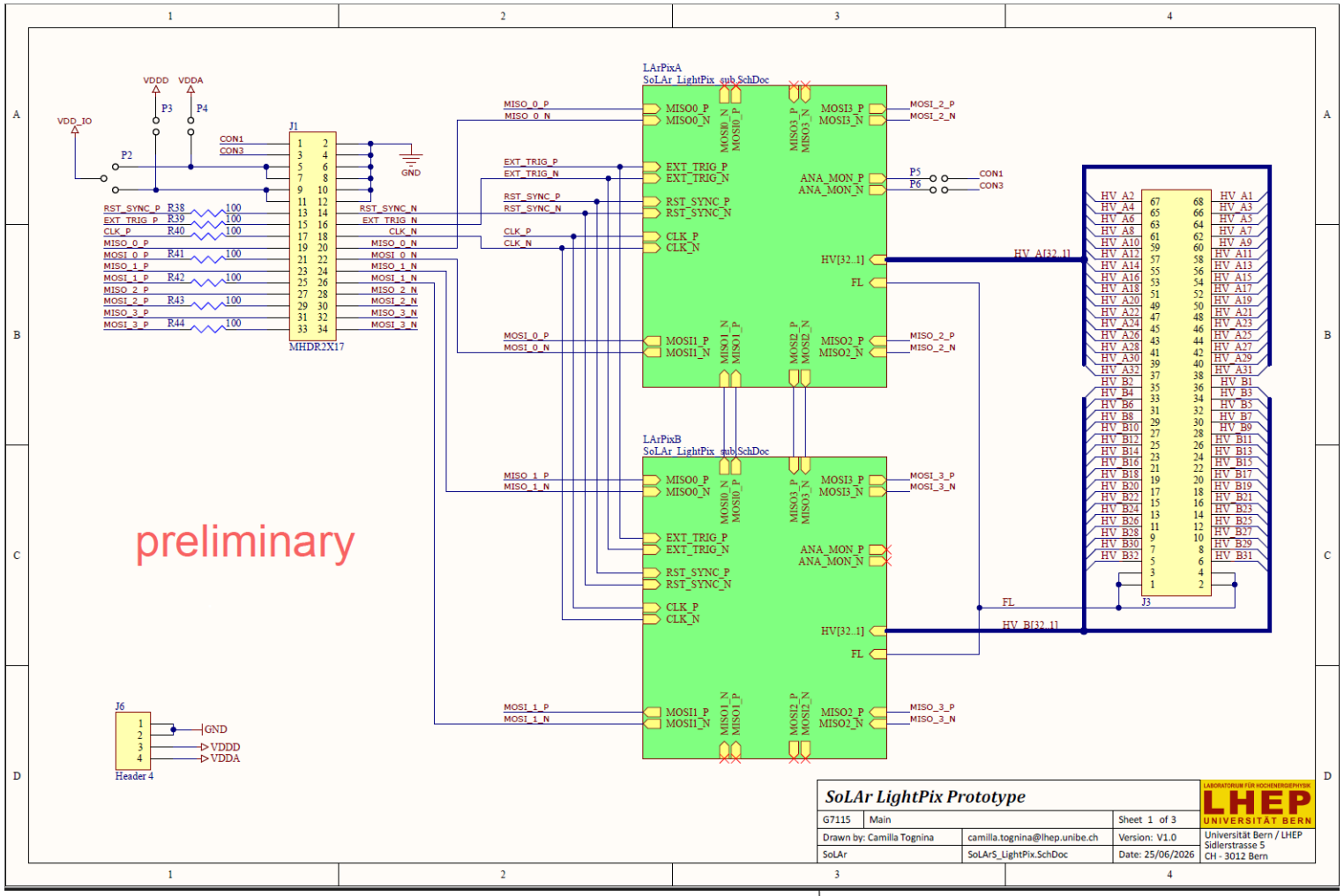


LightPix test board

Schematics of LightPix Test Board

Overview of:

- LightPix repeat block [Green]
- Data connector to feedthrough
- Power connector to feedthrough
- SiPM BiasV connector



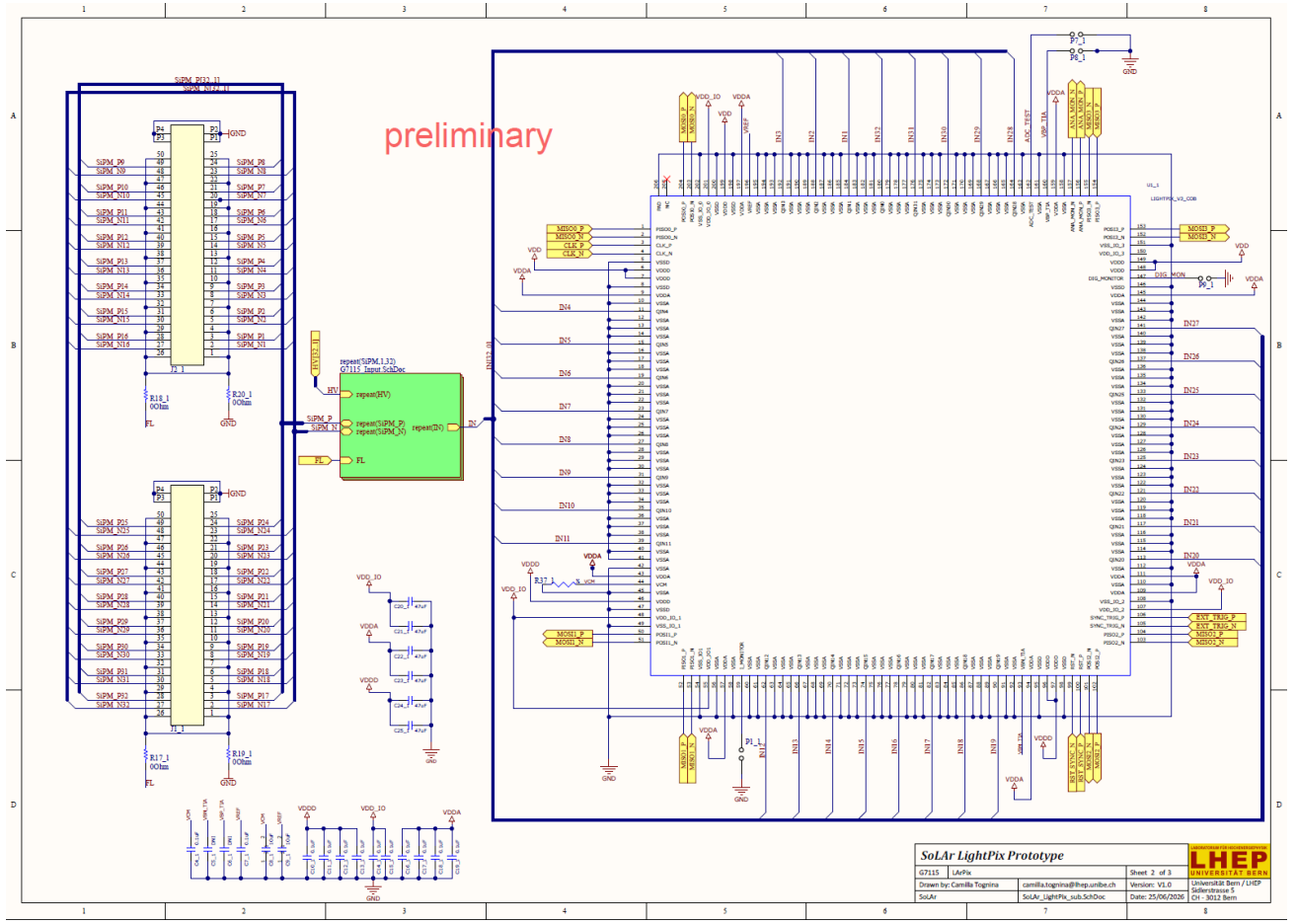
Sub-schematics
LightPix repeat Block

Overview of:

- LightPix wire bonding footprint
  - Channel inputs
  - VDDA, VDDD

- Molex connector for SiPM signal
- Input BiasV per channel x32
- SiPM Repeat block x32

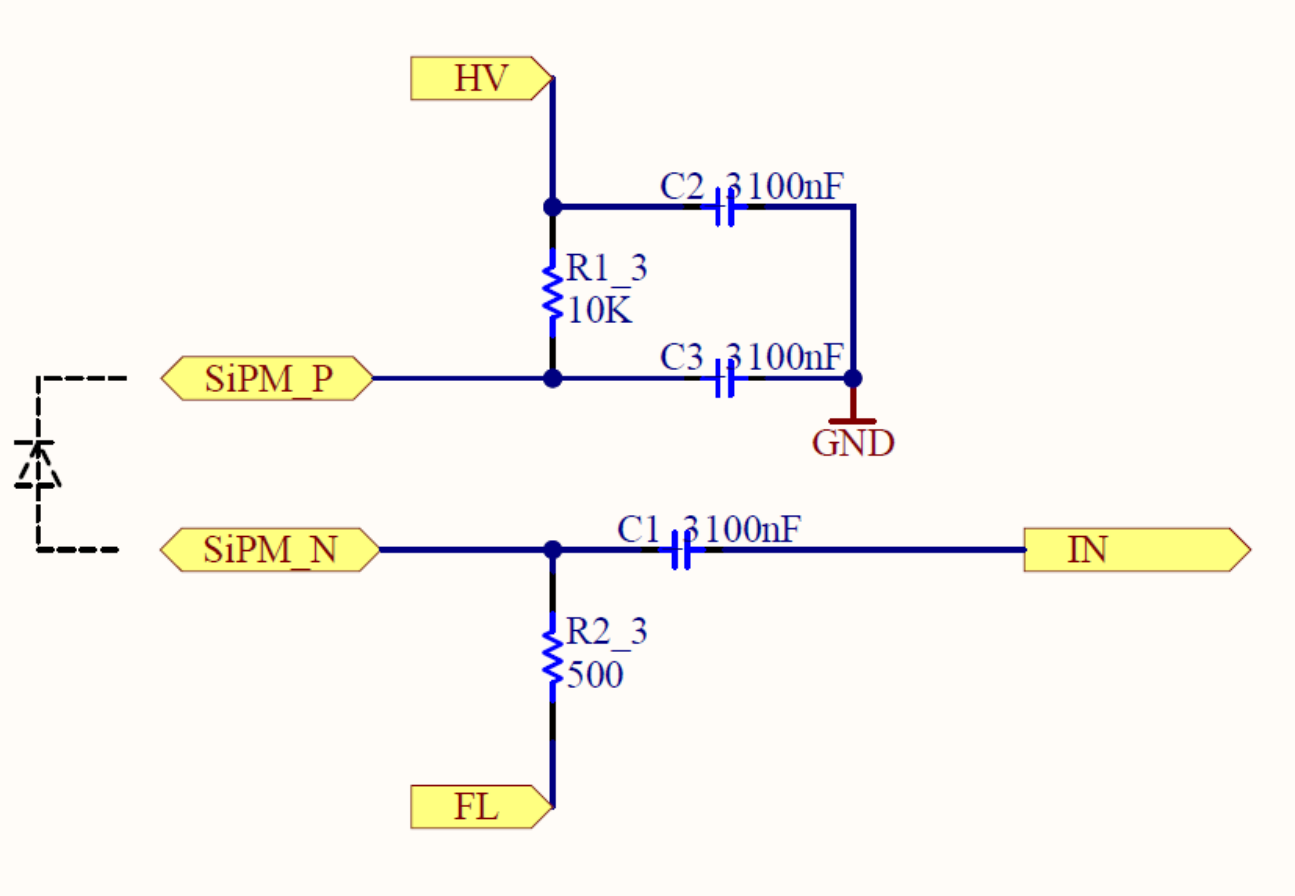
- Option for Float Low instead of GND
- Digital/Analogue monitor probe points



SiPM repeat Block

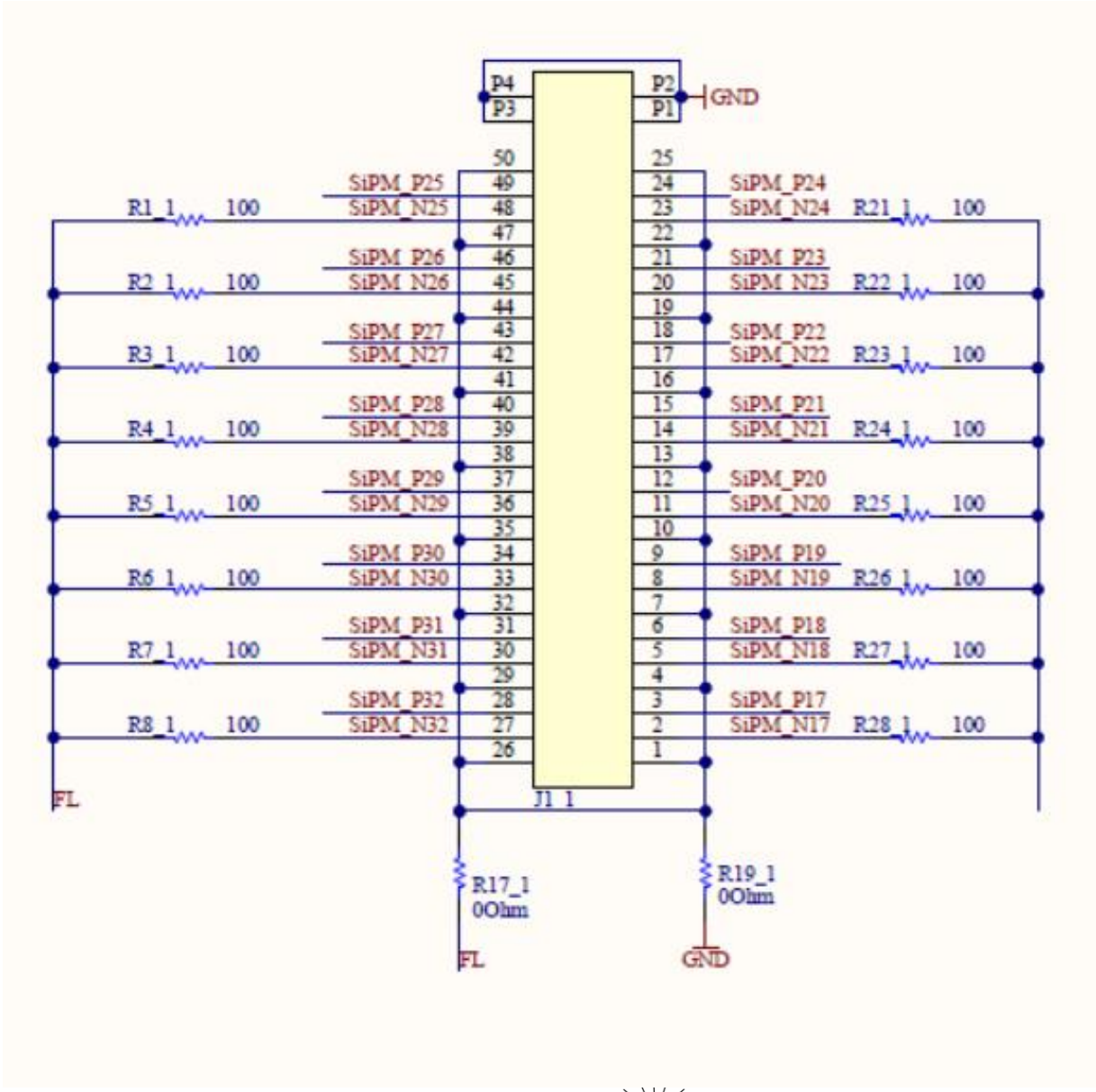
From Stephen:

We use AC coupling capacitor C1-3=150pF. There is no in-line resistor, and we use R2_3=500 Ohms



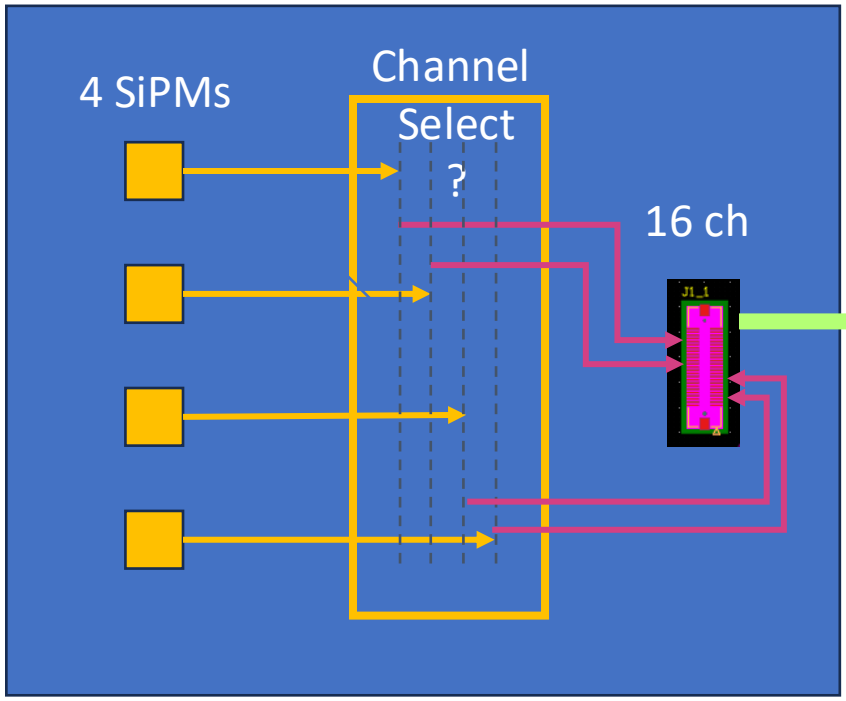
Milan VUV SiPMs, Daughter board

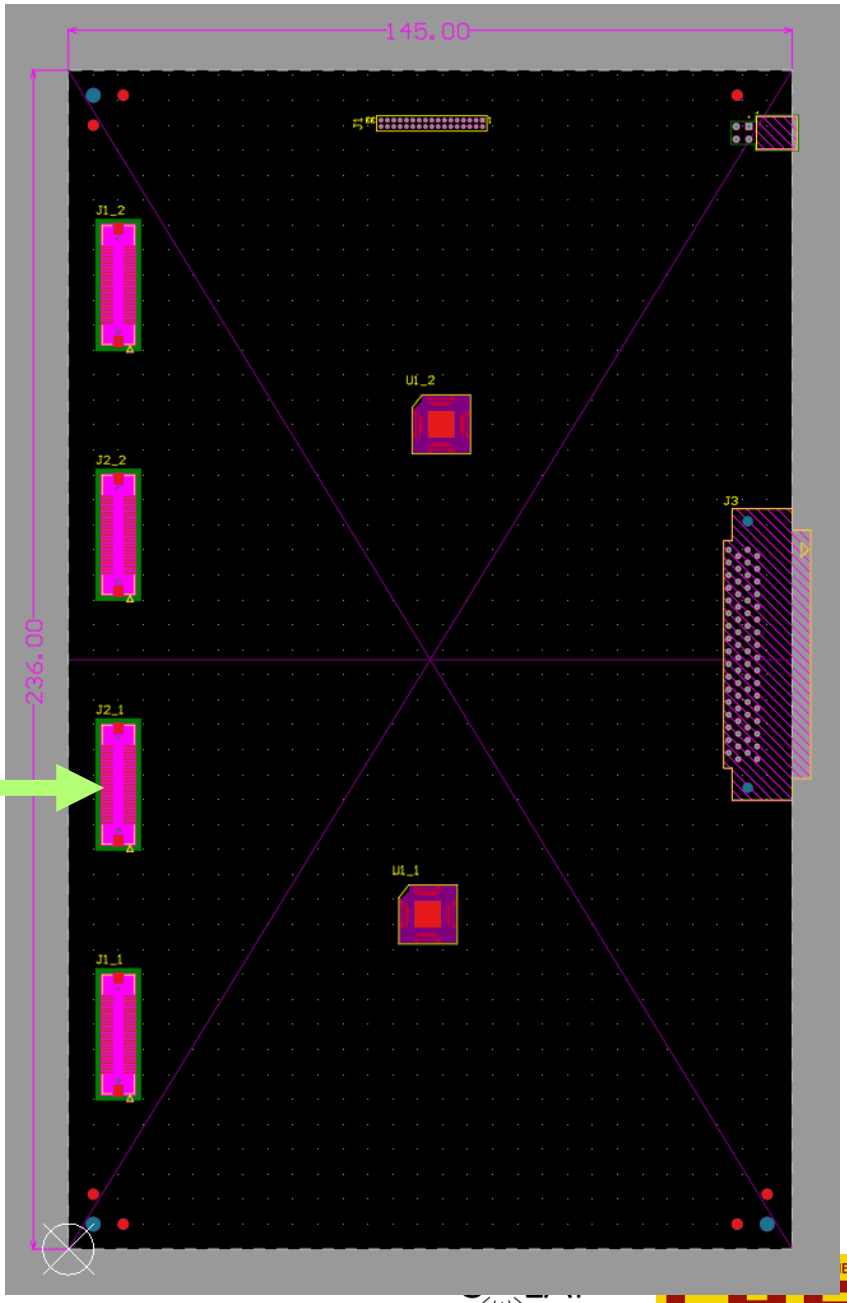
- Daughter board with 4 SiPMs
- A Molex FLEX connector with the PINout shown here can be coupled to the LightPix test board
- Maybe a jumper scheme to chose in which channel to inject the SiPM signal



Daughter Board proposed diagram

A daughter board + LightPix test board to be shipped to MIT for characterization and control software development





What are the next steps

While we produce and characterize the LightPix test board, work on next stages can start

- Schematics of the SoLAr–v3 tile
- Schematics of the Bias V control

Work on the PCB layout of SoLAr-v3 will begin after test board characterization completes.

- Let’s discuss person-power and availabilities over Summer period

Backup

SoLAr Prototype-v2

Readout scheme

- Charge readout: LArPix-v2b chips + PACMAN
  - Continuous Self-triggering ~ 100% live
  - Low power, low noise
  - Modest data volume ~ 1MB/s per m^2 anode
- Light readout: VUV SiPM+ Preamp + VGA + ADC
  - 62.5 MHz sampling frequency
  - 10 µs digitized window
  - Trigger logic on the Sum of up to 6 SiPMs