

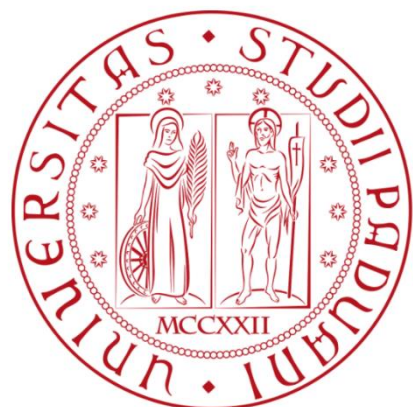


TRACK



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

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What For

System level

Signal from
detectors

Readout-
board

DAQ

Readout board:
BMOS v1
Trigger for BMOS
4 channels readout board

DAQ:
BMOS FPGA

Tools:
LTSPICE: theory simulation
Function level simulation



Tools:
VIVADO

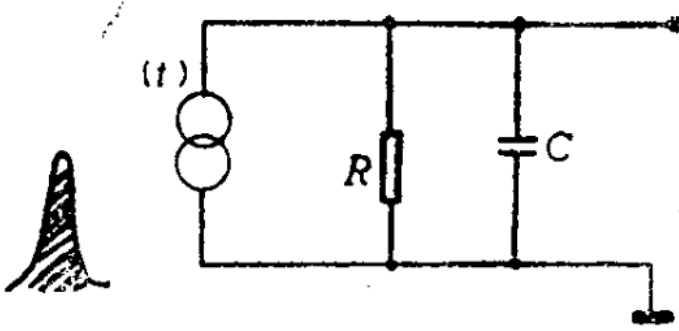
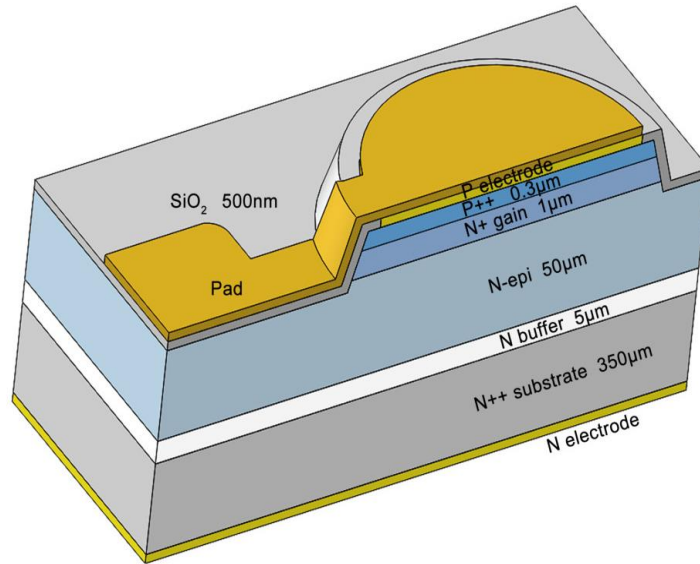
HFSS: S parameters extraction
Transmission Line Theory and Impedance Matching



KICAD/JIALICHUANG: Layout design



Detector: signal of detector



If decay time of signal $\ll$ constant time of readout circuit

For extremely short time Δt , during time from t to $t + \Delta t$, detector collect charge of Q , the current pulse of signal can be described by:

$$i(t) = \lim_{\Delta t \rightarrow 0} Q / \Delta t$$

In simulation, a pulse function can be used to approach the signal from unit function:

$$\delta(t - t_o) = \begin{cases} \lim_{\Delta \tau \rightarrow 0} \frac{1}{\Delta \tau} & t_o \leq t \leq t_o + \Delta \tau \\ 0 & t < t_o \\ & t > t_o + \Delta \tau \end{cases}$$

$$i(t) = Q \cdot \delta(t - t_o)$$

With consideration of statistical fluctuations

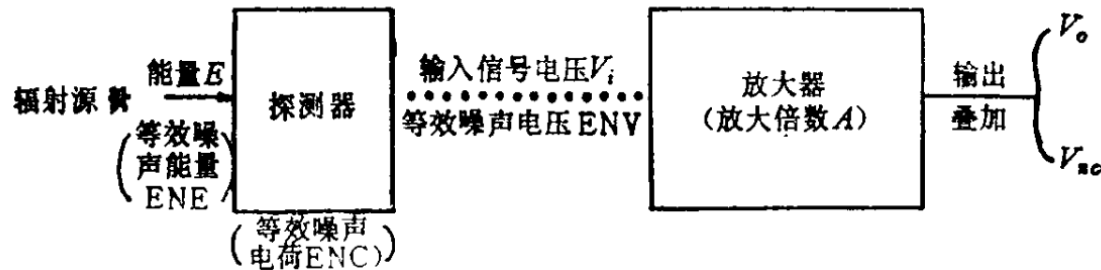
$$I(t) = \sum_i i_i(t) = \sum_i Q_i \cdot \delta(t - t_i)$$

Readout-board : noise

The noise level of a system cannot be judged from the average but from the RMS , for the average of the noise is always 0.

$$\overline{V_n^2} = \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T V_n^2(t) dt$$

From a typical detector system:



ENV, ENC, ENN and ENE can also reveal the noise level in a circuit including the amplifier.

$$(ENV) = \frac{V_{no}}{A} = \frac{V_{no}}{\left(\frac{V_o}{V_i}\right)} = \frac{V_i}{\eta}$$

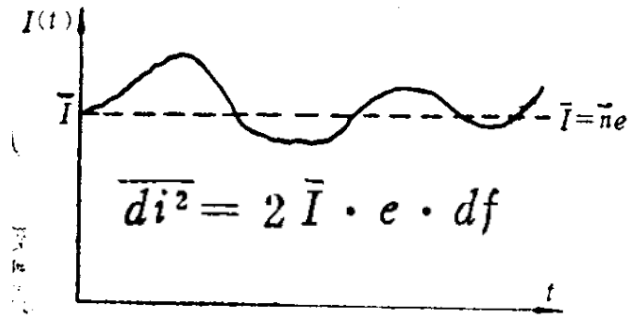
$$(ENC) = \frac{V_{no}}{A_{eq}} = \frac{QV_{no}}{V_o} = \frac{Q}{\eta}$$

$$(ENE) = (ENN) \cdot \overline{w} = \frac{Q}{e} \cdot \frac{V_{no}}{V_o} \cdot \overline{w}$$

$$(ENN) = \frac{(ENC)}{e}$$

Readout-board : noise

- Shot noise:
 - Origin from the leakage current of detector



For shot noise, a higher leakage current or a wider amplifier bandwidth results in higher noise.

- Shot noise from detector

$$\overline{di_D^2} = 2 \bar{I}_D \cdot e \cdot df$$

- Shot noise from amplifier

$$\overline{di^2 I_g} = 2 I_g \cdot e \cdot df$$

- Thermal noise:
 - From the thermal movement of carriers

$$\overline{di^2} = 4 kT / R \cdot df$$

For thermal noise, higher temperature results in higher noise.(also depends on the material due to different R)

- Low-frequency noise

$$\overline{dv_f^2} = \frac{A_f}{f} \cdot df$$

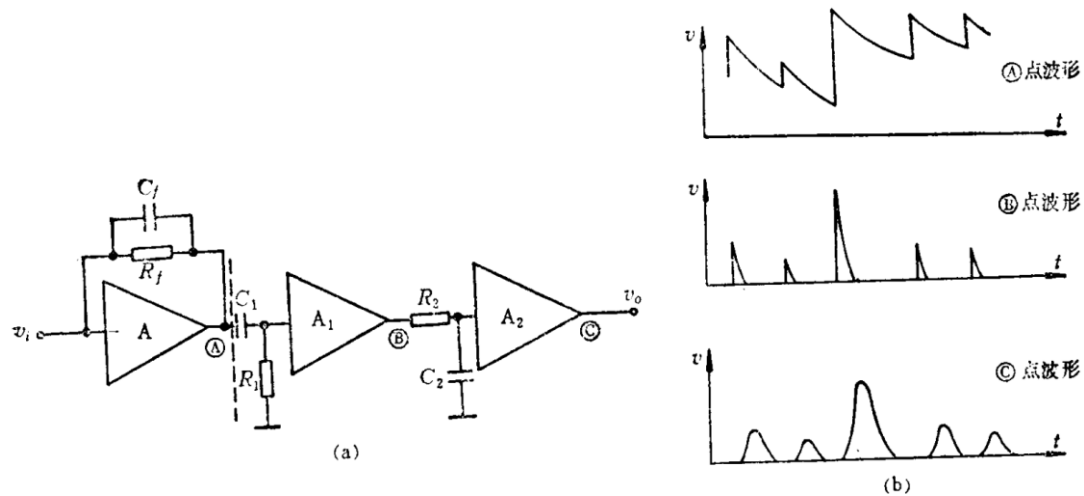
For Low-frequency noise, higher the smallest limit frequency results in lower noise.

Readout-board : Filter and shaper circuit

For:

- Reduce the noise in system
- Reshape the signal from the detector

CR-RC CIRCUIT



Pole-Zero Cancellation Circuit

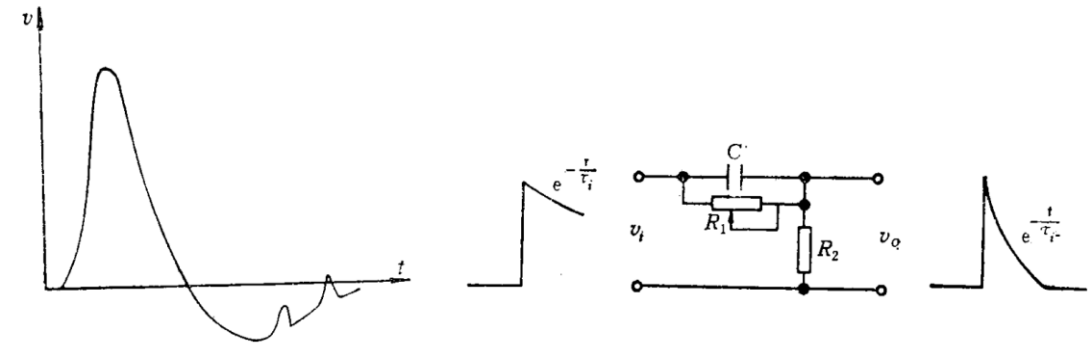
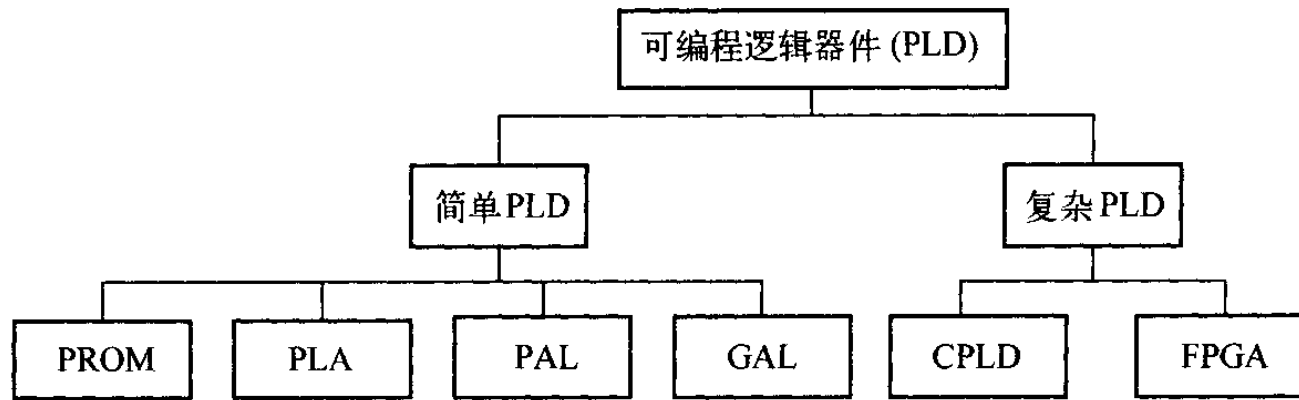


图3.3.11 大脉冲信号后下冲引起过载的现象

图3.3.12 极-零相消电路

PLD(Programmable Logic Device)



- PROM: Programmable Read-Only Memory
- PLA : Programmable Logic Array
- PAL : Programmable Array Logic
- GAL : Generic Array Logic
- CPLD : Complex PLD
- FPGA : Field Programmable Gate Array

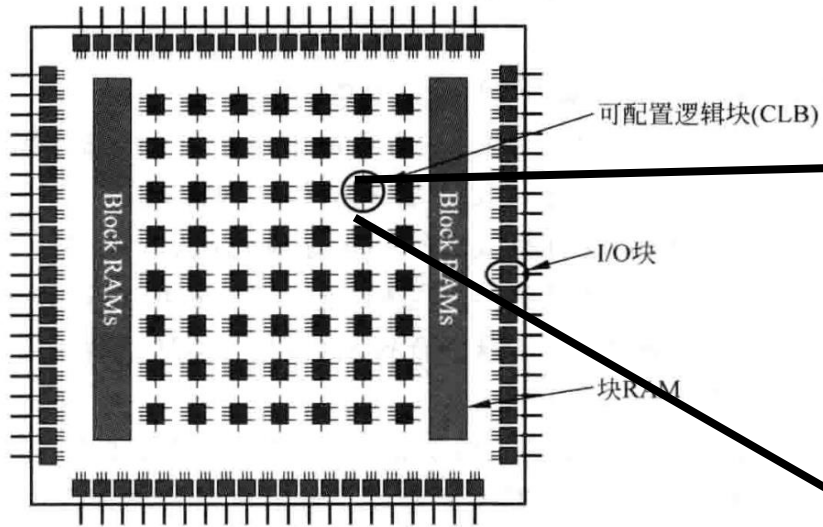
De Morgan's Theorems & Karnaugh Map

摩根定律又称为反演律，它有以下两种形式

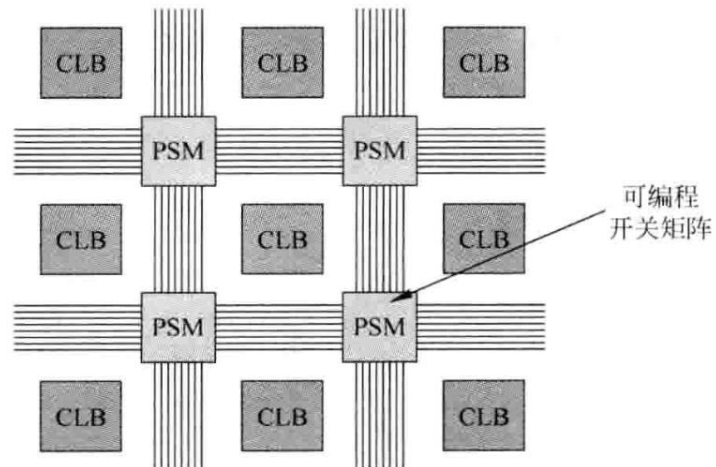
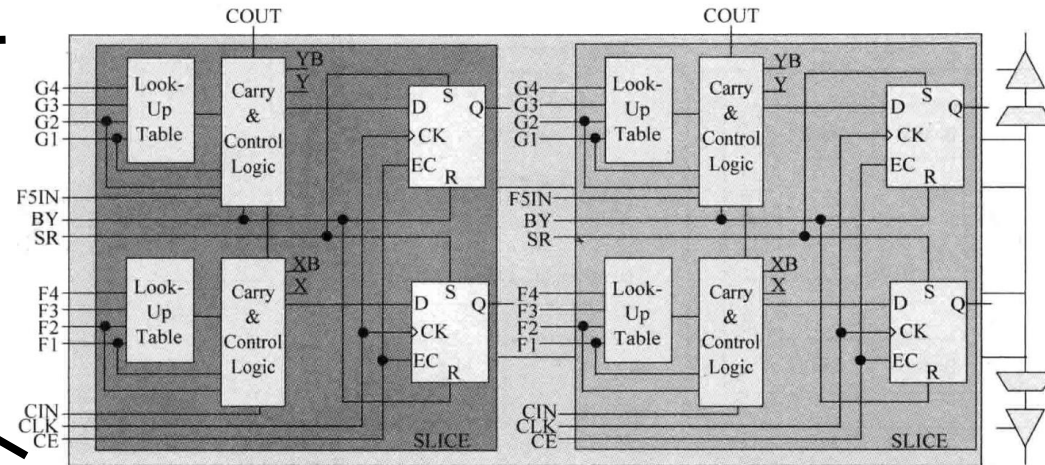
$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

"Any logic function can be simplified into a Sum of Products (SOP) logic equation."

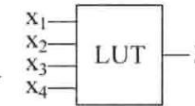
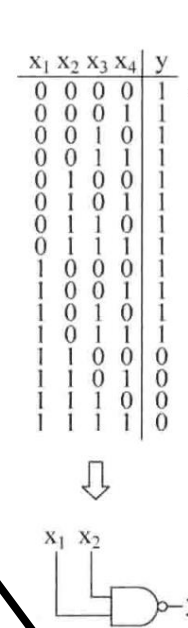
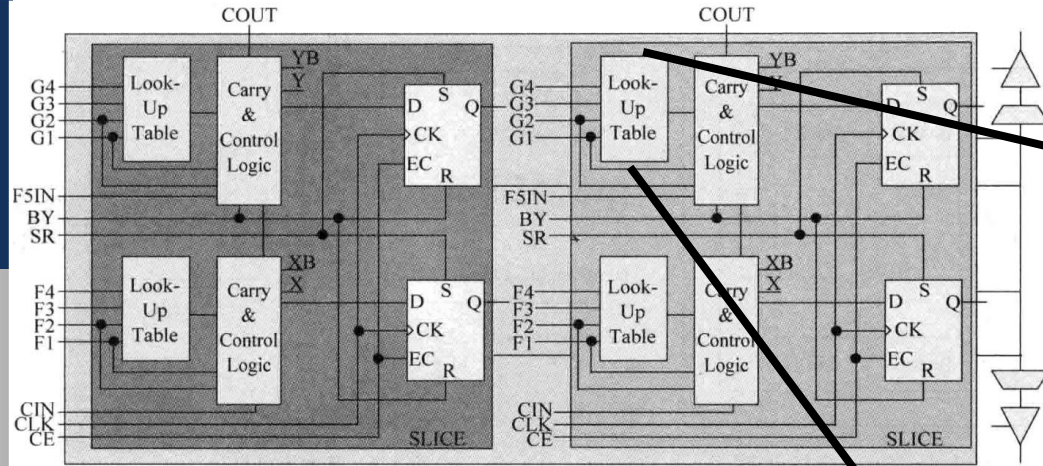


CLB module

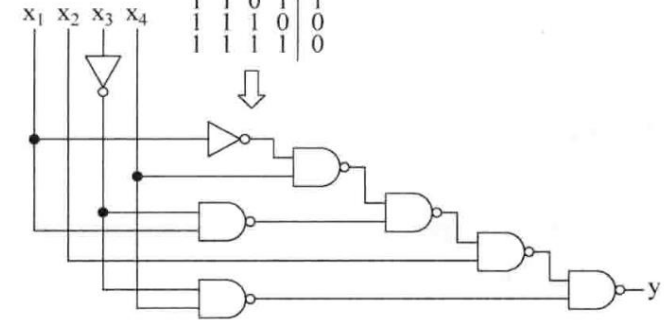


CLB primarily includes 2 LUT-FF pairs with carry logic and 2 global tri-state buffers (BUFT). A single LUT-FF consists of 2 4-input LUTs, 2 control and carry logic units, as well as 2 storage elements.

DAQ: FPGA Spartan II



x_1	x_2	x_3	x_4	y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0



The LUT (Look-Up Table) is the primary element for logic implementation, and each LUT can implement any 4-input function.

- Demand analysis
- Sub-module design
- Pre-simulation
- System simulation
- Logic Synthesis
- Layout
- Simulation
- Test

Design and implement a simple unit permitting to speed up encryption with RC5-similar cipher with fixed key set on 8031 microcontroller. Unlike in the experiment 5, this time your unit has to be able to perform an encryption algorithm by itself, executing 32 rounds...

设计需求

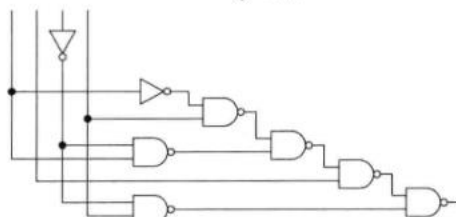
```
Library IEEE;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity RC5_core is
    port(
        clock, reset, encr_decr:in std_logic;
        data_input:in std_logic_vector(31 downto 0);
        data_output:out std_logic_vector(31 downto 0);
        out_full:instd_logic;
        key_input:in std_logic_vector(31 downto 0);
        key_read:out std_logic;
    );
end AES_core;
```

HDL描述



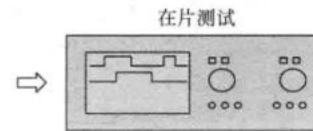
综合



实现

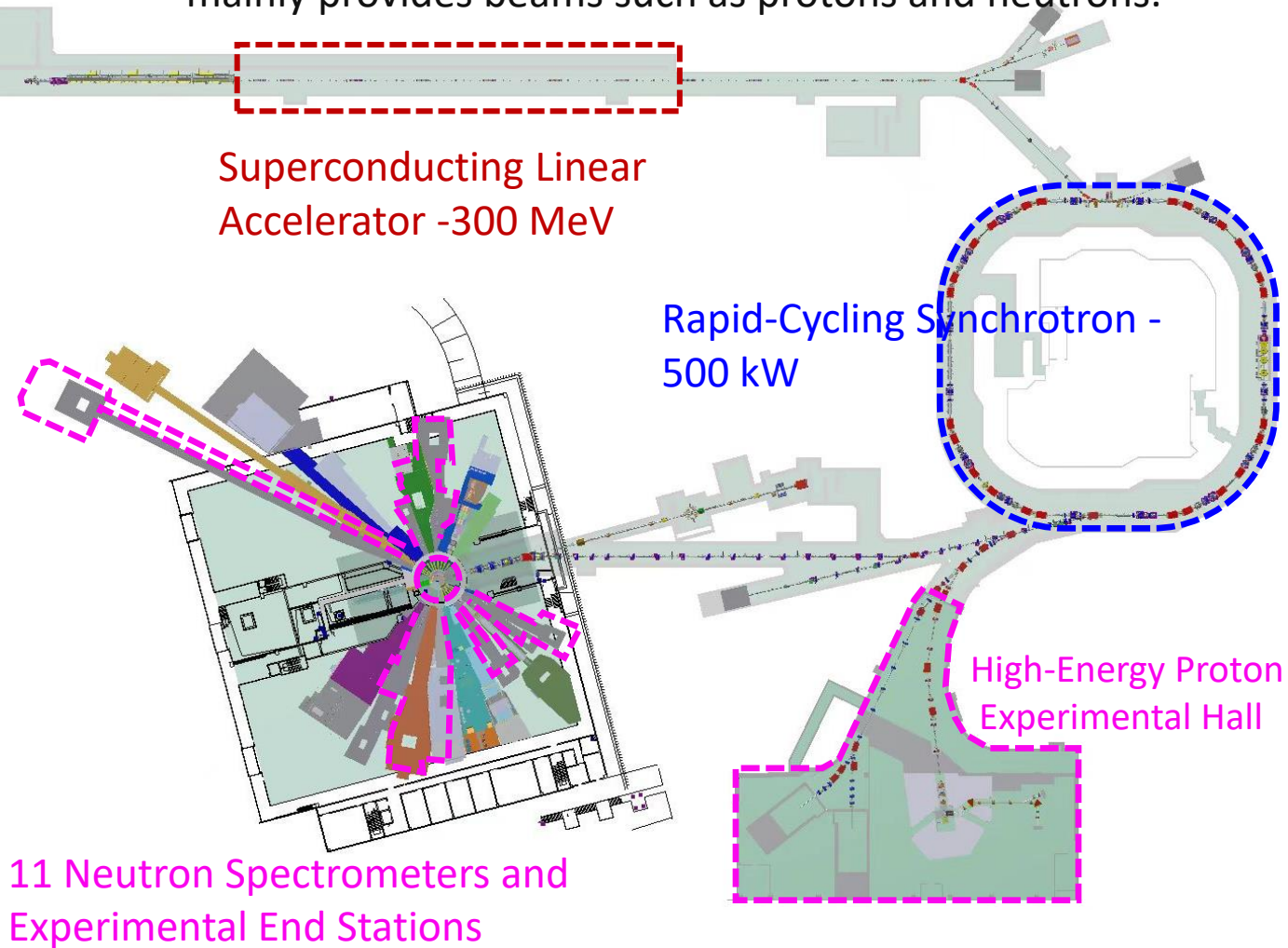


配置下载



Begin a project BMOS

China Spallation Neutron Source is located in Dongguan City, Guangdong Province, China. It mainly provides beams such as protons and neutrons.



The energy of the linear accelerator has been increased to 300 MeV.

The beam power has been increased to 500 kW.

The neutron flux has reached $1 \times 10^8 \text{ n/cm}^2/\text{s}$

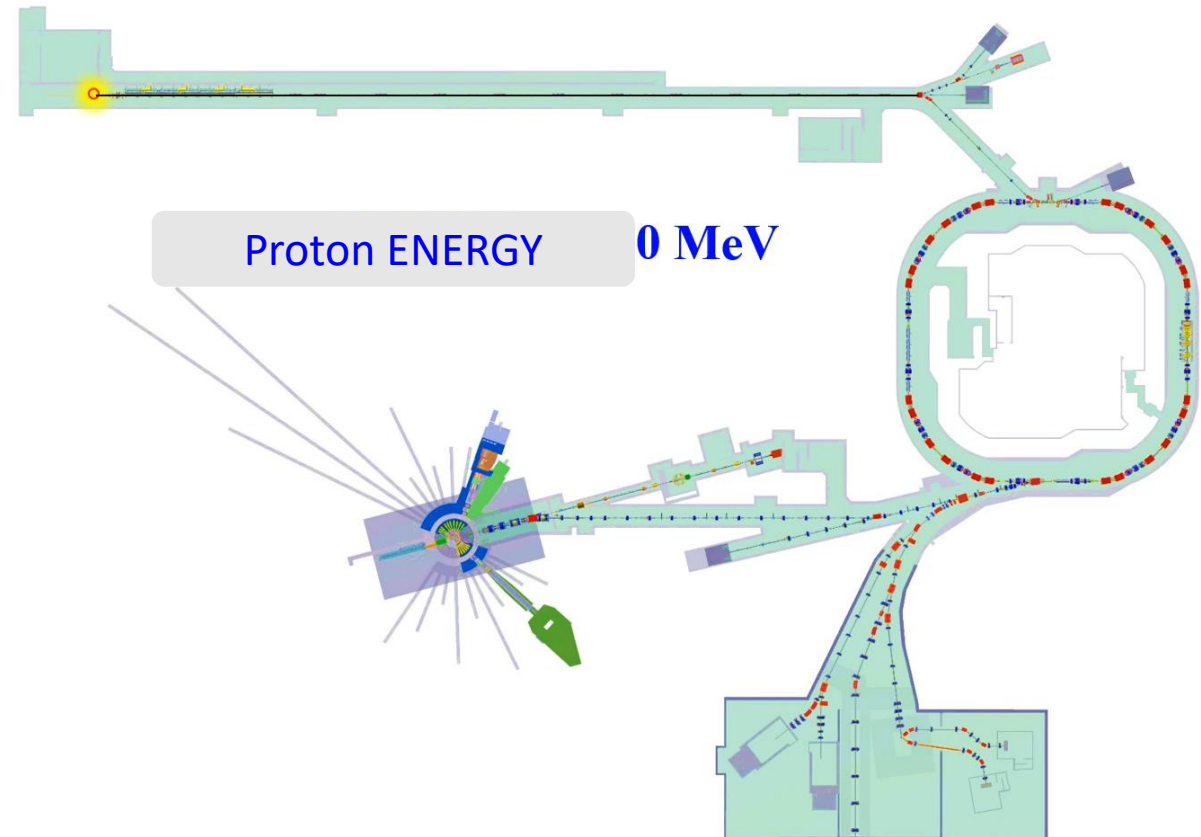
A total of 11 new neutron spectrometers and experimental end stations have been added and constructed.

- A high-energy proton experimental station (HPES) capable of providing a 1.6 GeV test beam.
- A surface muon source (MELODY)

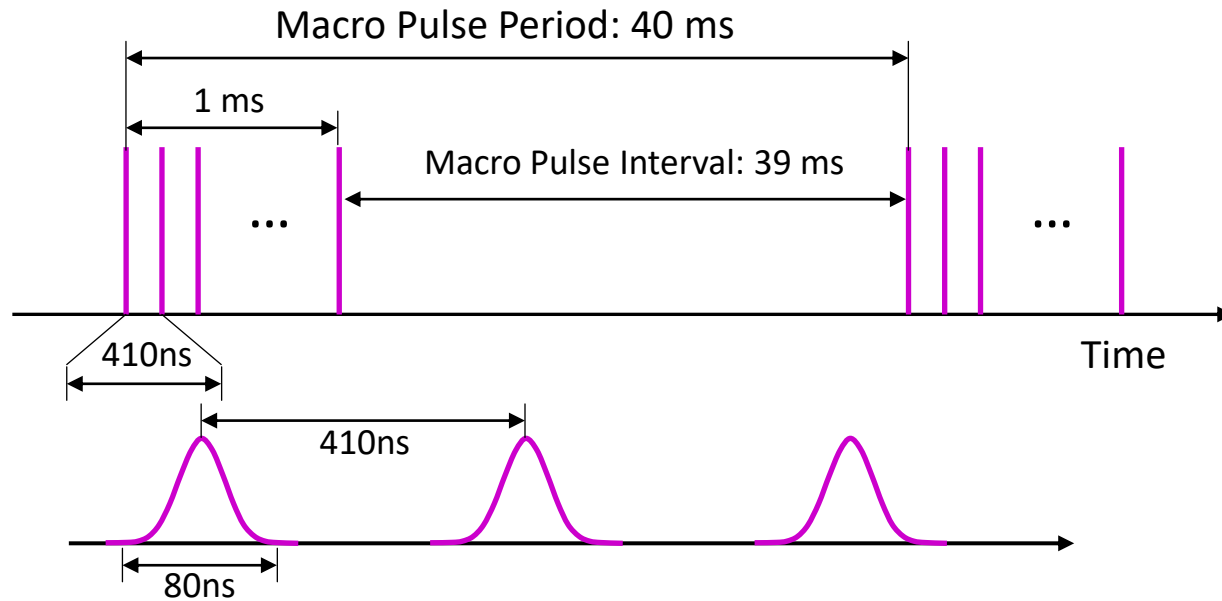
High-Energy Proton Experimental Station (HPES)

- ▮ According to testing requirements, both low-intensity and high-intensity proton test beams are provided.

Parameter	Design Targets
Proton Energy Range	0.8-1.6 GeV
Beam Pulse Frequency	24 Hz
High-Intensity Beam Flux	10^6 - 10^9 p/s
Low-Intensity Beam Flux	10^3 - 10^4 p/s



Begin a project



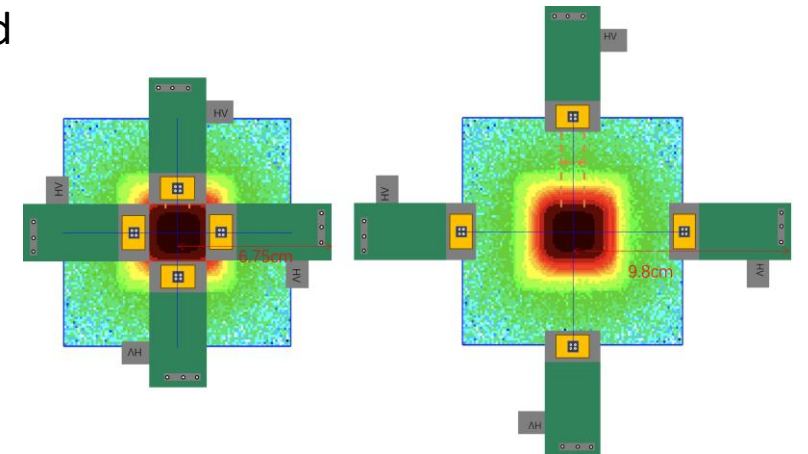
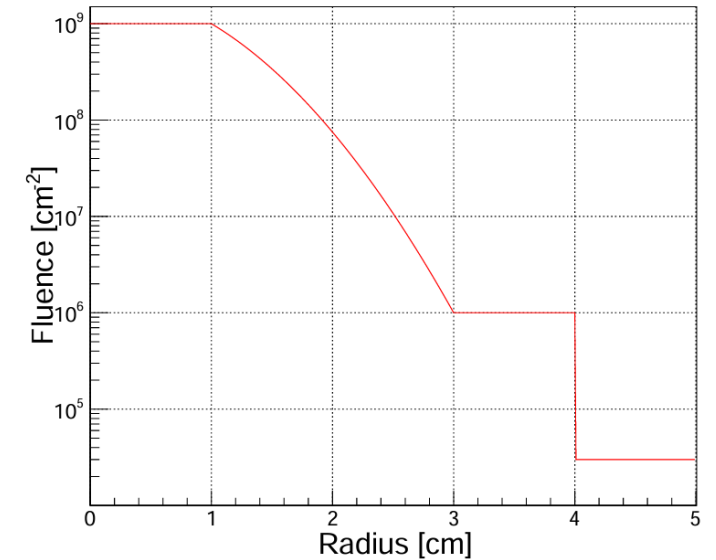
Schematic Diagram of Micro Pulse Time Structure

- Due to the beam characteristics of CSNS, the proton beam exhibits a two-level bunch structure in time :
 - Macro Pulse Frequency: 25 Hz (24 Hz effective)
 - Macro Pulse Length: 1 ms, Interval: 39 ms
 - Micro-pulse in macro-pulse
 - Micro-pulse period: 410 ns, Micro-pulse Length : 80 ns

BMOS ---- Beam Monitor Online System

Design target

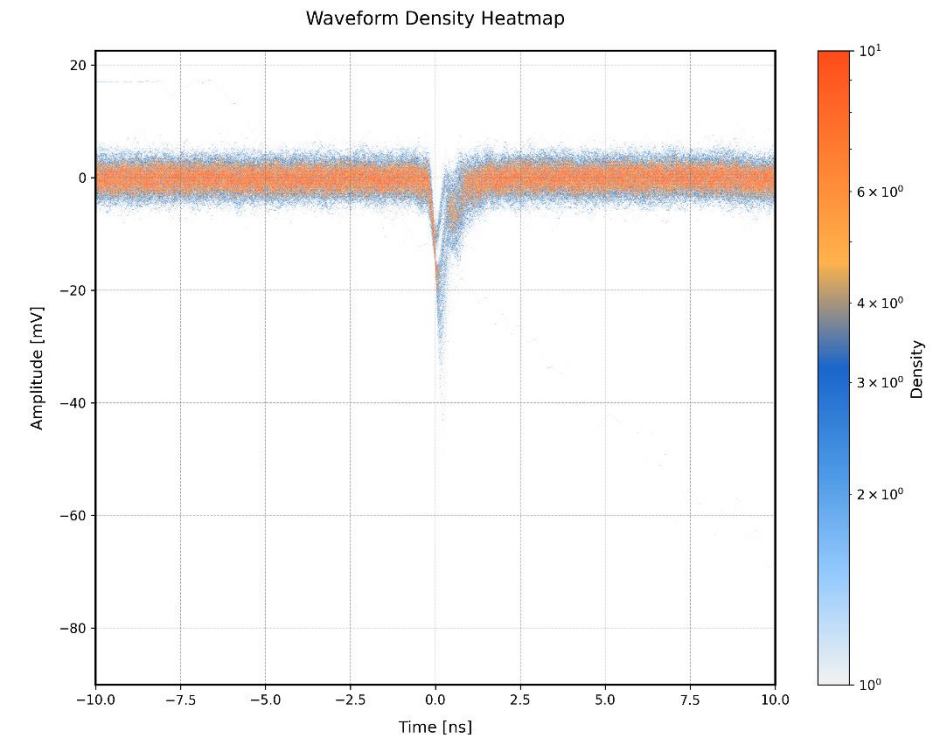
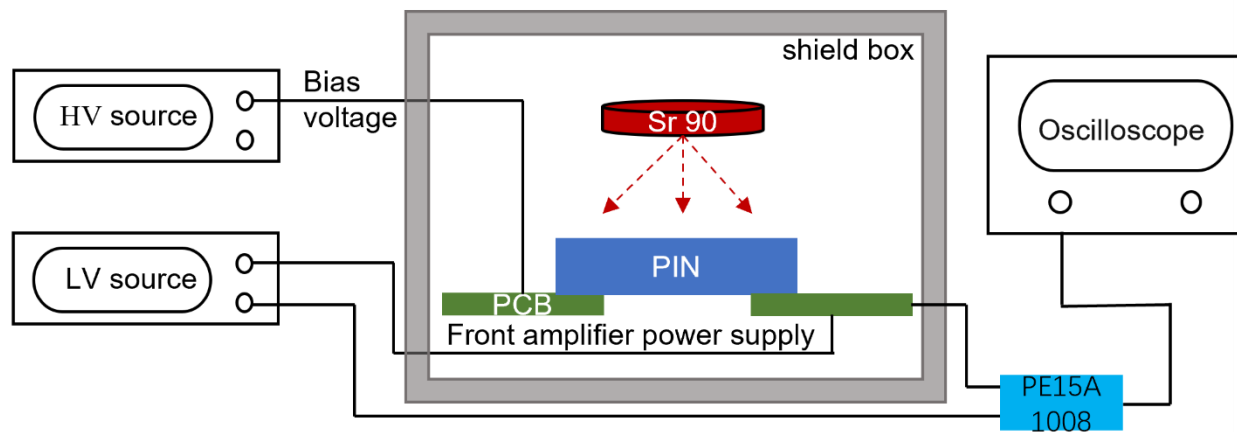
- Real-time monitoring of beam intensity, position, and uniformity
- Design life: 5000 hours/year
- Detection Strategy: Indirect Measurement Method
Place the detector at the adjustable edge of the beam center to avoid the high-dose irradiation zone, thereby ensuring detector lifespan and beam stability.
 1. Effective Beam Working Area: A central $2\text{cm} \times 2\text{cm}$ square.
 2. Detector Layout: Located in the edge non-direct irradiation zone.



Begin a project

Experimental Verification

- Test Platform: Based on IHEP SiC-PIN detector + UCSC board, for testing responses to different particles.
- Beta particles: 90Sr radiation source (approaching Minimum Ionizing Particles, MIPs, for validating low-energy signal response).
- Test Results
 - signal peak $\sim 20\text{mV}$
 - amplifier gain ~ 18
 - Board $R_f \sim$ about 400 Ohm
 - SiC Peak of Intrinsic Current Signal $\sim 2\text{ uA}$

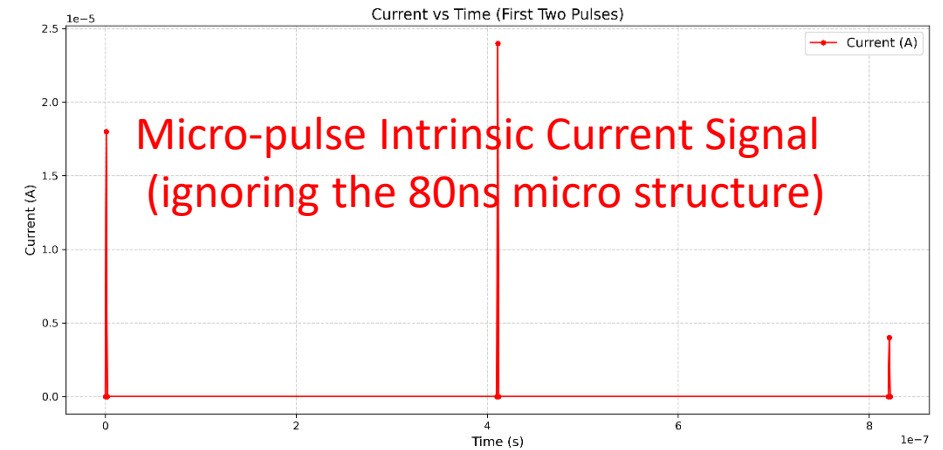
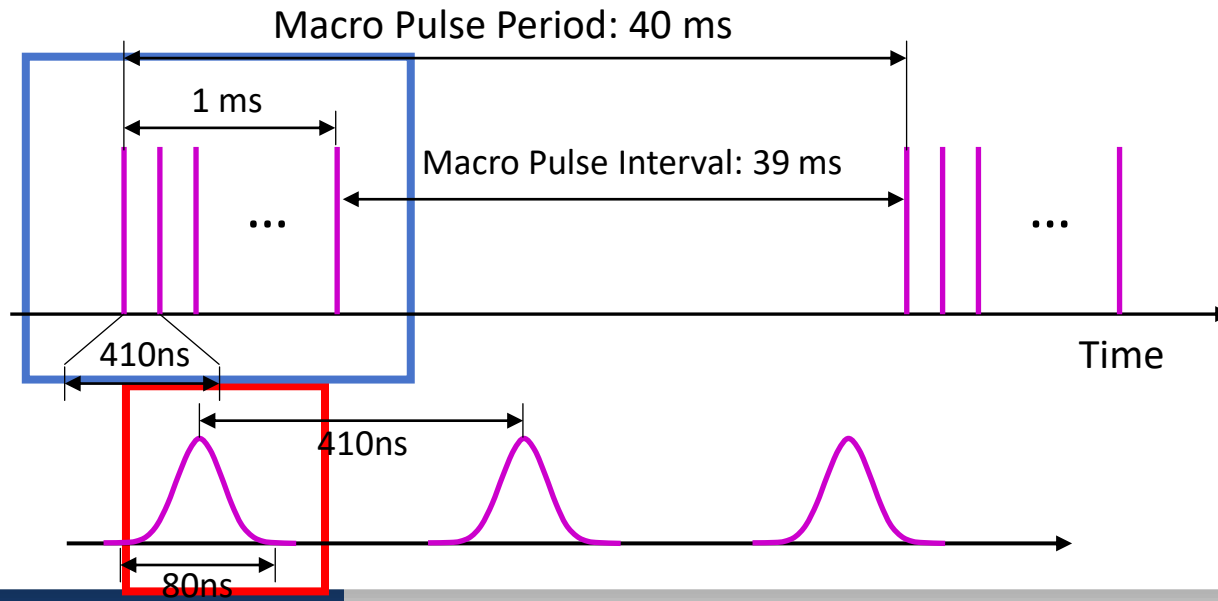


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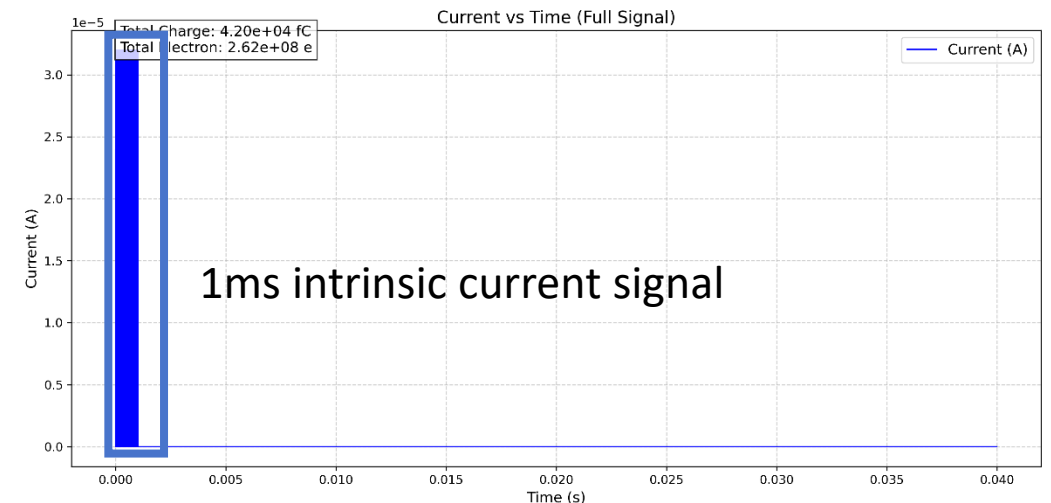
```
def generate_pulse_signal():  
    index_num = random.randint(1, 16)  
    time = [0, 1e-9, 2e-9]  
    current = [0, index_num * 2e-6, 0]  
    return time, current
```

Signal Response per Micro-pulse:

- Pulse information for 1–16 protons is generated using random numbers.
- Each proton excites a peak current of 2 μA (intrinsic signal for 1.6 GeV proton incidence).

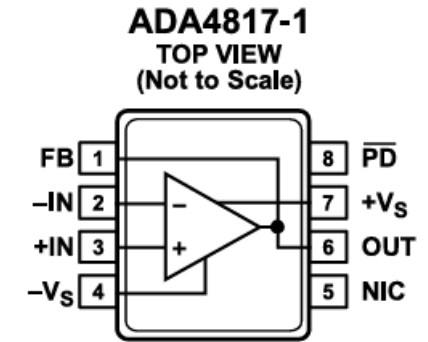
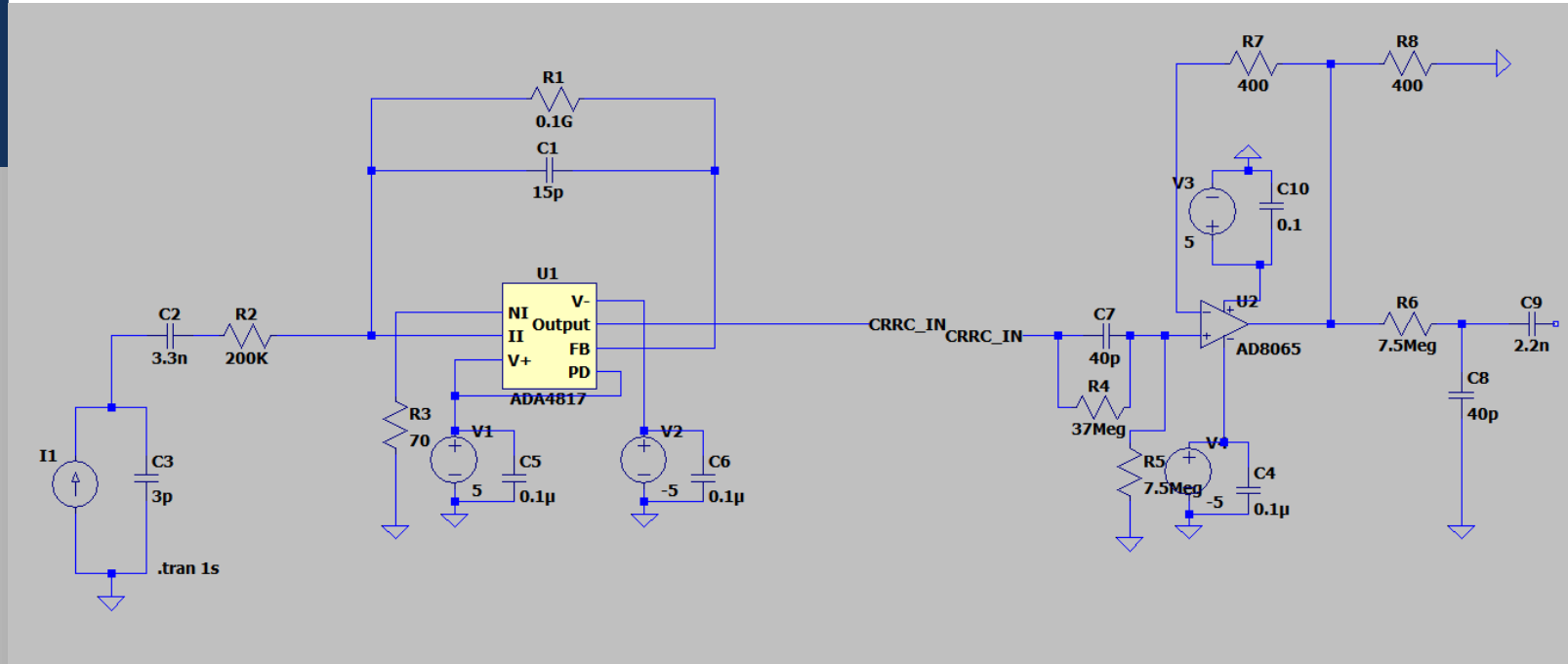


Macro-pulse Intrinsic Current Signal



Begin a project

The BMOS PCB design employs a charge integration circuit and a first-order CRRC shaper circuit.



NOTES

1. NIC = NO INTERNAL CONNECTION.

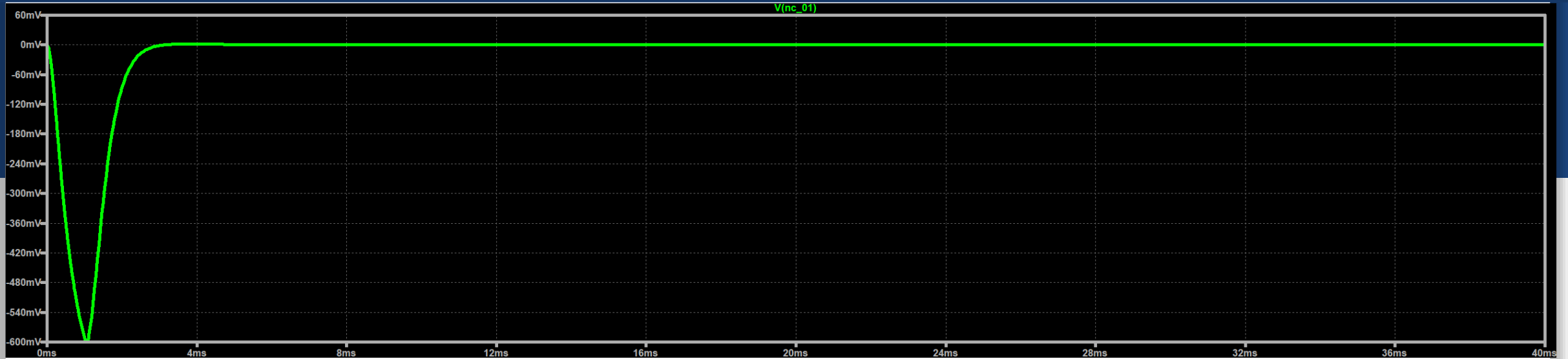
Core Circuit Parameter Design :

- Integration capacitance: 10 pF
- Discharge time: 15 ms (considering parasitic capacitance of 2~5 pF)

Key configure of ADA4817

- Input resistance $\sim 500 \text{ G}\Omega$
- Open-Loop Gain $\sim 65 \text{ dB}$

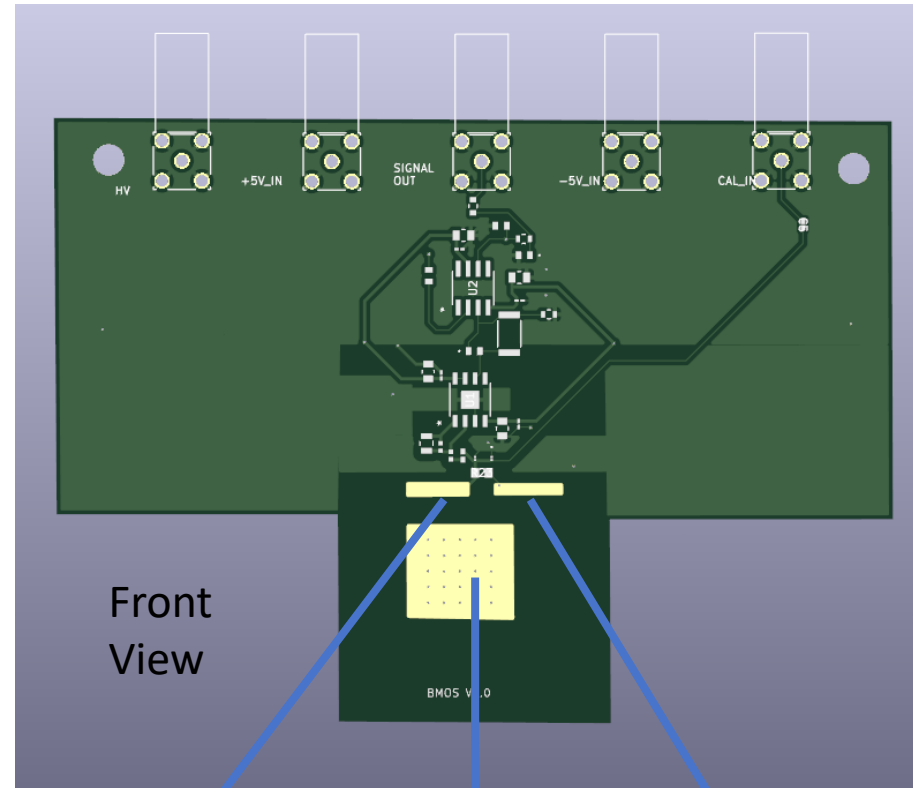
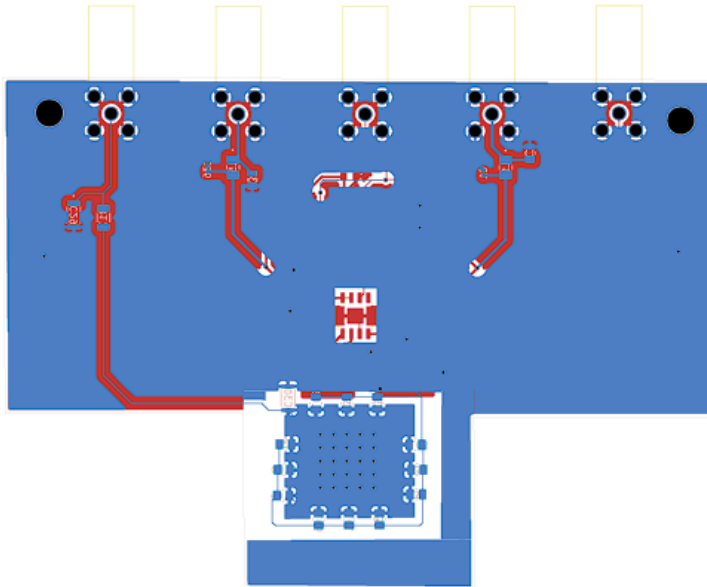
Begin a project



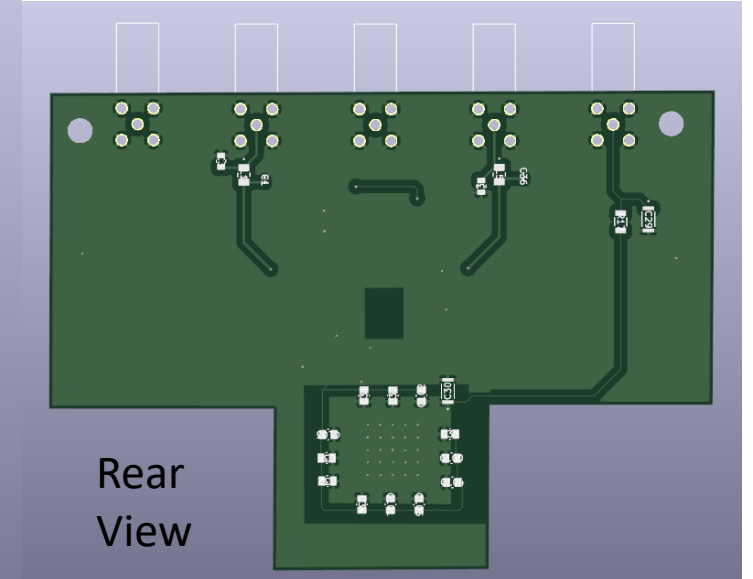
- Signal of output
 - More than 600 mV
 - 4 ms zeroing time

Considering the ADC and FPGA , the total system can be reset within 40 ms

Begin a project



Front View



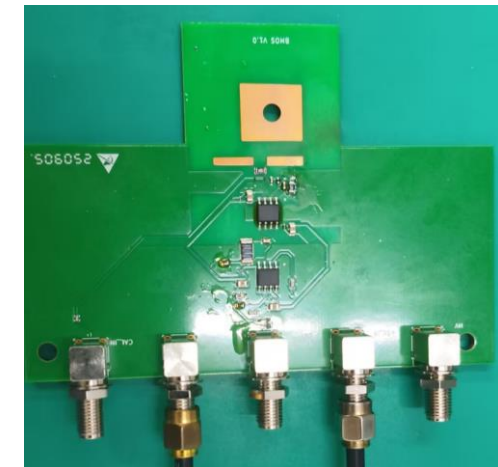
Rear View

- High-voltage traces should be kept away from signal traces.
- Power supply traces should be thicker.
- No ground plane is provided for high-bandwidth chips.

Signal bonding pad

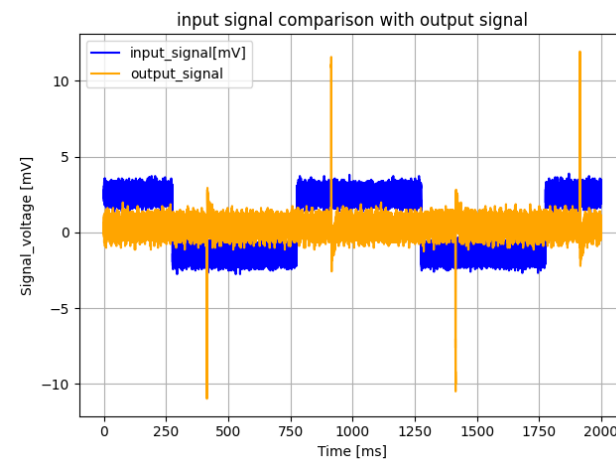
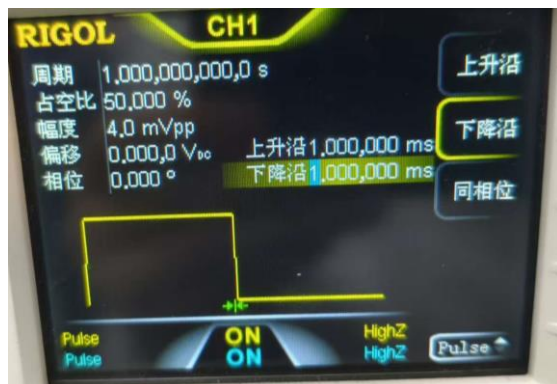
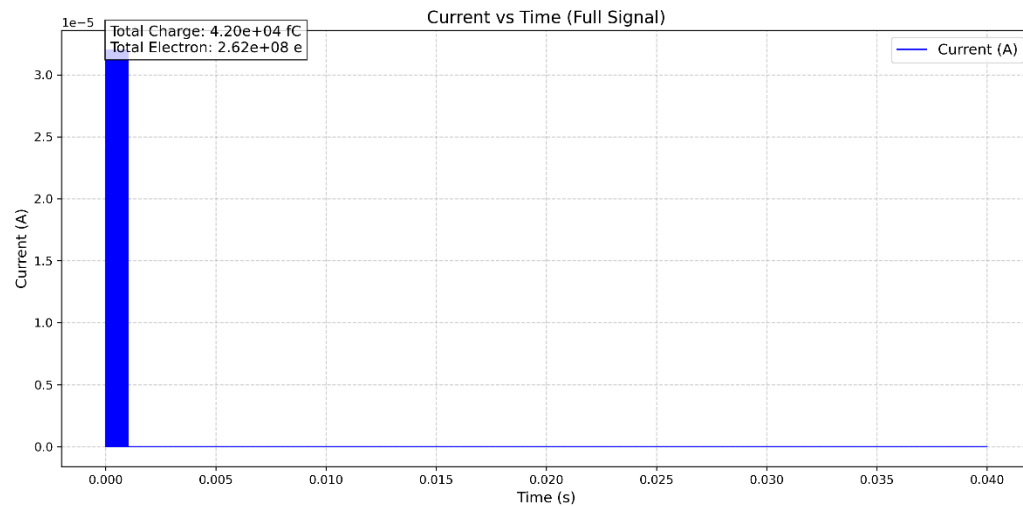
HV pad

Signal ground bonding pad



Begin a project

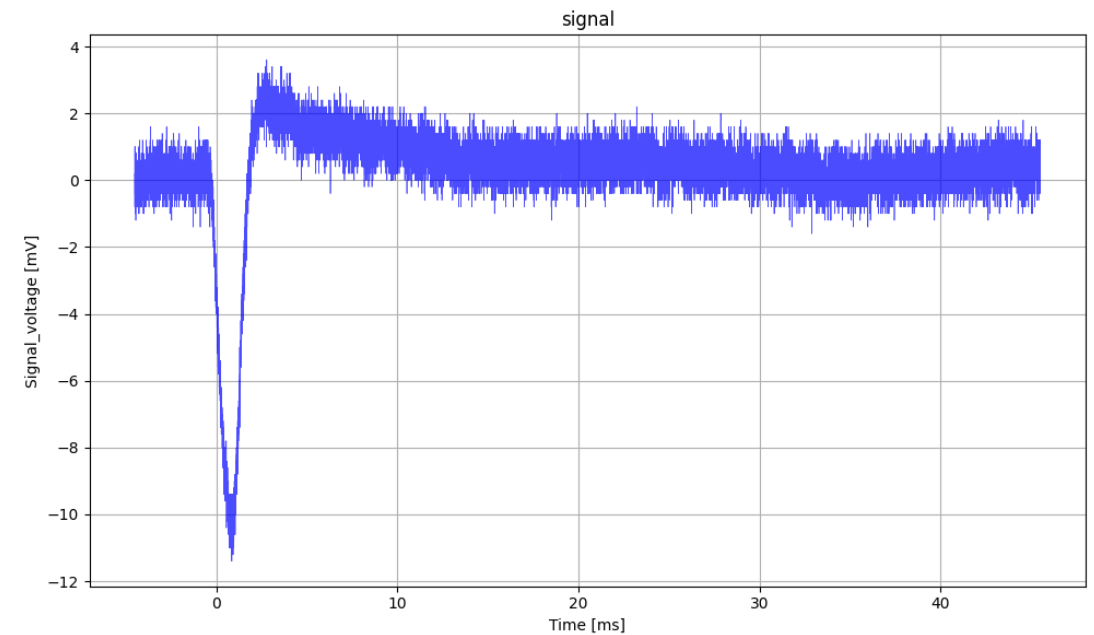
CAL_IN test



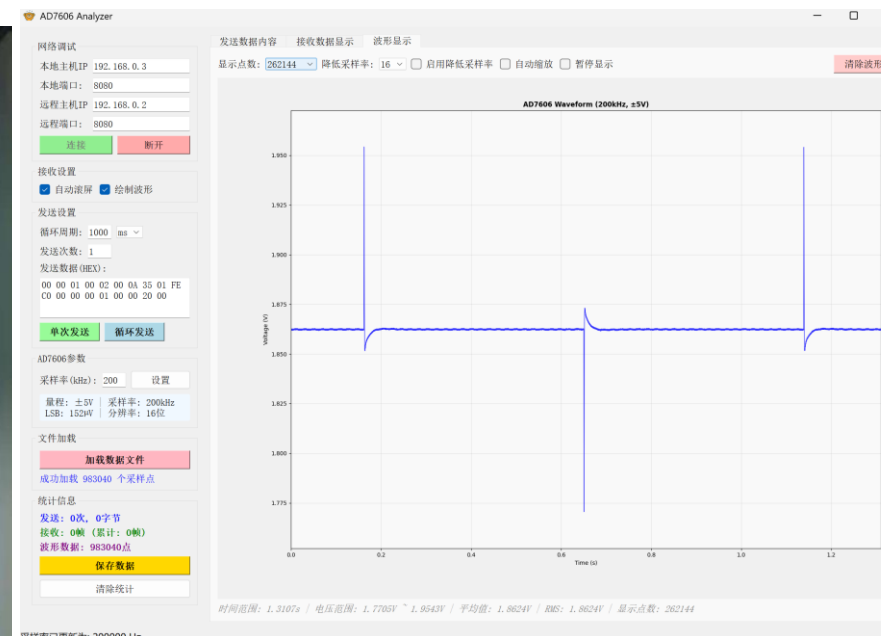
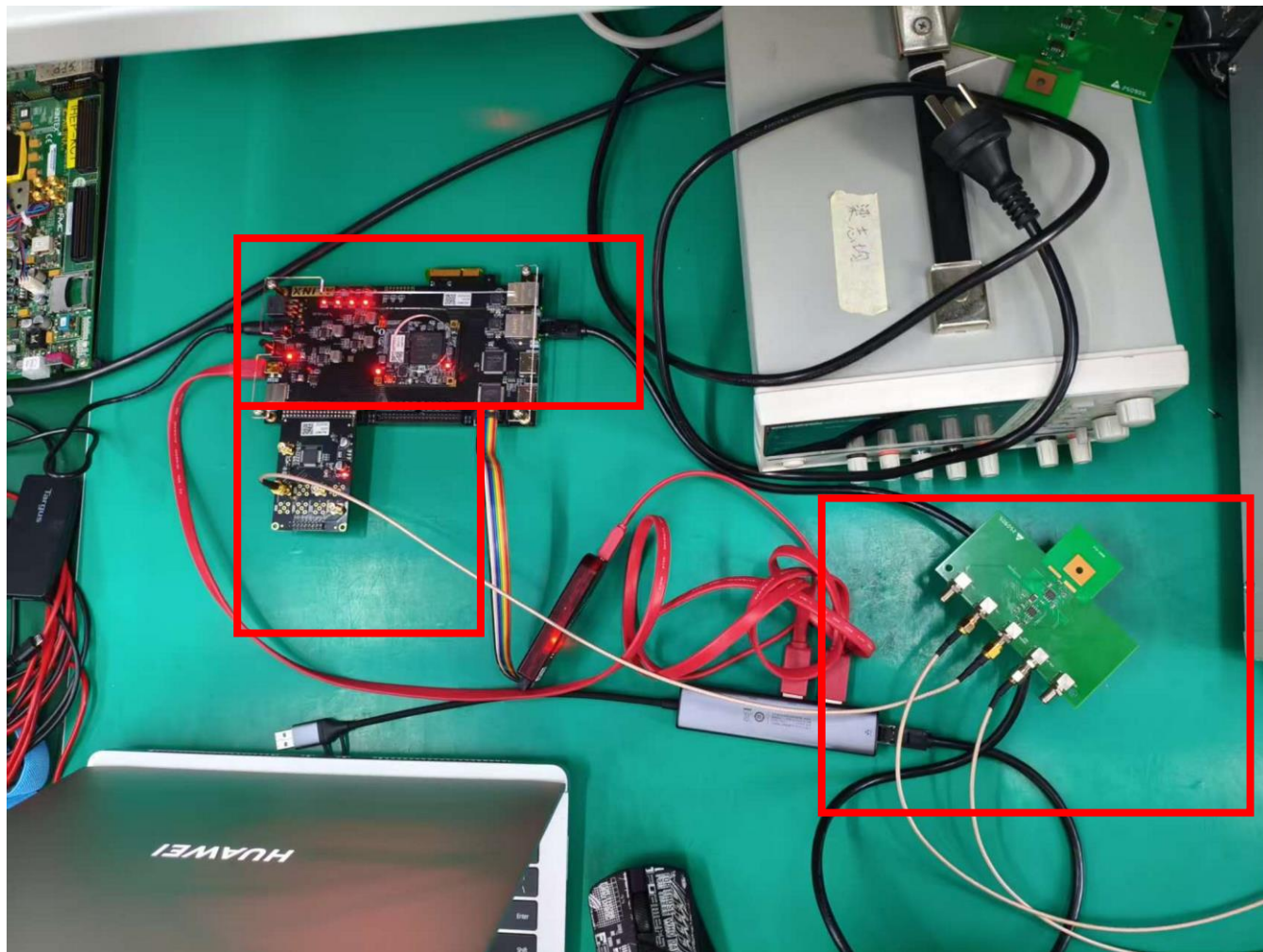
Inject 42pC of Charge

Cal_in:10nF

Cal_in:4mV



Begin a project



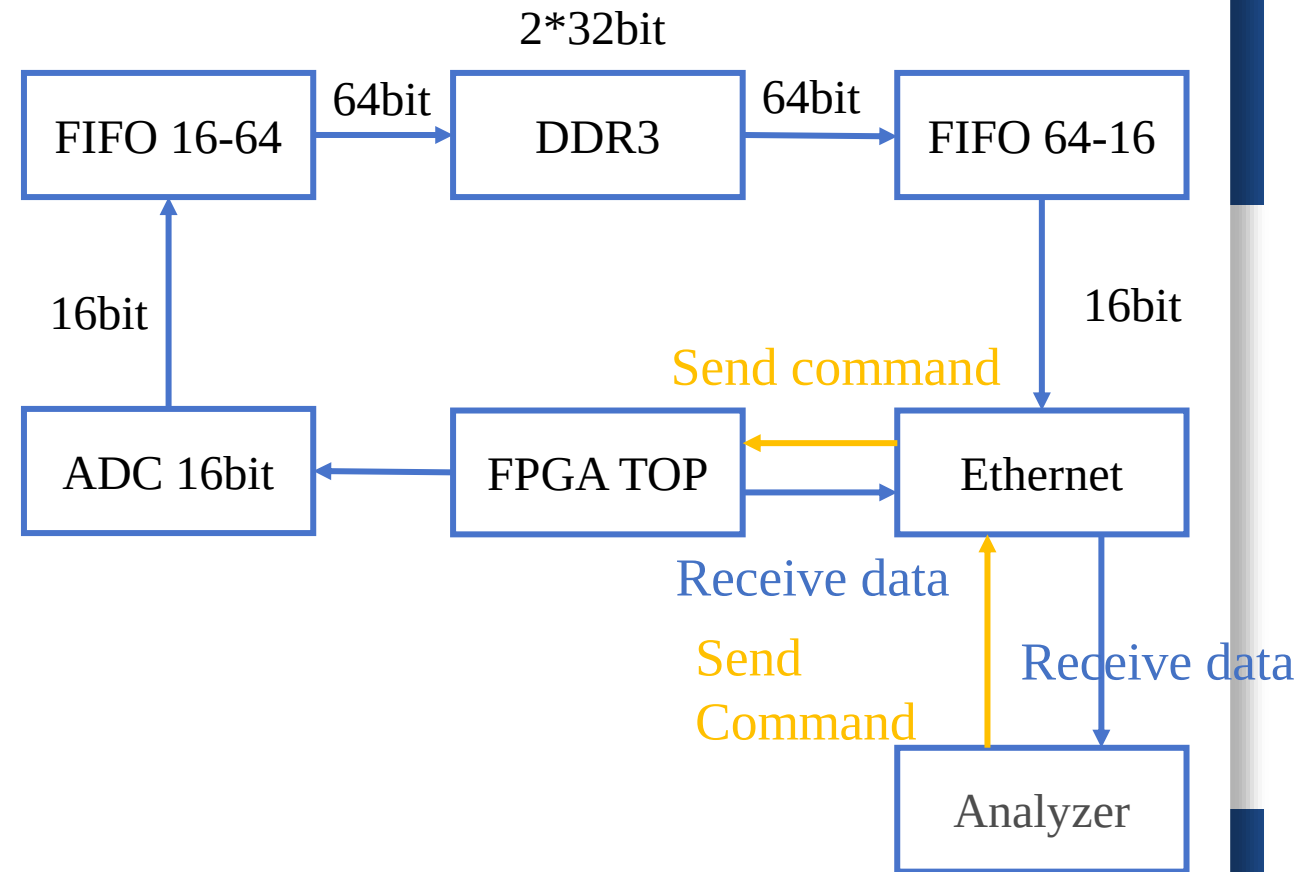
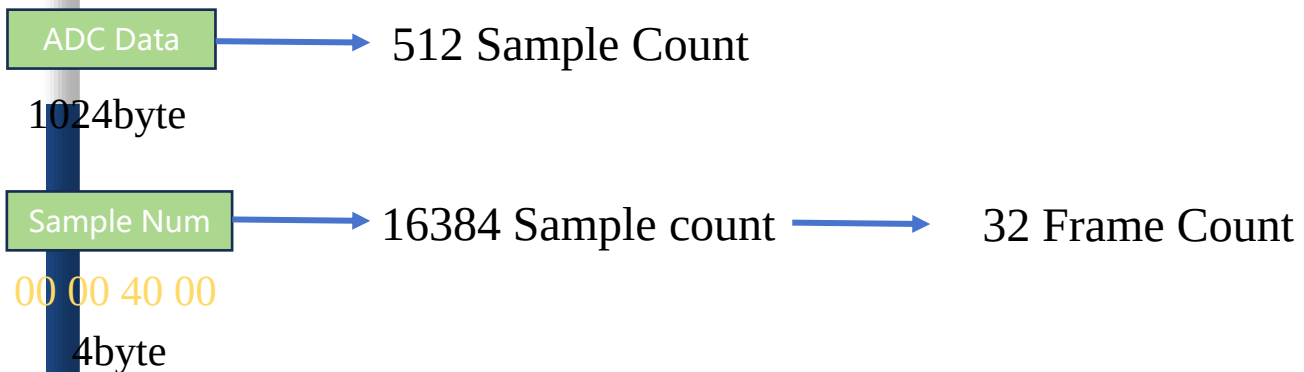
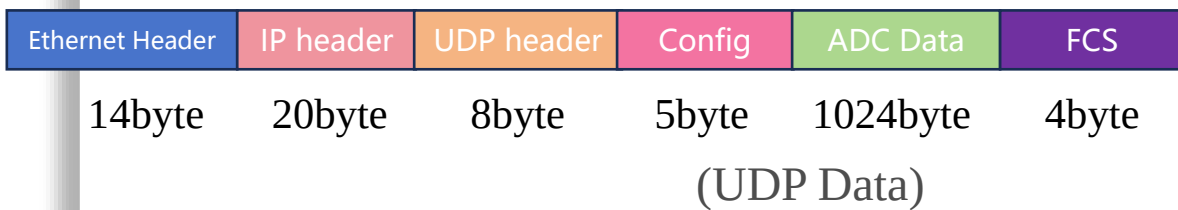
Begin a project

Send data (UDP Data)

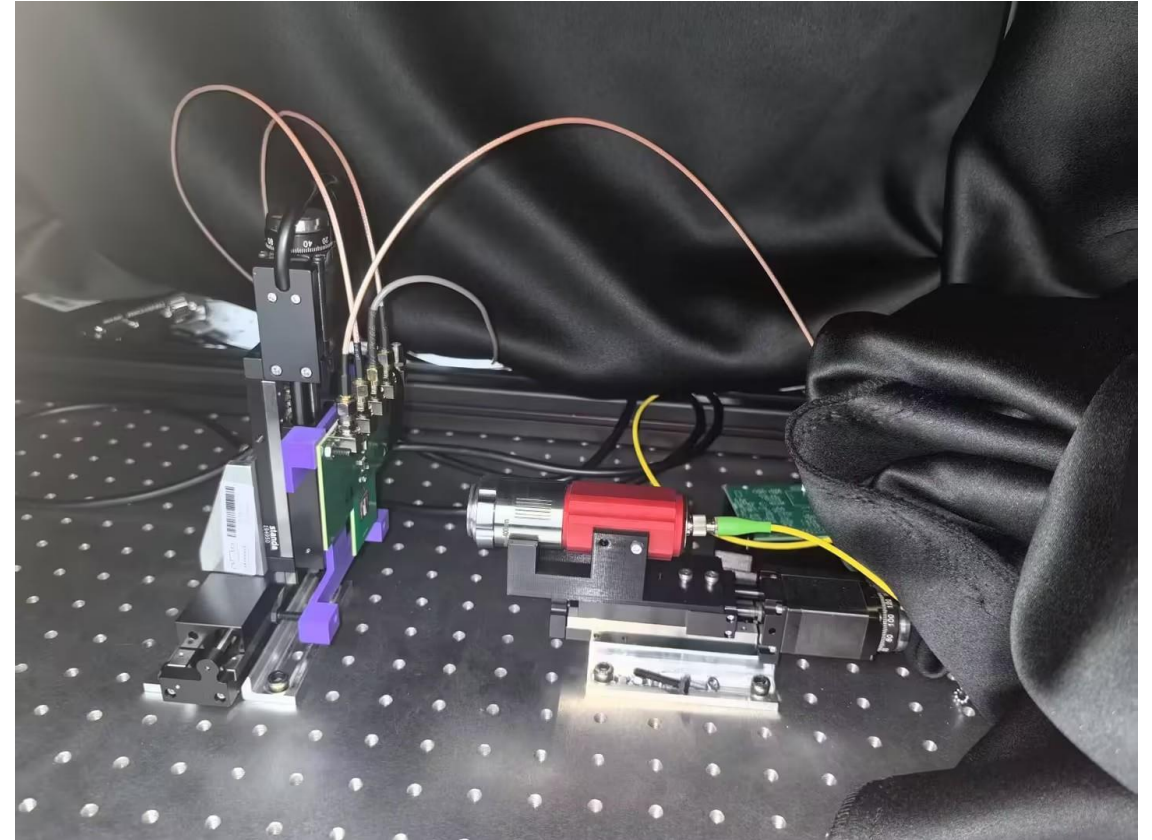


Eg : 00 00 01 00 02 00 0A 35 01 FE C0 00 00 00 01 00 00 40 00

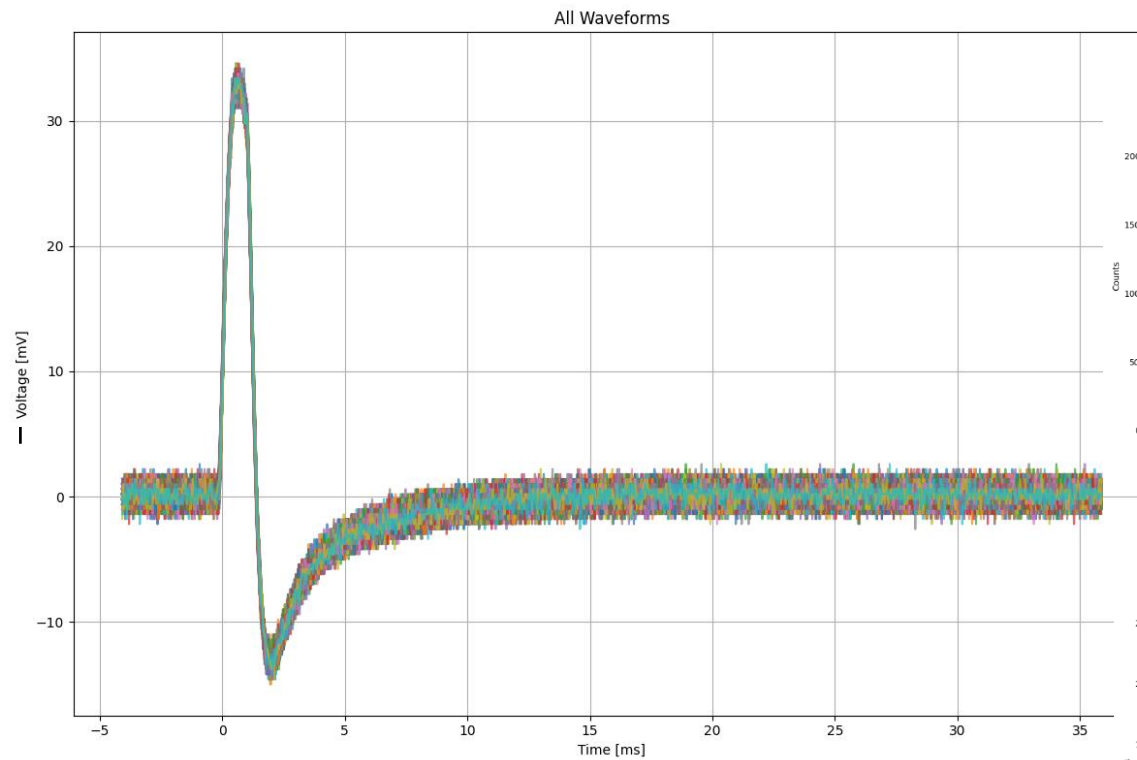
Receive data(Ethernet Frame)



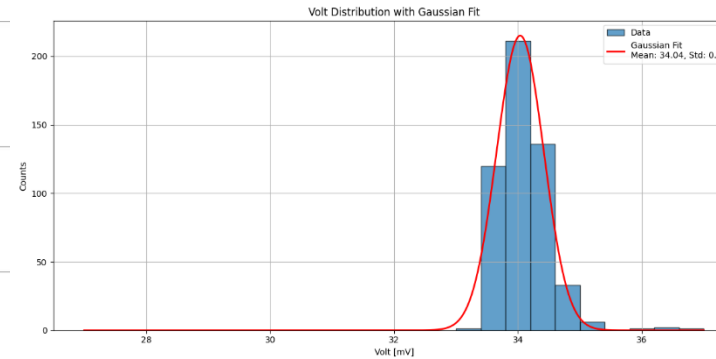
Begin a project



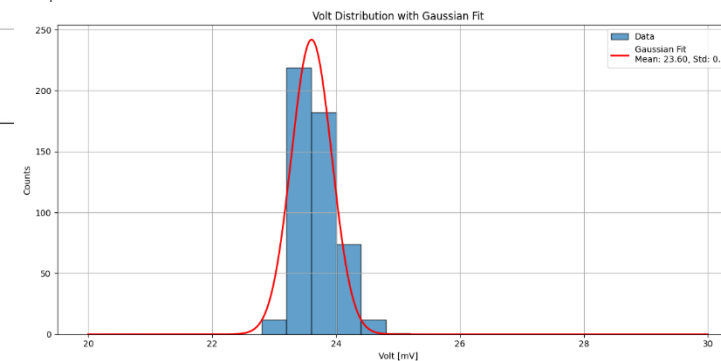
Begin a project



Tune = 0: peak: 34.04mV

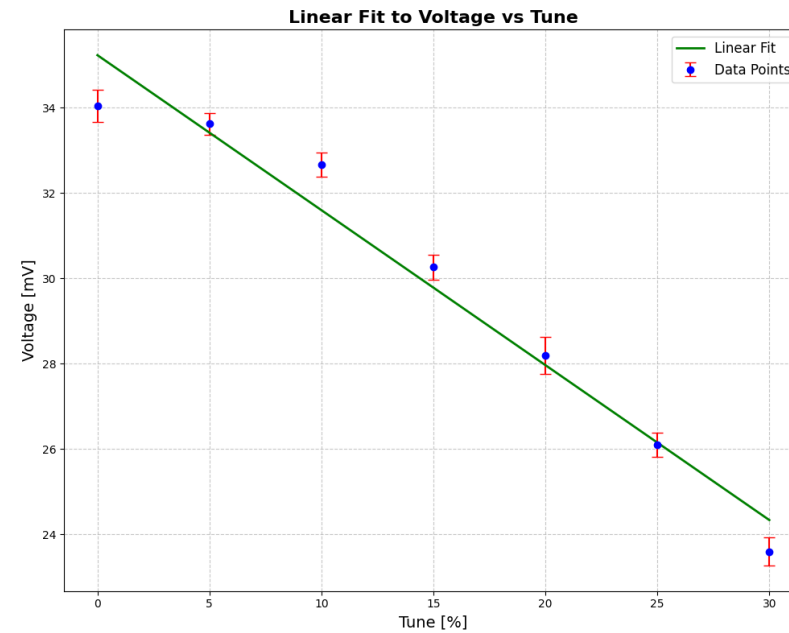
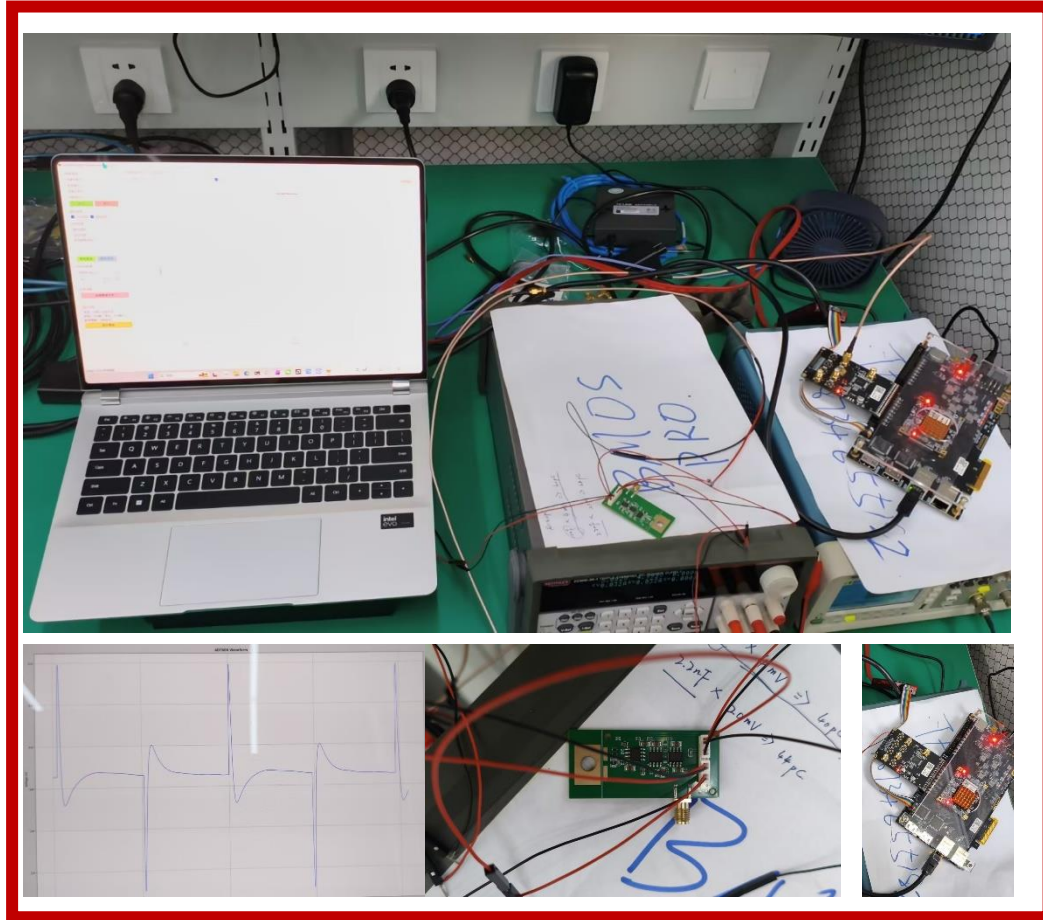


Tune = 30: peak: 23.60mV



Begin a project

BMOS system



Reach :

- Stable long time monitor
- Linear relation with e/h pairs

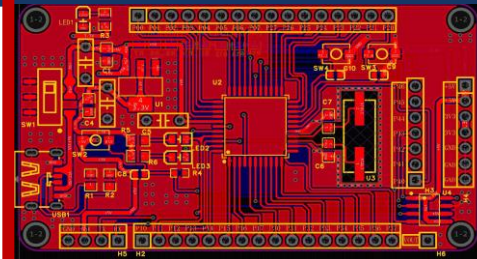
Begin a project



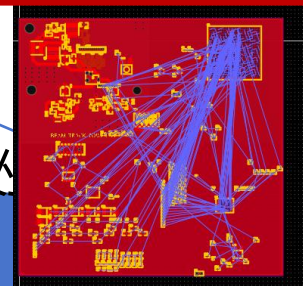
模拟信号

ADC

Adc数据进入core进行处
电荷, 展宽, 峰值



使能



Core

GPIO+升压

低压控制



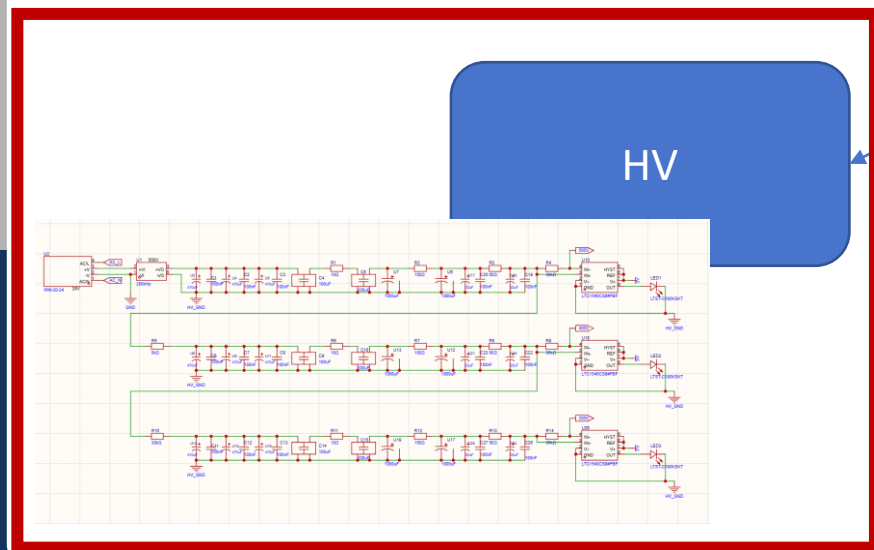
LV

HV

高压控制

温度, 电流,
工作状态

监控





Track upon the trace.

Welcome to join us!



中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

