US FCC Tracking/PID Meeting 13-May-2026 Summary

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https://indico.global/event/17982/

- This meeting originated out of the rescheduling of the international tracking meeting (5-8 May 2026 BNL)
- Leadership believed it would still be useful for this community to meet in person
- Also have been discussing a US MAPS meeting over the last 9 months
- BNL presents an opportunity to meet up with ePIC/EIC colleagues who share many of the same tracking and PID/timing requirements
- Take stock in where we are now
- What are US opportunities? Can we be more strategic?

Where are we?

- Our technical work has been funding limited
- Strong effort in place, and supported, on straw tube tracking. Status and results have been presented in a number of recent meetings
- Two funded MAPS efforts at SLAC and FNAL, but really not sufficient funding to have a large impact on the international effort yet
- Strong interest in large open drift chambers
- Novel schemes for mass reduction – CF wires
- Limited funding so far from non-US HFCC sources – LDRD etc
- Physics and performance studies – see next presentation (Christoph)
- Genesis Mission?

US Technical Strengths

- Wire chambers/straws/TPCs
- ASIC engineering at national labs with university groups – ie Penn, etc
- Fast timing LGADs, leading groups in silicon – UCSC, BNL, FNAL, SLAC, emerging SiC – LBNL, NCSU, BNL
- Low mass mechanics and materials
- DAQ
- AI/ML + industry
- Synergies with NP community ePIC/EIC, offices combined at DOE

What are important technical needs/opportunities?

- dN/dx: Electronics UM, Penn?, Gas mixtures
- MAPS – SLAC, FNAL, BNL, university groups
- Very low mass mechanics – already very active (ALICE etc) but need to gain technical capabilities more broadly in USA
- Novel low mass components and composites – ie CF wires, integrated structures, etc.
- TOF optimized for low mass and good position resolution – wrapper layers which can contribute to momentum measurement
  - Both technical developments and design/simulation/optimization
- Electronics with minimal cooling requirements
- How to control systematics in the design and function of the tracker/PID
  - Alignment, acceptance, efficiency, role in flavor tagging – all important issues for the Z pole

What could a healthy US effort look like?

- Strongly integrated into the international FCC MAPS community
- Cultivated US foundry(s) to source MAPS components
- US low mass mechanical resources – national labs and universities – are strongly engaged in both inner(pixel) and global support efforts
- Major deliverables in the gaseous tracking – for example a large drift or straw tube chamber(s)
- AI/ML developments in on-detector systems well established roles
- Leverage our experience and expertise in fast timing towards high performance wrapper layer(s)
- Concrete approaches to the control of systematic errors in the design of the tracker/PID system, integrated from the start

AM Agenda

- Intro
- FCCee Tracking: Christoph
- MAPS
  - FNAL: Artur
  - BNL: Leonardo Cecconi
  - SLAC: Caterina
- LBNL FCCee LDRD: CH, did not have time to present, but posted
- Discussion

PM Agenda

- ePIC/EIC Overview: Ernst Sichtermann
- ePIC SVT-1: Gian Michele Innocenti – ALICE → ePIC
- ePIC SVT-2: Gregor Deptuch – ASIC developments
- ePIC AC LGADS TOF and far forward: Alex Jentsch
- Monolithic AC-LGADs: Alessandro Tricoli
- Discussion

Tracking at FCCee (C.Paus)

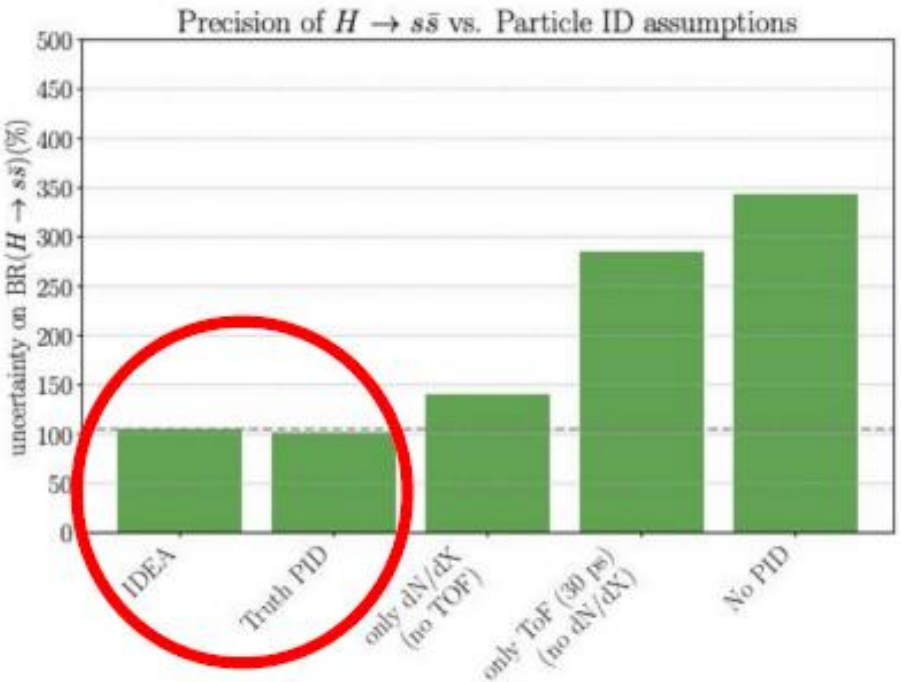
- Physics goal, run plan, requirements
- LEP trackers → FCCee tracker options
- How technology relates to resolution
- Survey of technologies – MAPS/SS, Gaseous, PID, mechanics
- PID solved? But TOF – role of an inner TOF (35-50 cm), t0 and pT cutoff
- Emphasize B field discussion, leading into
- Importance of early simulation efforts, many key studies remain to be done
  - Magnetic field
  - Tuning fast simulation
  - BIB
- Conclusions

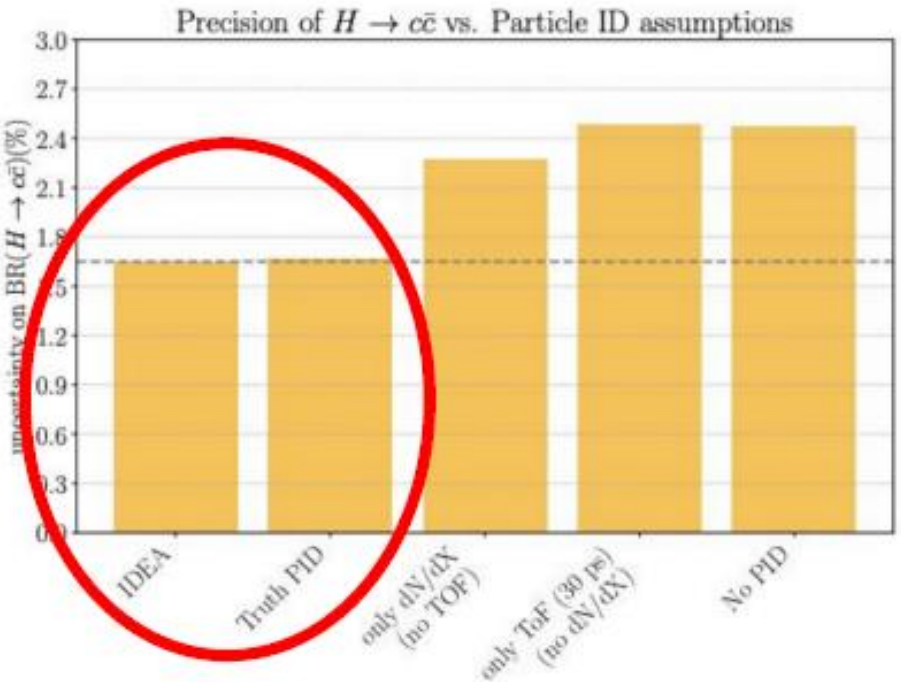
PiD challenge in theory 'solved'

Combination of known methods close to MC truth

- Version 1: Drift chamber (dN/dx) combined with <100 ps TOF
- Version 2: all silicon tracker + RICH and TOF at <100 ps
- Detailed simulations missing: ex. low momentum particles curl

US Opp.





In the plots dN/dx + TOF at 30 ps resolution was used

Early tracker simulation is essential

Is the tracker safe to operate?

- Particle rates and occupancy in particular close to the beam are critical
- Standard e+e- collisions not sufficient, beam induced background (BIB) important
- Implementation of generators still being worked on, not fully matched to experiment, remember: LEP did not do this (lower instantaneous luminosity)

Overall tracking design

- Simulation is key to test many integrated tracking designs to find the best
- What tracker configuration is best, and which magnetic field to choose ...
- Accurate fast simulation (Delphes) essential for first impressions, iterative studies
- Full simulation required to confirm many important details

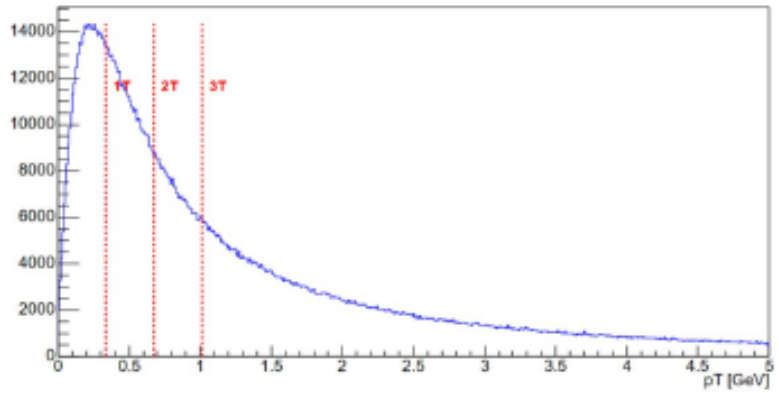
Weekly meetings in US on these topics

- Are you interested to join? Ask Jan Eysermans (jaeyserm@mit.edu) or Anja Beck (anbeck@mit.edu) to put you on the email list and join

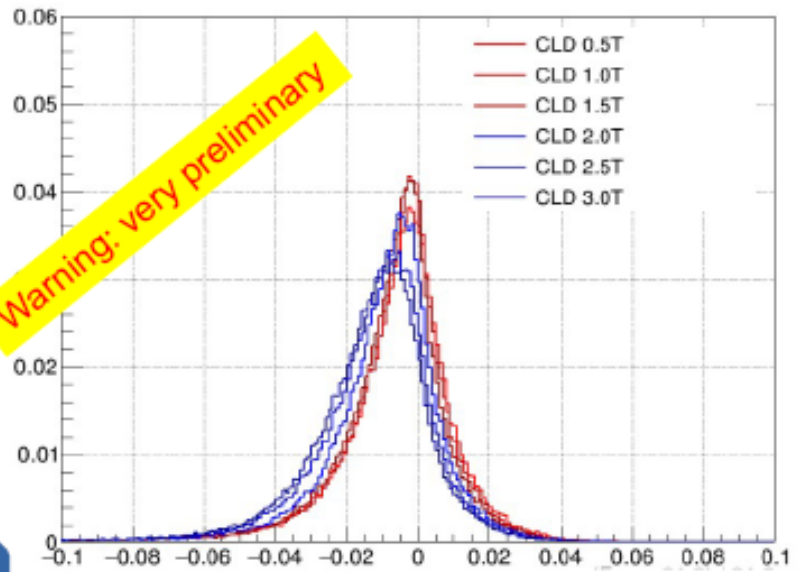
Magnetic field discussion

Some charge tracks will not reach the 'gaseous trackers' to measure momentum precisely

- Not an issue for dimuon events of course, but hadronic decays at all energy points will be affected, lost tracks are equivalent to an irreducible noise floor
- Hadronic decays are dominant and will be essential
- A full study is not trivial, because it needs to include a reasonably complete calibration process for hadronic decays
- Likely not an issue … but good to check in more detail



Hadronic Energy Resolution (qq) for CLD



US Opp.

Our "To do" list

Forming a community

- Single efforts need to expand to multi institute collaborations
- Coherent and complete detector concepts need to emerge
- Need a series of follow-up meetings

Feasibility study submitted, questions remain

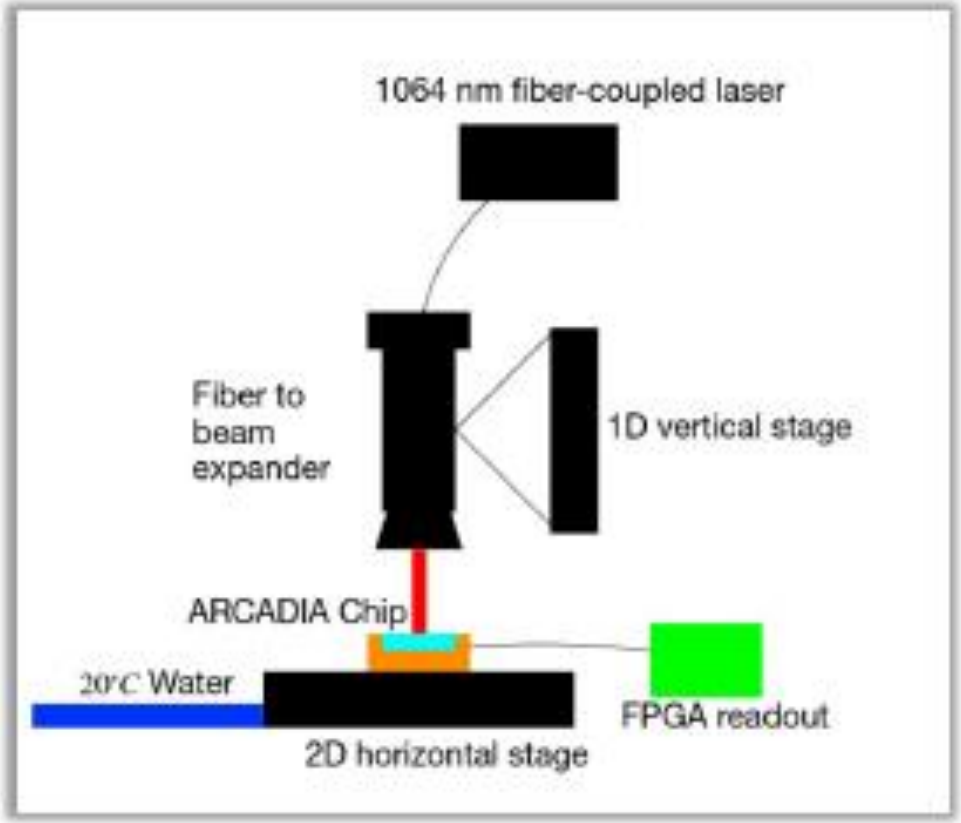
- Full Simulation study of most of everything
  - Particle ID: dN/dx and TOF and RICH
  - Can we do analog cluster counting (onboard)?
  - What gas mixtures will deliver best dN/dx at FCC conditions?
  - What is the cost of an inner precise wrapper for TOF, is it needed?
- Magnetic field: what is the right field for what period?
  - Loopers and their impact, endcap tracker design, ...

MAPS USA

- FNAL
  - Arcadia collaboration
  - Strong emphasis on (new) test and characterization capabilities – bench, test beam, HEERC facility
  - 3D MAPS project – integration of timing (LGAD structures) with MAPS
- BNL
  - Focus is working with ALICE3 (2033) to integrate knowledge from these efforts and then transition to FCCee, MOSAIX→ALMIRA
- SLAC
  - TPSCo 65 nm effort – SLAC/CERN/Brown/ORNL/Oregon collaboration
  - Looking forward to LESA test beam facility FY27, 2-8 GeV low intensity e beam

Measurements in the lab in HEERC

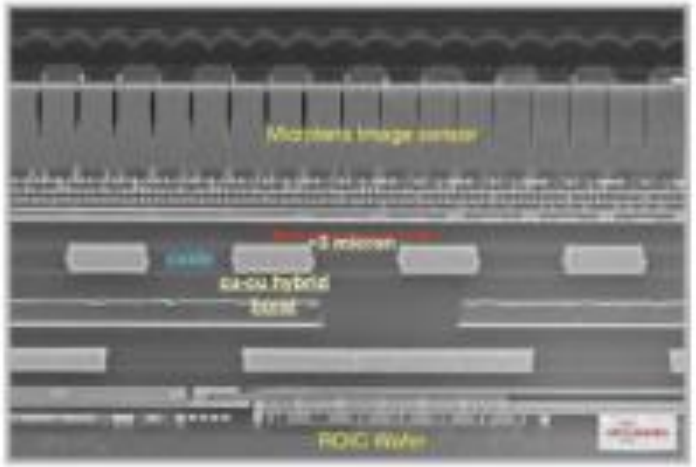
- Testing done in the new Precision Instrumentation and Timing (PIT) Lab at the Helen Edwards Engineering Center at Fermilab
  - Published in JINST 21 (***2026***) P04003



3D project

Fermilab SLAC
Lawrence Livermore National Laboratory

- The research program consists of three main thrusts towards developing the proposed detector:
  - **Thrust 1:** *Design and manufacture Low-Gain Avalanche Diodes (LGADs) devices compatible with **12" foundry processes** :*
  - **Thrust 2:** *Design application specific integrated circuit (ASIC) techniques to meet various application needs for granularity, precision timing, and power: **28 nm design***
  - **Thrust 3:** *Enable a new generation of particle detectors that utilize **3D-integration**:*



Section of the Sony Exmor camera chip showing the hybrid bond interface

CONTEXT: TWO FLAGSHIP NEXT-GENERATION EXPERIMENTS

Overview of ALICE3 at the LHC and the FCC-ee Vertex Detector

Although different in concepts and physics program, both designs push towards **deep spatial and time resolutions, high particle rate** with **significant background** processes, **minimal material budget** constraining cooling and **power consumption**

ALICE3 (LHC LS4, ~2033)

Next-generation heavy-ion ALICE experiment targeting significant improvements in tracking and vertexing performance

- Entirely silicon; first layer at **5mm, inside beam pipe (moving detector)**
- Target **2.5um** resolution at innermost layers
- Material budget at ≤ **0.1% X_0**
- Cooling, cabling limit on power consumption ~ **70 mW/cm²**
- Timing resolution < **100ns** for vertex
- Peak hit-rates (without vertex smearing) ~ **100 MHz/cm²** for *p-p* collisions
- Significant QED **background** for *Pb-Pb* collisions (under study)

[1]

FCC-ee Vertex Detector (~2040s)

High-luminosity lepton collider detector requiring the most stringent spatial resolution and material budget constraints

- First vertex layer at **~14mm**
- Target **3um** resolution
- Air cooling limit power ≤ **50 mW/cm²**
- Material budget ≤ **0.3% X_0**
- Dominant IPC **background** process
- *O*(**100 MHz/cm²**) ? peak hit-rate for innermost layer
- Timing resolution **~20ns** for vertex ? Maybe less ?

[2]

- **Enabling technologies** for silicon trackers (**MAPS**, stitching, thinning & bending,,…)
- Shift in **readout architecture concepts** (asynchronous, continuous, event-driven, …)
- Development of **design know-how**, dedicated **system prototyping and verification tools**

ALMIRA (**AL**ICE 3 **M**onolithic **I**ntegrated T**r**acker **A**SICs)
is the dedicated MAPS sensor-development project for ALICE 3

ALMIRA targets a **readout architecture**, **building blocks**, **custom IPs**, **design methodology and flow** to cover the needs of **ALICE3 silicon detectors** from vertex detector to outer tracker under a **common development**

In particular ALMIRA will target two ASICs:

- **ALMIRA-T**
  - reticle-size 20um + pitch for **middle and outer layers** (ML/OL)
  - ToA + ToT
  - < 30 mW/cm^2
  - needs to be ready **sooner** for volume production
- **ALMIRA-V**
  - large format (most likely stitched), 10um pitch optimized for the **Vertex Detector** (VD)
  - Only ToA
  - ~70 mW/cm^2 power budget

MAPS SLAC effort

Co-design approach: close interaction between physics studies and technology R&D

- MAPS developments with CERN (WP1.2 Collaboration): TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Builds on sensor optimization done for the TJ180 process[1-2], excellent charge collection efficiency and low capacitance [3]
    - Increased density for circuits: Higher spatial resolution, better timing performance at same power consumption.
  - Supports stitching: enable wafer-scale MAPS → **potential to greatly reduce costs of future experiments**
- ALICE ITS3 upgrade is the main driver of CERN WP1.2 efforts
- Several challenges towards wafer-scale devices → **large international effort needed to address all of them**
  - Large collaboration is interested in designing solutions for power distribution compatible with stitching and enabling O(ns) timing precision

[1] M. van Rijnbach *et al., Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker *et al., Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance*, 2019 *JINST* 14C05013
[3] S. Bugiel *et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, NIMA Volume 1040, 1 October 2022, 167213*
[4] J. E. Brau et al., *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, https://agenda.linearcollider.org/event/9211/sessions/5248, 2021.

Target Specs vs. State of the Art

JINST 19 (2024) 04, C04033

Chip name	Technology	Pixel pitch [μm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm^2]
Target Specification	**?**	**25 x 100**	**Sq / rect**	**1**	**< 20**
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	53
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

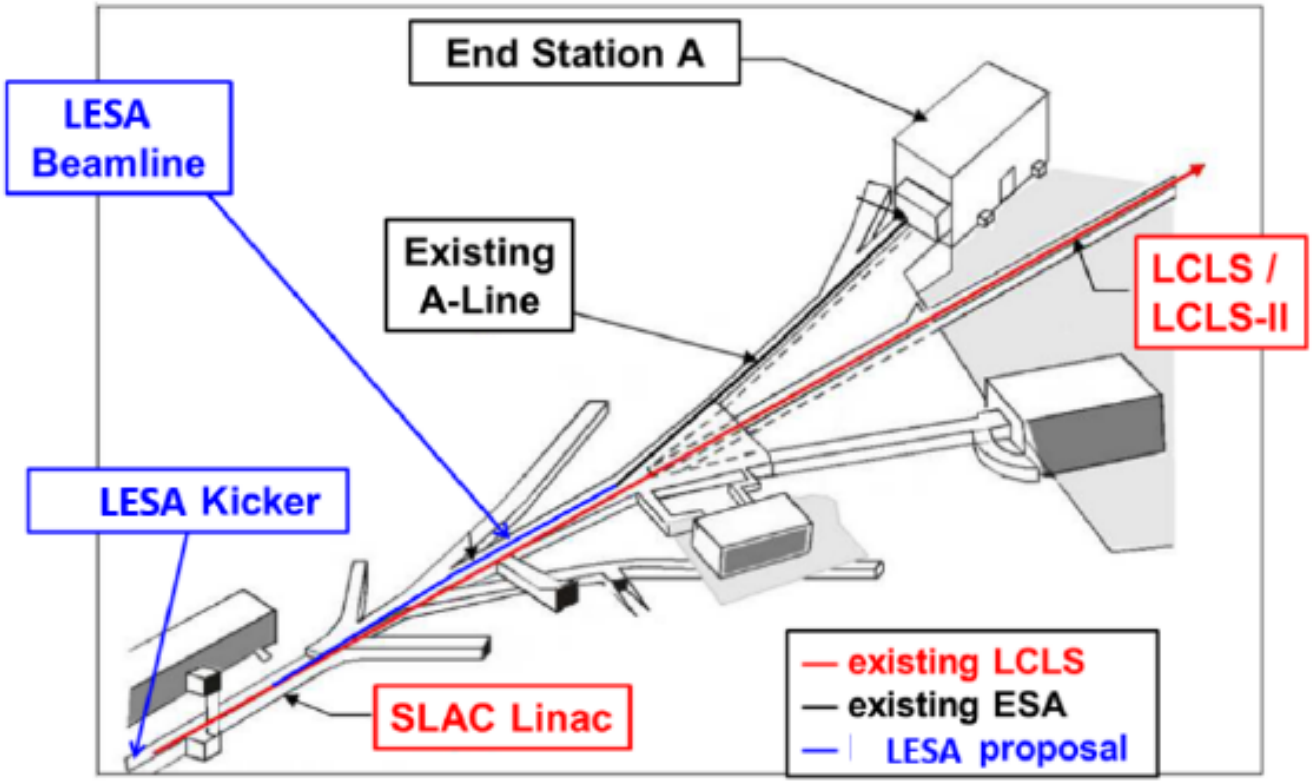
No design fulfills all target specification → The need to develop a custom design

We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

Linac to End Station A

High repetition rates, well-timed short bunches, and flexible operating modes makes it advantageous for advanced detector R&D.

Commissioning of beams towards End Station A (ESA) in late 2025, Test beam program could begin in 2027.



1–few electrons per bunch will be available at 2.0-8.0 GeV energies, with a bunch spacing of up to 10 Hz

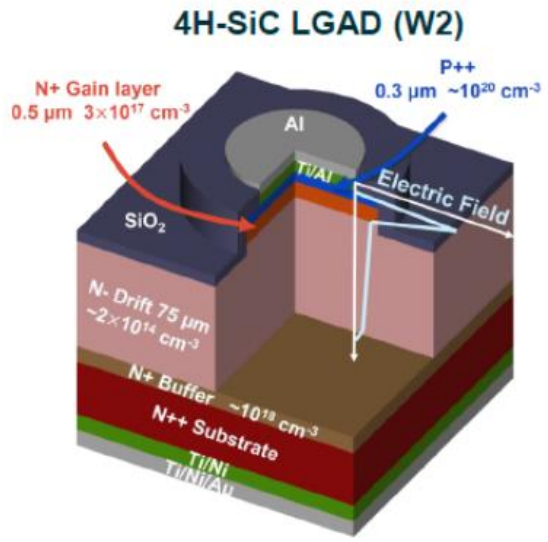
LBNL FY27 LDRD Proposal (under review)

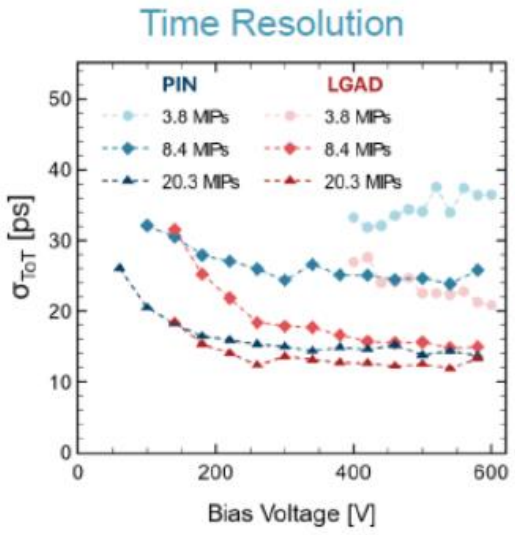
- Focus on acquiring new expertise/experience which would be relevant to a future Higgs factory
- Design, fabrication, and manipulation of extremely thin and low mass structures
- Leverage existing effort on wide-band-gap (SiC) LGADs towards the needs of an inner timing layer
- Focus on appropriate readout electronics (also WBG) and system issues

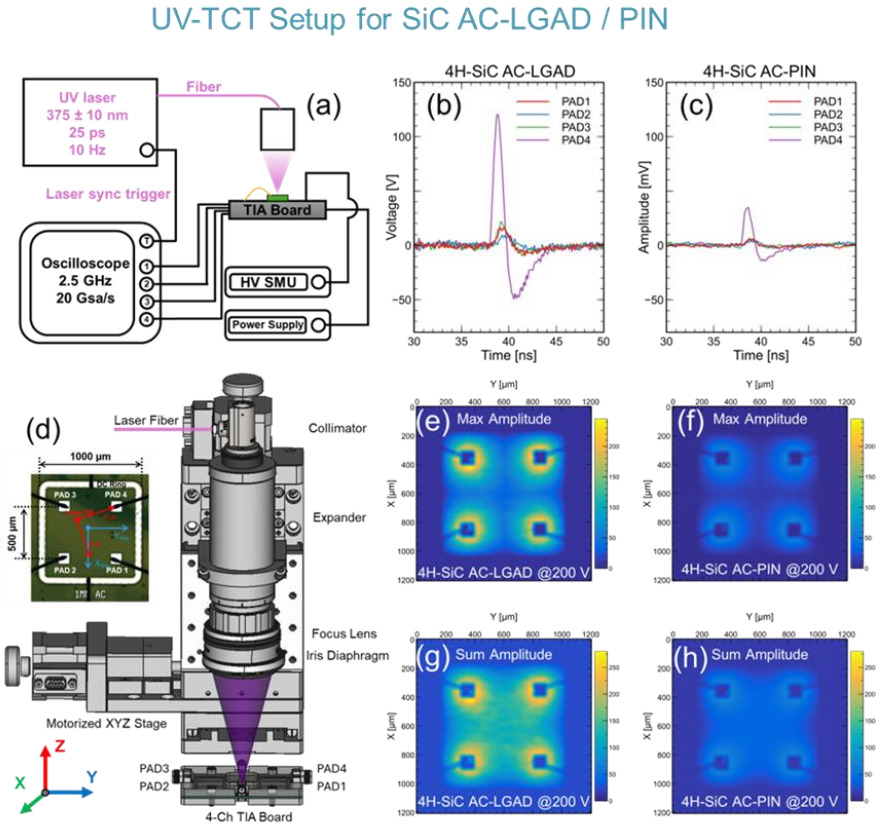
Target of Opportunity

- For high resolution tracking the B field results in a cutoff > 1 GeV at 2m
- **Solution is a low mass inner timing layer at R=0.5 m but t_res ~20 ps**

- LBNL/NCSU/BNL have developed wide-band-gap Silicon Carbide LGADs
- AC coupled with good spatial resolution (ML enhancements as well)
- **WBG/SiC = high temperature operation and very fast response**
- If implemented in a low mass layer with passive cooling and **appropriate high temperature electronics** this could be a great solution to **an INNER FAST TIMING LAYER**







LDRD Year 1 Proposal

- We propose to focus on **low mass and fast timing technologies**
- Leverages experience, facilities, and past LDRD and project investments

1. Manipulation of extremely thin semiconductors and carbon materials
2. Layout and design of a high performance inner fast timing/tracking layer
3. Emerging ASIC design using **wide band gap** WBG (SiC and GaN) processes to complement our SiC-LGAD effort
4. Simulation of extremely thin composite structures including thermal effects
5. Low mass electronic transmission lines in carbon nanotubes

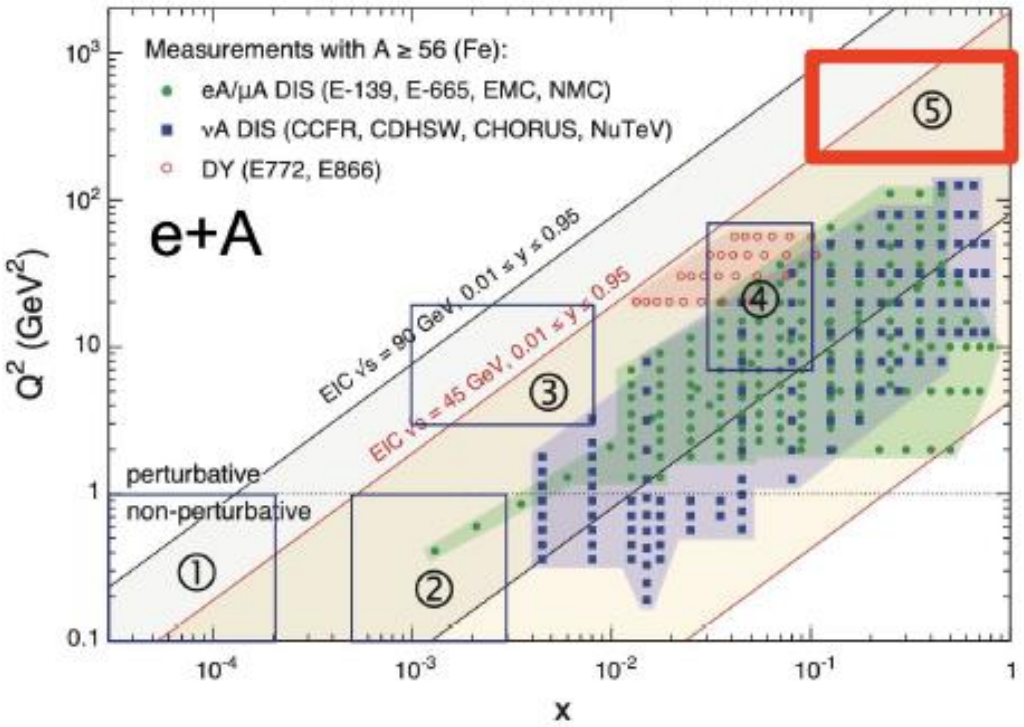
A second year would extend the prototyping of mechanical structure and include a fabrication of wide band gap ASIC

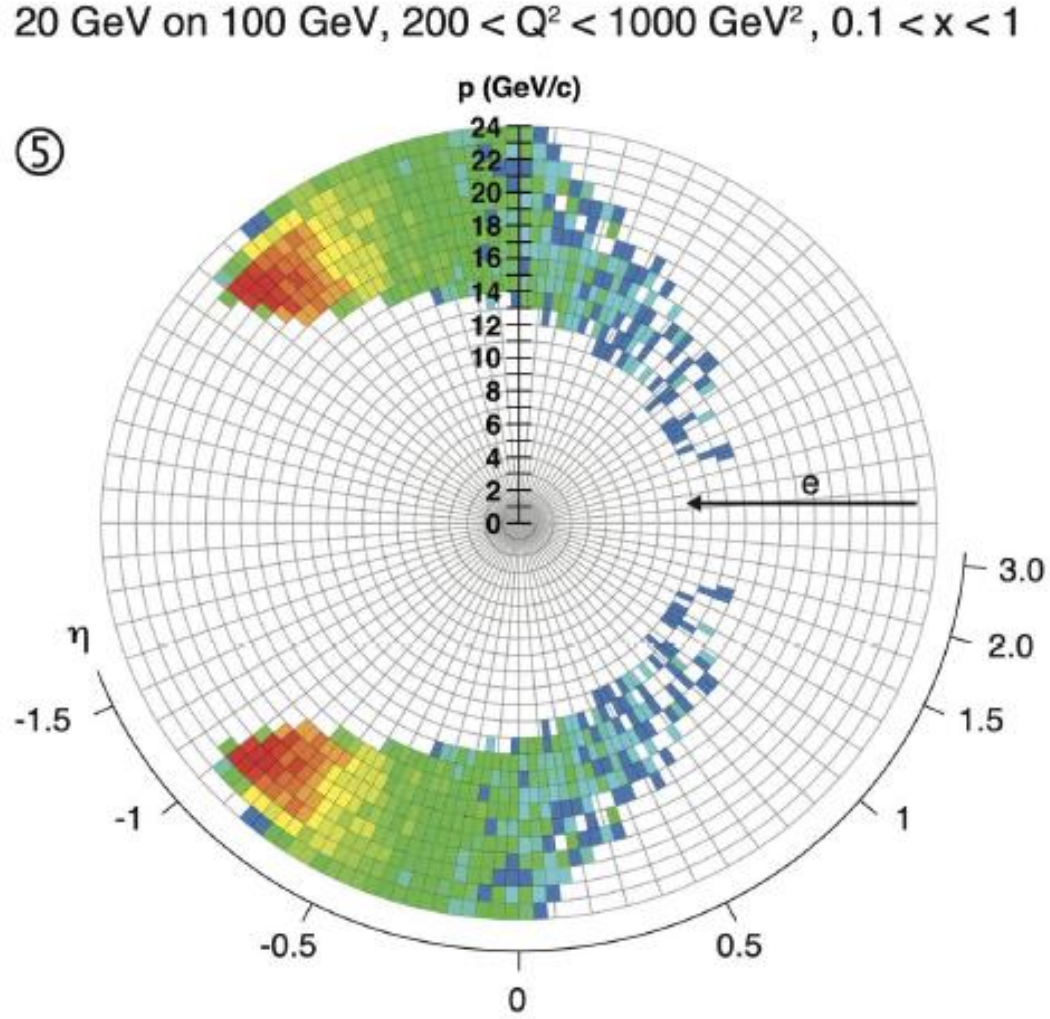
- **Eventual focus is an inner fast timing layer with only passive cooling by combining our SiC-LGADs with WBG ASICs and ultrathin supports**

ePIC/EIC Overview

- Uploading of slides are pending
- 2034 eA collisions, subject to funding and etc. delays
- Commonality of tracking requirements EIC/FCCee were clear already in the ECFA Detector R&D Roadmap
- ePIC/EIC is a deep inelastic scattering experiment in an asymmetric collider configuration. Layout of subdetectors strongly coupled to kinematics – coverage of various regions of x and Q^2 ,electron/hadron hemispheres

The energy and angle of scatter electron gives key variables x, y, Q^2





Brief Review of EIC Detector Requirements

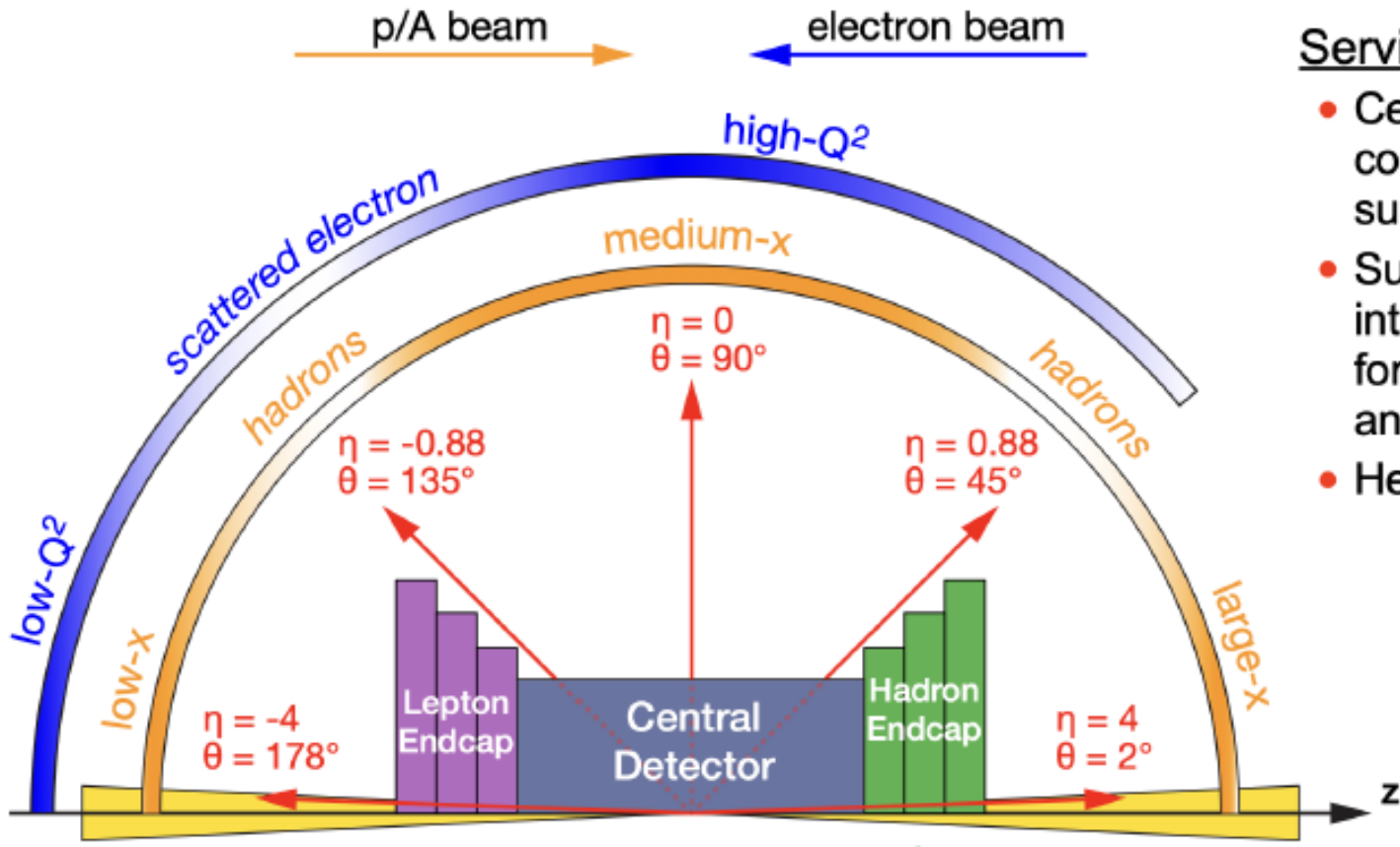
- Hermetic detector, low mass inner tracking
- Moderate radiation hardness requirements
- Electron measurement & jets in approx. -4 < η < +4
- Good momentum resolution
  - central: $\sigma(p)/p = 0.05\,\% p \oplus 0.5\,\%$
  - fwd/bkd: $\sigma(p)/p = 0.1\% \oplus 0.5\,\%$
- Good impact parameter resolution: $\sigma = 5 \oplus 15/p \sin^{3/2}\theta\ (\mu\mathrm{m})$
- Excellent EM resolution
  - central: $\sigma(E)/E = 10\,\%/\sqrt{E}$
  - backward: $\sigma(E)/E < 2\,\%/\sqrt{E}$
- Good hadronic energy resolution
  - forward: $\sigma(E)/E \approx 50\,\%/\sqrt{E}$
- Excellent PID π/K/p
  - forward: up to 50 GeV/c
  - central: up to 8 GeV/c
  - backward: up to 7 GeV/c
- Low pile-up, low multiplicity, data rate ~500kHz (full lumi)

Hermeticity, low mass, and PID requirements makes EIC detector design challenging

EIC General Purpose Detector Concept

Magnet

- Cannot affect the e beam to avoid synchrotron radiation ⇒ Solenoidal Field (common in HEP)
- Downside is missing bending power $\int B \cdot dl$ in forward and backward region putting extreme requirements on tracking (h) and calorimetry (e)

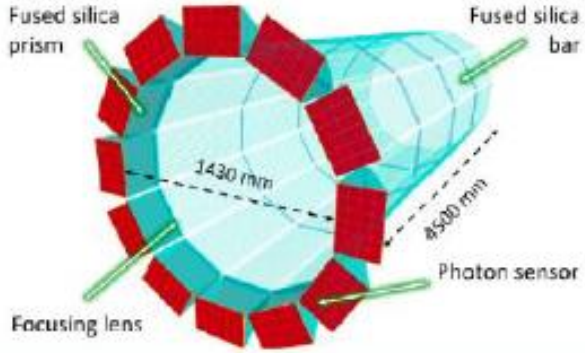


Services

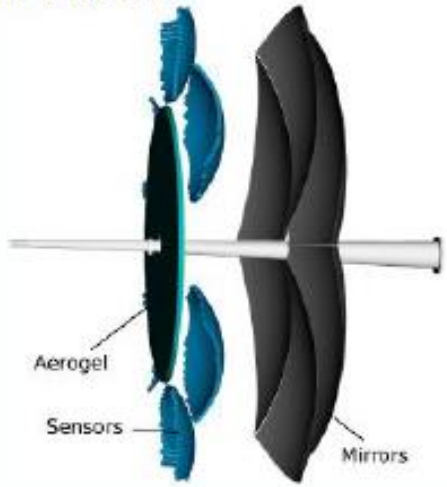
- Central detector will contain ~25 different subsystems
- Substantial integration challenge for power, cooling, and data services
- Hermeticity?!

Particle ID (PID)

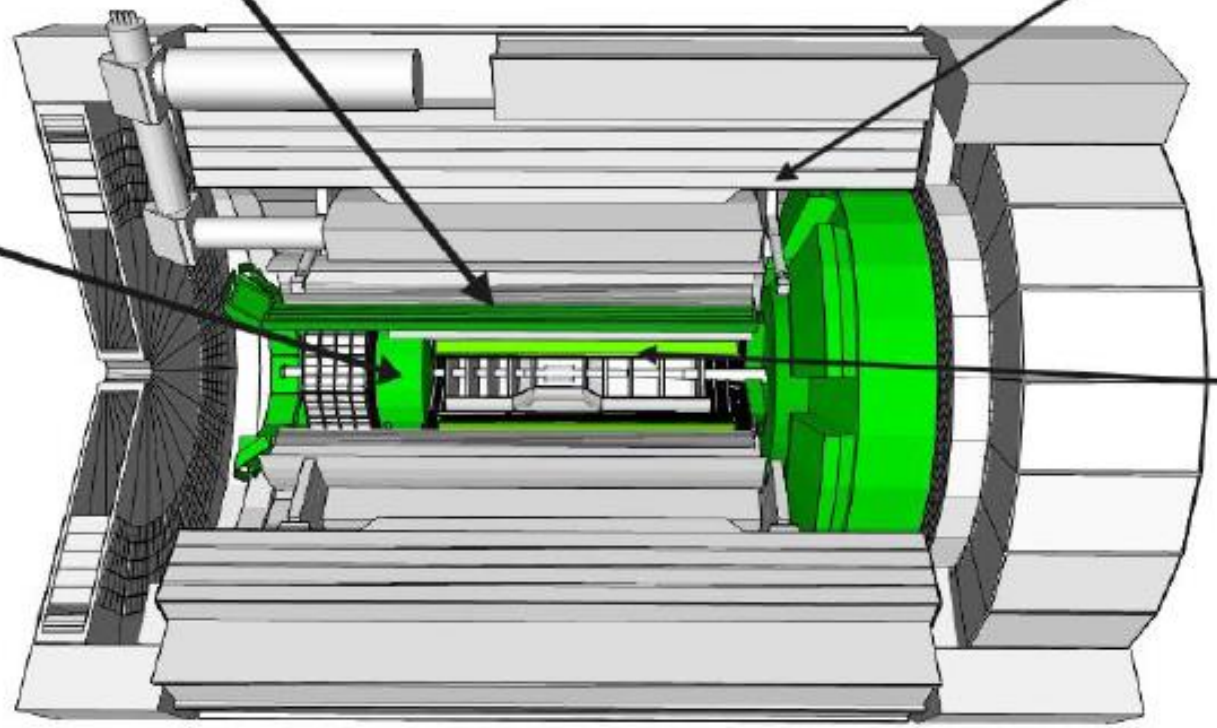
High-Performance DIRC (hpDIRC)

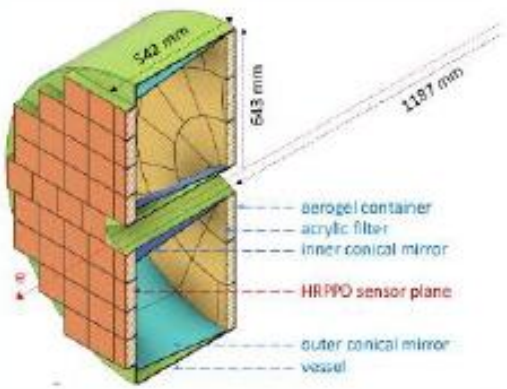


Dual-Radiator RICH (dRICH)

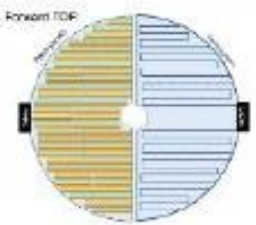


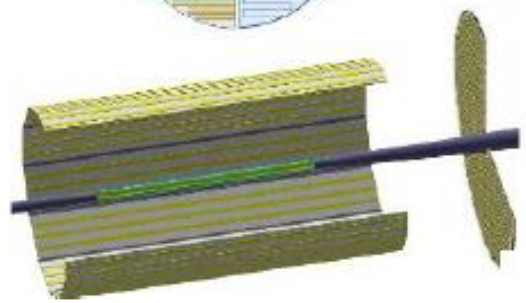
Proximity Focusing RICH (pfRICH)





Time-of-Flight (ToF)





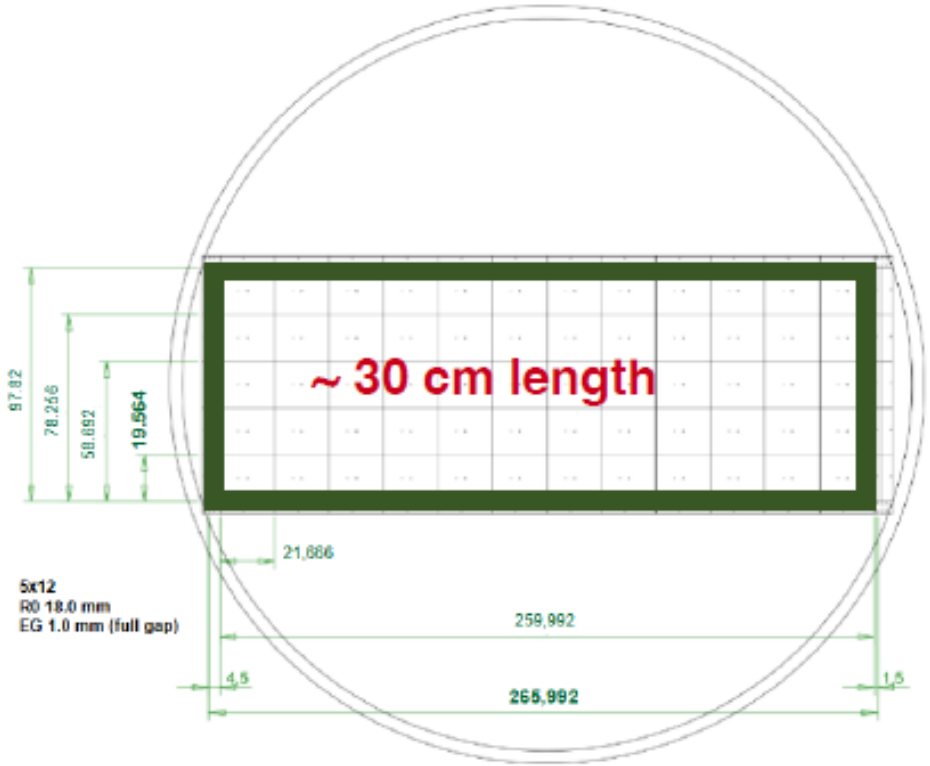
ePIC-SVT1

- Extensive review of ALICE ITS3 effort which dramatically advanced the state-of-the-art
  - Relatively large bent sensors
  - MOSAIX architecture
  - Jumping off point for ePIC application (and FCCee?) MOSAIX → LAS
- ePIC LAS changes driven by coverage, reduced hit rate, mass, integration, powering…
- But scale demands a new approach to testing
- Next challenges – data aggregation, application of ML to readout

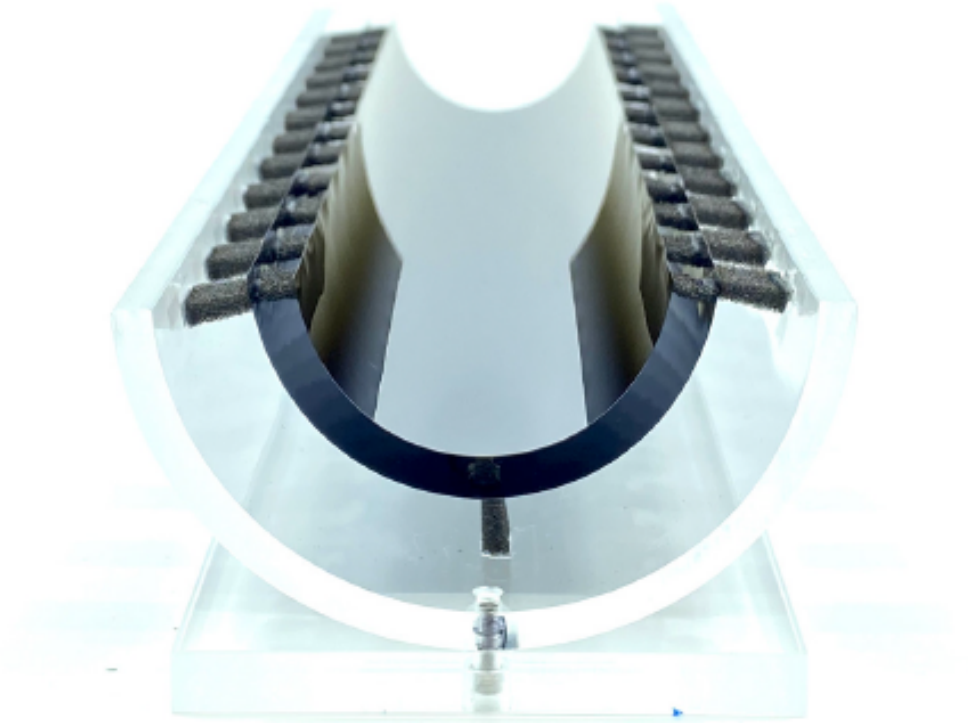
MOSAIX: stitched, bendable large-area MAPS

ALICE ITS3, CERN-LHCC-2024-003

The size of the photomask limits the monolithic sensor area
→ **Stitching overcomes that limit**



ALICE ITS3 prototype



- large sensors **with "stitching" techniques**
- **thinned** to ~40-50 µm
- **bent like paper into cylindrical layers!**

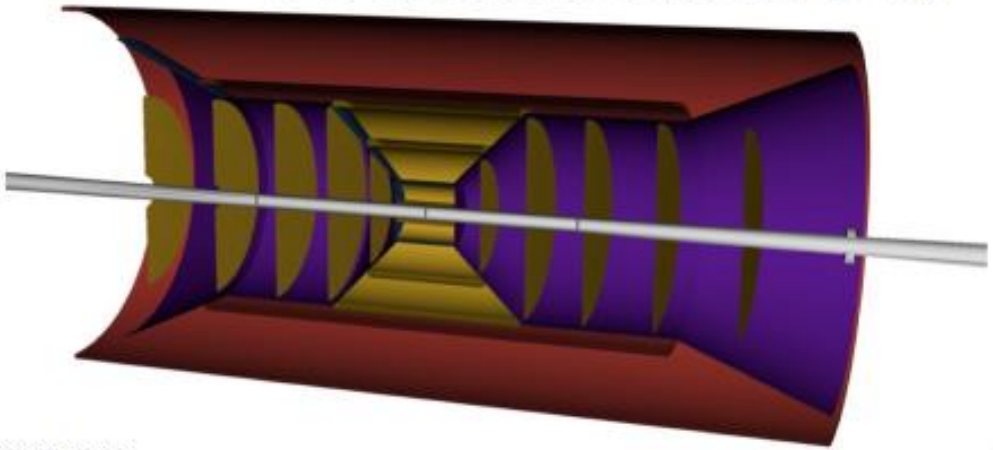
Technology proposed for the Inner layers of ALICE Inner Tracking System 3 (ITS3) for Run4:
→ now chosen as the pixel technology for the future ePIC tracker at the EIC

Silicon Vertex Tracker for ePIC: detector concept

ePIC SVT: from ITS3 concepts to a U.S. detector program
→ **First large-area hermetic detector using next-generation MAPS: ~ 8 m² of silicon**

ALICE ITS3

ePIC silicon vertex tracker (SVT)



Inner Barrel (IB)
3 layers with bent MOSAIX sensors

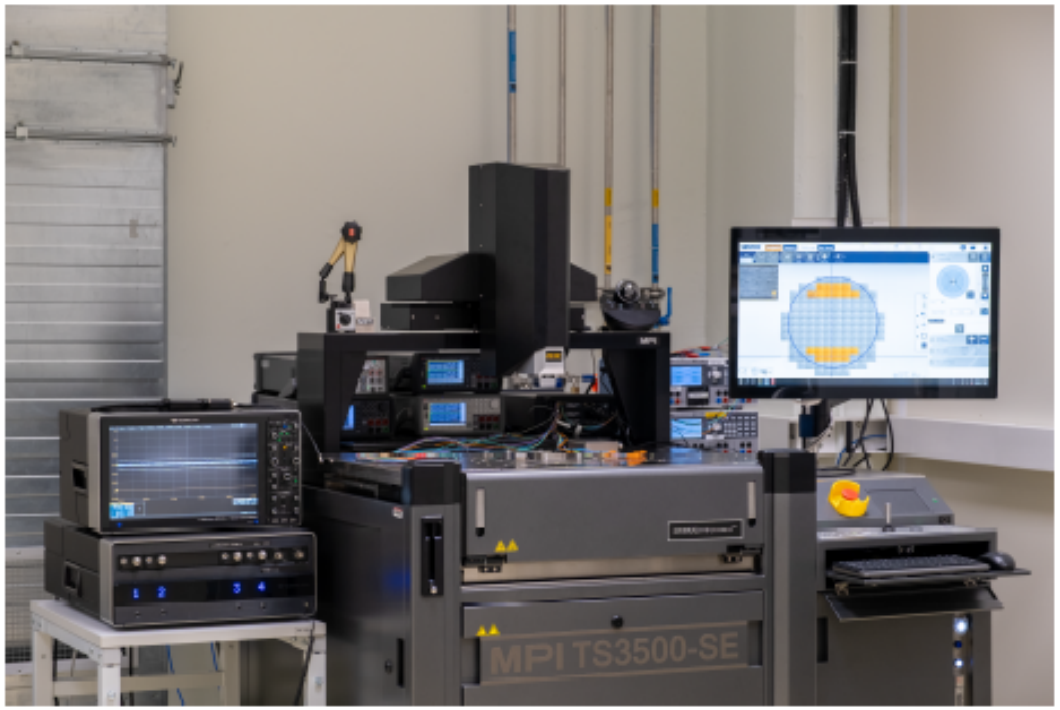
Outer Barrel (OB) and disks:
EIC-specific large-area sensors (LAS) derived from MOSAIX

- Build on strong CERN/LHC partnerships to mature MOSAIX technology
- **Lead the developments of next-generation technology for large-scale applications of MAPS sensors**

Ancillary chips for powering, biasing, and slow control

Large-scale sensor characterization using vertical probing

SVT introduced industry-style sensor testing into our community
→ Full characterization on non-diced wafers



MIT equipment located in the CERN DSF

MPI TS-3500 SE Automated test system acquired by MIT
300 mm (12”) wafers, fully optimized for large thin sensors
→ **installed in the CERN Departmental Silicon Facility (DSF)**

A growing team supported by the EIC project, closely working with the CERN MAPS/microelectronics team
→ **strategic resource for ePIC and beyond**

U.S. institutes are now leading the development of new techniques that are changing the way we perform testing in high-energy and nuclear physics

ePIC-SVT2 – Beyond the ePIC baseline

- Series of test chiplet submissions – ADC, driver, transmission, front end
- 3D stacked MAPS – to add additional functionality
- anASIC – support/control and power management

Motivation for 3D-stacked MAPS layers

Physics-Driven Detector Needs in Lepton-Collider Environments

– Operation in regimes dominated by synchrotron and beam-induced X-ray backgrounds in the vertex and inner tracking regions.
– Exceptional vertex resolution, low-momentum tracking performance, and ultra-low material budgets precision ⇨ physics goals (Higgs couplings, flavor / heavy-quark tagging, τ physics, rare decays).
➡ Common need for detectors that remain performant in background-dominated conditions, not merely higher-granularity versions of today's planar pixel sensors.

Rethinking "AI at the Edge" for Vertexing and Tracking

– AI/ML models inside pixel sensors are power- and area-prohibitive, and lack access to contextual information ⇨ ineffective.
– For vertexing and tracking, meaningful intelligence must be architectural, not algorithmic: shaping what data are generated, when they are generated, and what metadata accompany them.
– AI is to be downstream, operating on detector outputs that are already structured, sparse, and information-rich.
➡ AI-suited rather than "AI-embedded" detectors: early correlations, directionality, quality flags, and uncertainty information.

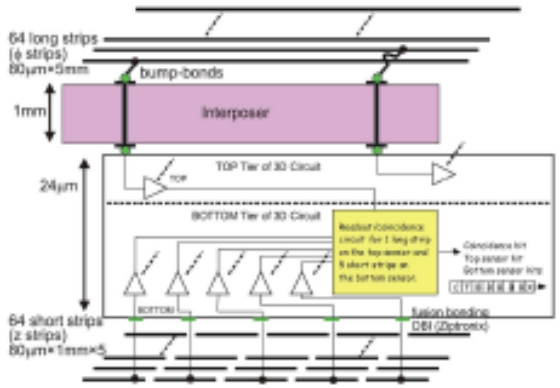
Intelligent Stacked MAPS as an Enabling Architecture

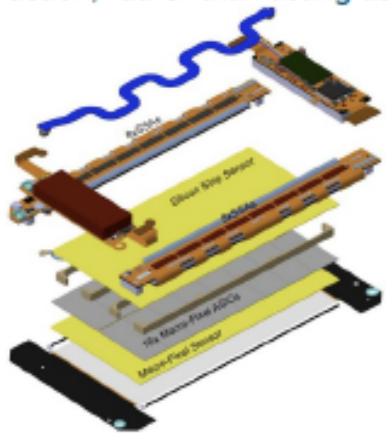
– Stacked MAPS with vertically integrated sensing and processing tiers and event-driven operation.
– Local coincidence, charge/timing correlation, and simple topological logic to reject X-ray background and identify correlated hits.
– Early tracklets and directionality metadata inside the detector before full readout.
– Only background-cleaned, correlated data to higher-level acquisition and reconstruction.

Impact on Tracking, Vertexing, and System Design

– Early tracklet formation reduces hit combinatorics and lowers downstream computational load.
– May enable fewer layers, optimized spacing, alternative topologies, while maintaining or improving physics performance.
- Establishes a path toward detectors that actively participate in reconstruction, rather than acting as passive imaging devices.

L1 trigger in the tracker upgrade of the CMS experiment at SLHC using the VICTR chip (Deptuch et al., IEEE Trans. on Nucl. Sci., Vol. 57, No. 4, AUGUST 2010)





exploded view of the PS module: key components are: the strip sensor (yellow), MPAs (grey) and the macro-pixel sensor in the central part of the module. (M.Osherson CMS collab. 2022 JINST 17 P06039)

Brookhaven National Laboratory

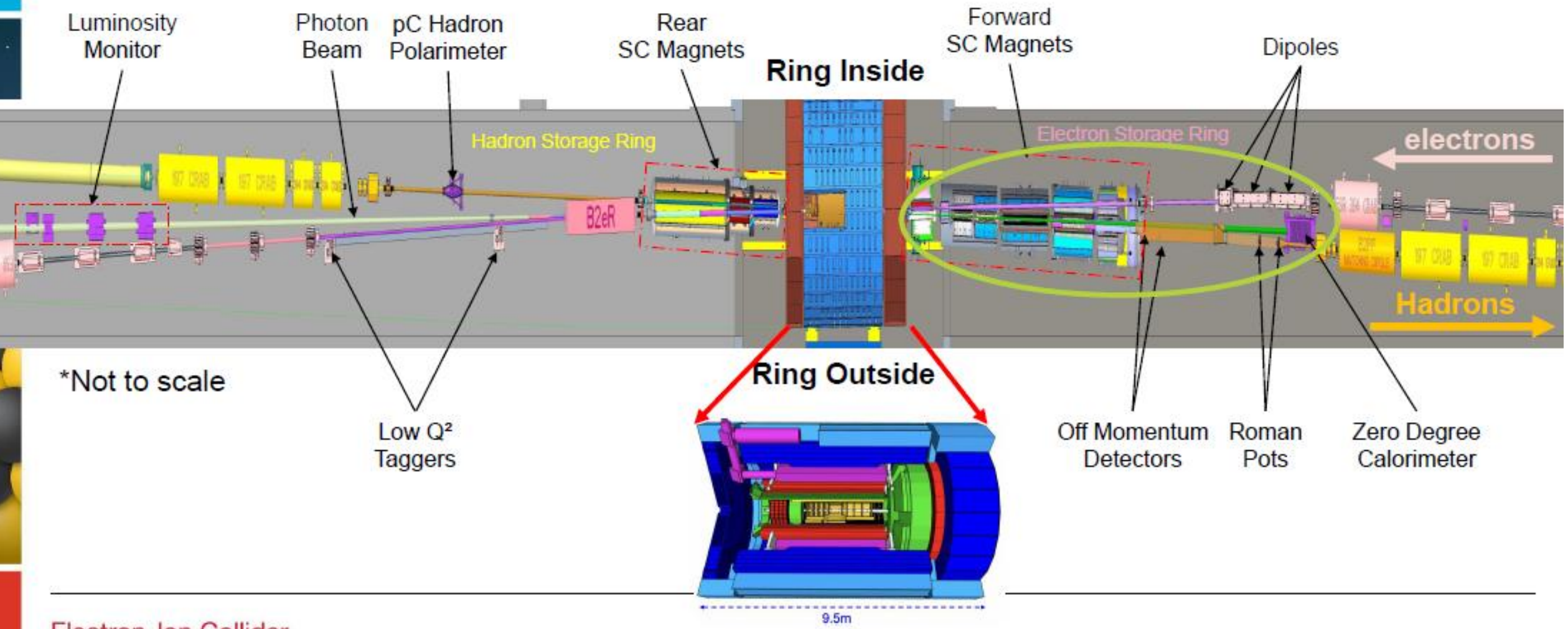
Why AncASIC?

- ePIC SVT contains tens of billions of MAPS pixels tracking system, creating stringent requirements on scalable power and control distribution.
- Outer SVT barrel layers and disks adopt serial powering to minimize material budget, cabling complexity, and power distribution overhead.
- AncASIC_XT011 was developed as a dedicated support ASIC enabling serially powered MAPS operation in the ePIC SVT environment.
- The ASIC integrates multi-domain shunt regulation to stabilize power delivery across chained detector modules.
- AncASIC provides programmable negative bias generation required for depletion and operation of radiation-sensitive MAPS sensor volumes.
- The chip is implemented in XFAB 0.11 µm HV PD-SOI technology, enabling isolated substrate islands and improved radiation tolerance.
- Thin PD-SOI substrate suppresses back-gate effects and improves resilience against ionizing radiation and single-event effects.
- AncBrain, the embedded custom processor operating at 160 MHz, manages communication, monitoring, synchronization, and system control.
- AncASIC interfaces directly with lpGBT ePort links and supports daisy-chain operation compatible with one ASIC per MAPS module architecture.
- Integrated monitoring functions include voltage, temperature, leakage current sensing, ADC-based diagnostics, and programmable synchronization strobes for autonomous sensor readout.

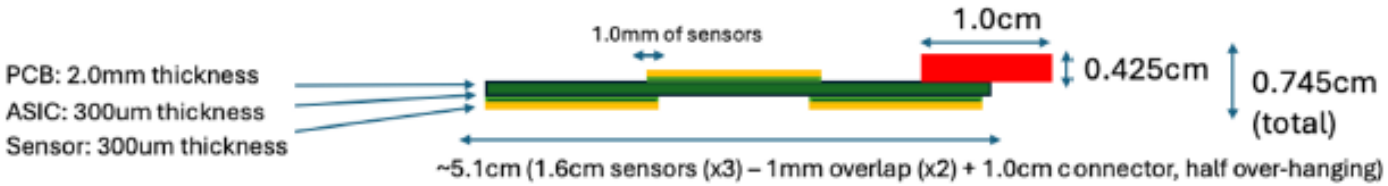
ePIC TOF and far forward detectors

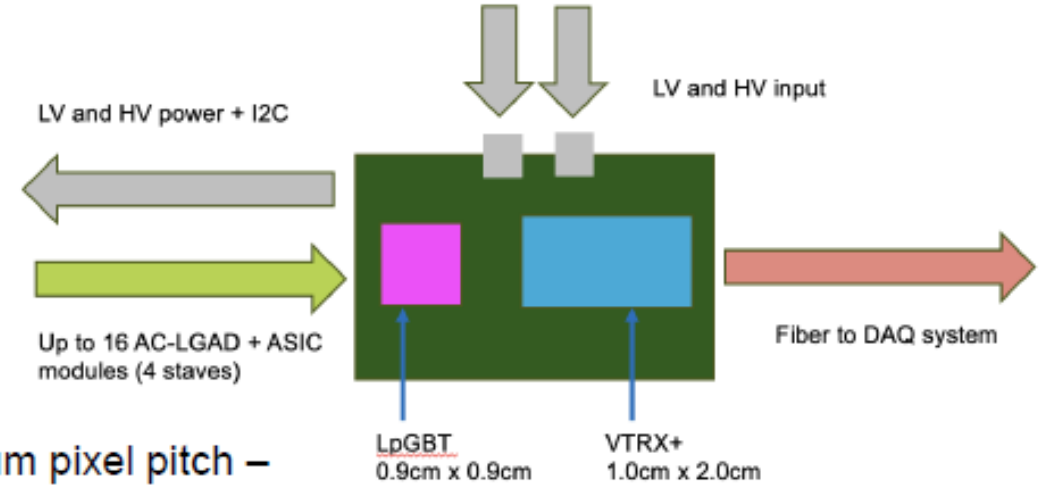
- Extensive discussion of AC-LGADs deployed in the far forward system
- Commonality of implementation with “central” TOF
- Performance results of AC-LGADs from BNL
- Presentation of EICROC dedicated readout ASIC for LGADs at EIC
- Excellent results presented on spatial and temporal resolution when integrated with EICROC ASIC

ePIC Far-Forward Detectors



AC-LGADs for FF Tracking and TOF





- Sensor "staves" will have three 1.6cm x 1.6cm AC-LGADs with 500um pixel pitch – bump-bonded to **EICROC ASICs****, staggered on a two-sided PCB to provide full active-area coverage.
  - These sensors have 32x32 channels, matching the EICROC.
- Sensors, ASICs, and Front-end readout/power will share design with the Forward TOF → only difference is sensor stave/module, and the separation of the FEB for flexibility for FF detector needs.
- Stave dimensions will be updated once EICROC1 schematic is in-hand.

**EICROC is a new ASIC specifically for the pixilated AC-LGADs in ePIC.

Summary

- ePIC far-forward subsystems are leveraging new technologies to meet EIC physics needs.
- Integration of the subsystems into the beamline a significant challenge → lots of interdependence.
- Cooling systems in early design stage, along with motion systems and supports → depends on the machine, as well, so lots of communication to satisfy all requirements.
- **AC-LGADs**
  - Sensors chosen due to capability to provide precise timing (~35 ps) and spatial resolution (~ 20um, or less).
    - Demonstrated with 4x4 channel sensors in test-beam, and with same sensors + early ASIC version.
    - Timing a primary capability of LGADs, in-general (FF has less-stringent requirement compared to TOF).
  - Spatial resolution delivered via charge sharing (500um pixels → normally deliver ~ 140um spatial resolution, beam tests show ~20um possible with charge sharing).
    - Especially important for the B0 tracking.
  - Sensors irradiated to 1e15 neutron MEQ → almost no change in gain up to that point, ~ 2-3 orders of magnitude more than expected ePIC irradiation in first 10-15 years.
  - Power consumption of the ASICs expected to be ~ 1-2 mW/ch (~ 250W upper bound per layer of Roman pots).

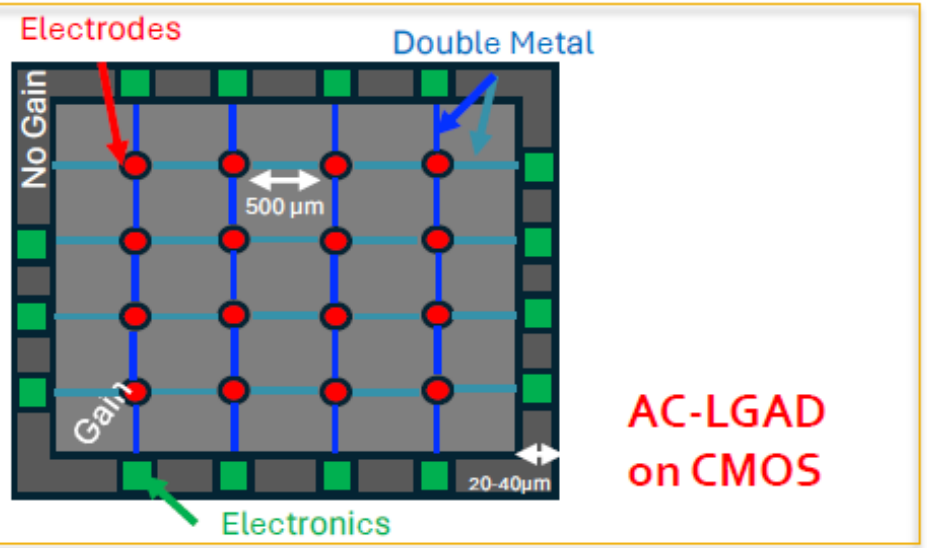
Monolithic AC-LGADS

- Effort embedded in the broader “4D-Tracking” community
- Targets “silicon wrapper” and/or TOF layer(s)
- Surveyed a variety of technical implementation underway
  - Europe: CASSIA, MadPIX, Cactus-GL
  - US/Japan (BNL et al): LGAD on CMOS, SOI AC-LGAD
    - LGAD on CMOS – double metal, electronics on the periphery
    - Vendor survey for SOI fabrication: LAPIS and XFAB
- Use of machine learning for signal processing from AC-LGAD to improve position resolution*

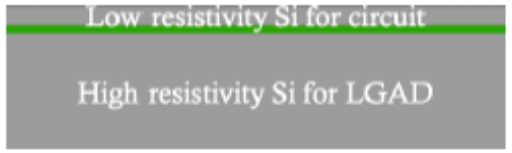
* Have a parallel effort at LBNL on SiC-LGAD also using ML techniques to improve both time and position resolution

Monolithic LGADs development at BNL

- Still early days for the R&D of MAPS with Gain Layer
  - New foundries and technologies can be tried out, e.g. US-based foundries, different processes
  - Performance improvements, e.g. 100% fill factor, low power consumption
- Two main approaches are studied on TCAD at BNL as part of US-Japan Collaboration
  1. AC-LGAD on CMOS bulk
  2. SOI AC-LGAD
     - High-resistivity handle wafer of the SOI substrate
     - AC-coupled electrode in the conventional AC-LGAD structure is replaced by a deep-well structure in the circuit layer



AC-LGAD on CMOS



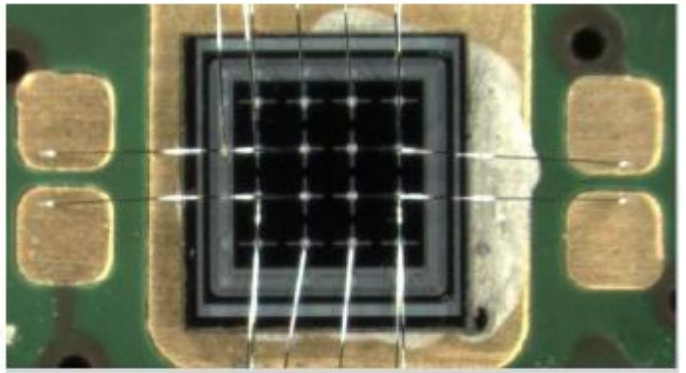
SOI AC-LGAD

(a) AC-LGAD sensor structure

(b) Structured AC-LGAD in SOI wafer

Impact of Machine Learning

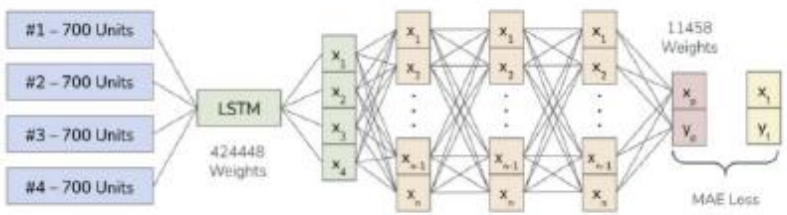
- **Machine learning to extract maximal information from AC-LGAD waveforms to predict particle hit coordinates**
- Traditional methods (analytic charge-sharing and matrix inversion methods) use reduced summaries of waveforms (e.g. peak amplitudes or relative amplitudes between channels).
- **Neural networks can take in full waveforms output by AC-LGADs**, and learn nonlinear patterns that capture the effects of small variations in timing and amplitude

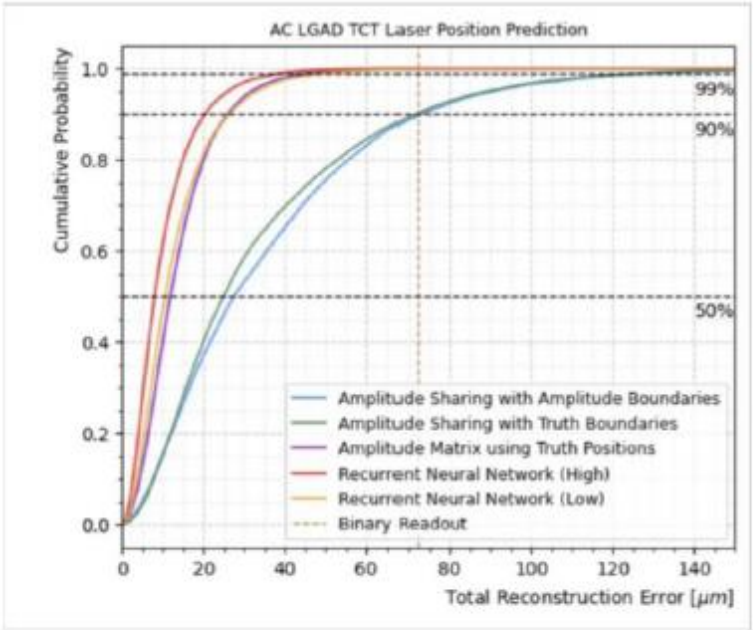


BNL-Manufactured AC-LGAD
Active thickness: 30 μm
Pad size: 200 μm
Pitch: 500 μm
2x2 pads readout

Recurrent Neural Network

Layer (type)	Output Shape	Param #
input_layer (InputLayer)	(None, 4, 350)	0
lstm (LSTM)	(None, 8)	11,488
dense (Dense)	(None, 16)	144
dense_1 (Dense)	(None, 16)	272
dense_2 (Dense)	(None, 16)	272
dense_3 (Dense)	(None, 2)	34





- TCT scan results:
- ML potential resolution of **~10 µm** from pixels with 500 x 500 µm² pixels
- Testbeam analysis ongoing

Reference Presentation

Conclusions and Outlook

- **The Silicon Wrapper as a 4D detector (Time+Space)**
  - Adding time information comes with small overhead to tracking, and may reduce (with AC-LGADs) channel count with same tracking resolution
  - Monolithic device will reduce material budget
- **BNL is studying different designs for a Monolithic AC-LGAD** in a US-Japan collaboration
  - **CMOS-based design** with electronics at periphery of active region to isolate fast electronics from fast signals (~GHz)
  - **SOI-based structure ← novel approach**

- TCAD and NGSpice designs are ongoing for sensor and electronics, as well as experimental tests with incremental prototypes
- Market survey suggests XFAB as leading candidate for SOI structure, and LPIS as back-up

Conclusions (mine)

- Believe a coherent and well-balanced program/opportunity exists for the US in tracking and timing
- Some key elements are already in-place but funding commitments will be needed to really get this underway with more participation
- Concerning performance the B-field/timing questions are an obvious set to address early on, and take a position
- In spite of low funding from US HFCC there is a strong USA MAPS effort already underway in a broader (generic/4D/legacy) context
- We already knew that the ePIC/EIC community faced similar tracking requirements
- Impressive progress across a variety of technical fronts (!)
- Interesting and collegial exchanges
- Continued dialogue/collaboration with this community would be a very positive development – hope to see some representation at the US FCC Workshop in September (SLAC)

Backup Slides

Structure of this meeting

- Hopefully ample time for unstructured discussions around talks
- AM
- Tracking overview from L1
- 3 presentations on US MAPS efforts
- LBNL LDRD proposal
- Lunch at the cafeteria
- PM – meet with ePIC/EIC colleagues
- ePIC/EIC overview
- Several MAPS/SVT talks
- PID/TOF with AC-LGADs
- Dinner