Monolithic AC-LGAD R&D at BNL

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BNL

4D Detector Challenges

- **Complexity**
  - Pixels or short strips (~1-2 cm) are needed for good timing
  - Many readout channels
- **Material Budget**
  - Silicon detector adds considerable material before calorimeter
- **Readout**
  - Advanced 4D ASICs are needed (under development)
  - Power consumption depends on technology used
- **Cooling**
  - Depending on technology, active cooling may be needed
- **Costs**
  - Large surface area for silicon
  - Development of advanced electronics

→

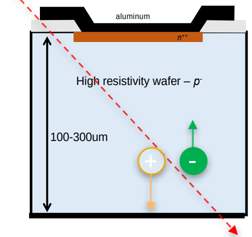
- No showstoppers
- Progress is made fast in this field
- Large interested community: multiple scientific applications
- We have time and human resources for innovation

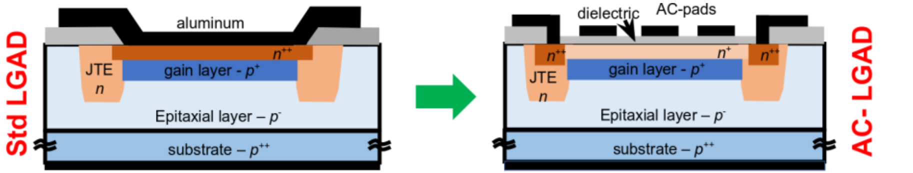
Technologies for Si-Wrapper or TOF

- **Proposed detector technologies for Si-Wrapper: Strips**
  - **Microstrips** (available) ← Tracking only
  - **DMAPS** (advanced) ← Low mass tracking
  - **LGAD** (advanced) ← Timing in addition to Tracking (4D)
  - ***Monolithic LGAD !?*** *(interesting idea)* ← *4D + Low mass*

→ **Adding *timing* capabilities to Si-Wrapper comes with limited extra effort/resources**

Std Pixel/Strip

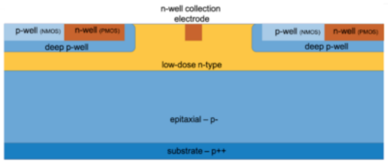




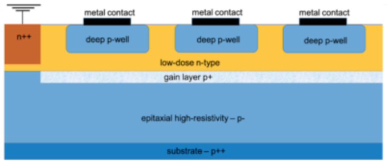
Large pads (~1 mm²) → Timing only

Can be finely pixelated → Time+Space (4D)

- **100% fill factor and fast timing information at a per-pixel/strip level → 4D**



CMOS sensor



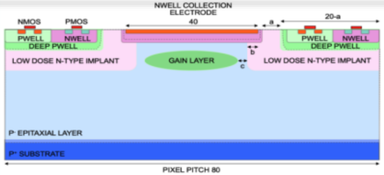
Monolithic AC-LGAD

- **4D detector capabilities as an AC-LGAD + readout circuitries in same substrate**

Monolithic LGADs in Europe (DRD3)

❖ **MAPS with Gain Layer is the next major technological goal**

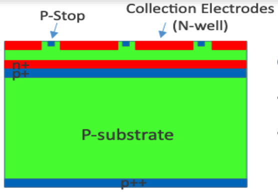
- It reduces hybrid interconnections, parasitic capacitance, material budget, ensures larger signals, faster response, higher signal-to-noise, and makes use of a commercial process at reduced cost
- **Several on-going or planned developments**, several ones with good timing and no gain layer (only a sample is presented here)



Reference Presentation

CASSIA : internal gain in CMOS pixels (Tower 180 nm) for 4D-tracking MAPS

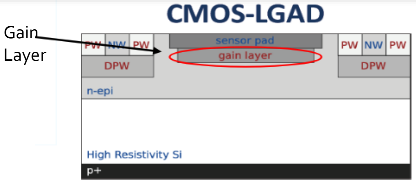
- CASSIA-1 : 3×3 sensor matrices and pixels without in-pixel electronics
  - Studies of breakdown characteristics, gain, and dark count rate; first results confirming internal gain
- CASSIA-2 : integrates in-pixel electronics, total chip area: 6 × 5 mm², submitted



Reference Presentation

CACTUS-GL: fabrication in 2024 with LFoundry 150 nm - Deep junction LGAD concept with buried pn-junction

- Tests ongoing and charge multiplication is observed
- Plan to submit a MiniCactus V2 with Gain Layer chip (with integrated FE, suitable for timing) and improved test structures (higher breakdown voltage) in 2026



Reference Presentation

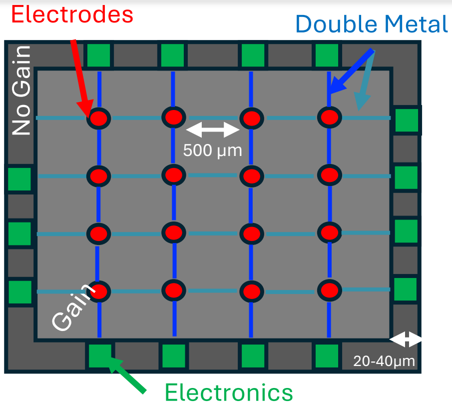
MadPix (ARCADIA Coll.): fully depleted CMOS MAPS with LFoundry 110 nm

- Active thickness 48 µm, pixels of 250 µm x 100 µm
- Gain observed in prototype since 2023 test-beam
- Time resolution achieved so far 75 ps
- Aim for 20 ps timing in 2026 engineering run, larger pixels and thinner sensor

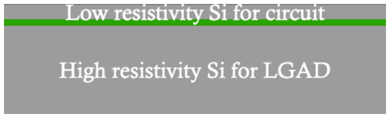
Monolithic LGADs development at BNL

- **Still early days for the R&D of MAPS with Gain Layer**
  - **New foundries and technologies can be tried out, e.g. US-based foundries, different processes**
  - **Performance improvements, e.g. 100% fill factor, low power consumption**

- **Two main approaches are studied on TCAD at BNL as part of US-Japan Collaboration**
  1. **AC-LGAD on CMOS bulk**
  2. **SOI AC-LGAD**
     - High-resistivity handle wafer of the SOI substrate
     - AC-coupled electrode in the conventional AC-LGAD structure is replaced by a deep-well structure in the circuit layer



AC-LGAD on CMOS



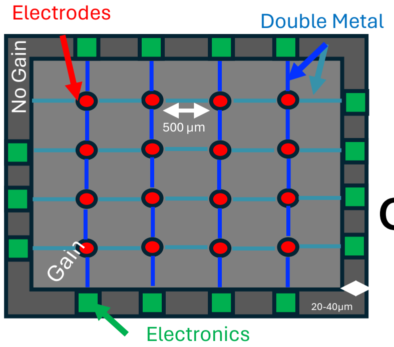
SOI AC-LGAD

(a) AC-LGAD sensor structure

(b) Structured AC-LGAD in SOI wafer

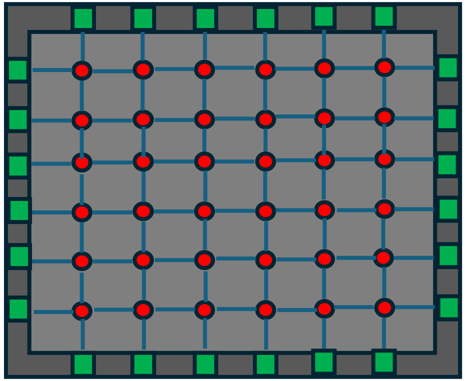
1. Monolithic AC-LGADs on CMOS

❖ **Initial studies on AC-LGAD on CMOS bulk with off-pixel electronics**

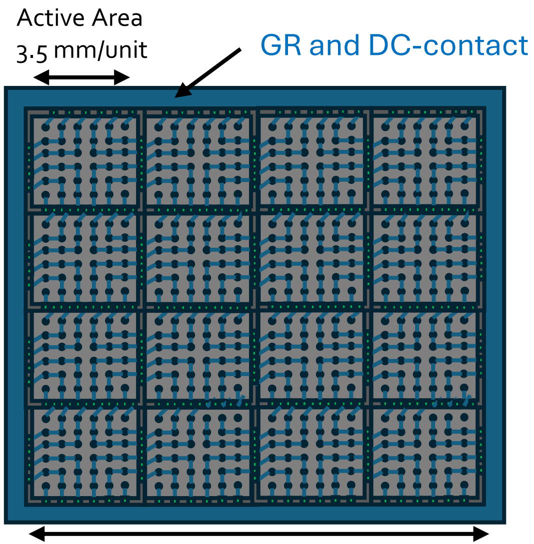


Unit: 4x4, 500x500 µm²

OR



Unit: 6x6, 500x500 µm²



Tota Area: ~1.425 x 1.425 cm2
Total Active Area : 1.4 x 1.4 cm2

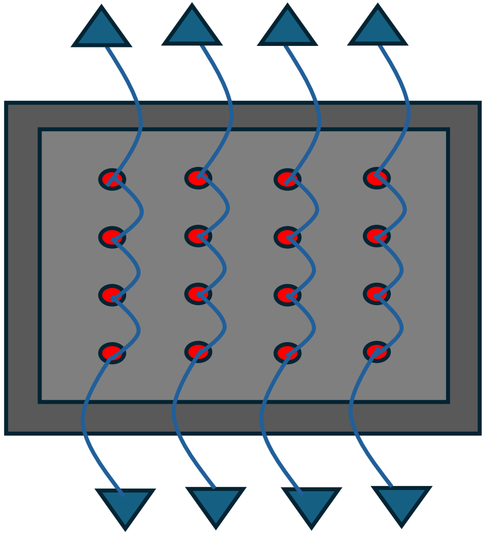
4x4 or 6x6 Units
(500x500 µm² with small dead-area between units)
~97% fill factor

- **Electronics in No-Gain area: no signal going through fast electronics**
- No-Gain Area: 20 – 40 µm depending on TDC size in CMOS processing
  - 40x60 µm² in 65 nm
  - 20x30 µm² in 28 nm
- Thin and short double-metal connecting small electrodes will introduce small C and R wrt strips: better performance than strips
- **ML to reconstruct particle hit position**

1. Monolithic AC-LGADs on CMOS

❖ **First test of Monolithic ACLGAD on CMOS sensor concept**

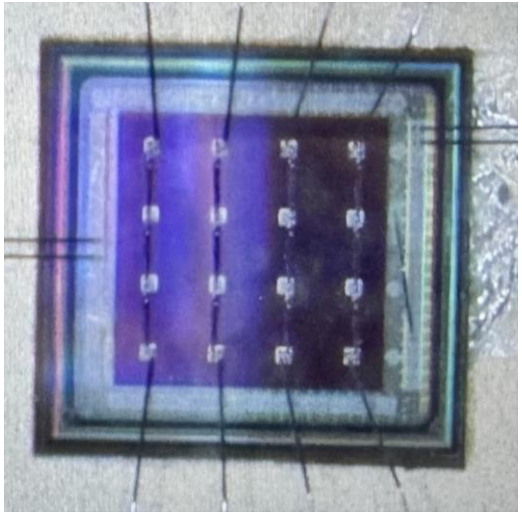
Standard AC-LGAD with desy-chain wires



EICROC-compatible ACLGAD:

- 4x4, 500x500 µm^2
- Double read-out per column
- Use 16-ch. FNAL board

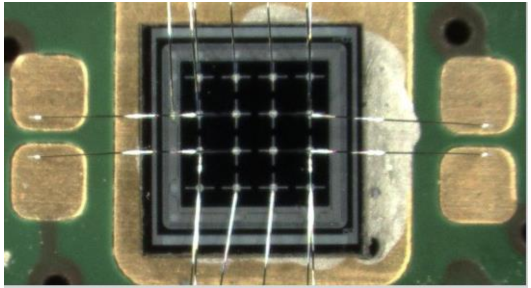
➔ **IR laser measurements on-going**



Impact of Machine Learning

❖ **Machine learning to extract maximal information from AC-LGAD waveforms to predict particle hit coordinates**

- Traditional methods (analytic charge-sharing and matrix inversion methods) use reduced summaries of waveforms (e.g. peak amplitudes or relative amplitudes between channels).
- **Neural networks can take in full waveforms output by AC-LGADs**, and learn nonlinear patterns that capture the effects of small variations in timing and amplitude



BNL-Manufactured AC-LGAD

Active thickness: 30 μm

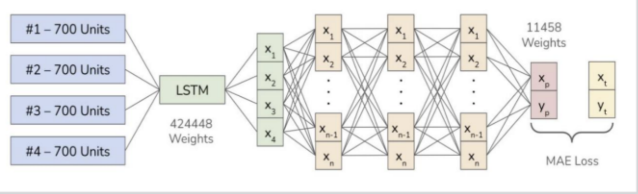
Pad size: 200 μm

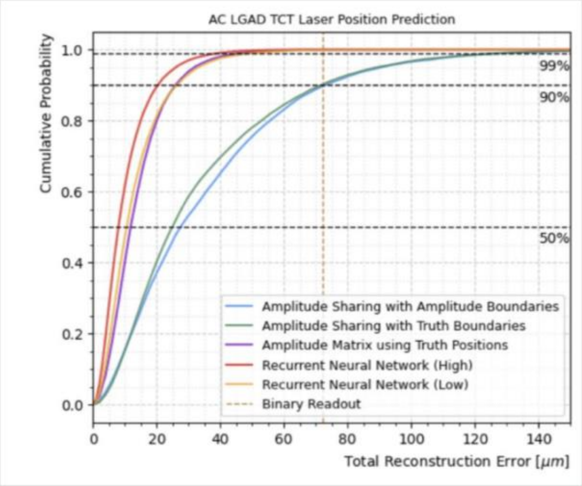
Pitch: 500 μm

2x2 pads readout

Recurrent Neural Network

Layer (type)	Output Shape	Param #
input_layer (InputLayer)	(None, 4, 350)	0
lstm (LSTM)	(None, 8)	11,488
dense (Dense)	(None, 16)	144
dense_1 (Dense)	(None, 16)	272
dense_2 (Dense)	(None, 16)	272
dense_3 (Dense)	(None, 2)	34





➢ TCT scan results:

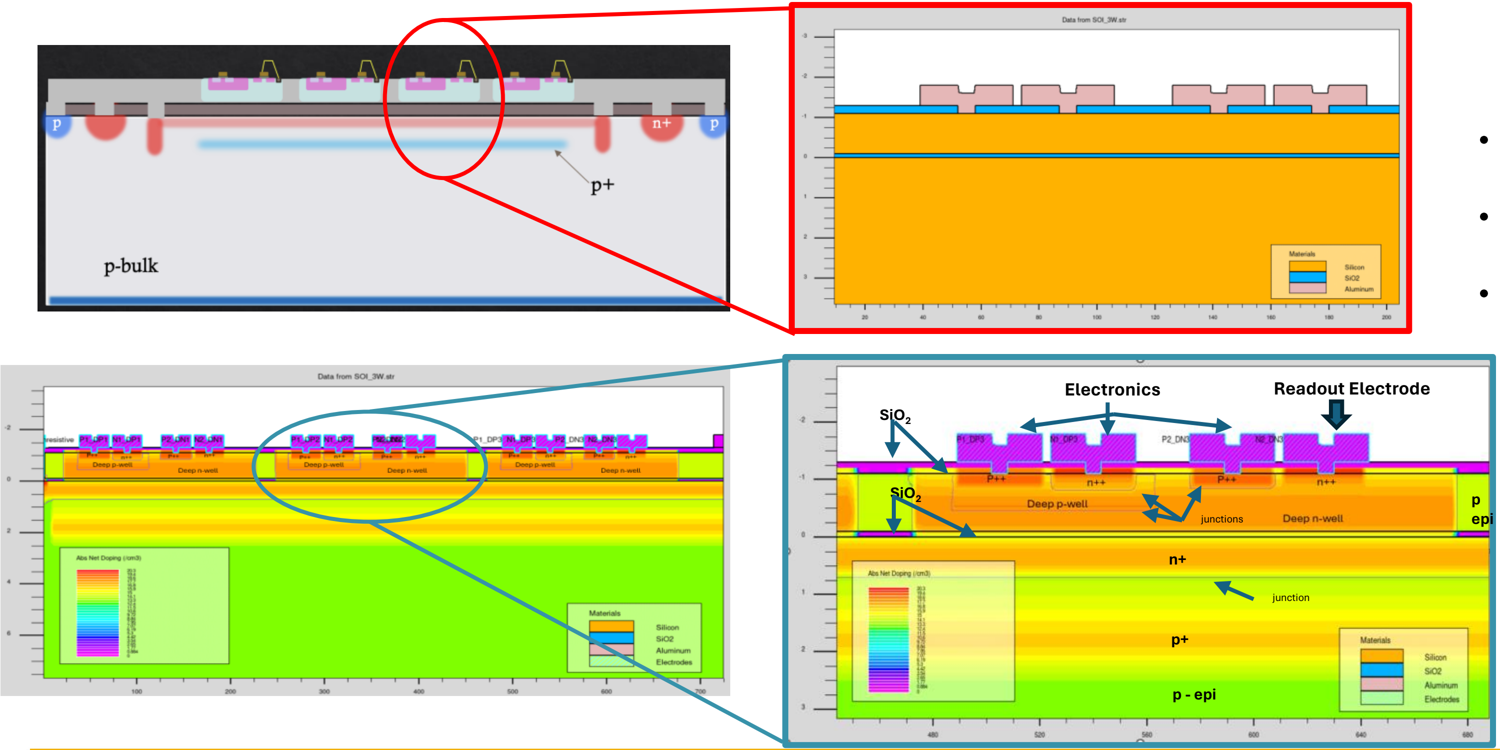
- ML potential resolution of **~10 μm** from pixels with 500 x 500 μm^2 pixels

➢ Testbeam analysis ongoing

[Reference Presentation](#)

2. Monolithic SOI AC-LGAD

❖ **New concept: SOI AC-LGAD** (Geometrical layout inspire by Koji Nakamura)

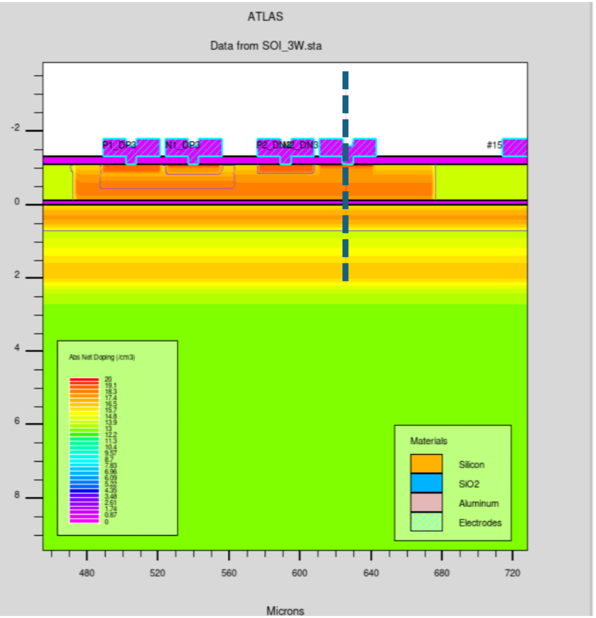


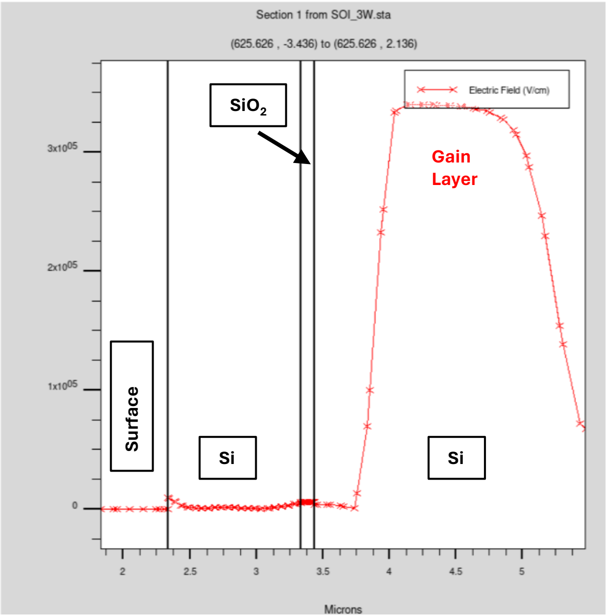
- Substrate biased at V_{bias} = -240 V
- SOI layer partially depleted or undepleted
- Doping
  - Bulk p = 10^{13}
  - SOI p = 10^{14}
  - Deep n-well ~10^{18} atm/cm3
  - p++ ~ 10^{19} atm/cm³

2. Monolithic SOI AC-LGAD

❖ New concept: SOI AC-LGAD

Electric field on cutout through readout electrode





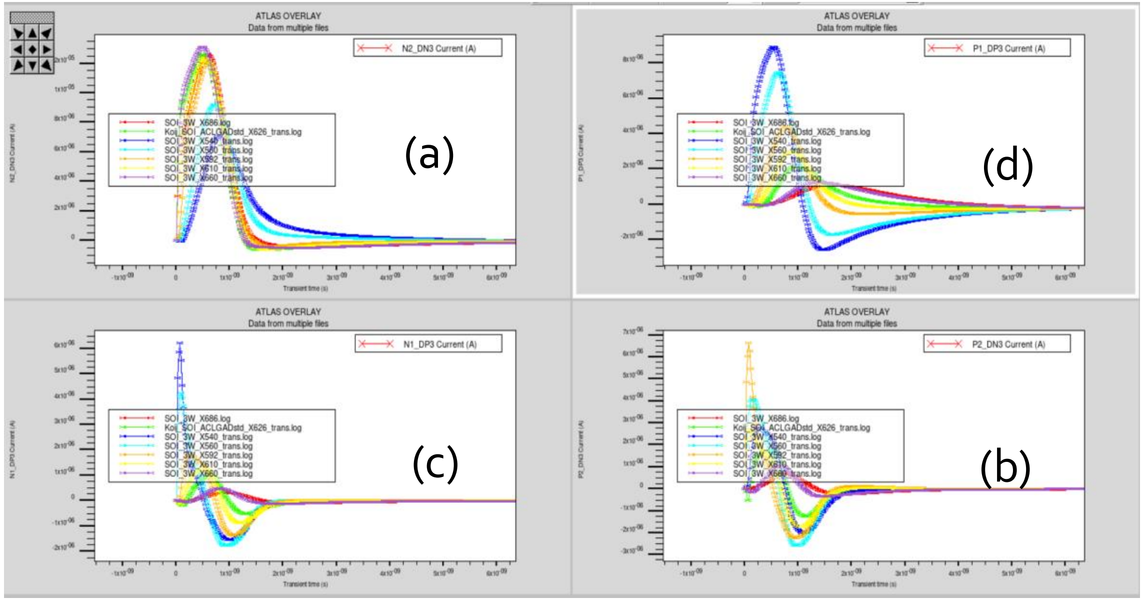
- **Good:** Electric field in bulk only
- **Good:** Gain layer field in bulk > 300k V/cm

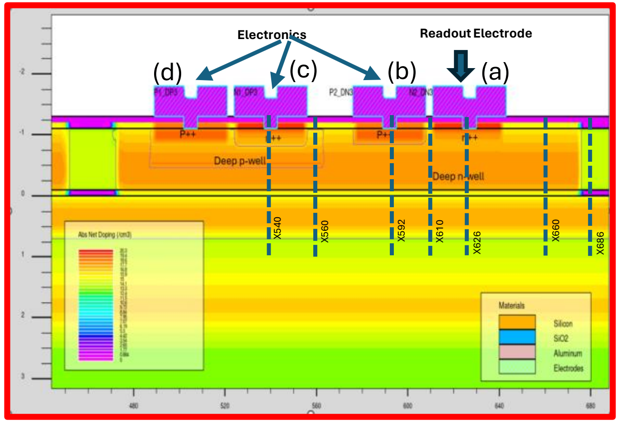
SOI layer is mostly undepleted (no electric field)

2. Monolithic SOI AC-LGAD

❖ New concept: SOI AC-LGAD

Currents at different electrodes for different MIP positions

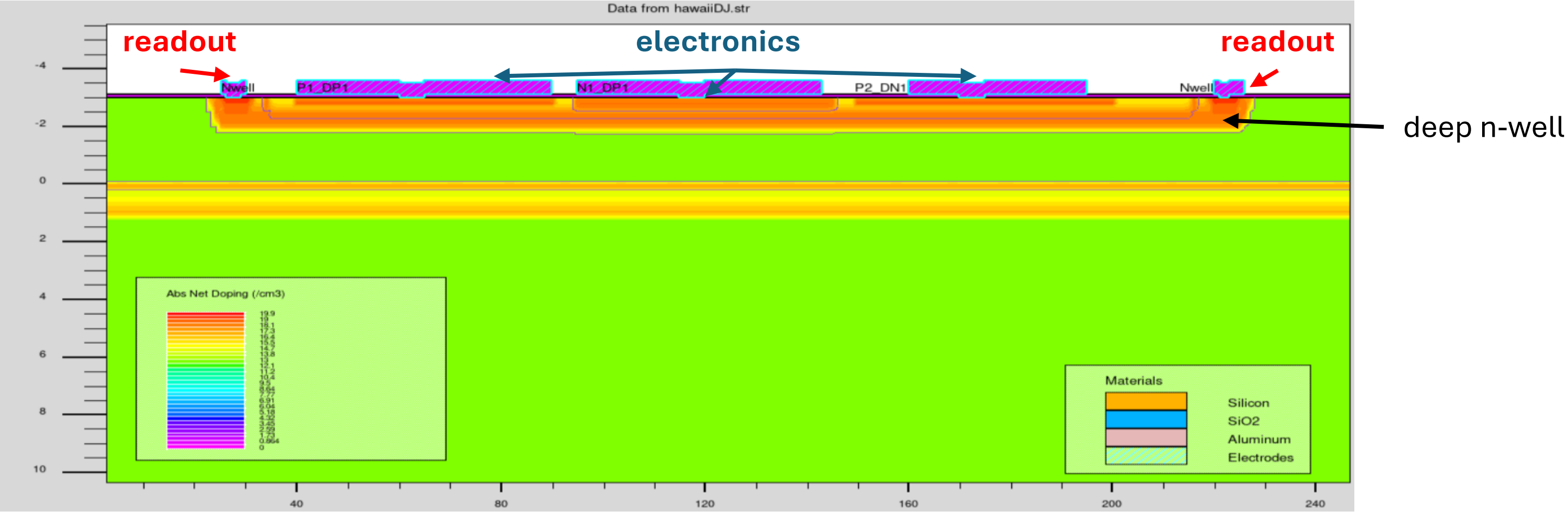




- **Good:** no dead area - readout electrode (a) sees signal over all area
- **Bad:** large fast signal in electronics (b), (c), (d)

2. Monolithic SOI AC-LGAD

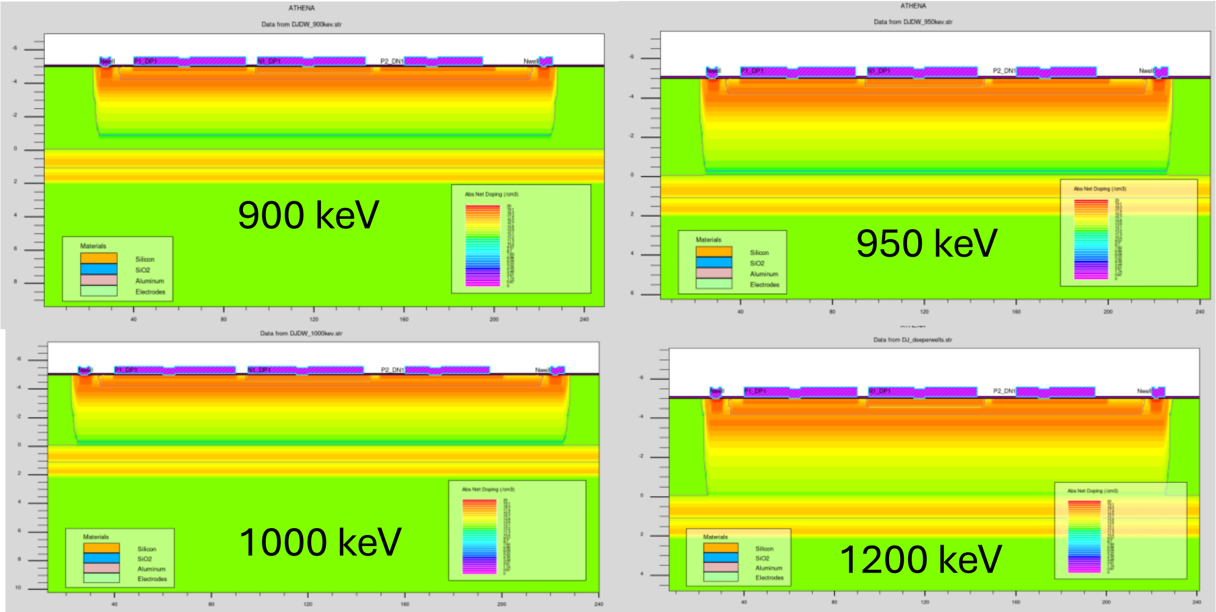
❖ **Study Deep Junction LGAD (DJ-LGAD) as a steppingstone towards an SOI AC-LGAD**
- A simplified DJ-LGAD with deep n-well as signal readout and electronics inside it
- Goal to study the performance of this structure, to understand signal in readout electrode as well as signal in electronics



2. Monolithic SOI AC-LGAD

- **Study Deep Junction LGAD (DJ-LGAD) as a steppingstone towards an SOI AC-LGAD**
  - Study different depths of deep n-well and their impact on signal pulses in readout and electronics electrodes

Variation of n-well implantation energy (Phosphorus)



No significant change in pulses is observed

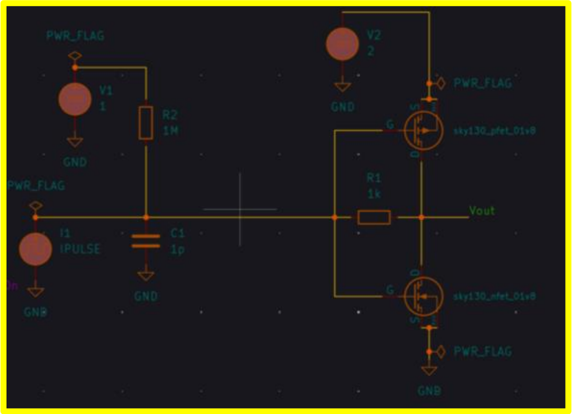
2. Monolithic SOI AC-LGAD

❖ **Study Deep Junction LGAD (DJ-LGAD) as a steppingstone towards an SOI AC-LGAD**

- Change in design of deep n-well to reduce electrode capacitance, thus signal share
- Implementation of realistic electronic circuits (e.g. amplifier, shaper, discriminator etc.)

➢ **Capacitance at each electrode is reduced by an order of magnitude**

➢ **Work ongoing to extract signal pulses with new design**



➢ **Implementation of circuits in NGSpice with SkyWater 130 nm process**

2. Monolithic SOI AC-LGAD

- **SOI AC-LGAS Market Survey**

1. **LAPIS**
   - Fully Depleted (FD) SOI process at the *200 nm technology node*, with a very thin circuit layer (~88 nm)
   - MPW run is possible
2. **XFAB**
   - Partially Depleted (PD) SOI process in the *180 nm (or 110 nm) technology node*, with a relatively thick circuit layer (~3.5 µm)
   - No MPW run is possible

- **XFAB is the primary candidate foundry**
  - The relatively thick circuit layer available in the XFAB PD-SOI process provides significant advantages for analog circuit design, electrode capacitance optimization, and stable operation under high electric fields, which are critical for achieving uniform timing performance

Conclusions and Outlook

- **The Silicon Wrapper as a 4D detector (Time+Space)**
  - Adding time information comes with small overhead to tracking, and may reduce (with AC-LGADs) channel count with same tracking resolution
  - Monolithic device will reduce material budget
- **BNL is studying different designs for a Monolithic AC-LGAD** in a US-Japan collaboration
  - **CMOS-based design** with electronics at periphery of active region to isolate fast electronics from fast signals (~GHz)
  - **SOI-based structure ← novel approach**

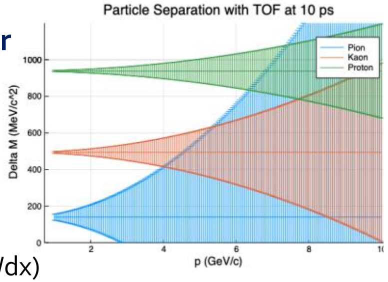
- TCAD and NGSpice designs are ongoing for sensor and electronics, as well as experimental tests with incremental prototypes
- Market survey suggests XFAB as leading candidate for SOI structure, and LPIS as back-up

Backup

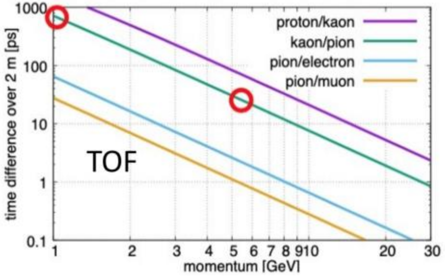
Timing Layer Specifications

- ❖ **Large-radius timing layers in front of the calorimeter can provide Time-of-Flight (ToF) for PID**
  ➔ Flavor physics, H→ss

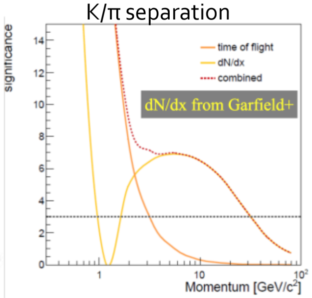
- ❖ **Need 10 ps resolution over 2 m lever-arm for K/π separation at low momentum (up to ~4-5 GeV)**
  - Drift chamber: PID by dE/dx or cluster counting (dN/dx)
    - 3σ for K/π separation up to 35 GeV
    - Complemented with TOF for hole at 1 GeV



Study for SiD at ILC (arXiv:2110.09965)



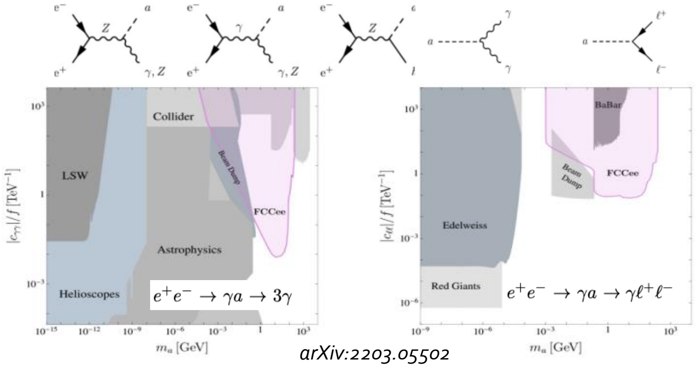
N. Morange, https://indico.mit.edu/event/876/contributions/2672/attachments/1042/1708/allegro-concept.pdf



P. Giacomelli, https://indico.mit.edu/event/876/contributions/2670/attachments/1034/1765/IDEA_detector-concept-FCC-US-2024.pdf

- **Exploit high luminosity Z run of FCC-ee to search for LLP**:
  - Heavy Neutral Leptons
  - Axion-like particles
  - Exotic Higgs decays
- **Timing information:**
  - Simultaneous determination of mass and proper decay time combining decay path and ToF
  - Combination with displaced vertex reconstruction for enhanced performance

Ariel Schwartzman, https://indico.slac.stanford.edu/event/8992/contributions/10627/attachments/4753/12818/4DTracking_physics.pptx.pdf

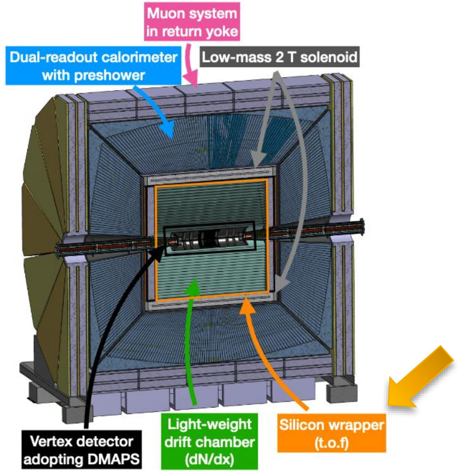


arXiv:2203.05502

Current Silicon Wrapper Design

***ALLEGRO** Detector Concept (FCC-ee)*

***IDEA** Detector Concept (FCC-ee)*



In Simulation (Full-Sim):

Barrel

	R [mm]	L [mm]	Si eq. thick. [μm]	X0[%]	Pixel size [mm^2]	area [cm^2]	# of channels
Layer 1	2040	±2400	450	0.5	0.05×100	616K	12.3M
Layer 2	2060	±2400	450	0.5	0.05×100	620K	12.4M

Endcap

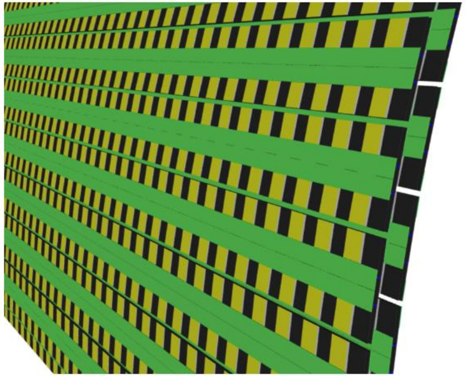
	R^{in} [mm]	R^{out} [mm]	z [mm]	Si eq. thick. [μm]	X0[%]	Pixel size [mm^2]	area [cm^2]	# of channels
Disk 1	350	2020	±2300	450	0.5	0.05×100	250K	5M
Disk 2	354	2020	±2320	450	0.5	0.05×100	250K	5M

https://fcc-ee-detector-full-sim.docs.cern.ch/IDEA/

❖ Tracking Information
- Improve momentum resolution thanks to long lever arm
- Extend tracker coverage in forward regions
- Precise and stable ruler for acceptance definition

- Covered area: ~100 m^2
- Low material budget: ~ 1% X/Xo
- Two barrel layers and two disks, to have at least one silicon hit, but most of the cases we have two silicon hits
- Multi-module tiles on staves (ATASPIX3 quad module concept)
- No detailed layout of the mechanical structure yet

Current Silicon Wrapper Design



Two layers to cover gaps

Barrel:

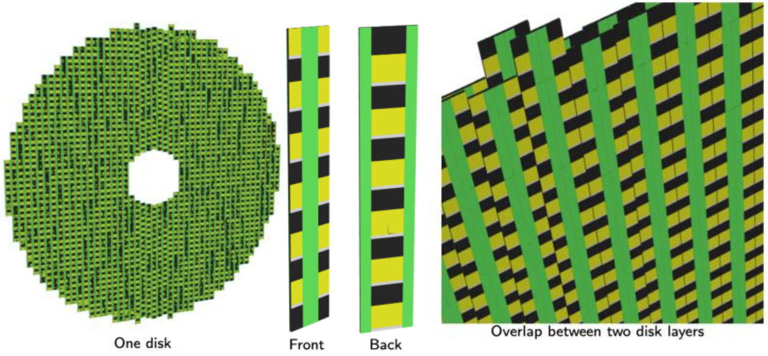
- Each stave is a long tile
- Each layer made up of 151 staves with 129*2 modules

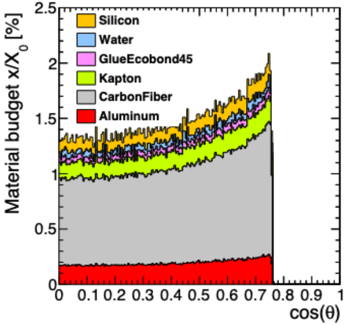
➔ Total of 77,916 modules

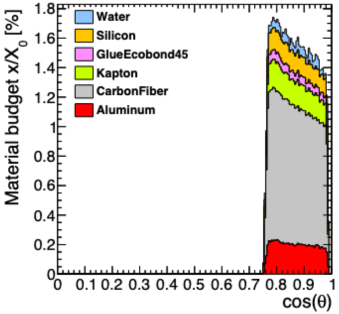
Disks:

- Tiling the disks with tiles of 6, 12 and 24 modules

➔ Total of 30,432 modules







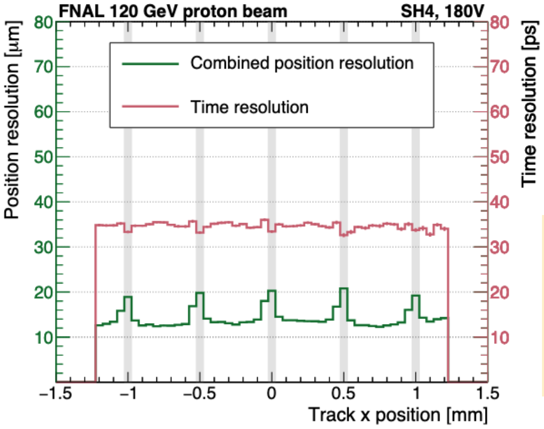
Material:

- Flex and cooling pipes (same as in vertex outer barrel and disk)
- 50 μm silicon
- 1.4 mm of carbon fibre

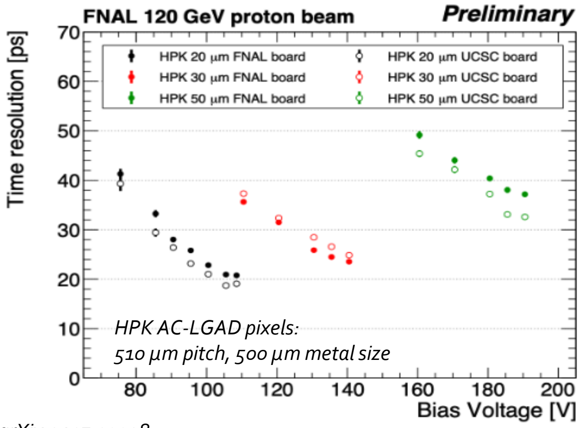
LGAD Sensor Performance

❖ **Long AC-LGAD strip sensors performance**

- **Position reconstruction**
  - Achieve **15-20 µm** resolution in *1 cm strips, 500 µm pitch*
  - ➔ Same resolution as microstrips with larger pitch
- **Excellent time resolution**
  - Achieve **30-35 ps** for *1 cm strips, 50 µm active thickness*
  - ➔ Same time resolution as LGAD



Signal shared between neighboring electrodes in AC-LGADs:
Measure position based on signal ratios



arXiv:2407.09928

- **AC-LGAD with smaller thickness: 20, 30 µm**
  - Faster Rise-Time
  - Time resolution improves with smaller active thickness
  - For 20 µm time resolution <20 ps

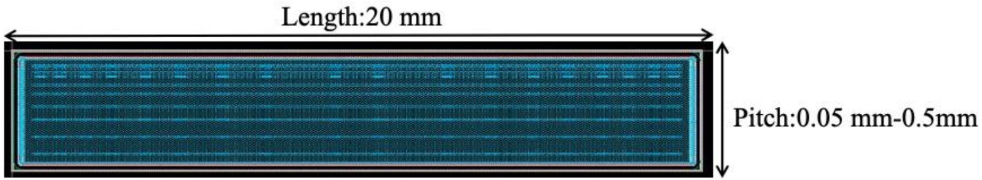
➢ **Fast-time readout ASICs for 4D detectors are also becoming available**

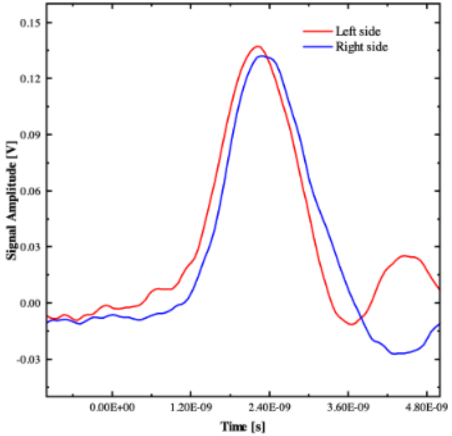
LGAD Sensor Performance

❖ **Long LGAD strips can be read from both ends ➔ longer strips**

original idea by UCSC

- **Position reconstruction**
  - Based on time-lag between two ends
  - Good linearity
  - Position resolution along z~0.9 mm (intrinsic 5.5 mm) for a total strip length of 19mm
- **Time resolution**
  - Achieve ~37 ps with 19 mm strip length





Waveform Variation at two ends

Weyi Sun
https://indico.cern.ch/event/1439336/contributions/6242215/attachments/2977964/5243205/4d_aclgad_swy_7.pdf

Synergies

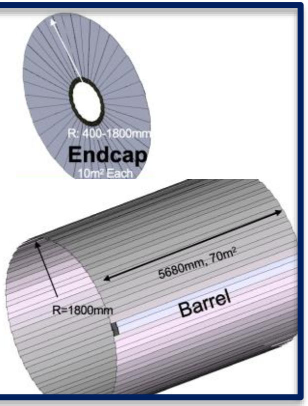
DRD3
Semiconductor Det.
https://drd3.web.cern.ch/

- 143+ institutions
- 600++ people

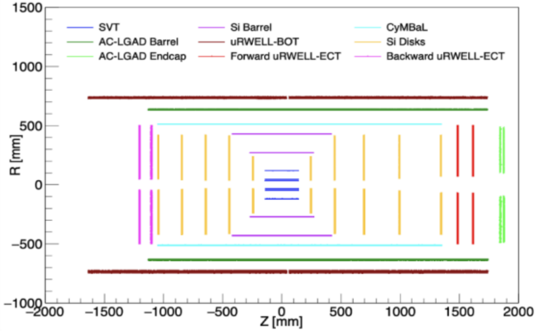
WG2 research goals <2027	
	Description
RG 2.1	Reduction of pixel cell size for 3D sensors
RG 2.2	3D sensors for timing ($\leq 55 \times 55$ μm, < 50 ps)
RG 2.3	LGAD for 4D tracking < 10 μm, < 30 ps, wafer 6" and 8"
RG 2.4	LGAD for ToF (Large area, < 30 μm, < 30 ps)

Design target of CEPC ToF Barrel

Area	~ 70 m^2
Radius	1.8m
Length	5.8m
Strip Length	20 mm (to be determined)
Strip Pitch	100-500 μm (to be determined)
Channel number	~ 10^7 channels
MIP Time resolution	~50 ps
Spatial resolution	~ 10 μm (R-Φ)

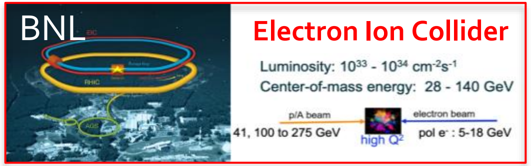


ePIC Det. Tracking System

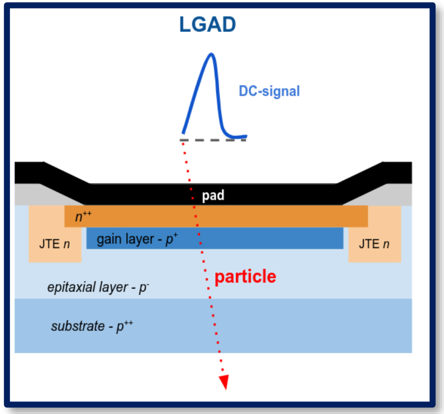


❖ AC-LGAD:

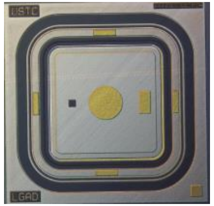
- **PID Time of Flight** detectors to cover PID at low pT
  - Also provide time and spatial info for tracking
  - Resolution: ~30 ps, 30 um (with charge sharing)
- **Barrel (BTOF):** 0.05 x 1 cm strip, 1% X/Xo
- **Forward disk (FTOF)** : 0.5 x 0.5 mm² pixel, 8% X/Xo
- **Far-Forward Detectors:** Luminosity Monitor (strips), Bo (pixels), Roman Pots (pixels)
- **ASICS** being developed

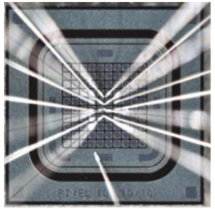


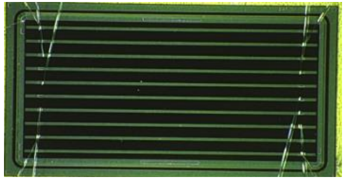
LGAD Technologies



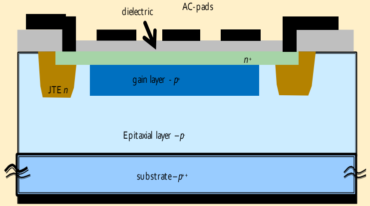
- **Low Gain Avalanche Diode (LGAD) is advanced technology for precision timing**
  - Used in ATLAS and CMS for HL-LHC timing detectors
  - Several foundries in China, Europe, US and Japan
- **Thriving field of research for 4D detectors: pixels or strips with various processes**



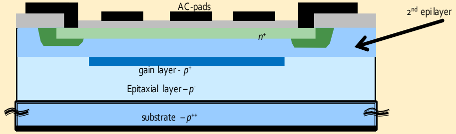


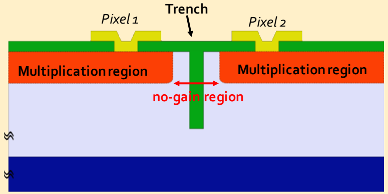


AC-LGAD
100% fill factor, excellent spatial resolution with signal sharing, for low interaction rates



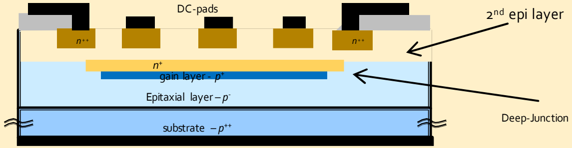
Deep-Layer AC-LGAD
an AC-LGAD with higher rad-hardness





Trench-Isolation LGAD
~100% fill factor, signal in single pixel (no share)

Deep-Junction LGAD
Position resolution given by pitch, as in std pixels/strips



Monolithic Detectors

Chip name	Experiment	Subsystem	Technology	Pixel pitch [μm]	Time resolution [ns]	Power Density [mW/cm²]
ALPIDE	ALICE-ITS2	Vtx, Trk	Tower 180 nm	28	< 2000	5
Mosaic	ALICE-ITS3	Vtx	Tower 65 nm	25x100	100-2000	<40
FastPix	HL-LHC		Tower 180 nm	10 - 20	0.122 – 0.135	>1500
DPTS	ALICE-ITS3		Tower 65 nm	15	6.3	112
NAPA	SiD	Trk, Calo	Tower 65 nm	25x100	<1	< 20
Cactus	FCC/EIC	Timing	LF 150 nm	1000	0.1-0.5	145
MiniCactus	FCC/EIC	Timing	LF 150 nm	1000	0.088	300
Monolith	FCC/Idea	Trk	IHP SiGe 130 nm	100	0.077 – 0.02	40 - 2700
Malta	LHC, ..	Trk	Tower 180 nm	36x40	25	> 100
Arcadia	FCC/Idea	Trk	LF 110 nm	25	-	30

C. Vernieri: https://indico.mit.edu/event/876/contributions/2694/attachments/1039/1721/MIT-workshop-Detector.pdf