ALICE3 & FCC-ee SILICON DETECTORS

Technological Convergence and Readout Concepts

May 13, 2026

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ALICE3 & FCC-ee SILICON DETECTORS

AGENDA

- ALICE 3 and FCC-ee requirements and technologies
- ALICE 3 project background and structure
- Readout concepts, methodologies and studies
- The road so far and future developments

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CONTEXT: TWO FLAGSHIP NEXT-GENERATION EXPERIMENTS

Overview of ALICE3 at the LHC and the FCC-ee Vertex Detector

Although different in concepts and physics program, both designs push towards **deep spatial and time resolutions, high particle rate** with **significant background** processes, **minimal material budget** constraining cooling and **power consumption**

ALICE3 (LHC LS4, ~2033)

Next-generation heavy-ion ALICE experiment targeting significant improvements in tracking and vertexing performance

- Entirely silicon; first layer at **5mm, inside beam pipe (moving detector)**
- Target **2.5um** resolution at innermost layers
- Material budget at **≤ 0.1% X_0**
- Cooling, cabling limit on power consumption **~ 70 mW/cm²**
- Timing resolution **< 100ns** for vertex
- Peak hit-rates (without vertex smearing) **~ 100 MHz/cm²** for *p-p* collisions
- Significant QED **background** for *Pb-Pb* collisions (under study)

[1]

FCC-ee Vertex Detector (~2040s)

High-luminosity lepton collider detector requiring the most stringent spatial resolution and material budget constraints

- First vertex layer at **~14mm**
- Target **3um** resolution
- Air cooling limit power **≤ 50 mW/cm²**
- Material budget **≤ 0.3% X_0**
- Dominant IPC **background** process
- *O*(**100 MHz/cm²**) ? peak hit-rate for innermost layer
- Timing resolution **~20ns** for vertex ? Maybe less ?

[2]

- **Enabling technologies** for silicon trackers (**MAPS**, stitching, thinning & bending,,…)
- Shift in **readout architecture concepts** (asynchronous, continuous, event-driven, …)
- Development of **design know-how**, dedicated **system prototyping and verification tools**

CONTEXT: ALICE 3 TRACKERS BACKGROUND AND EXPERIENCE

Overview of ALICE3 at the LHC and the FCC-ee Vertex Detector

ALICE3 trackers will build significantly on the experience from MOSAIX ITS3 and earlier prototypes

MOSAIX is the full-scale stitched sensor prototype for **ITS3**, built in **TPSCo 65 nm**
(now under final revision for production run)

Implements **enabling concepts**, tools and technologies explored in earlier prototypes (**MOSS, MOST**):

- **Wafer-scale stitching** design and verification flows
- **Yield resilient design** techniques (DFM custom cells, power segmentation for fault isolation, …)
- On-chip **low power, long distance data transmission**
- **IR drop mitigation** over wafer-scale distances
- **Thinning and bending** of wafer-scale sensors
- **Testing infrastructure** for qualification and validation

Bent detector mock up assembly
(P.V. Leitao, TWEPP 2025)

ALICE 3 TRACKERS DEVELOPMENT: ALMIRA PROJECT

ALMIRA project: origin, purpose and scope

ALMIRA (**AL**ICE 3 **M**onolithic **I**ntegrated T**r**acker **A**SICs)

is the dedicated MAPS sensor-development project for ALICE 3

ALMIRA targets a **readout architecture**, **building blocks**, **custom IPs, design methodology and flow** to cover the needs of **ALICE3 silicon detectors** from vertex detector to outer tracker under a **common development**

In particular ALMIRA will target two ASICs:

- **ALMIRA-T**
  - reticle-size 20um + pitch for **middle and outer layers** (ML/OL)
  - ToA + ToT
  - < 30 mW/cm^2
  - needs to be ready **sooner** for volume production
- **ALMIRA-V**
  - large format (most likely stitched), 10um pitch optimized for the **Vertex Detector** (VD)
  - Only ToA
  - ~70 mW/cm^2 power budget

ALICE 3 SENSOR DEVELOPMENT: ALMIRA PROJECT METHODS AND TOOLS

ALMIRA project: virtual prototyping with PixESL

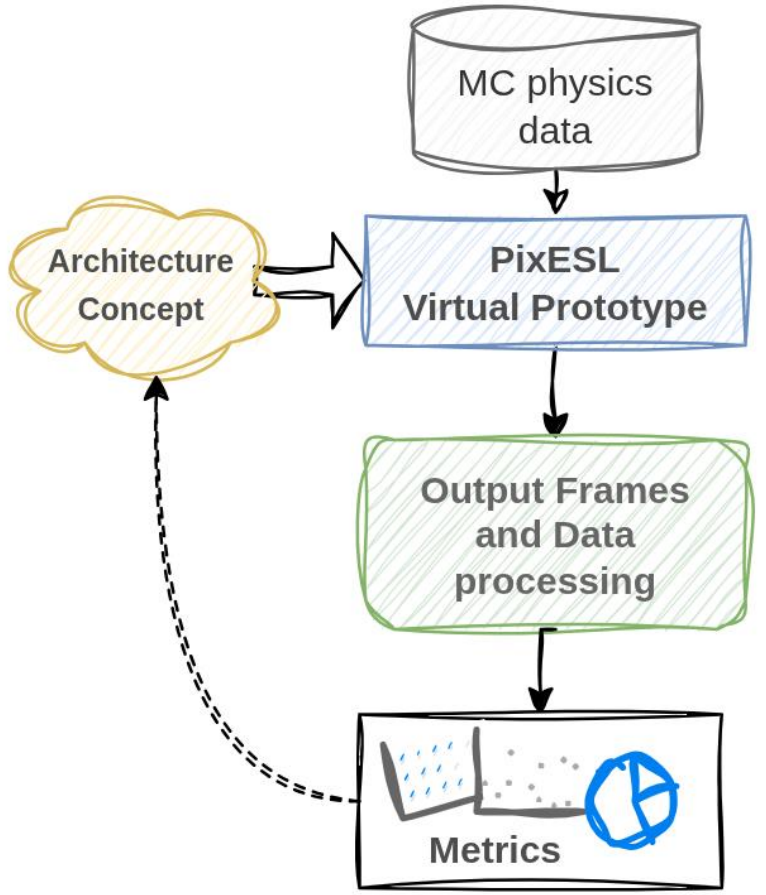
Early virtual prototyping methodology:
Architecture ideas tested against transport MC physics data early through **high level modeling with PixESL**

PixESL (developed at CERN) is a **virtual prototyping platform** for the **design and simulation of pixel detector electronics**

- C++ / System C / TLM
- Models ASIC **from sensor signal generation to readout electronics**
- **Abstracts HW complexity** by staying cycle accurate at the interfaces

What's the gain ?

- Insights on how **hit statistics interact with the design**
- Identify early show-stoppers
- **Estimates for system level metrics** (BW, pile-up, accuracy …)
- Feedback to **reduce hardware design space**
- Later **reference model** for RTL verification

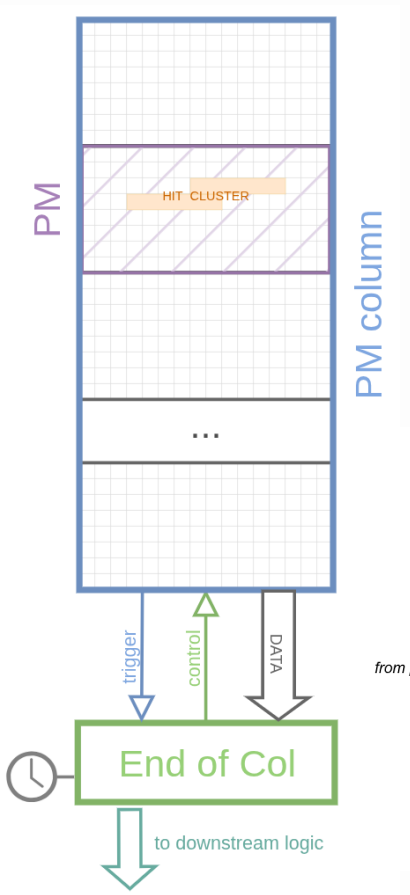


ALICE 3 SENSOR DEVELOPMENT: ALMIRA ARCHITECTURE HINTS

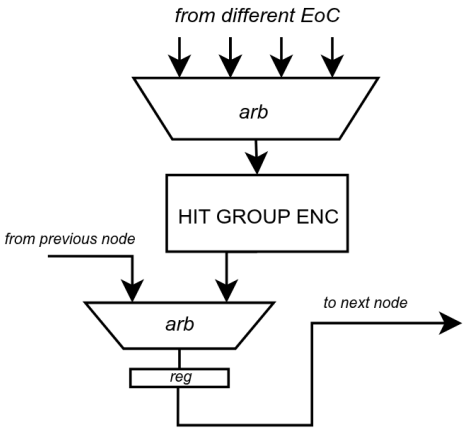
ALMIRA project: readout system architecture

ALMIRA is currently targeting a modular event-driven architecture that can be parametrized and assembled for different needs of ML/OL vs VD

- **Clock-less asynchronous matrix**
  - divided in columns of independent **Pixel Macro** units (PM)
    - Sharing **fast-OR** line(s) to signal hit events to periphery
  - **In-pixel memory** for delayed reads
- **Clocked End-of-Column logic**
  - **Timestamp hit events** and steer matrix controls (write, read, clear)
  - Only PM with data are read (first order **zero-suppression**)
  - Control frames **time integration** window
  - **Buffer reads** in FIFO
- **Modular data-driven routing fabric** (early proposal)
  - **Encoding of frame** data (second order zero-suppression)
  - **Rate and power scale** with op. frequency
  - Route packets to local serializer (on/off chip data transmission under study)



Thanks to the ALMIRA collaboration



ALICE 3 SENSOR DEVELOPMENT: ALMIRA DEVELOPMENT

ALMIRA project: the road so far in the development

The road so far: virtual prototype studies, block implementations and RTL

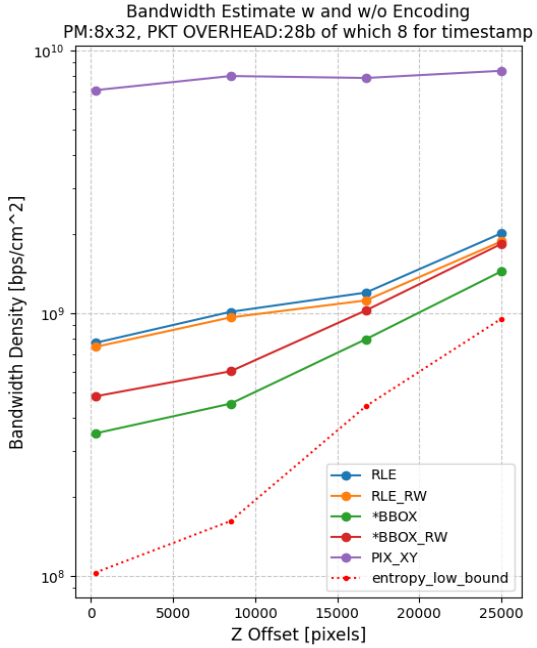
PixESL virtual demonstrator** (includes LUT for sensor + analog FE model):
- Tested for *p-p* events IR=24 MHz ~400us of data
- Pile-up loss < 0.2 % (by analog-FE only)

Digital matrix* first implementation (with dummy analog FE):
- 10x16 um routable with STD cells
  - room for optimization to 10x10 um
- Power consumption **~10 mW/cm²** (without leakage)

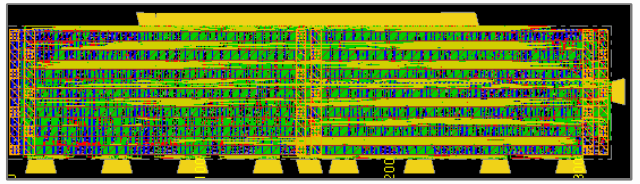
End-of-Column logic first implementation
- Two different version: fully data-driven & "time-tag driven"
- **< 70um** strip of non-active area
- **< 5 mW/cm²** at the expected rates

Routing Fabric and frame **data encoding RTL**
- Studied BW for different frame encoding strategies
- RTL ready, basic functionalities verified

**thanks to D. Ceresa*
***thanks to D.Chiappara*



Example Study: BW along Z for different encoding methods



End-of-Column PnR iteration

NEXT STEPS & CONCLUSIONS

ALMIRA project and FCC-ee trackers next steps and conclusions

First prototype ER target Q1-Q2 2027

- reticle-scale prototype (mixed 10um and 20um pitch)
- virtual prototype studies will continue to verify and fine-tune architecture

In parallel, same methodologies and flow can be applied to FCC-ee vertex detector:

- Virtual prototyping of some architecture ideas
- Dry run implementations of architecture concepts and building blocks

Technologies, tools, concepts and methodologies under development for ALICE3 upgrade can help greatly the silicon trackers development effort for FCC-ee

Thank you