MAPS R&D at BNL
Beyond ePIC SVT baseline

G.W. Deptuch,

05/13/2026

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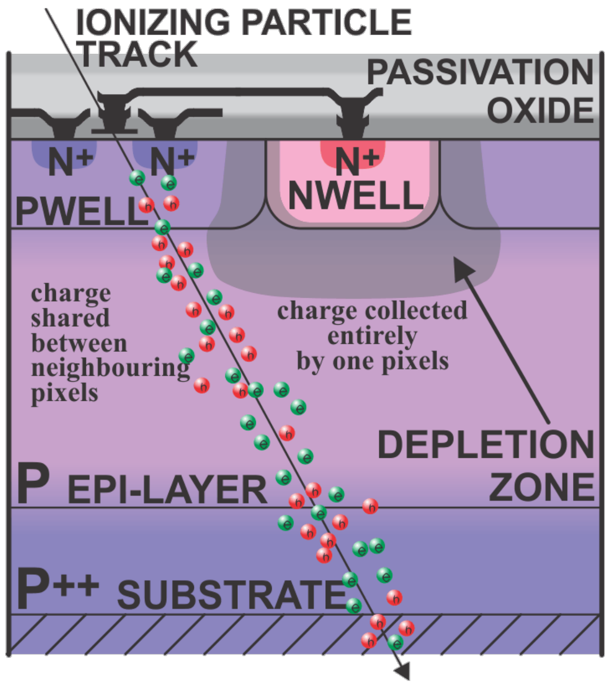
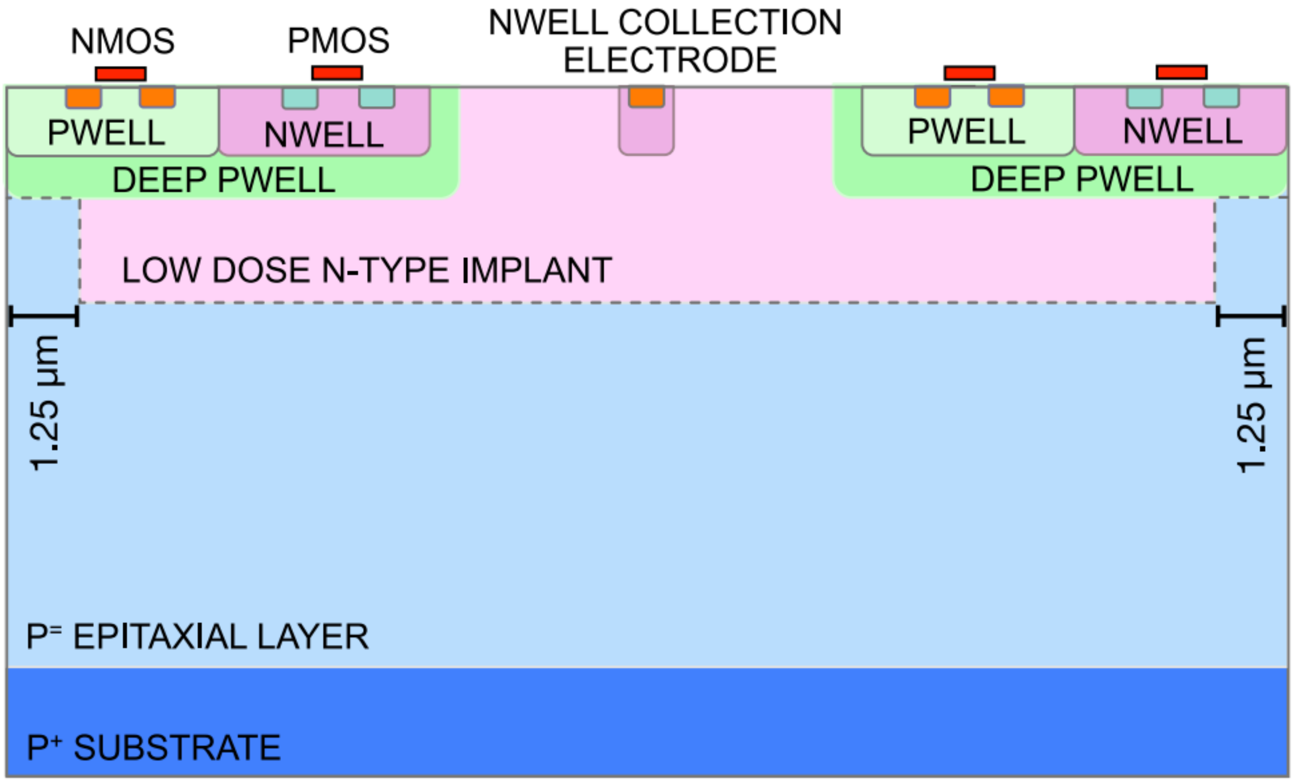
Old vs. New MAPS

OLD MAPS (2000)



volume in which charge is generated by traversing particles **is non depleted** + PMOS transistors cannot be used as NWELLs collect charge

NEW MAPS (2020)



volume in which charge is generated by traversing particles **is largely depleted** + PMOS transistors can be used as NWELLs are shielded by DEEP PWELLs

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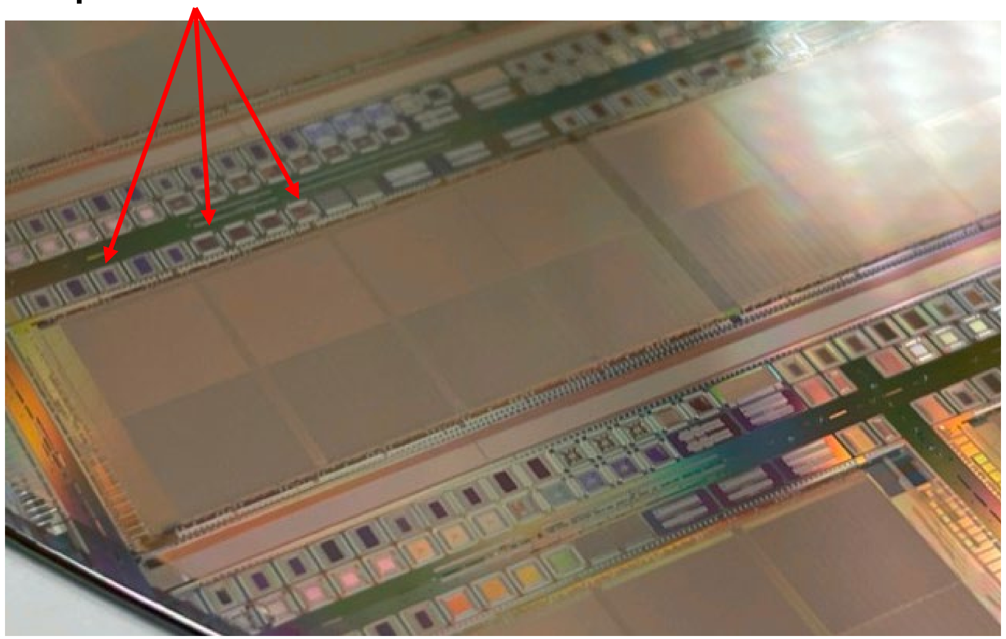
G. Deptuch, PhD thesis, 2002 (https://theses.hal.science/tel-00011109/file/these_deptuch.pdf)

G. Aglieri Rinella et al. Nuclear Inst. and Methods in Physics Research, A 1056 (2023) 168589 (https://doi.org/10.1016/j.nima.2023.168589)

ER2 submission with chiplets

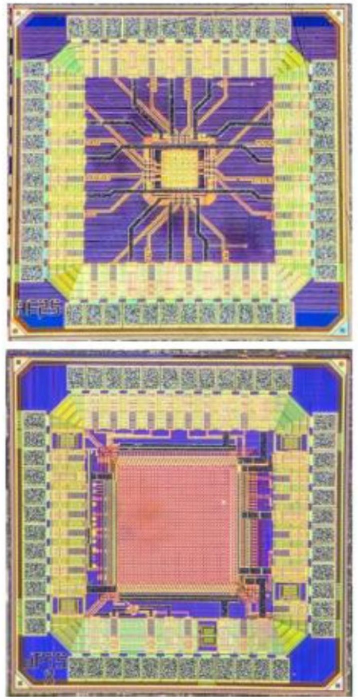
- **Chiplet = small 1.5 × 1.5 mm^2 design**
- **Multiple institutions presented proposals and some of them were selected by CERN team to be added to ER2 reticle to :**
  - **test concepts before inclusion on final sensor design,**
  - **explore R&D concepts.**

Chiplets on ER1



TWEPP23: ALICE ITS3: a bent stitched MAPS-based vertex detector - Speaker: O. Groettvik

APTS and DPTS were chiplets



Examples of chiplets in ER2

institution	Chiplet name	Additional information
U. Bari	ER2_SEU3	SEE Upset test chips
CPPM	ER2_RING_OSC_v1	ring oscillator test chip first version ported to new metal stack
CPPM	ER2_RING_OSC_v2	new ring oscillator test chip
HEIDELBERG	ER2_HEID	
IPHC	ER2_SPARC	event-driven pixel
SLAC	ER2_NAPA_v2	
BNL	ER2_BNL_ADC ER2_BNL_DATATR	ER2_ BNL_ADC_VFM ER2_BNL_BTLE

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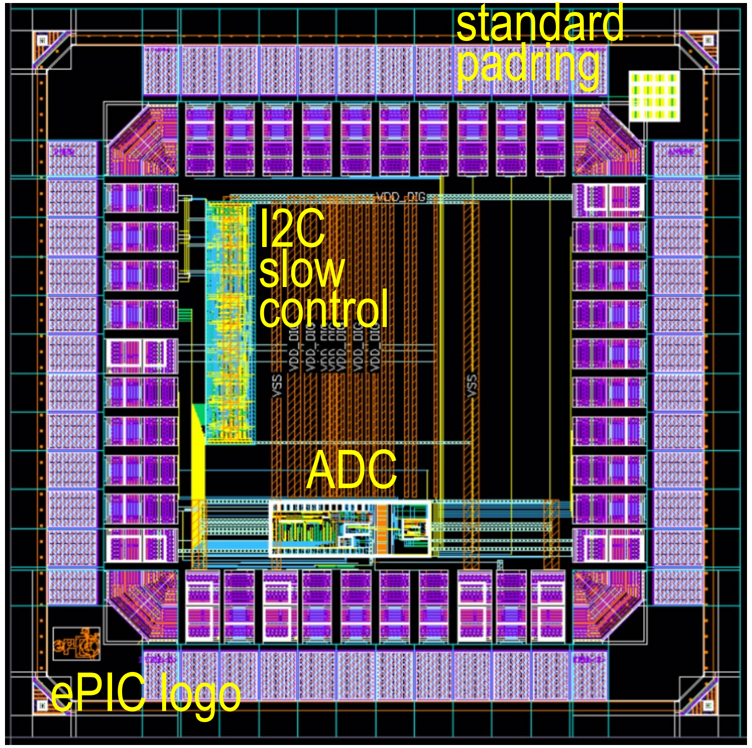
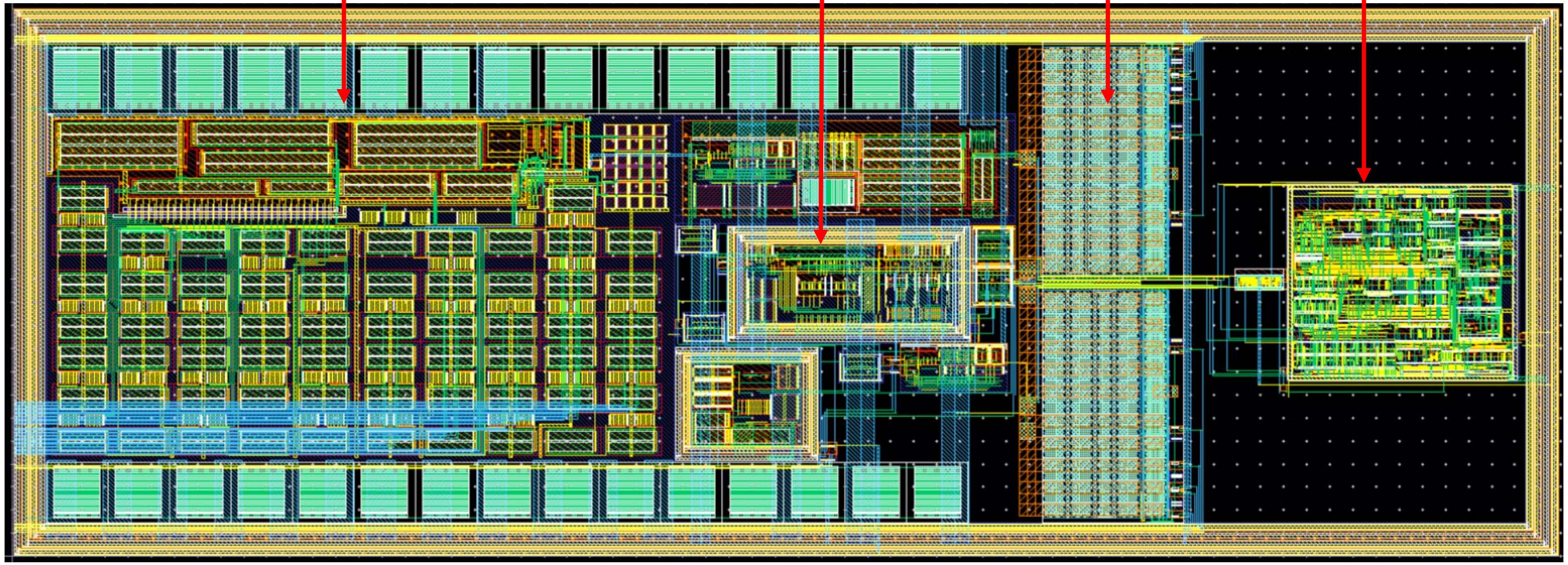
VFM_ ADC - Layout





Area: 335 x 119 μm^2

- Serial DAC capacitors are laid out on higher metal layers and placed next to one another
- Trimming DAC for each capacitor is placed directly next to each capacitor
- Nothing is placed below either the serial DAC capacitors or trimming DAC capacitors as to not introduce non-linear parasitic elements

BTLE_Driver - Motivation

Baseline of Backbone Transmission in MOSAIX

- **Baseline**: Transmit data across stitched sensor (~20 cm) at 160 Mb/s with repeaters between RSUs
- **Proposed Upgrade:** Avoid repeaters at boundaries, as they
  - create dead space where detection cannot occur
  - add to power consumption.
- **Key Challenge:** High R and C density of the thin, on-chip metal layers severely limits the bandwidth of long-range wired links across RSUs

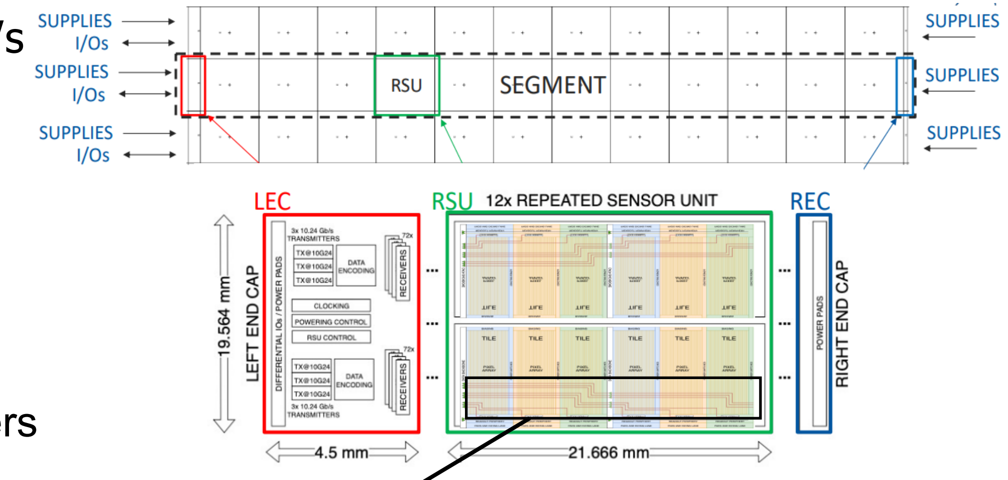
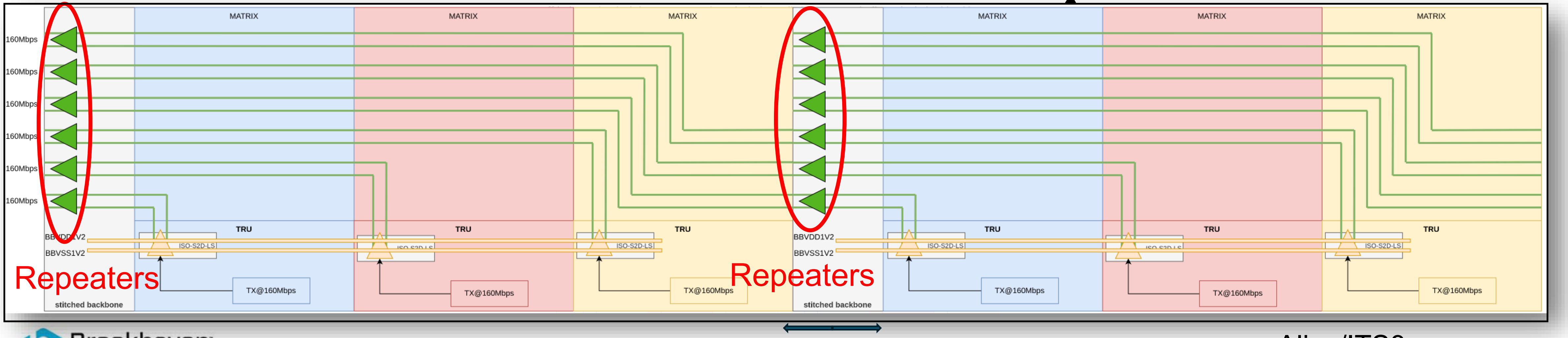
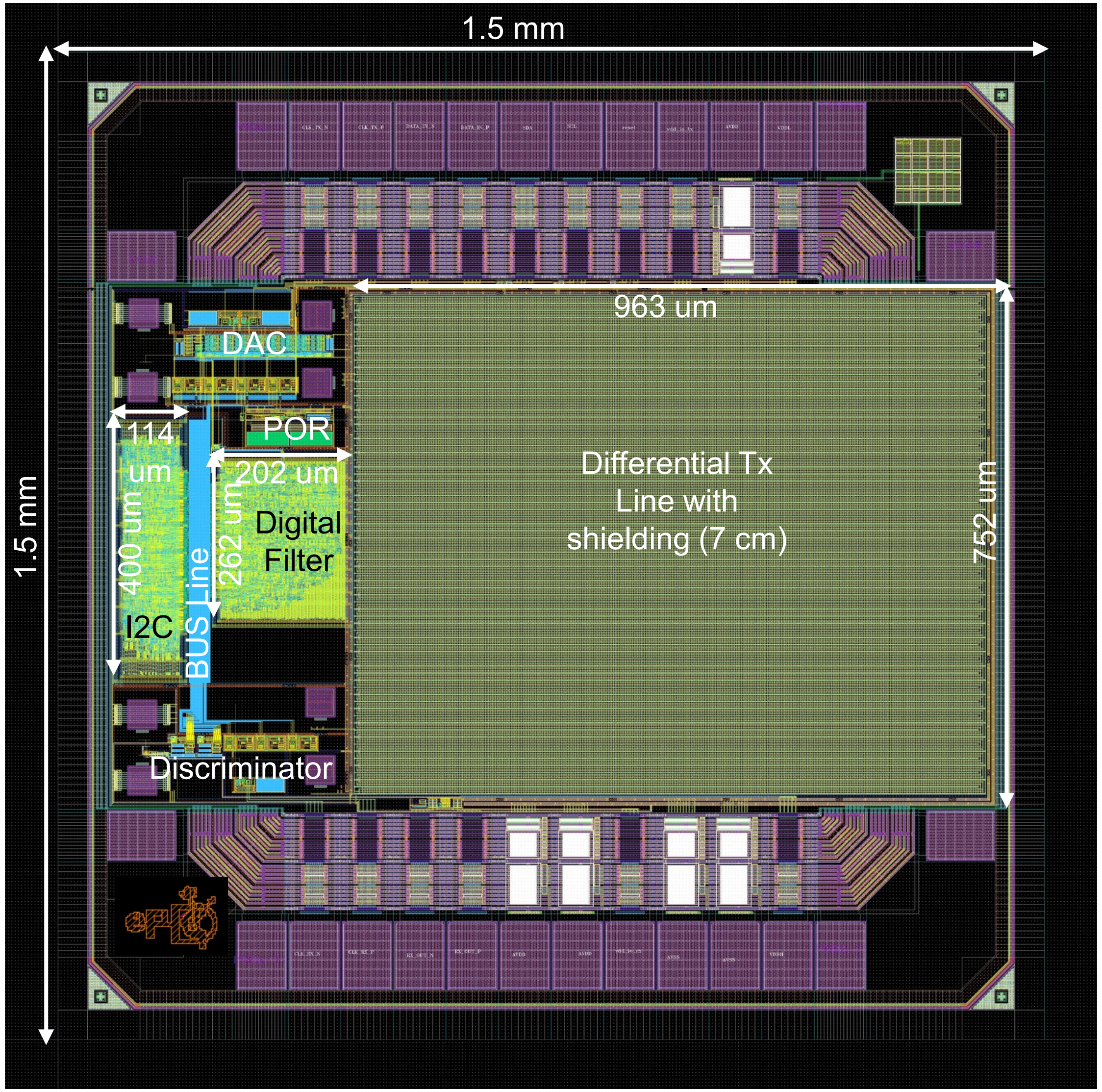


Figure 3.34: Block diagram of the sensor segment.

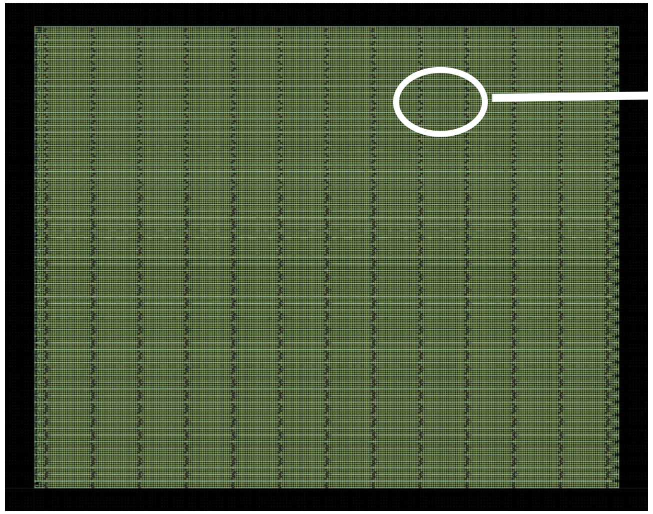


Alice/ITS3

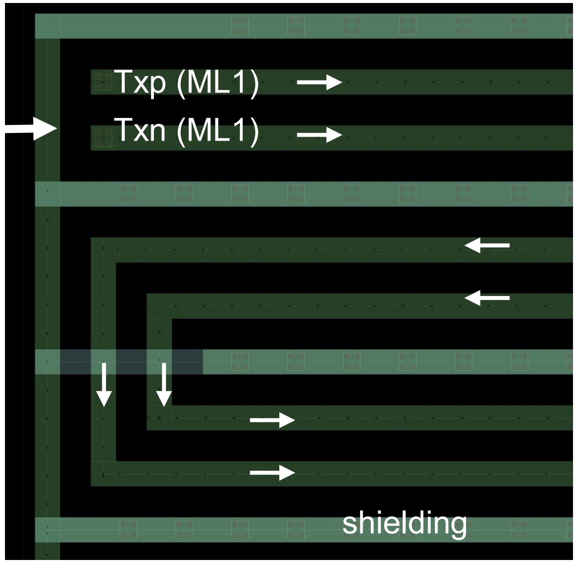
Layout of BTLE-Driver (Test Chip)



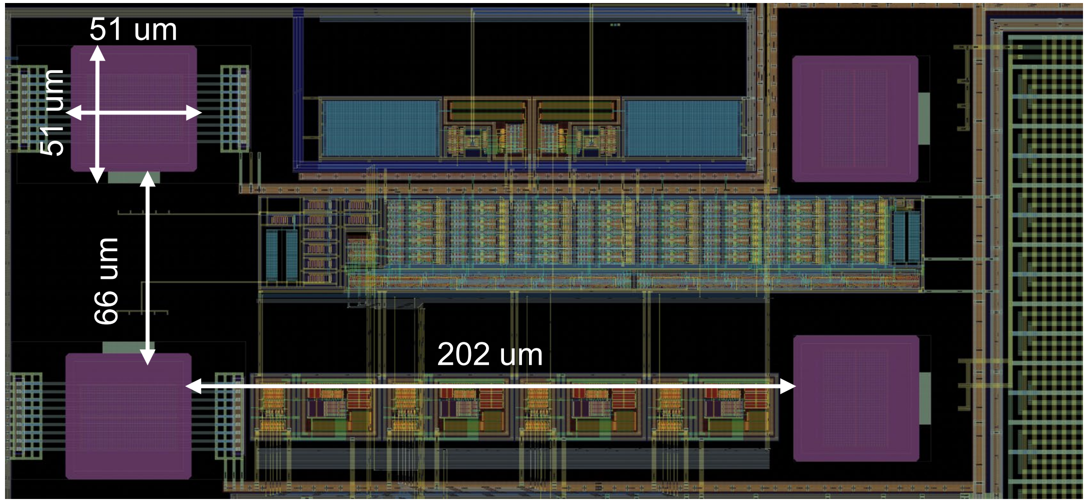
Layout of BTLE-Driver



Folded Differential Tx Line (7 cm)



Orientation of the Tx Line
Metal: ML1
Width: 1.6 um Spacing: 2 um



Open Bond pad

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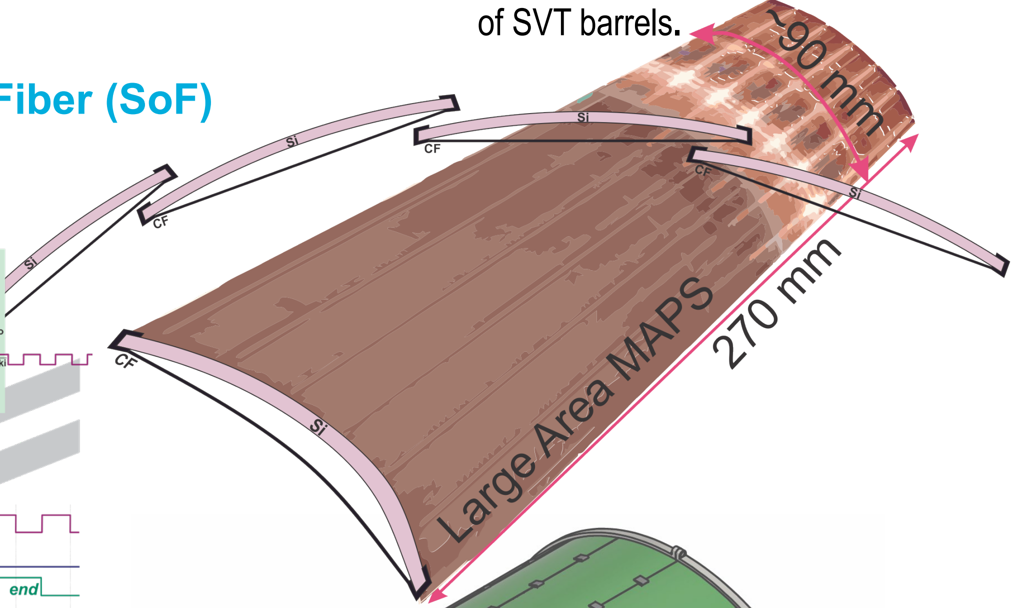
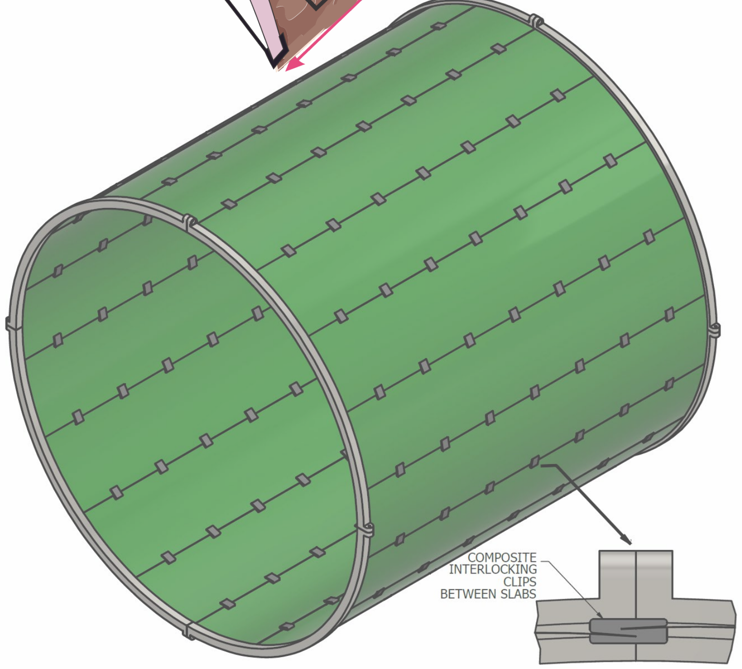
Original research goals for LDRD

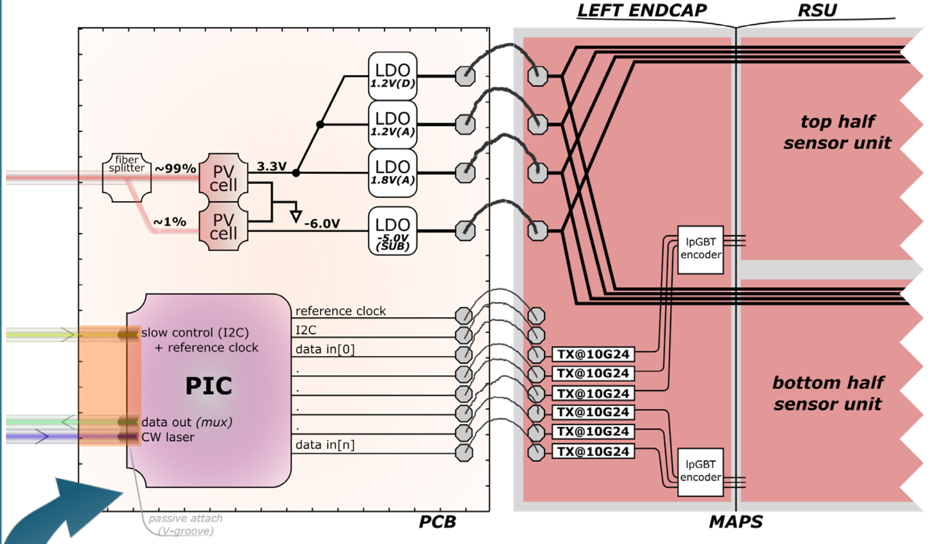
Provide solution for MAPS-based SVT for EIC (upgrade – aka Detector2)

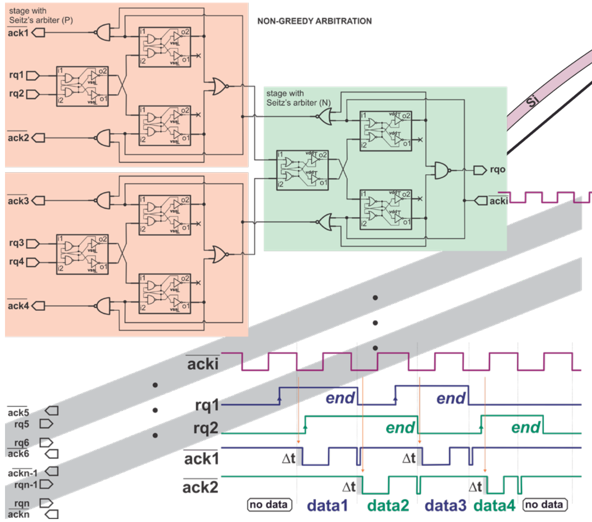
- **Timing resolution: ~100 ns or better**
- **Lightweight detectors: self supporting barrel layers**
- **Power and signal integrity: Power over Fiber (PoF) and Signal over Fiber (SoF)**

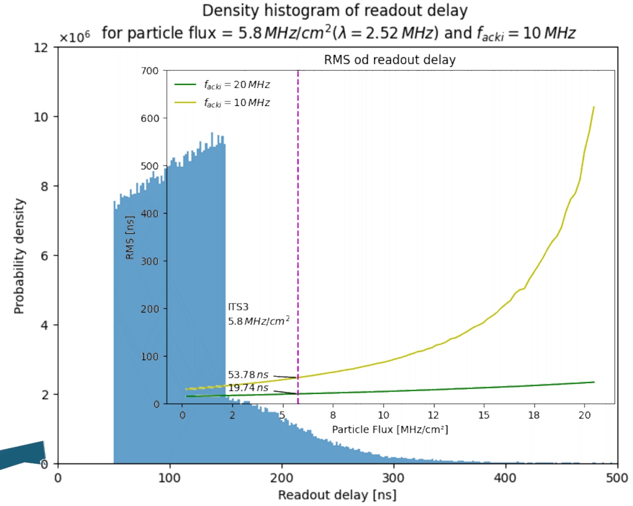
Develop self-supporting staves made of pre-bent large-area MAPS clipped to form “cylinders” of SVT barrels.











Develop Photonic PCB technology hosting to be develop Photonic Integrated Circuit for High-Speed Wavelength Division Multiplexed Data Transmission and to be develop Watt-level power delivering over fiber

Develop Next Generation (Half-Duplex) Event Driven with Access and Reset Decoder EDWARD (partially LDRD 21-020) enhanced by direct communication of configuration and calibration data to pixel for frame-less (~100ns timing resolution) readout

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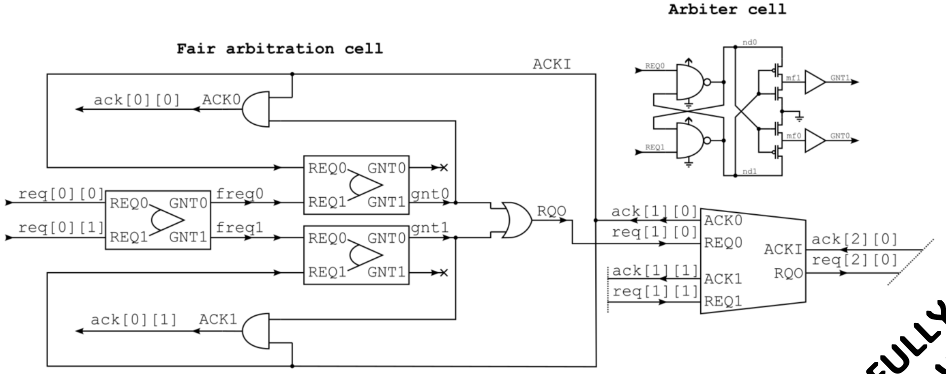
ReadOUT (EDWARD implementation)

0.5V supplied Analog Front-End in TPSCo65

Per pixel power supply - invariable and temperature - compensated nA-level current reference developed to complete previously achieved analog front-end design

Half-Duplex (HD) event-driven readout

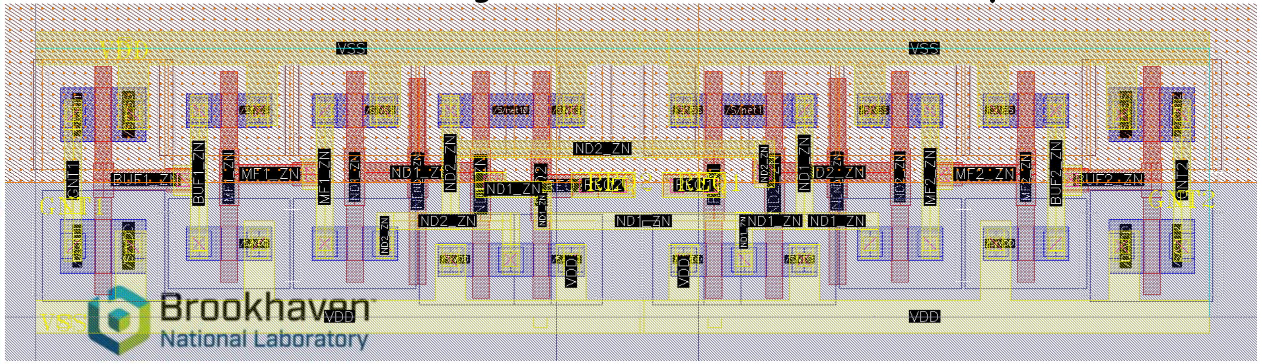
DYNAMIC ARBITRATION TREE (aka EDWARD – patent pending), enhanced with return communication to pixels using arbitration resources for ultra-compact implementation (aka SIRENA – ROI submitted and transferred to patent attorney).

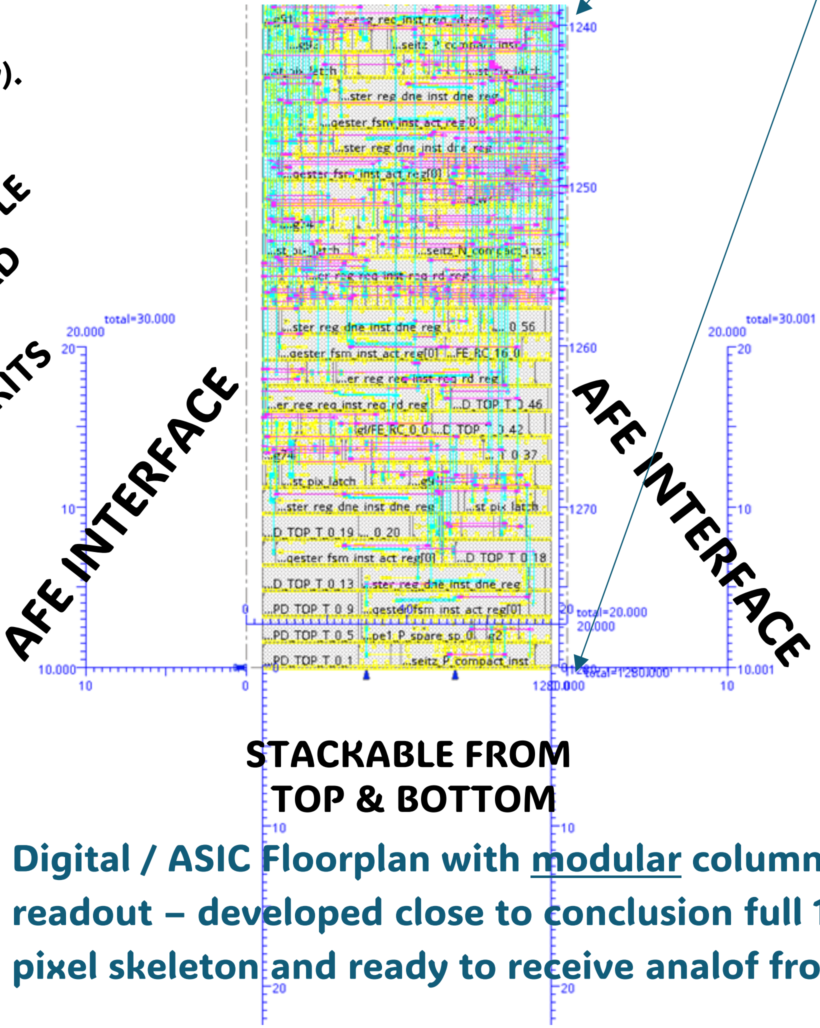


FULLY IMPLEMENTABLE WITH STANDARD DIGITAL DESIGN KITS

ASYNC EVENTS ⇨ SYNC READOUT

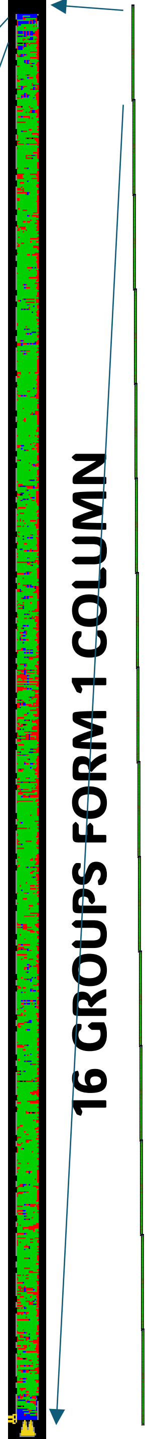
CUSTOM MADE 8T STD LIBRARY INCLUDING NON-STANDARD CELLS - developed and characterized for timing models suitable for CAD/Eda implementation





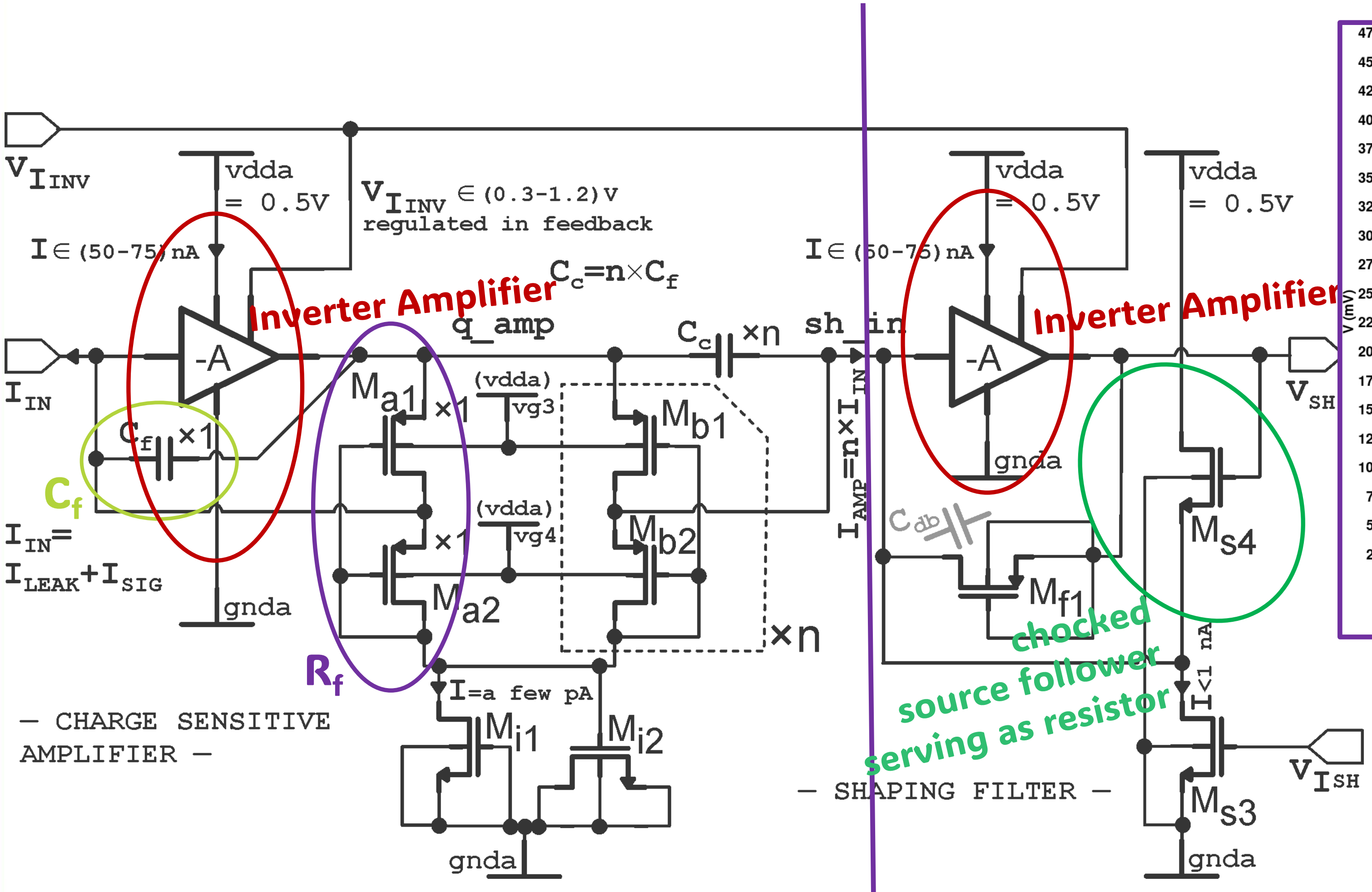
STACKABLE FROM TOP & BOTTOM

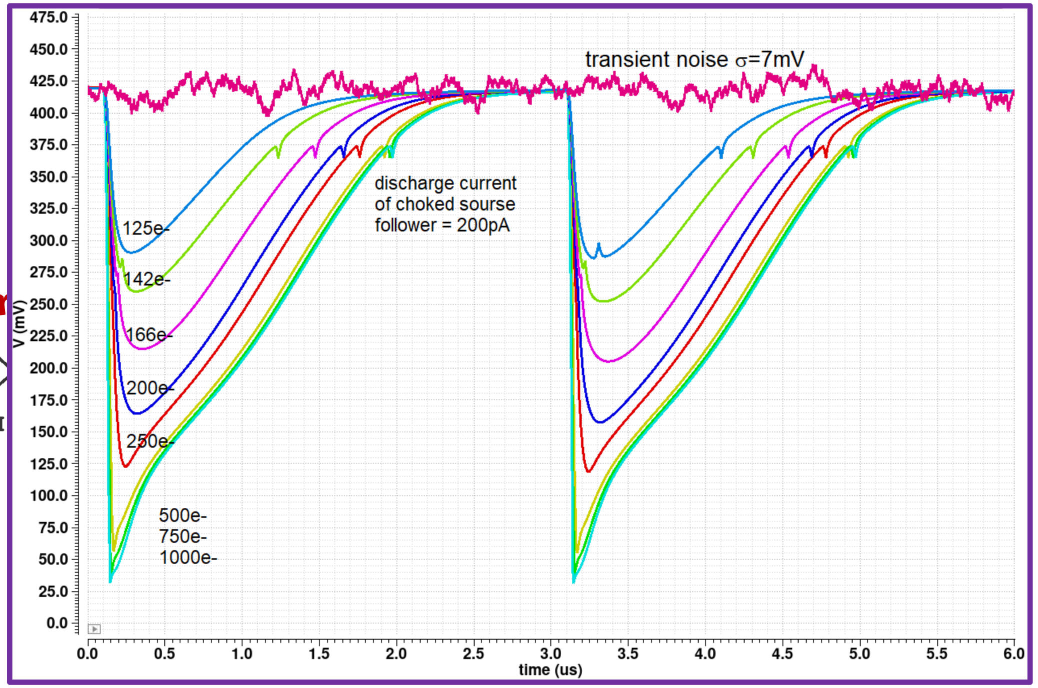
Digital / ASIC Floorplan with modular column readout – developed close to conclusion full 1M pixel skeleton and ready to receive analof front-end



Front-end (CASCADE implementation)

Analog Front-End for Binary Readout





waveforms from transient simulations of the CSA-shaping filter part for input charge signal ∈(125 e- , 1000 e-) showing ~1 mV/e- sensitivity

charge multiplier ← | → I→V stage / shaping filter

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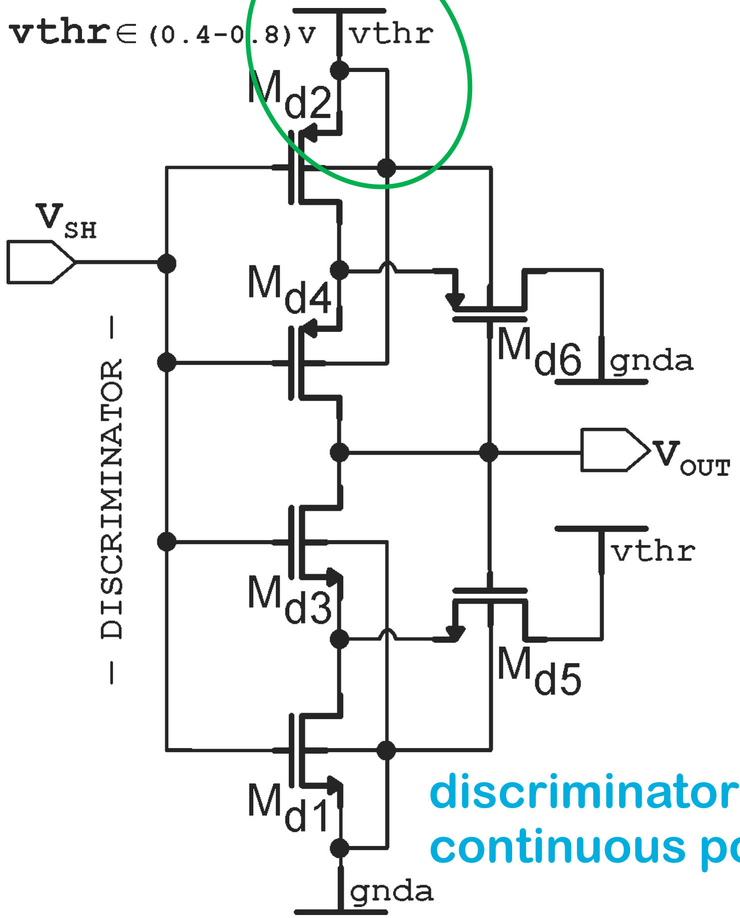
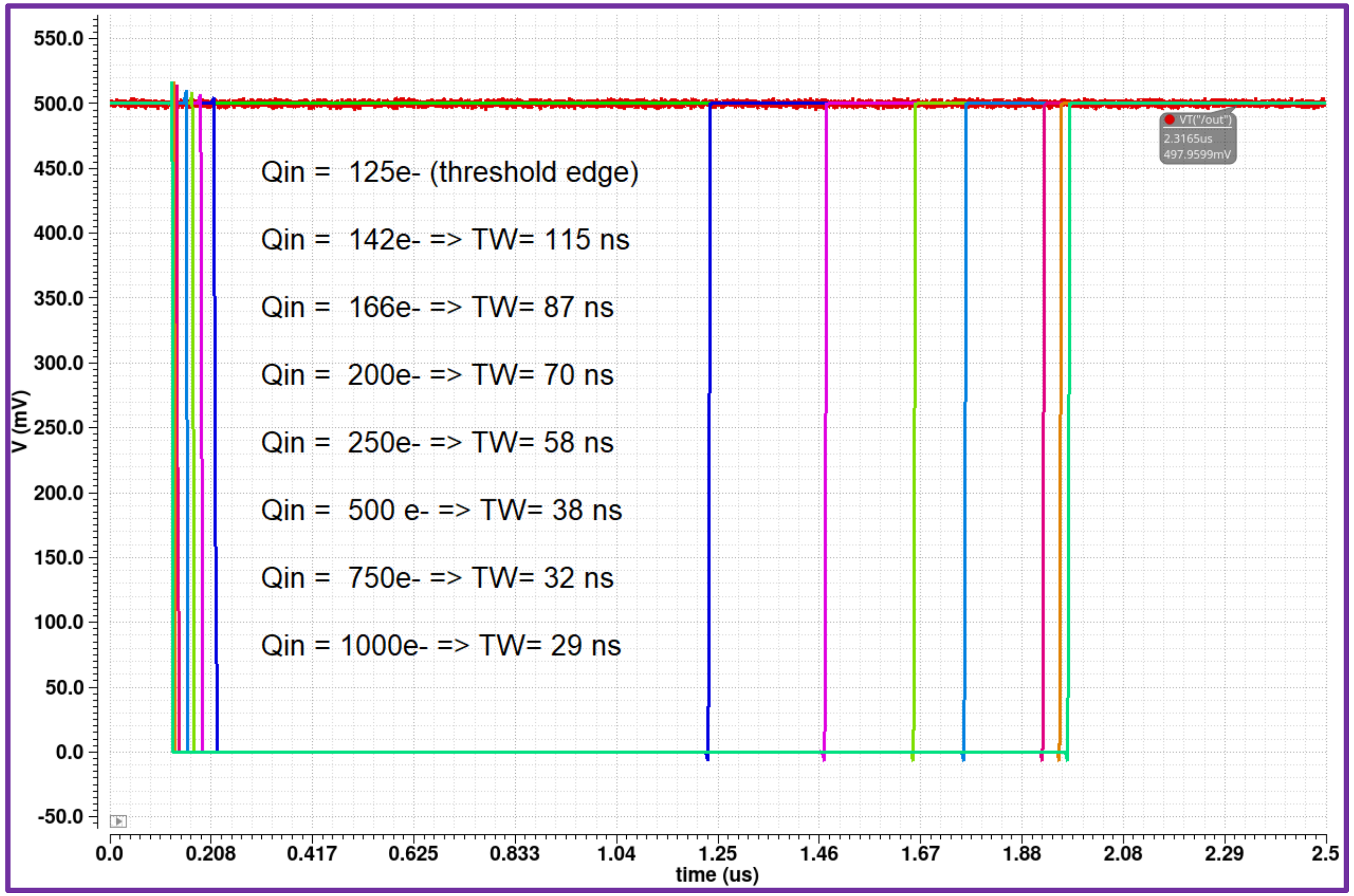
C’ed

Discriminator

power supply
⇨ threshold



discriminator zero continuous power



responses of Schmitt trigger gate used as a discriminator for input charge signal from ∈(125 e^- , 1000 e^-) @ TimeWalk < 115 ns

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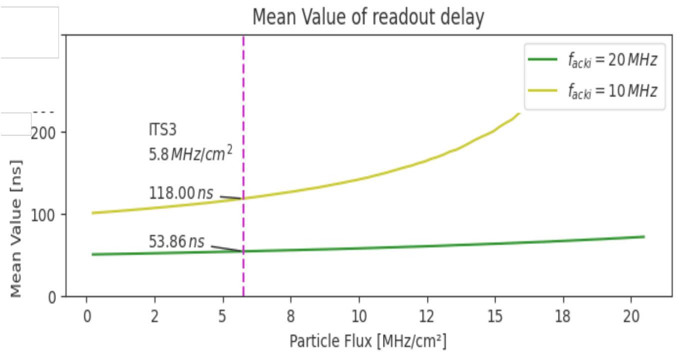
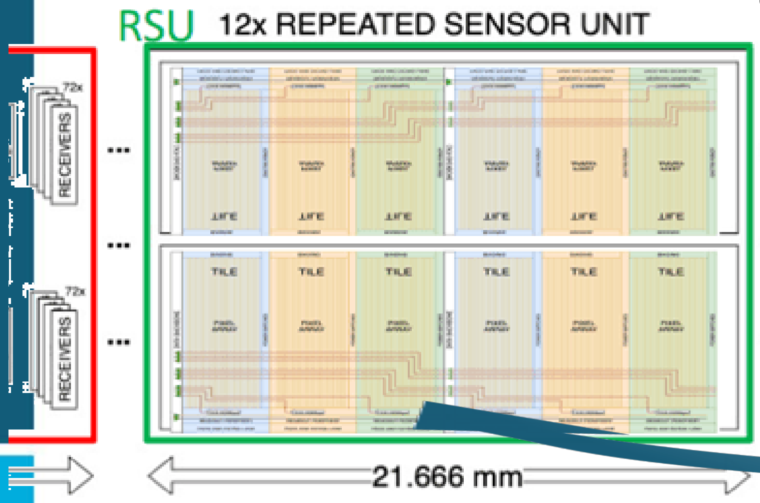
Submission for fabrication

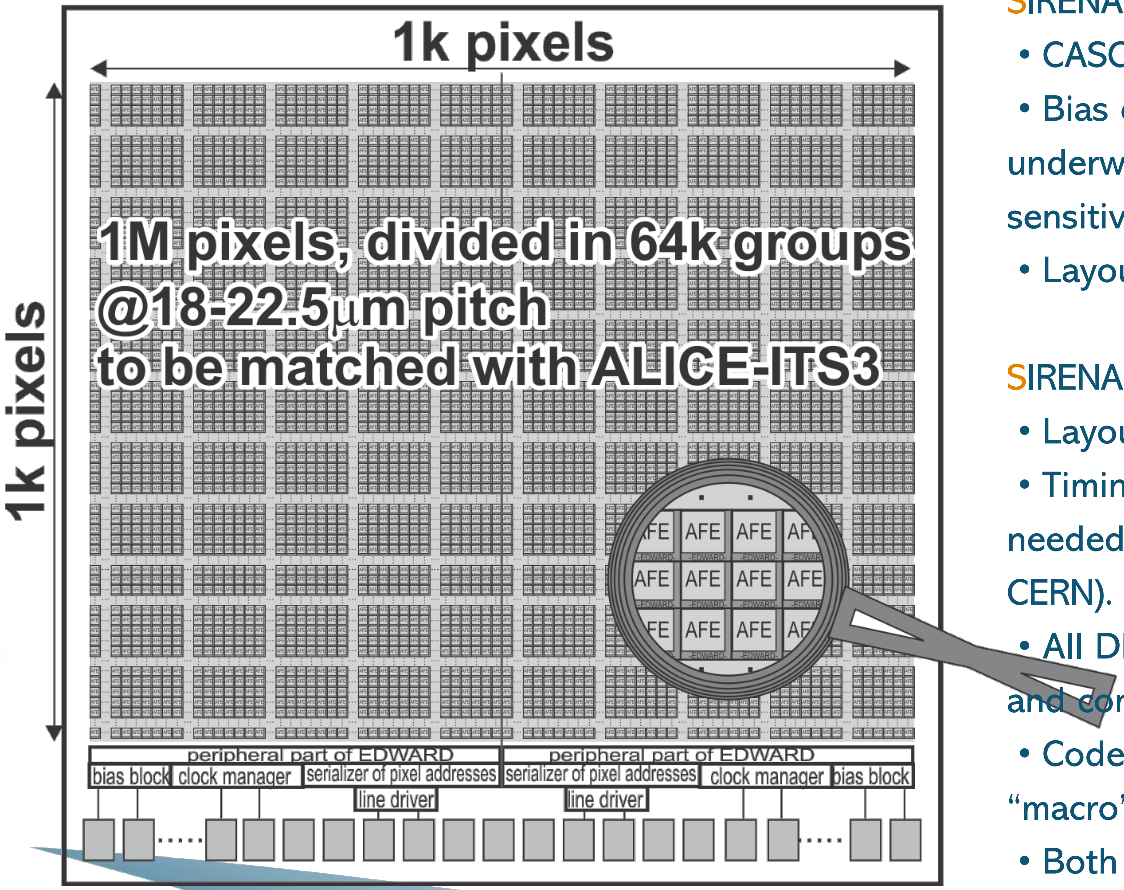
- ALICE-ITS3 is **priority-encoder** based with
- **framed readout** ➡ poor σ_t=5 μs);
- ePIC at EIC **need event-driven** ➡ σ_t=~100 ns);

EDWARD ability



ALICE –ITS3 TDR and technical presentations





to be produced (good demonstrator, basic experiments, train before stitching) suitable for replacing ALICE-ITS3 RSU

MAPS Core Development

SIRENA – CASCADE related

- CASCADE – amplifier schematics is ready.
- Bias current / pixel stabilization circuits is underway (temperature and power supply sensitivity reduced).
- Layout is ready to be started.

SIRENA – EDWARD related

- Layout library is ready.
- Timing libraries are in preparation (still needed to re-characterize the cells from CERN).
- All DRC, LVS, and PEX checks are satisfied and complete.
- Code has been modified so that all "macro" cells are applied without changes.
- Both digital and analog simulations confirm the functionality of the architecture.
- Column is nearly ready for synthesis and reimplementation.

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Technical goals

Immediate Term (MAPS)

Fabrication of ASIC: 1Mega-Pixel Monolithic Active Pixel Sensors MAPS

- pixel size: 22.5×22.5 μm^2 - 27.0×27.0 μm^2 , pixel array size: 960×960 - 1024×1024 pixels (physical size close to reticle dimension)
- sensitivity: to relativistic charged particles including electrons (tracking and imaging)
- readout: binary information ‘yes’ or ‘no’ hit per pixel, event-driven readout ➡ improved timing resolution
- target: upgrades of electron-Proton / Ion Collider (ePIC) Silicon Vertex Tracking (SVT) Detector for U.S.-based Electron-Ion Collider (EIC) [https://www.bnl.gov/eic/epic.php]
- process: Uozu Fab Process, the same TPS65ISC process as CERN’s ALICE ITS3 detector with 7-metal layer option (7M2L1F) on high-resistivity substrate with extra doping
- fabrication options:
  - dedicated mask set
  - can we have pioneer shuttle run (for development)?
- formal status: NDA and DKLA agreements finalized; Tower’s team to provide a cost estimate and timeline
- design readiness status: implementation of half-duplex Event-Driven With Access and Reset Decoder digital implementation (US20240193116A1) and sub 100 nW Analog Front End (WO/2024/086081) is underway,

Results of LDRD21-020, LDRD24-054

and other combined sources of funding

EDWARD
Event-Driven W/ Access And Reset Decoder

The only existing solution in the detector community that most closely approaches the ideal event-driven readout: performing arbitration between asynchronously arriving input signals, non-framing, free of geographical preference, collision-free in data transfer, and equipped with an automatic mechanism reconciling the asynchronous nature of input signals with the typically synchronous character of acquisition systems. While many groups are currently pursuing event-driven readout, ours is the only one experimentally validated with these features, making it a valuable basis for establishing collaborations.

patent pending: *Event-driven readout system with non-priority arbitration for multichannel data sources*
WO EP US JP AU US20240193116A1 • Priority 2021-04-16 • Filed 2022-03-31 • Published 2024-06-13

SIRENA
Segmented Ionizing Radiation with Event-Notified Acquisition

An overarching solution that builds on prior developments and adds key features:

- Half-duplex communication - essential for mega/giga-pixel systems to selectively program, calibrate, and test individual pixels, while reusing the hardware arbitration resources already present for readout, yielding major hardware savings.
- Autonomous triggering - enabling each pixel to define events through potentially complex data-processing algorithms. This is highly valuable, from realizing the fastest counting detectors to implementing artificial intelligence models.

Selected for participation in:

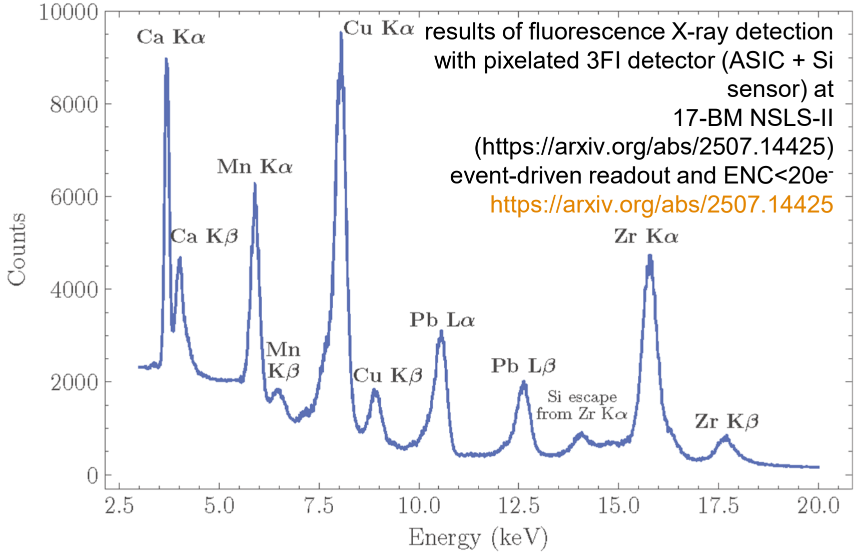
- TCF DOE BOOST program led by Sandia with BNL as one of the partner labs.
- Energy Innovation Commercialization Fellowship (Formerly MSI Connect).

patent application in process: *Segmented electronic system with event-driven readout, selective configuration programming, and multi-channel analysis integrated in each element* • Priority 2024-10-15 • Filed XX • Published XX

A new charge amplifier — no longer relying on the traditional Krummenacher feedback scheme for sensor leakage current absorption. This approach enables pole-zero cancellation, allowing direct amplification of the charge signal in an unconditionally stable manner, fully compatible with compact amplifier–filter architectures for pixel detectors. It also supports operation at significantly reduced supply voltage, ensuring low power consumption while still achieving excellent signal-to-noise performance.

CASCADE
Charge Amplifier
w/ Self-Cascoded Adaptive Discharge Element

patent pending: *Charge-sensitive amplifier with pole-zero cancellation*
WO WO2024086081A1 • Priority 2022-10-17 • Filed 2023-10-16 • Published 2024-04-25



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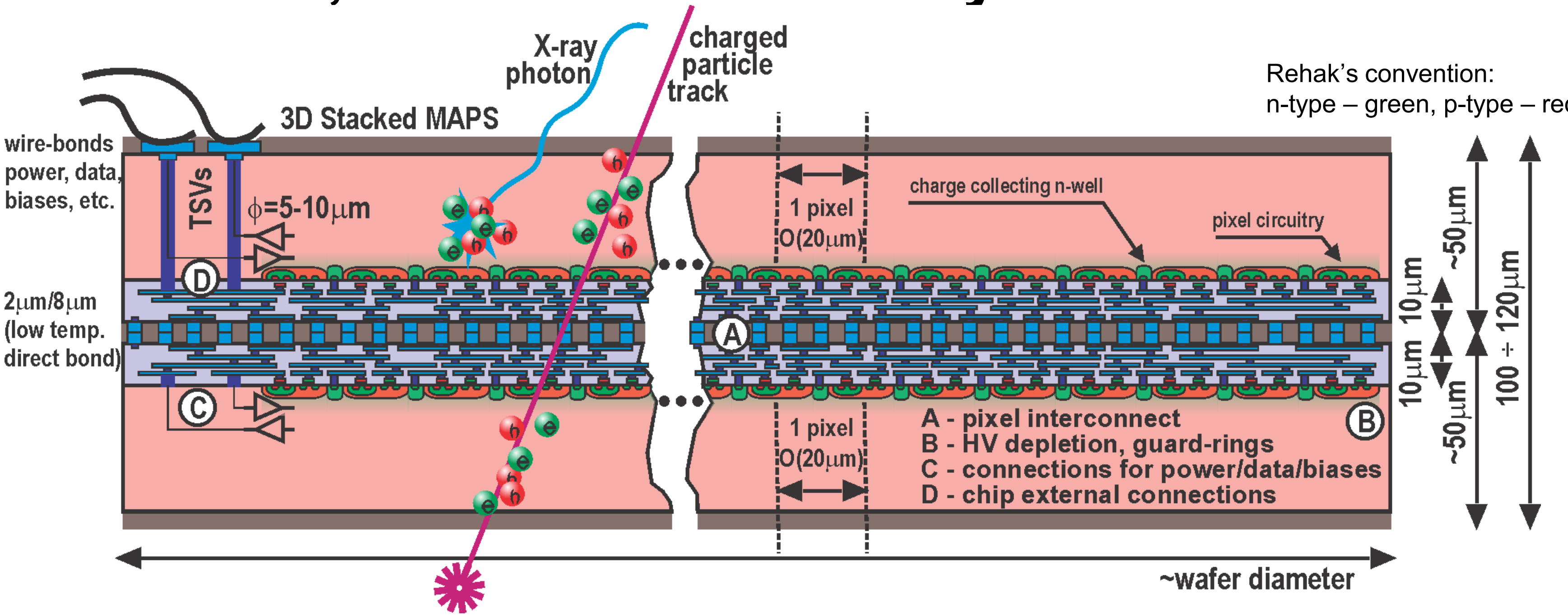
Other sources of funding: DOE Office of BER B&R: 456165021; NASA Grant NNX16AC42G; DOE Office of Science, DE-SC0012704, KA2501032/FWP# PO024; TM 24-01 ATRO/IO - FY24TMAUG

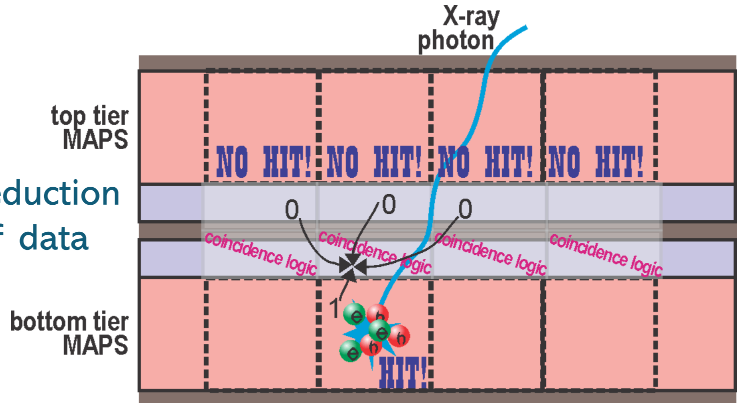
Direction on enhanced, 3D-stacked MAPS layers

Rehak's convention:
n-type – green, p-type – red

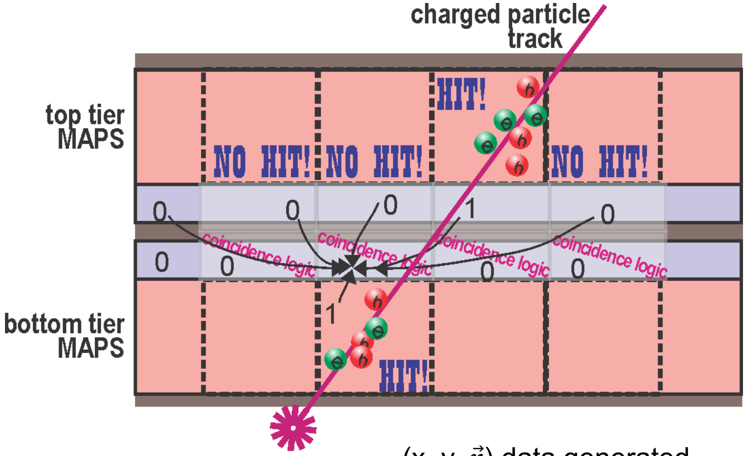


Thin, 3D-stacked, large-area MAPS detector, providing in-situ x-ray background rejection and generating tracking primitives (x, y, local direction, time, quality flags) ⇨ AI-ready vertexing and tracking

reduction of data



no data generated



(x, y, $\vec{r}$) data generated

reduction of combinatorics in reconstruction / tracking

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Motivation for 3D-stacked MAPS layers

Physics-Driven Detector Needs in Lepton-Collider Environments

– Operation in regimes dominated by synchrotron and beam-induced X-ray backgrounds in the vertex and inner tracking regions.

– Exceptional vertex resolution, low-momentum tracking performance, and ultra-low material budgets precision ⇨ physics goals (Higgs couplings, flavor / heavy-quark tagging, τ physics, rare decays).

➡ Common need for detectors that remain performant in background-dominated conditions, not merely higher-granularity versions of today's planar pixel sensors.

Rethinking "AI at the Edge" for Vertexing and Tracking

– AI/ML models inside pixel sensors are power- and area-prohibitive, and lack access to contextual information ⇨ ineffective.

– For vertexing and tracking, meaningful intelligence must be architectural, not algorithmic: shaping what data are generated, when they are generated, and what metadata accompany them.

– AI is to be downstream, operating on detector outputs that are already structured, sparse, and information-rich.

➡ AI-suited rather than "AI-embedded" detectors: early correlations, directionality, quality flags, and uncertainty information.

Intelligent Stacked MAPS as an Enabling Architecture

– Stacked MAPS with vertically integrated sensing and processing tiers and event-driven operation.

– Local coincidence, charge/timing correlation, and simple topological logic to reject X-ray background and identify correlated hits.

– Early tracklets and directionality metadata inside the detector before full readout.

– Only background-cleaned, correlated data to higher-level acquisition and reconstruction.

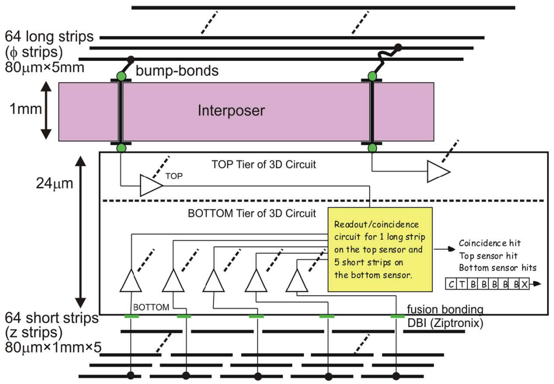
Impact on Tracking, Vertexing, and System Design

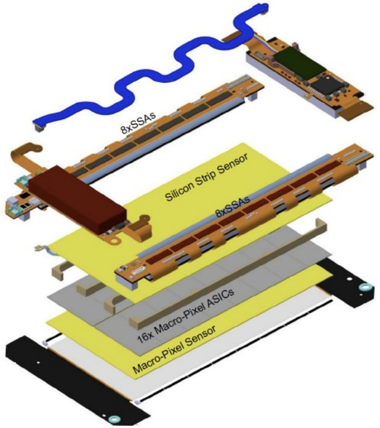
– Early tracklet formation reduces hit combinatorics and lowers downstream computational load.

– May enable fewer layers, optimized spacing, alternative topologies, while maintaining or improving physics performance.

- Establishes a path toward detectors that actively participate in reconstruction, rather than acting as passive imaging devices.

L1 trigger in the tracker upgrade of the CMS experiment at SLHC using the VICTR chip (Deptuch et al., IEEE Trans. on Nucl. Sci., Vol. 57, No. 4, AUGUST 2010)





exploded view of the PS module: key components are: the strip sensor (yellow), MPAs (grey) and the macro-pixel sensor in the central part of the module. (M.Osherson CMS collab. 2022 JINST 17 P06039)

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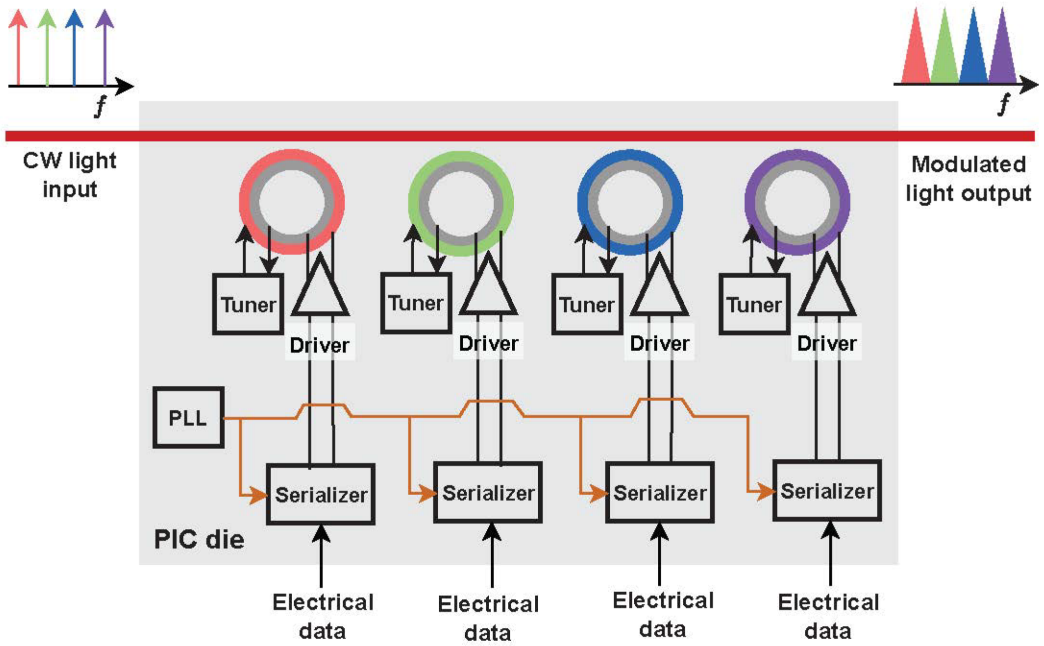
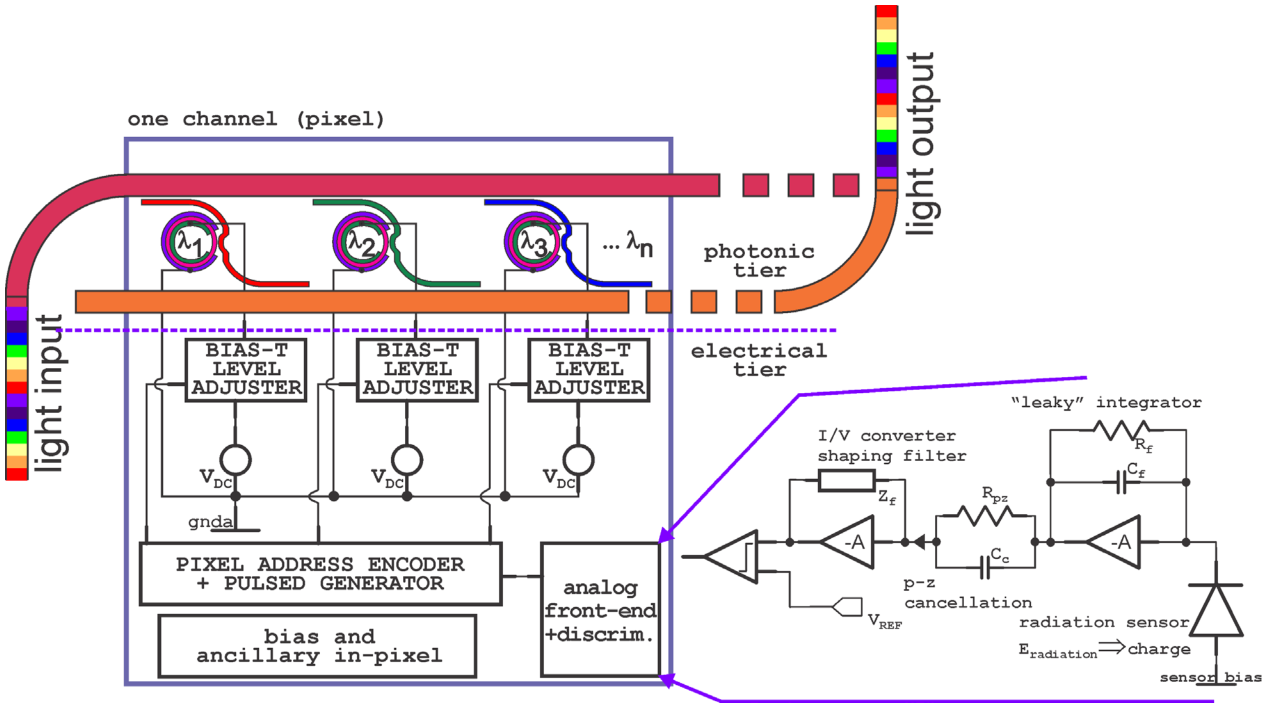
Electro-Photonic Detector Readout



micro-ring resonant modulators are used for data transmission, allowing modulation of CW in data transmission



through 3D integration of MAPS with Si-photonics, electrical data transfer can be eliminated

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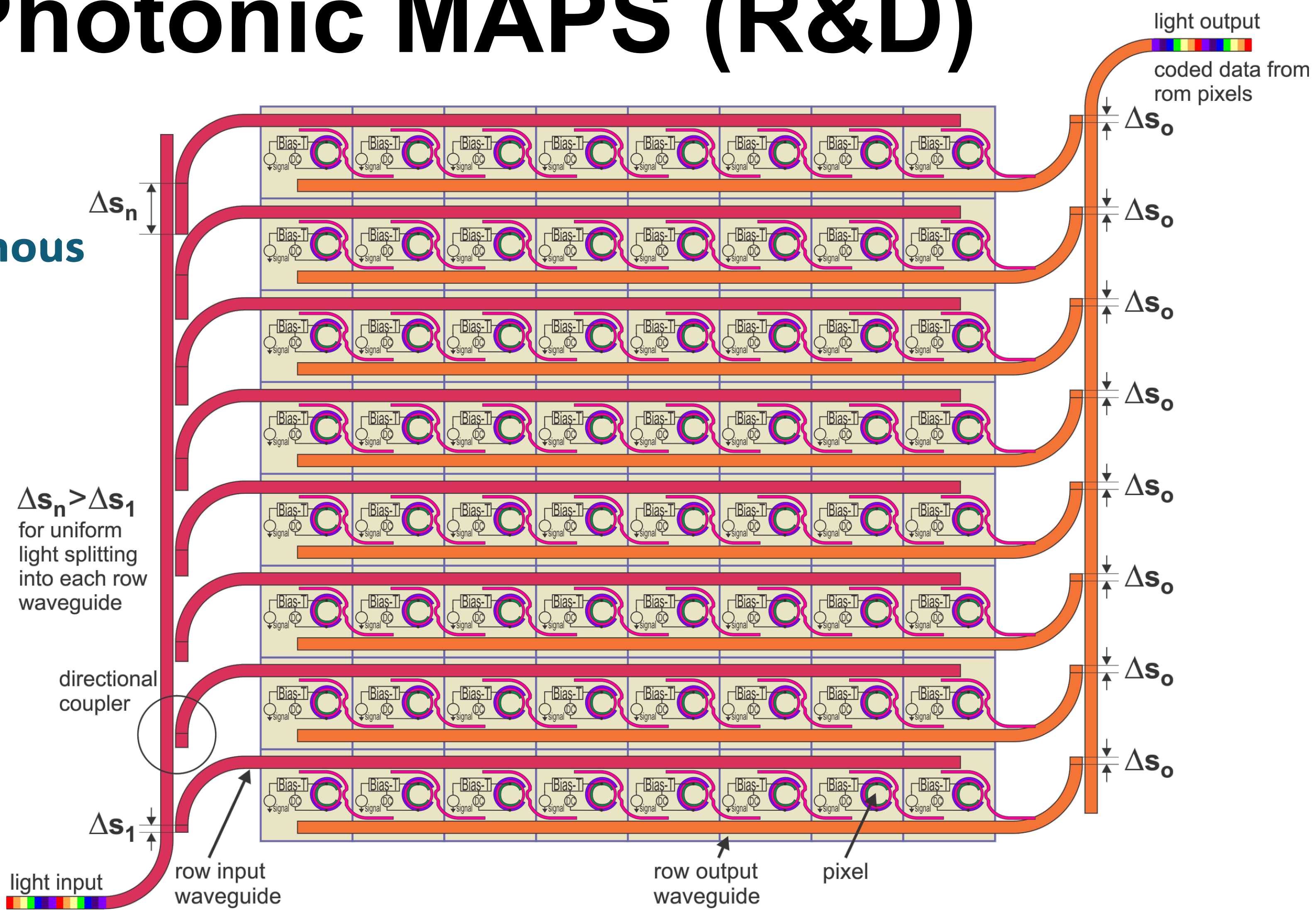
Electro-Photonic MAPS (R&D)

Optical MAPS
Based on heterogenous integration



➨ funded DOE proposal !⬅

[Department of Energy Announces $179 Million for Microelectronics Science Research Centers | Department of Energy]

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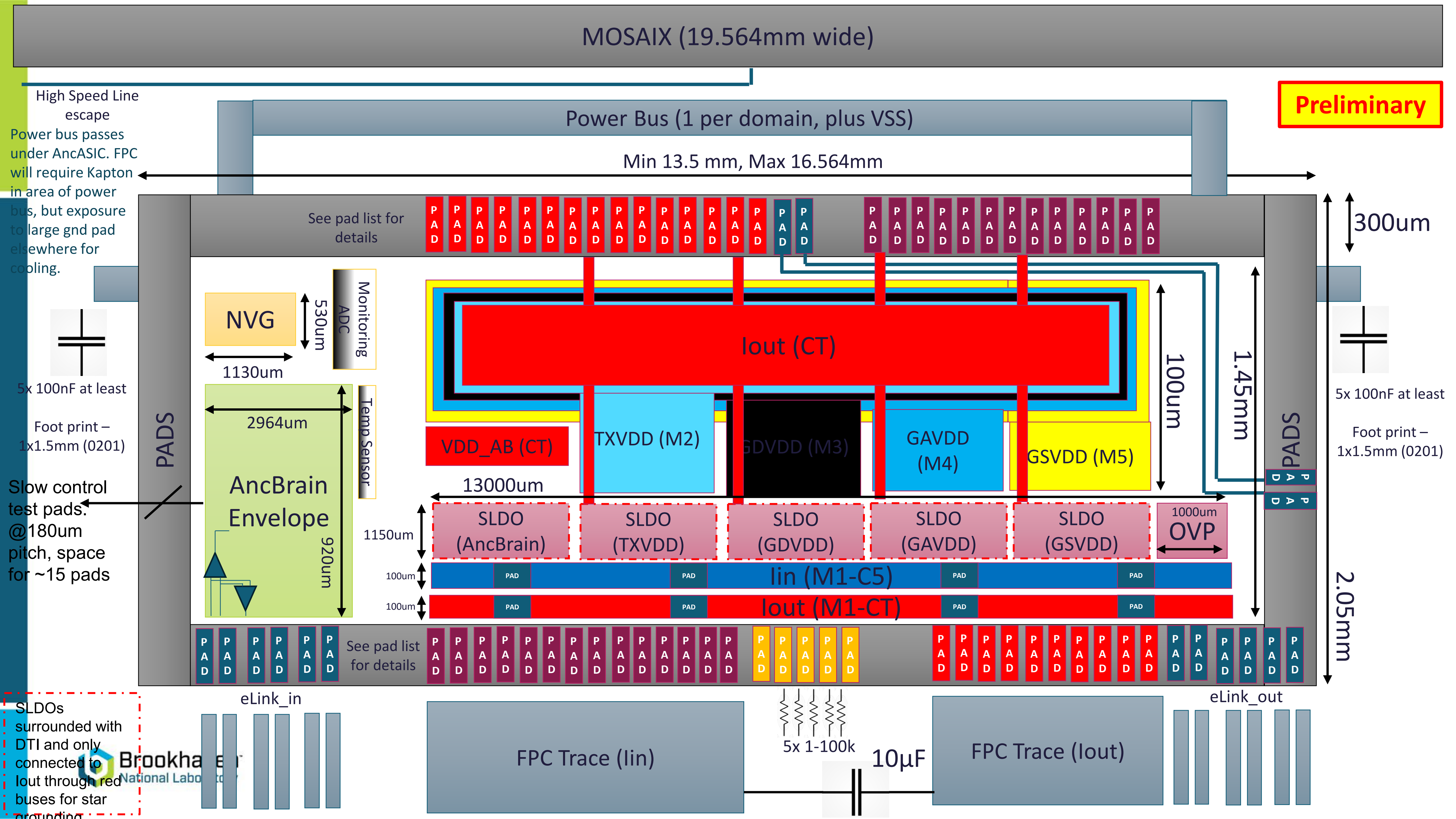
AncASIC required for:
- Power
- Negative Bias
- Slow Control Management

G.W. Deptuch,

05/13/2026

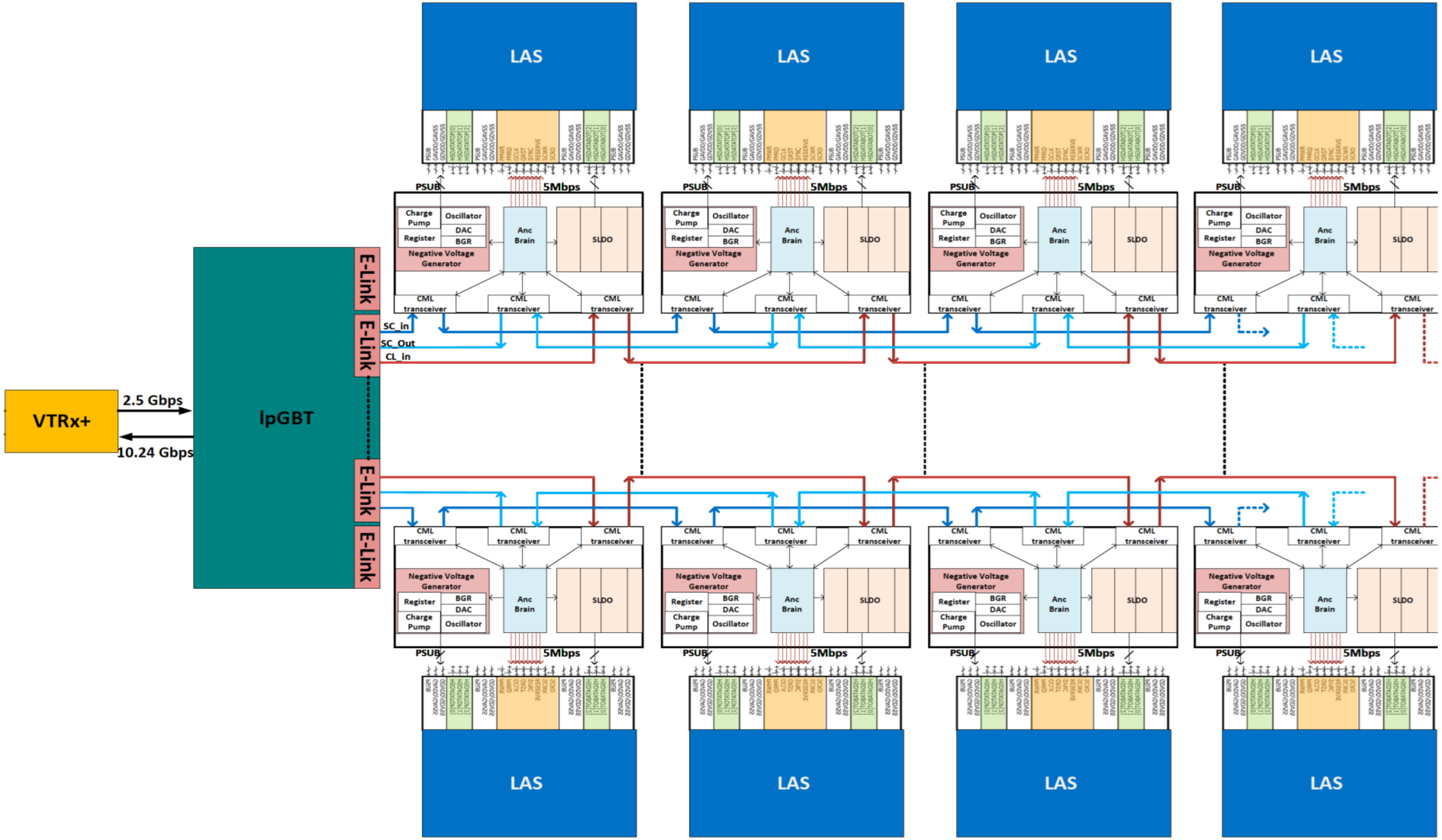
Why AncASIC?

- ePIC SVT contains tens of billions of MAPS pixels tracking system, creating stringent requirements on scalable power and control distribution.
- Outer SVT barrel layers and disks adopt serial powering to minimize material budget, cabling complexity, and power distribution overhead.
- AncASIC_XT011 was developed as a dedicated support ASIC enabling serially powered MAPS operation in the ePIC SVT environment.
- The ASIC integrates multi-domain shunt regulation to stabilize power delivery across chained detector modules.
- AncASIC provides programmable negative bias generation required for depletion and operation of radiation-sensitive MAPS sensor volumes.
- The chip is implemented in XFAB 0.11 μm HV PD-SOI technology, enabling isolated substrate islands and improved radiation tolerance.
- Thin PD-SOI substrate suppresses back-gate effects and improves resilience against ionizing radiation and single-event effects.
- AncBrain, the embedded custom processor operating at 160 MHz, manages communication, monitoring, synchronization, and system control.
- AncASIC interfaces directly with lpGBT ePort links and supports daisy-chain operation compatible with one ASIC per MAPS module architecture.
- Integrated monitoring functions include voltage, temperature, leakage current sensing, ADC-based diagnostics, and programmable synchronization strobes for autonomous sensor readout.



MOSAIX (19.564mm wide)
Preliminary
High Speed Line escape
Power bus passes under AncASIC. FPC will require Kapton in area of power bus, but exposure to large gnd pad elsewhere for cooling.
Power Bus (1 per domain, plus VSS)
Min 13.5 mm, Max 16.564mm
300um
See pad list for details
PAD
5x 100nF at least
Foot print – 1x1.5mm (0201)
NVG
530um
1130um
Monitoring ADC
Iout (CT)
100um
1.45mm
2.05mm
PADS
2964um
Temp Sensor
AncBrain Envelope
920um
VDD_AB (CT)
TXVDD (M2)
GDVDD (M3)
GAVDD (M4)
GSVDD (M5)
13000um
Slow control test pads. @180um pitch, space for ~15 pads
1150um
SLDO (AncBrain)
SLDO (TXVDD)
SLDO (GDVDD)
SLDO (GAVDD)
SLDO (GSVDD)
1000um
OVP
100um
Iin (M1-C5)
Iout (M1-CT)
See pad list for details
eLink_in
eLink_out
FPC Trace (Iin)
FPC Trace (Iout)
5x 1-100k
10µF
SLDOs surrounded with DTI and only connected to Iout through red buses for star grounding

Location of AncASIC



Some Results (NVBG)

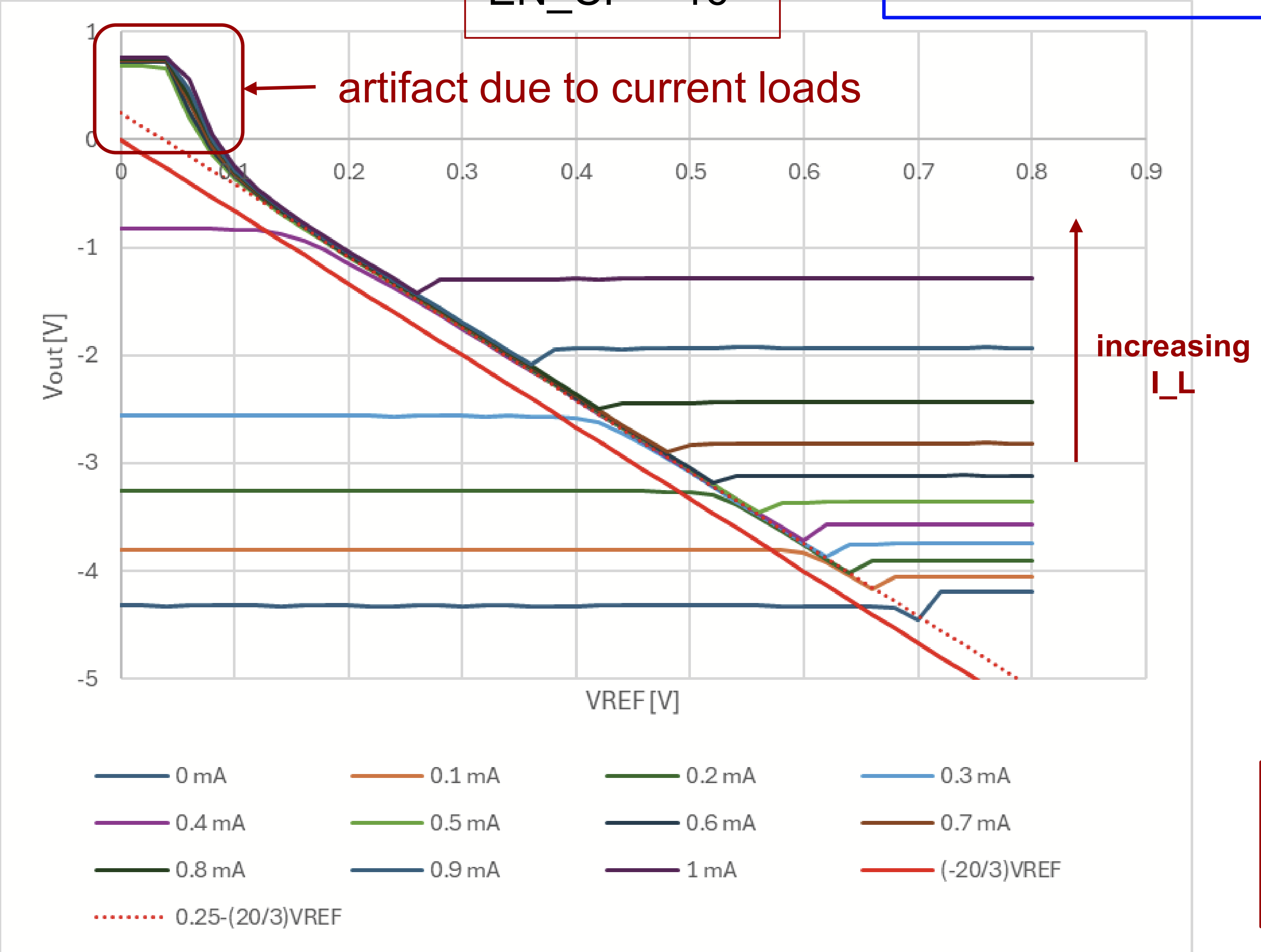
I2C Configuration:

- **Closed Loop, EN = 111**
- **Int. Vc, Main/Aux. CP ON**
- **Ioff, Ivco, Iint = 0000111**

EN_CP = 16

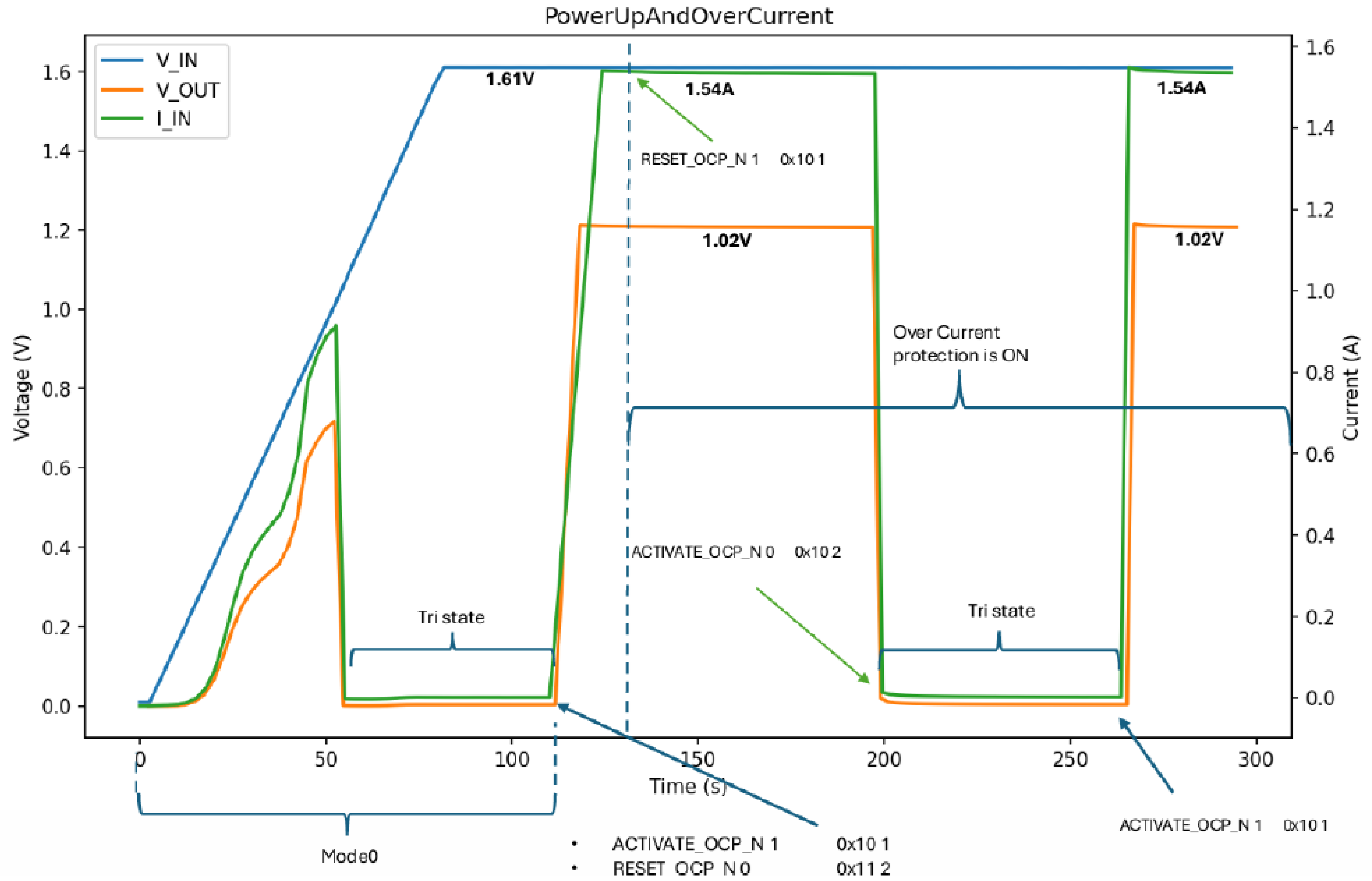
current loads

From previous presentation
WP2 meeting, 03.23.2025



- Closed loop at fixed EN_CP = 16
- All other register values were kept fixed
- Vout5 for different current load in parallel with 1nF capacitive load
- Vout5 follow the linear relationship between VREF with slope (-20/3)
- No load reach ~ -4.5 V
- Positive Vout at low VREF (< 0.1 V) for I_L > 0.4 mA, an artifact due to constant current load

Results (SLDOs)



Test results showing the tests of the SLDO in tri-state mode. In this test, the SLDO is powered up normally, then the tri-state is enabled at around 200s and normal operation resumed at around 260s.