SLAC - TPSCo 65 nm MAPS

Caterina Vernieri on behalf of

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BNL Tracking Workshop

SLAC NATIONAL ACCELERATOR LABORATORY

BNL, May 13 2026

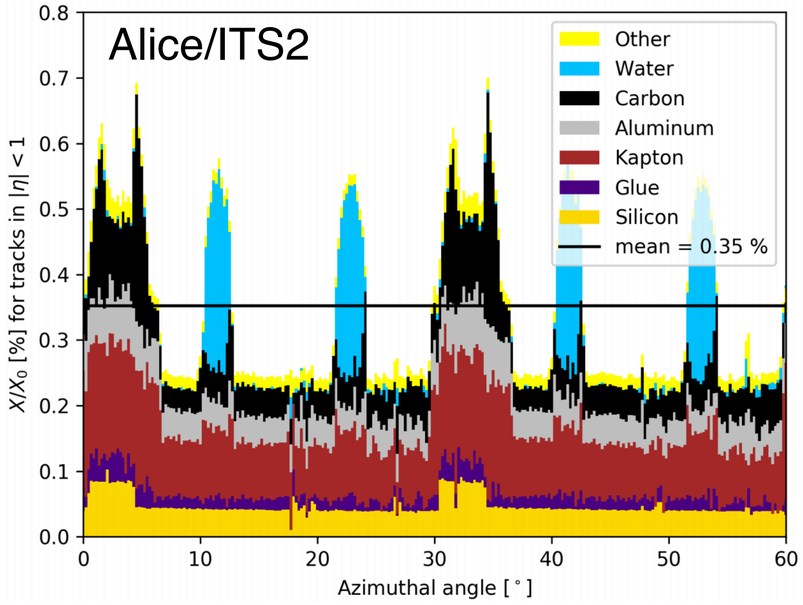
Stanford University | U.S. DEPARTMENT OF ENERGY

Sensors technology requirements for Vertex Detector

Several technologies are being studied to meet the physics performance

- Sensor's contribution to the total material budget is 15-30%
  - Services cables + cooling + support make up most of the detector mass
- Sensors will have to be less than 75 μm thick with at least 3-5 μm hit resolution (17-25 μm pitch) and low power consumption
- Beam-background suppression
  - ILC/C^3 - evolve time stamping towards O(1-100) ns (bunch-tagging)
  - FCC, continuous r/o integrated over ~10μs with O(1) ns timing resolution for beam background suppression

CERN-LHCC-2019-018



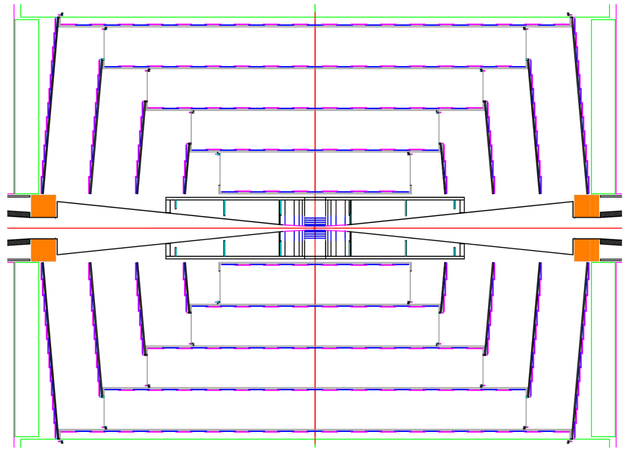
Physics driven requirements		Running constraints		Sensor specifications	
σ	*< 3 µm*			Small Pixel	*~15µm*
Material budget	*0.1%X_0/layer*			Thinning to	*50 µm*
		Cooling		Low Power	*20-50 mW/cm^2*
r of the Inner most layer	*12-14 mm*	Beam-background		Fast Readout	*~1-10 µs*
		Radiation damage		Radiation Tolerance	*10 MRad, 10^{14} n_{eq} / /cm^2*

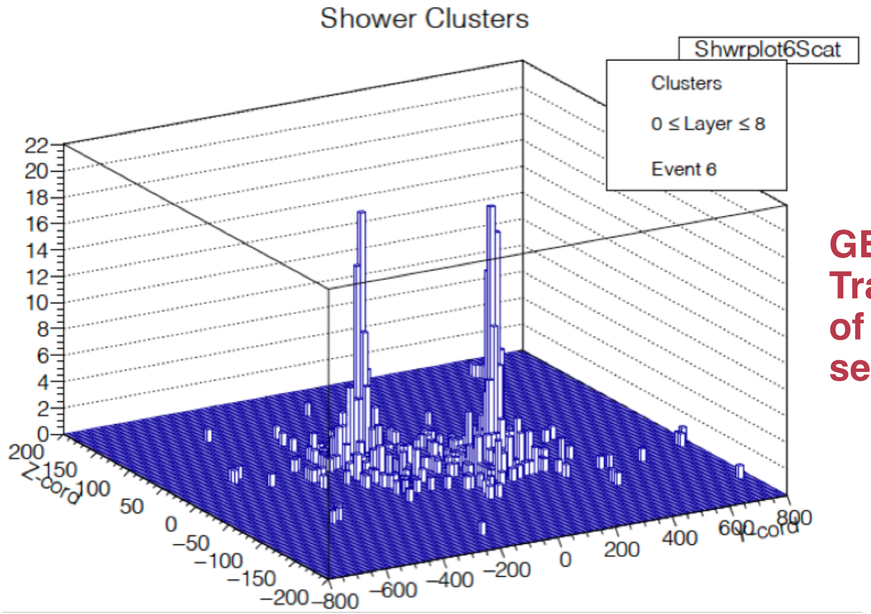
arXiv:1306.6329

Tracking & Calorimeter detectors

Instruments 2022, 6(4), 51

A diverse set of options targeting unprecedented precision





GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

- Full **silicon detectors** (SiD, CLID) aiming at 0.1-0.15% X_0 in the central region
  - MAPS (TJ 65 nm) being investigated but also AtlasPix3 - TSI 180 nm process, 50μm pitch, 175 mW/cm^2 (target 100 mW/cm^2)
- For the ECAL detector
  - Fine granularity allows for identification of two showers down to the mm scale of separation
  - The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR

MAPS SLAC effort

Co-design approach: close interaction between physics studies and technology R&D

- MAPS developments with CERN (WP1.2 Collaboration): TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Builds on sensor optimization done for the TJ180 process[1-2], excellent charge collection efficiency and low capacitance [3]
    - Increased density for circuits: Higher spatial resolution, better timing performance at same power consumption.
  - Supports stitching: enable wafer-scale MAPS → **potential to greatly reduce costs of future experiments**
- ALICE ITS3 upgrade is the main driver of CERN WP1.2 efforts
- Several challenges towards wafer-scale devices → **large international effort needed to address all of them**
  - Large collaboration is interested in designing solutions for power distribution compatible with stitching and enabling O(ns) timing precision

[1] M. van Rijnbach *et al., Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034
[2] M. Munker *et al.*, *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,* 2019 *JINST* 14C05013
[3] S. Bugiel *et al., Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology, NIMA Volume 1040, 1 October 2022, 167213*
[4] J. E. Brau et al., *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, https://agenda.linearcollider.org/event/9211/sessions/5248, 2021.

Large area MAPS – Highlights & Next Steps

Approach:

- Focus on long-term R&D, targeting simultaneously:
  - ~ns timing resolution
  - Power consumption compatible with large area and low material budget
  - Fault-tolerant circuit strategies for wafer-scale MAPS

Highlights:

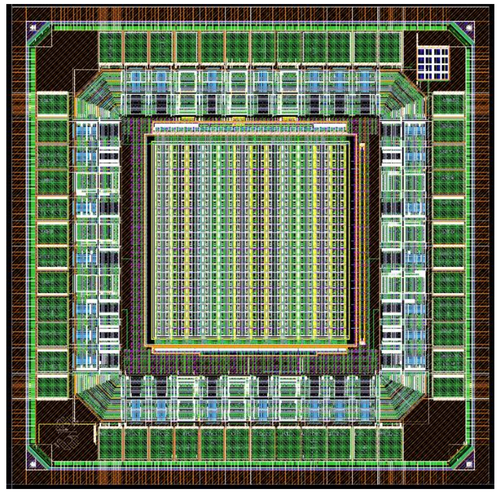
- 1st SLAC prototype on TJ65nm (2023) as part of a CERN WP1.2 shared run
  - NAPA_p1: NAnosecond Pixel for large Area sensors – Prototype 1
- 2st SLAC prototype on TJ65nm (2024) as part of a CERN WP1.2 shared run
  - New design combining O(ns) timing precision and low-power (exp. Summer 2026)

Next steps:

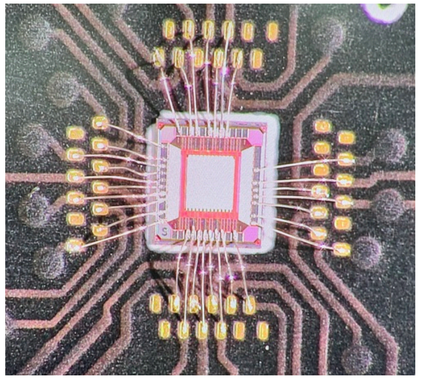
- Finalize characterization of Napa-p1 with laser system
- Characterization Napa-p2 - new DAQ already commissioned

Engagement :

- Higgs Factory detector initiative R&D
- DRD 3.1/7.6 on common issues of power distributions compatible with stitching



Layout of SLAC prototype for WP1.2 2022 shared submission on TowerSemi 65nm



NAPA-p1

Target Specs vs. State of the Art

JINST 19 (2024) 04, C04033

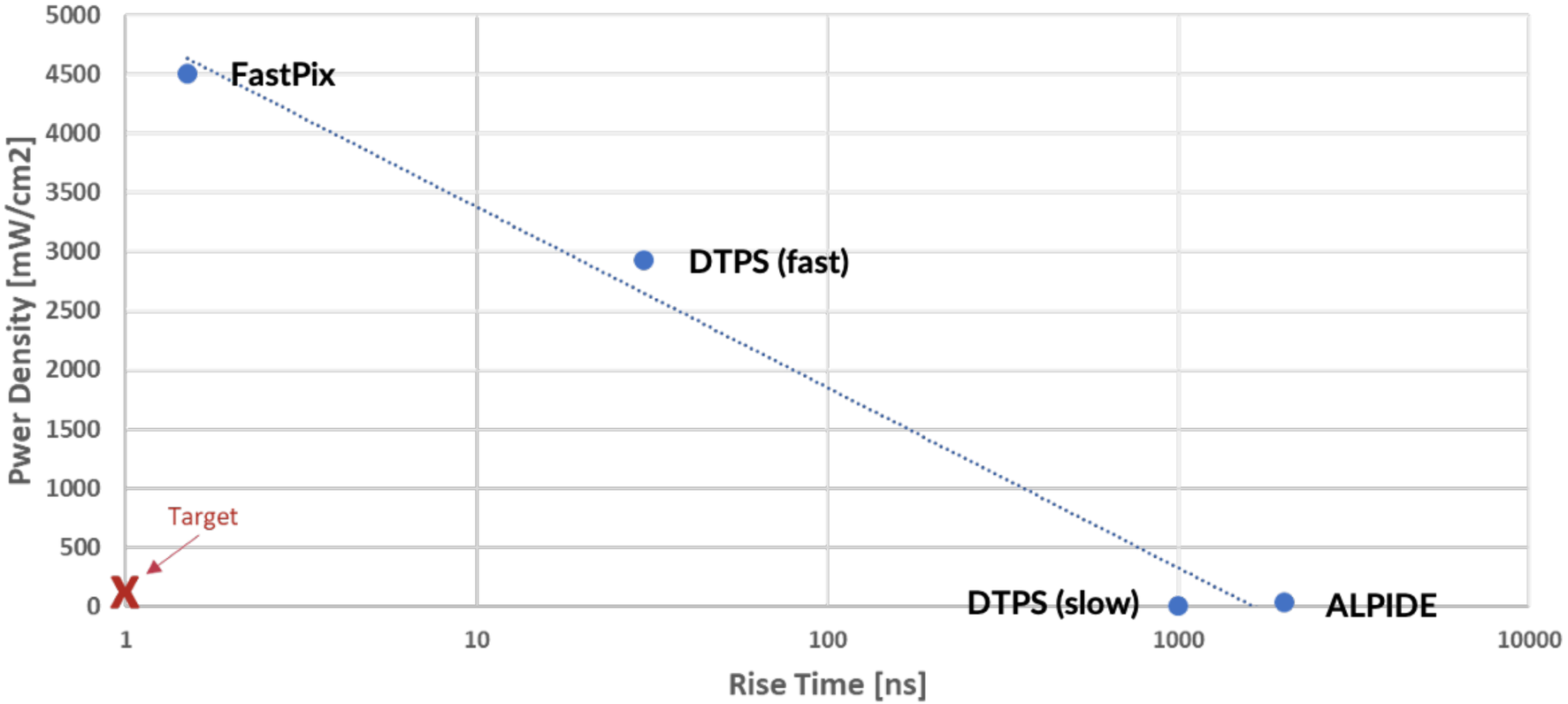
Chip name	Technology	Pixel pitch [μm]	Pixel shape	Time resolution [ns]	Power Density [mW/cm^2]
Target Specification	**?**	**25 x 100**	**Sq / rect**	**1**	**< 20**
ALPIDE [2][3]	Tower 180 nm	28	Square	< 2000	5
FastPix [4][5]	Tower 180 nm	10 - 20	Hexagonal	0.122 – 0.135	>1500
DPTS[6]	Tower 65 nm	15	Square	6.3	53
Cactus [7]	LF 150 nm	1000	Square	0.1-0.5	145
MiniCactus [8]	LF 150 nm	1000	Square	0.088	300
Monolith [9][10]	IHP SiGe 130 nm	100	Hexagonal	0.077 – 0.02	40 - 2700

No design fulfills all target specification → The need to develop a custom design

We decided to go with the Tower 65nm technology, which has been optimized by CERN WP1.2 to have low sensor capacitance allowing very good performance with low power consumption.
+ it has the possibility of a wafer-scale stitched sensor
+ it has been proven to be radiation tolerant

Target Specs vs. State of the Art

JINST 19 (2024) 04, C04033



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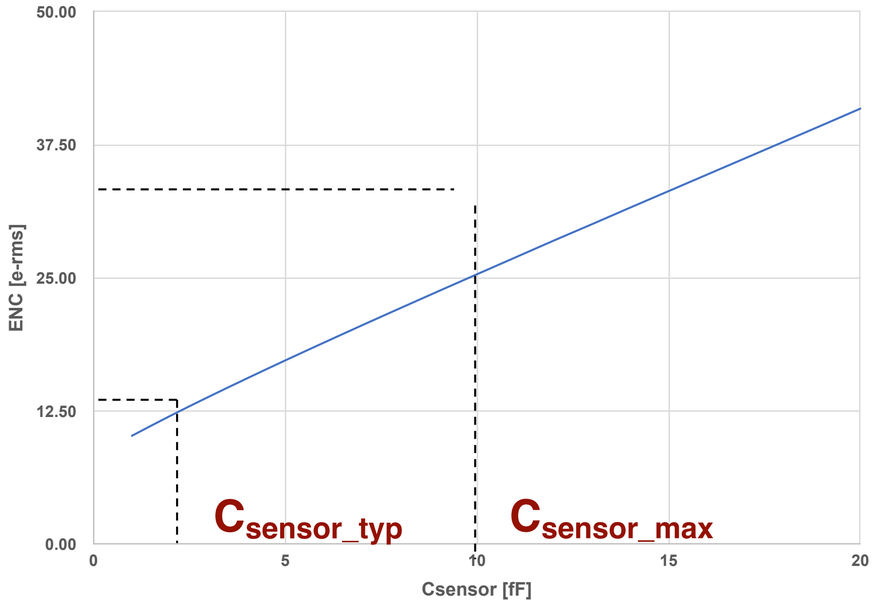
Summary of NAPA-p1 Performance

JINST 19 (2024) 04, C04033

	Specification	Simulated NAPA-p1
Time resolution	1 ns-rms	0.4 ns-rms ✓
Spatial Resolution	7 μm	7 μm ✓
Noise	< 30 e-rms	13 e-rms ✓
Minimum Threshold	200 e-	~ 80 e- ✓
Average Power density	< 20 mW/cm^2	0.1 mW/cm^2 for 1% duty cucle ✓

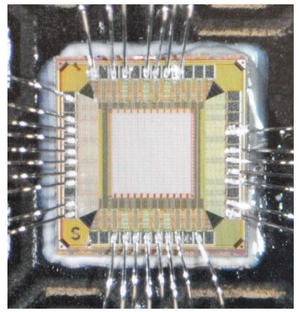
ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF

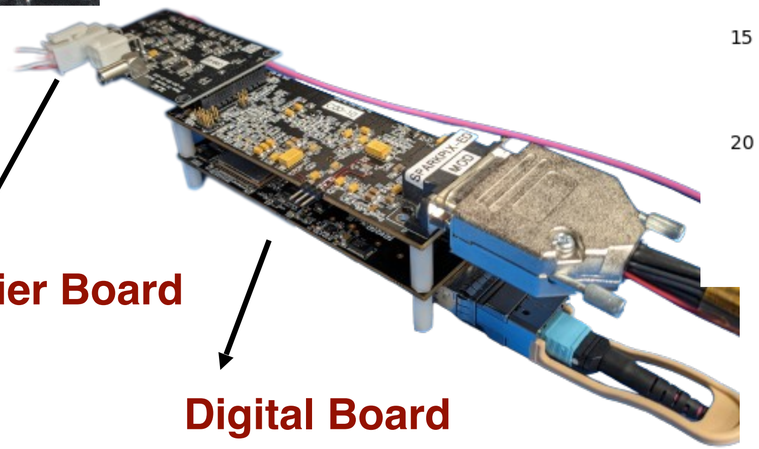


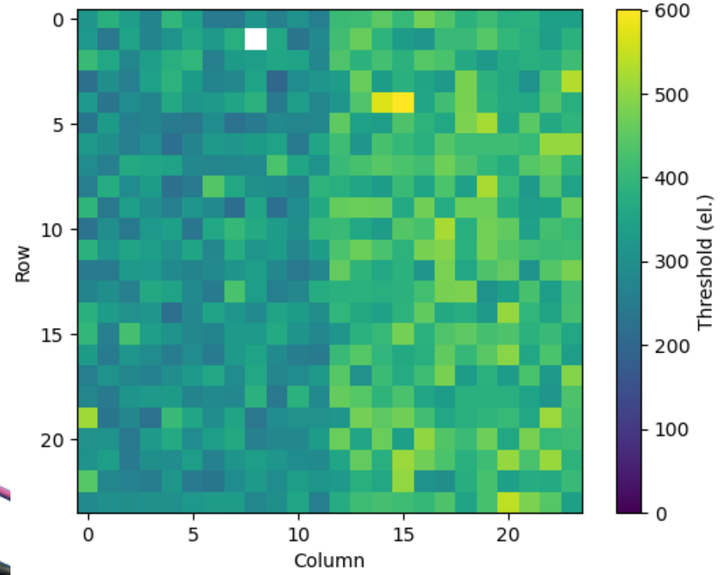
Characterization of NAPA

Chips were received in September 2023

- A custom carrier was designed at SLAC for the NAPA-p1 chip providing all analog references
- The chip was wire-bonded at SLAC
- The carrier boards connects to a digital board containing an FPGA and several DAC's

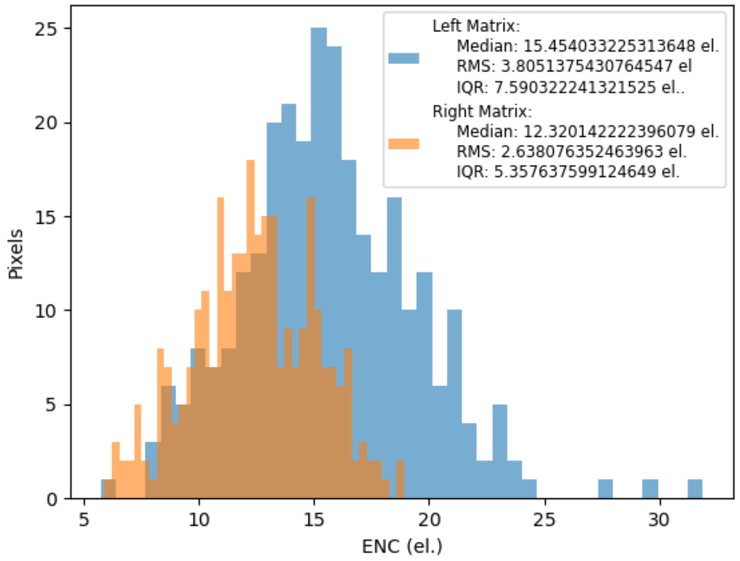






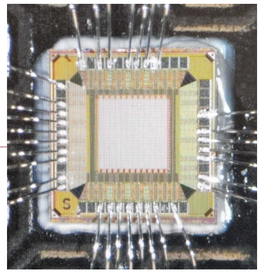
Left Matrix:
Nominal Pixel Variant

Right Matrix:
Pixel Variant with DC leakage current compensation



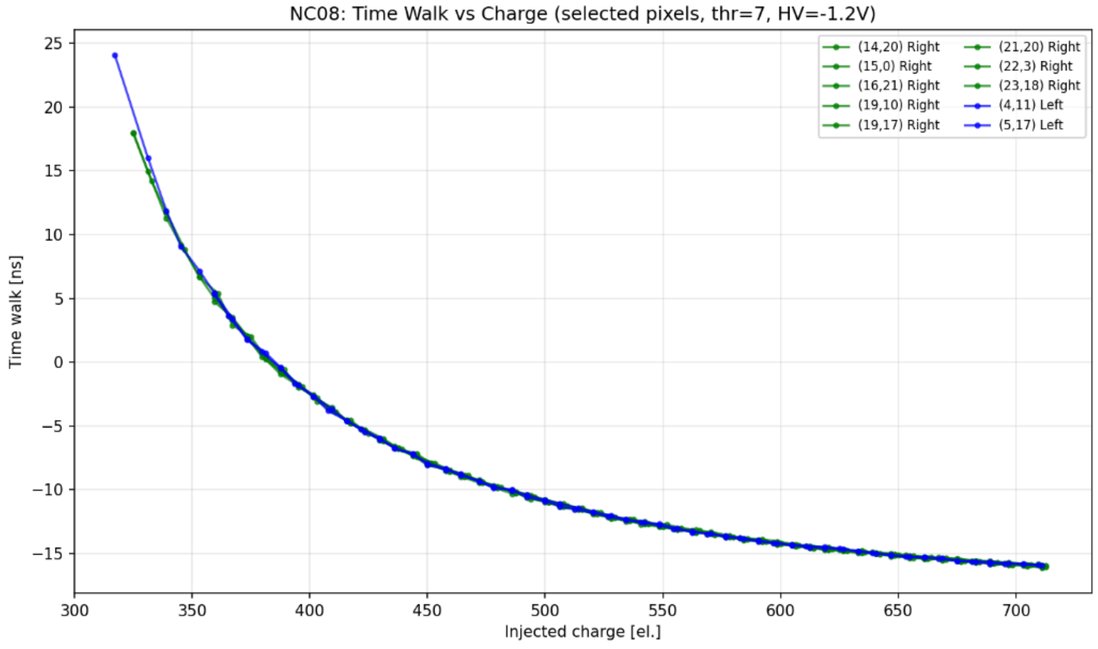
DC leakage current variant has less noise

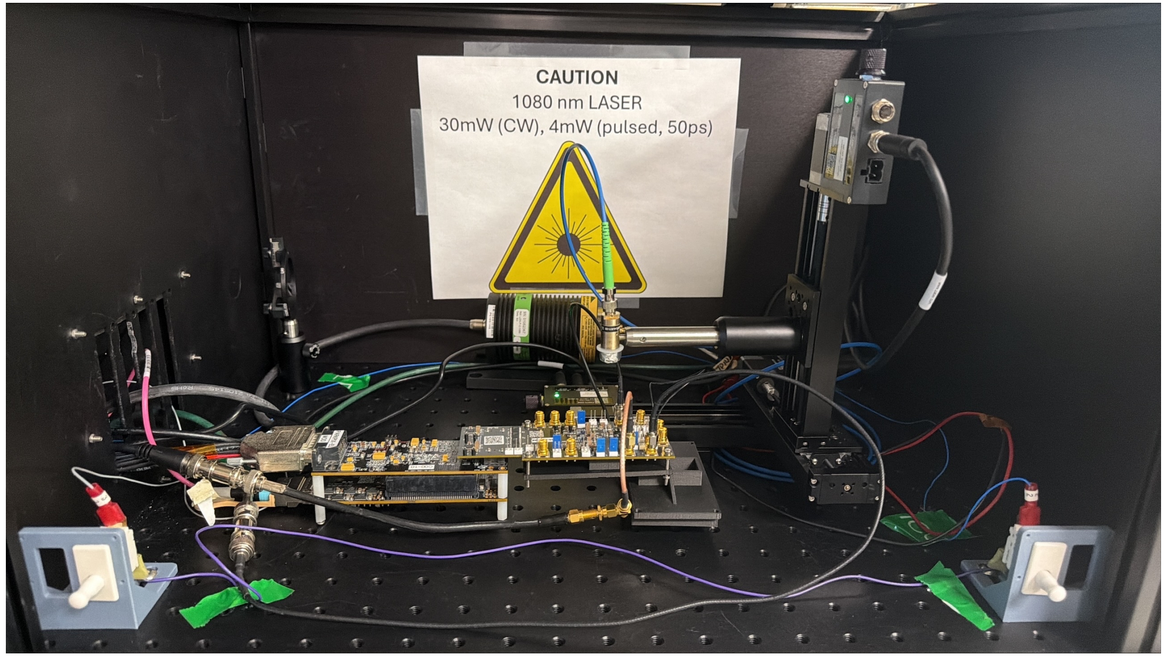
Characterization of NAPA



New carrier board in 2026

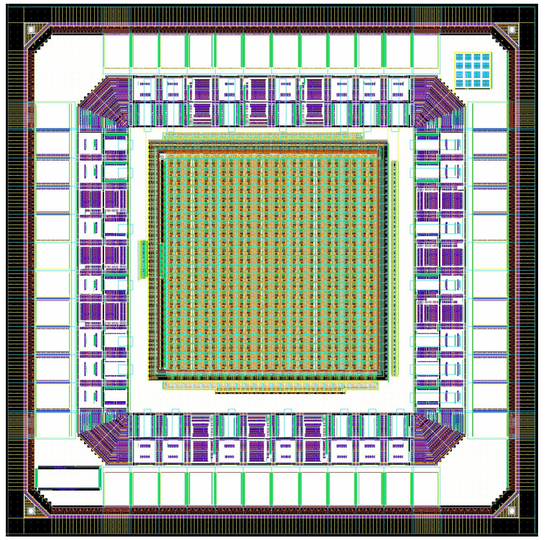
- A custom carrier was designed at SLAC for the NAPA-p2 and back-compatibility with Napa-p1
- Next - perform timing measurement with laser setup.





NAPA p2

- Further improve timing resolution & power trade-off: goal is to achieve x10 improvement over current state-of-the-art
- Exploring system-level timing resolution:
  design of compact, low-power Time-to-Digital Converter (TDC).
  - Integration of TDC into MAPS is particularly challenging due to the tight area, routing and power constraints.
  - The chip contains a novel low-power and small-area Vernier delay line, which is the core building block of a sub-ns TDC, with a programmable time resolution as low as 20ps.
- We have finalized the design of the TDC and we are engaging within DRD7 on how to integrate the TDC into a pixel design as part of Octopus collaboration.

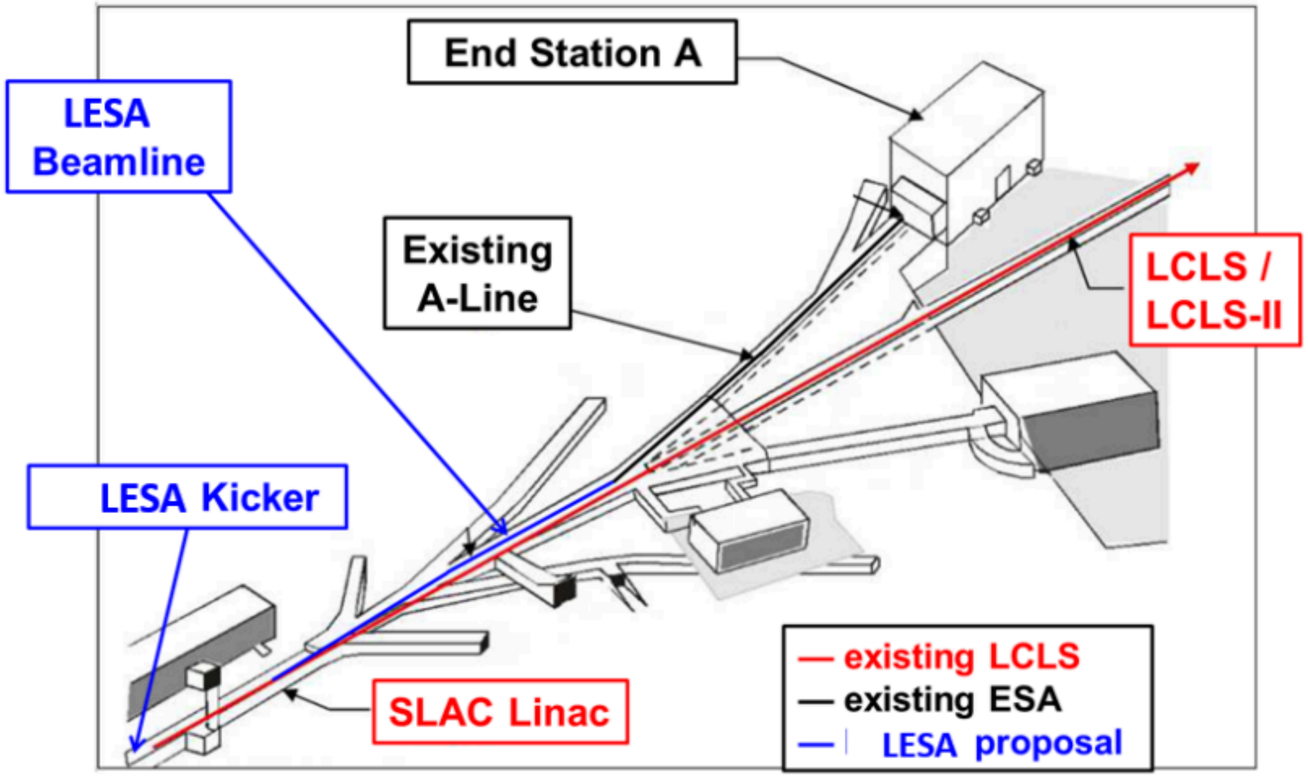


NAPA-p2

Linac to End Station A

High repetition rates, well-timed short bunches, and flexible operating modes makes it advantageous for advanced detector R&D.

Commissioning of beams towards End Station A (ESA) in late 2025, Test beam program could begin in 2027.



LESA Parameters

Electron beam at energy of 8 GeV and various operating scenarios

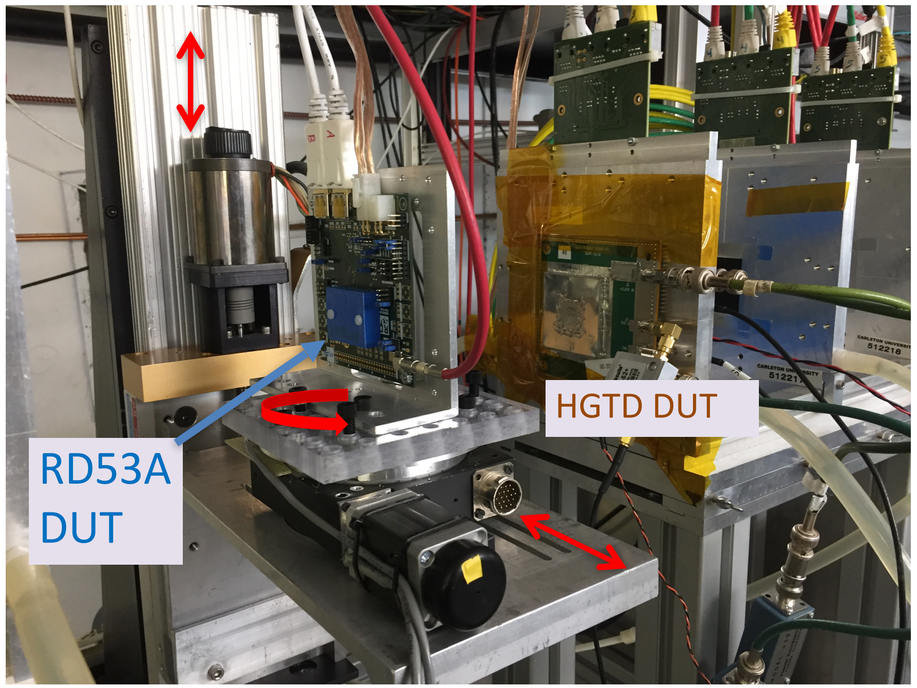
From LCLS-II-HE: Up to 100Hz of primary LCLS-II-HE pulses could be sent into ESA:

1–few electrons per bunch will be available at 2.0-8.0 GeV energies, with a bunch spacing of up to 10 Hz

2028
- X-L laser mode: Possibility to have MHz pulses to LESA for test beams
- LESA laser mode: 37MHz with controlled bunch charge for LDMX
- Dark Current mode

Accelerator Parameters	Interleaved	X-LEAP Laser	LESA Laser	Dark current
SRF Linac Energy	8 GeV	8 GeV	8 GeV	8 GeV
Max Current in LESA	<10 nA	25 nA	25 nA	$<\sim$ 1 pA
Maximum Kicker Rate	100 Hz	929 kHz	929 kHz	929 kHz
# bunches per Kick	1	1	18	100
Avg. Bunch Charge	10-100 pC	>167ke-(27 fC)	>4.2ke-(0.7 fC)	0.07 e-
Bunch spacing	$>$ 10 ms	$>$ 1.08 μs	26.9 ns	5.4 ns
Max beam power	8 - 80 W	200 W	100 W	8 mW

Current setup: Caladium EUDET Telescope + DUT



- **Caladium EUDET telescope** resident at ESTB since Dec/2015,
- Loan from Carleton University, **Thomas Koffas,** supporting/ operating the telescope
- EUDET: 6 planes of CMOS MIMOSA-26 (up to ~10KHz trigger)
- 18.5x18.5µm pixels, X*Y aperture ~2x1 cm and **~3µm spatial resolution.**

- Augmented by remote controlled movers
- Overall XY stage for telescope+DUT
- dedicated DUT XY & rotation stage (new: mounting electrical insulation)

SLAC

https://confluence.slac.stanford.edu/spaces/Atlas/pages/198092343/TestBeam

Thank you!

Beam Format and Detector Design Requirements

arXiv:2003.01116
FCC Mid Term Report

FCC@ZH Bunches 1 μs apart

FCC@Z Bunches 20 ns apart

- Impact of beam-induced background to be mitigated through MDI and detector design
  - Timing resolution of O(ns) can further suppress beam-backgrounds and keep occupancy low
  - O(1-10) ns for beam background rejection and/or trigger decision before reading out the detector
  - Tracking detectors need to achieve good resolution while mitigating power consumption

Beam induced backgrounds at future HF

D. Ntounis (2023)
G. Marchiori (2023)
TDAQ@Annecy2024

Same tools and methodology between ILC & FCC within Key4HEP

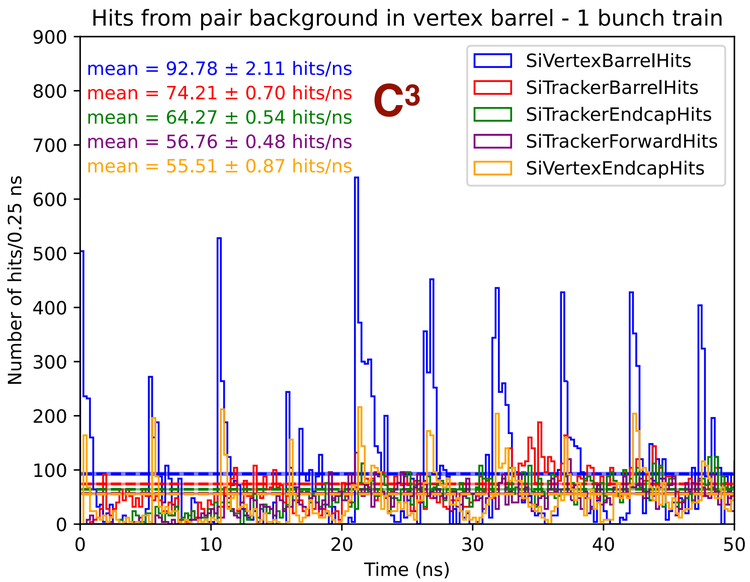
- ILC physics studies are based on full simulation data and some have been recently repeated for C^3
  - Time distribution of hits per unit time and area on 1st layer ~ $4.4 \cdot 10^{-3}$ hits/(ns·mm^2) ≃ 0.03 hits/mm^2 /BX
- CLD detailed studies @FCC show an overall occupancy of 2-3% in the vertex detector at the Z pole

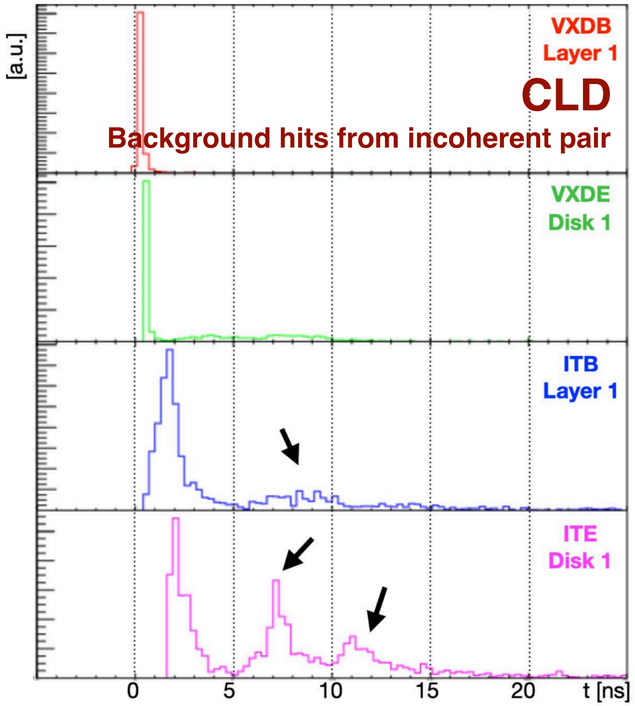
$$occupancy = hits/mm^2/BX \cdot size_{sensor} \cdot size_{cluster} \cdot safety$$

$$size_{sensor} = \frac{25\mu m \times 25\mu m\ (pixel)}{1mm \times 0.05mm\ (strip)} \qquad size_{cluster} = \frac{5\ (pixel)}{2.5\ (strip)} \qquad safety = 3$$

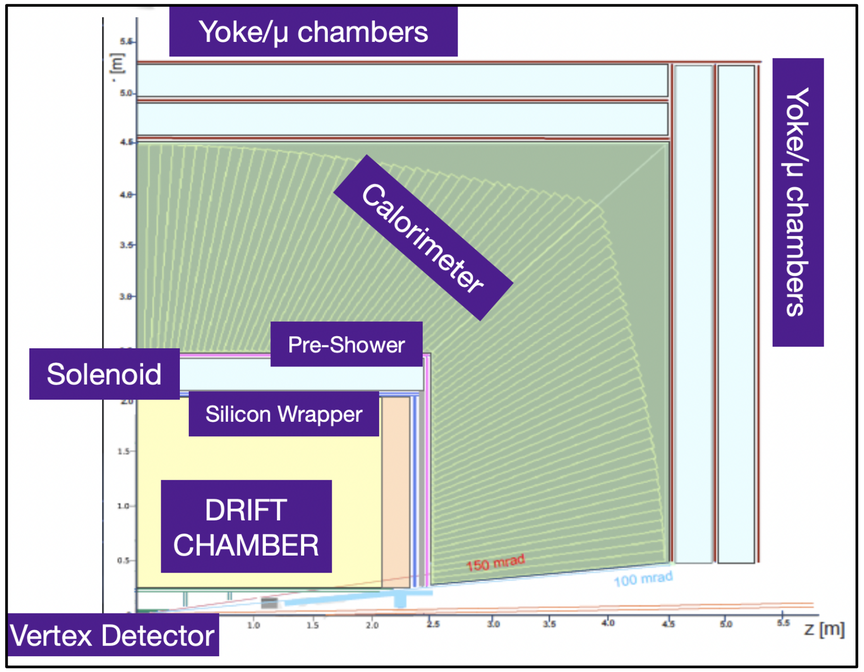
	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

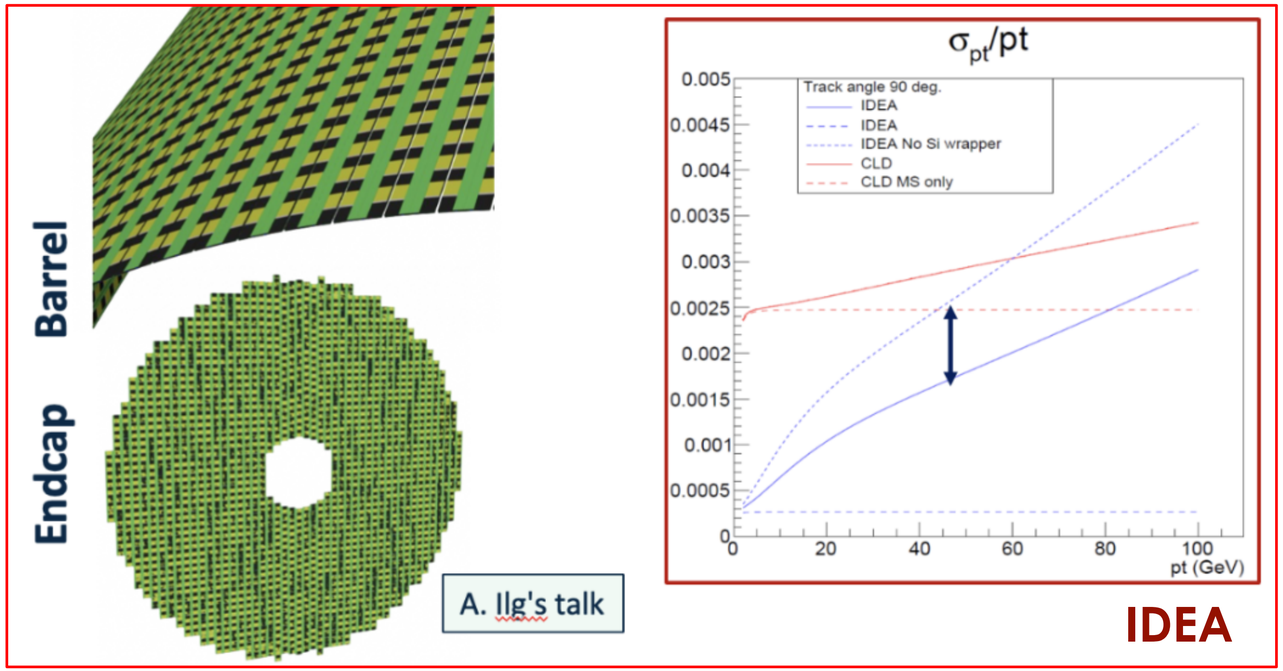
Occupancy in readout window (10μs)





FCC-ee Timing Layers





- **Precision silicon layer around the central tracker**
  - Two barrel and two disks, ~100m^2 of total covered area
  - 10μ*m* hit spatial resolution to Improve track momentum resolution
  - Extend forward coverage of drift chamber
  - **Time of flight for particle identification and long lived particle searches**
- **R&D required:** engineering mechanical design, how many silicon hits, time resolution, pixel/strips, sensors, electronics, vertex t_0, physics performance

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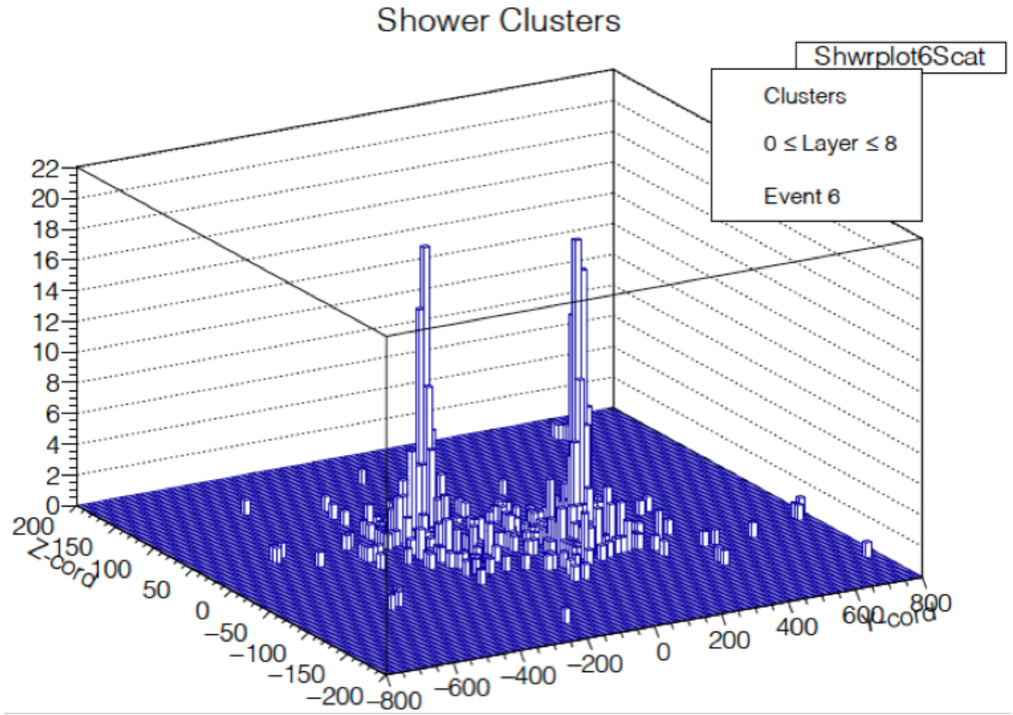
MAPS for ECal

Fine granularity allows for identification of two showers down to the mm scale of separation

- SiD detector configuration with 25x100 μm^2 pixel in the calorimeter at ILC
  - With no degradation of the energy resolution
- ***The design of the digital MAPS applied to the ECal exceeds the physics performance as specified in the ILC TDR***
- The 5T magnetic field degrades the resolution by a few per cent due to the impact on the lower energy electrons and positrons in a shower
- Future planned studies include the reconstruction of showers and π^0 within jets, and their impact on jet energy resolution



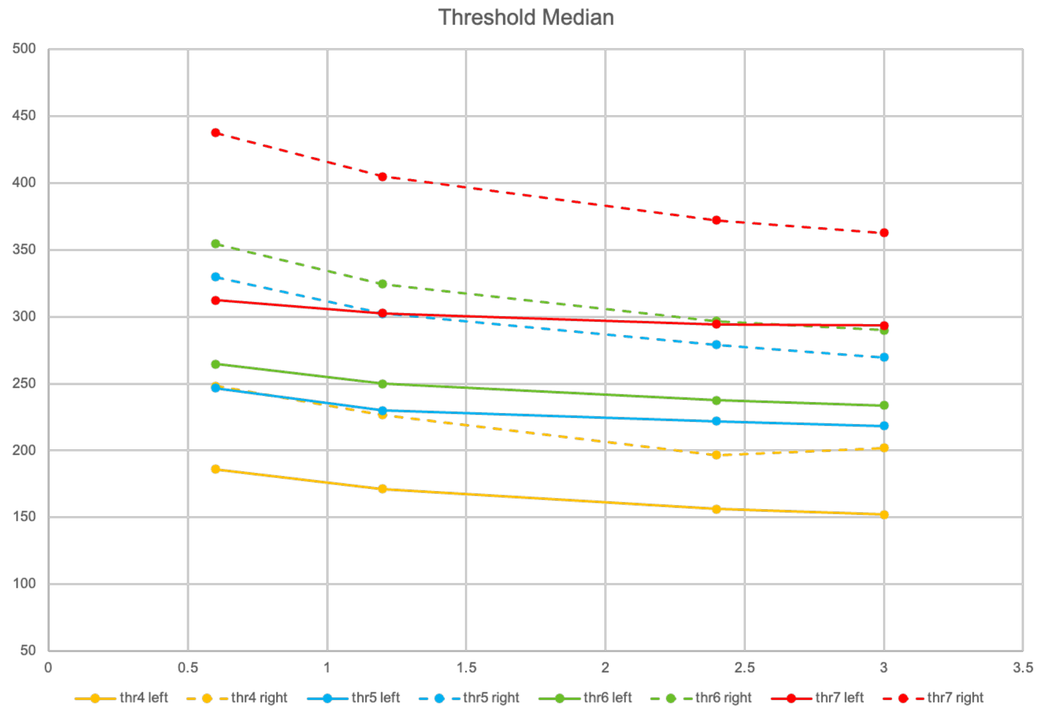
GEANT4 simulations of Transverse distribution of two 10 GeV showers separated by one cm

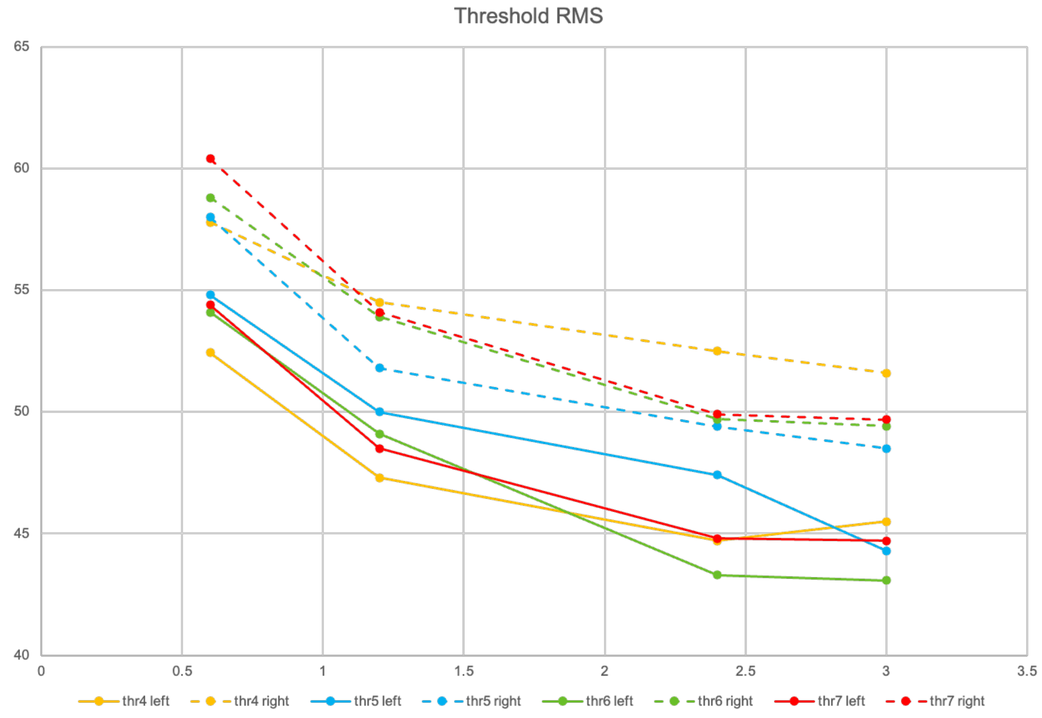
Threshold/ENC as a function of voltage and threshold

Threshold/ENC median and rms decreases with reverse bias.
In particular, left matrix ENC median and rms decrease more dramatically.

Left

Right





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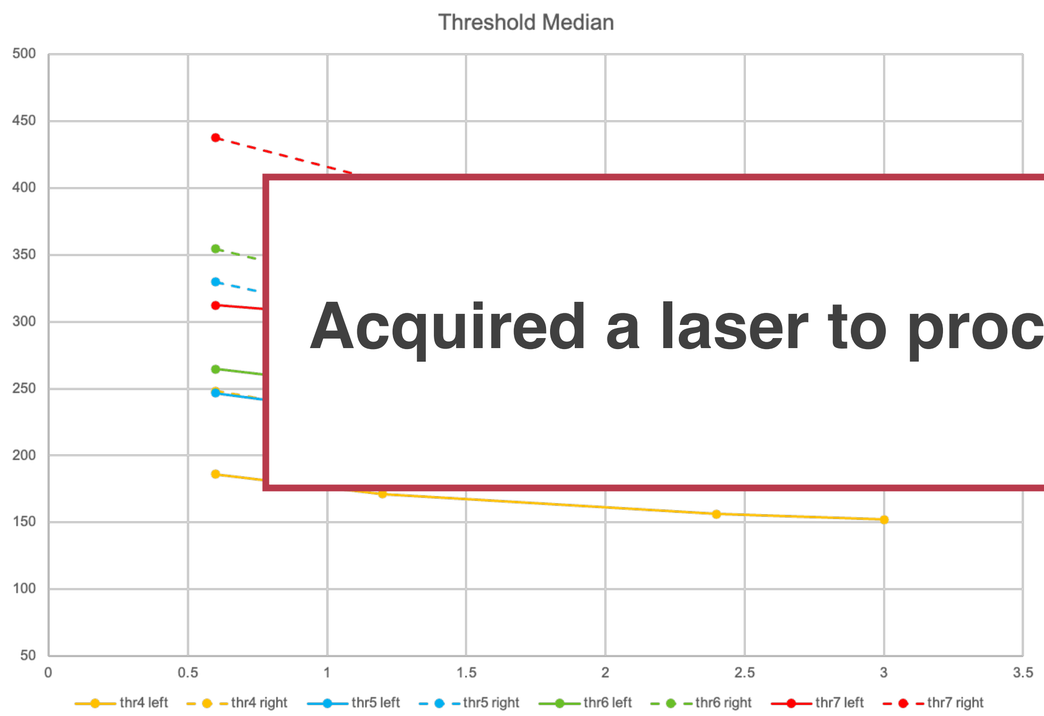
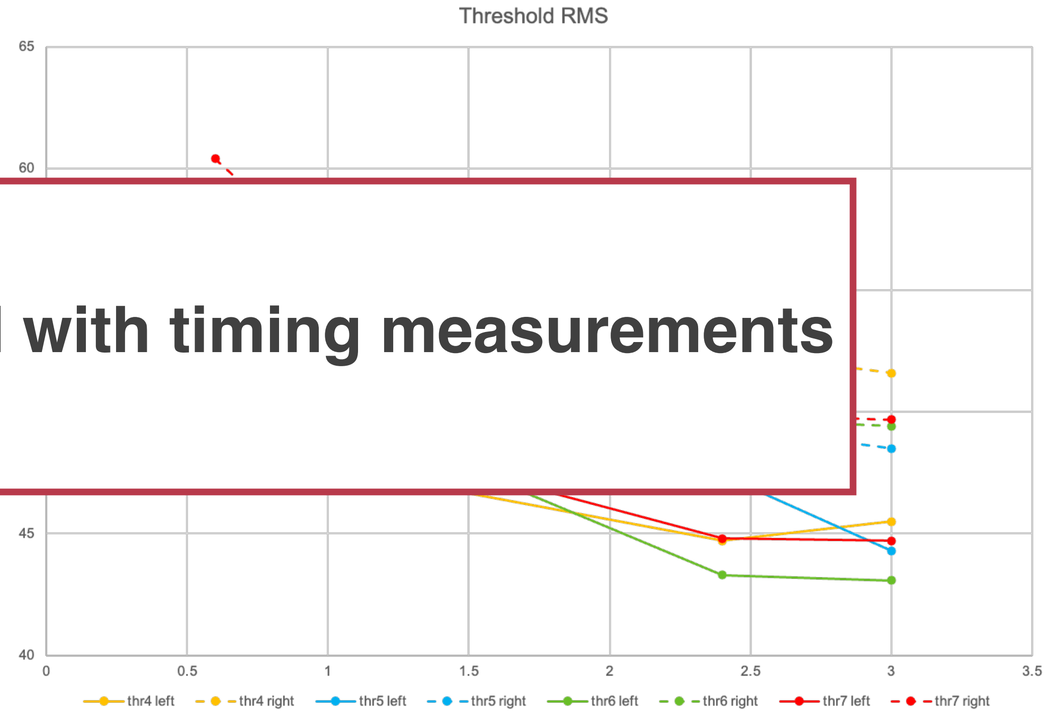


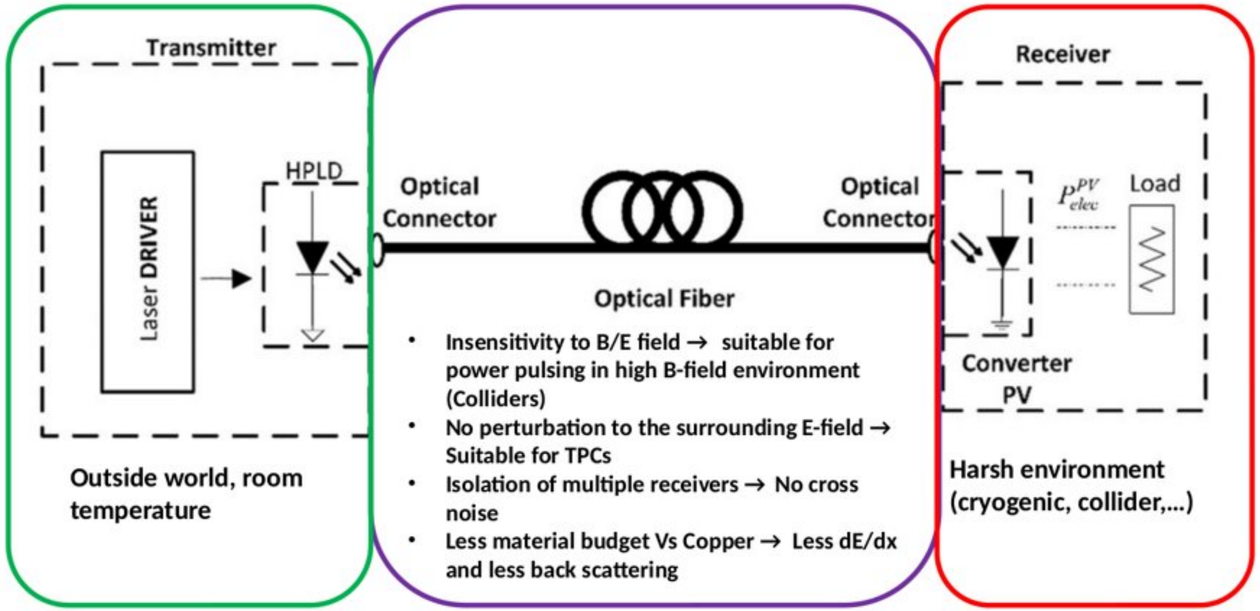


Acquired a laser to proceed with timing measurements

Power over fiber

New effort at SLAC targeting various experimental applications

- Power over Fiber (PoF) offers an innovative solution by delivering power through optical fibers, which are immune to electric and magnetic fields, and boast 1000X lower thermal conductivity compared to coax.
- We are developing radiation-hardened photonic links that can be used in future e+e- collider environments, where radiation levels can exceed 100 krad.
- This approach will investigate advanced photovoltaic materials like perovskites and their potential to surpass current GaAs-based photodiodes in power-to-weight ratio and radiation tolerance.



Enabling technical capabilities at SLAC

Microwave Annealing & Device modeling and simulations

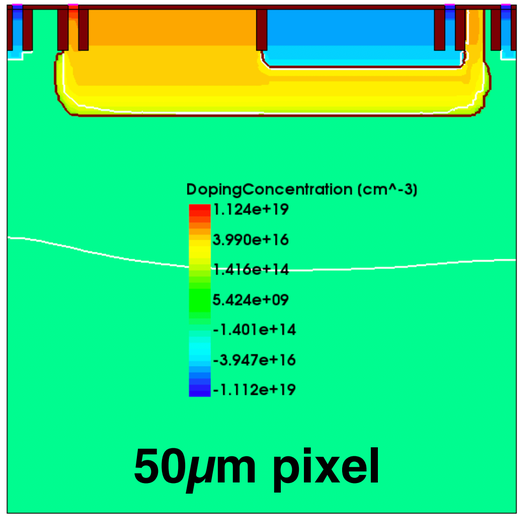
AXOM Microwave Annealing System in SLAC cleanroom

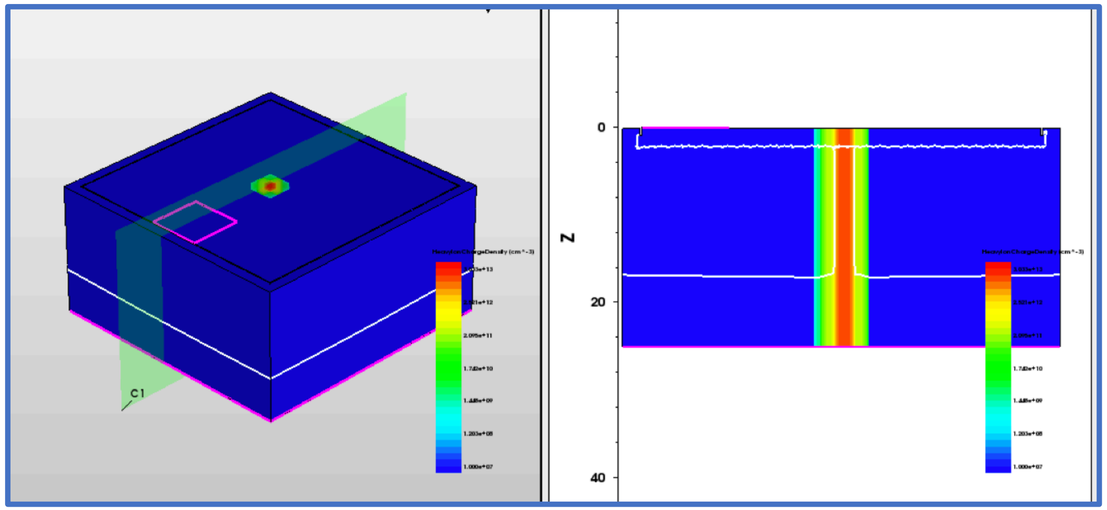
- Optimization of material to obtain desired properties (semiconductors, ceramics, polymers) often requires annealing (heat)
  - Heat may change, damage or destroy other elements of a structure
  - Heating materials is energy intensive process
- Microwave annealing (MWA) is a non-equilibrium annealing technique which selectively transfers energy to defects, dopants, interfaces or impurities
  - Tool facilitates development of novel device structures for sensors, ASICs
  - SLAC has developed several HEP applications using microwave annealing
  - MWA is compatible with CMOS processing, allowing advanced integration
- Experience in Device modeling and simulations
  - TCAD full characterization of new processes

MAPS on novel CMOS technologies

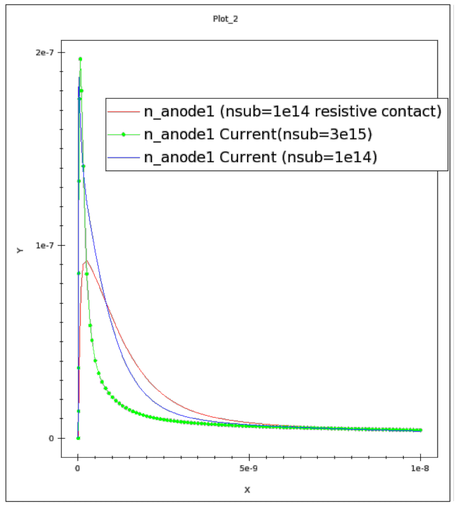
Blue-sky R&D on CMOS 22nm FDSOI

- Fully-Depleted Silicon-On-Insulator process enables implementation of sensor in substrate
- Promising CMOS process with excellent mixed-signal performance
- TCAD simulations and initial pixel design to evaluate key performance parameters:
  - Detector capacitance
  - Charge collection time
  - Cross-talk





3D Charge collection simulations (MIP)

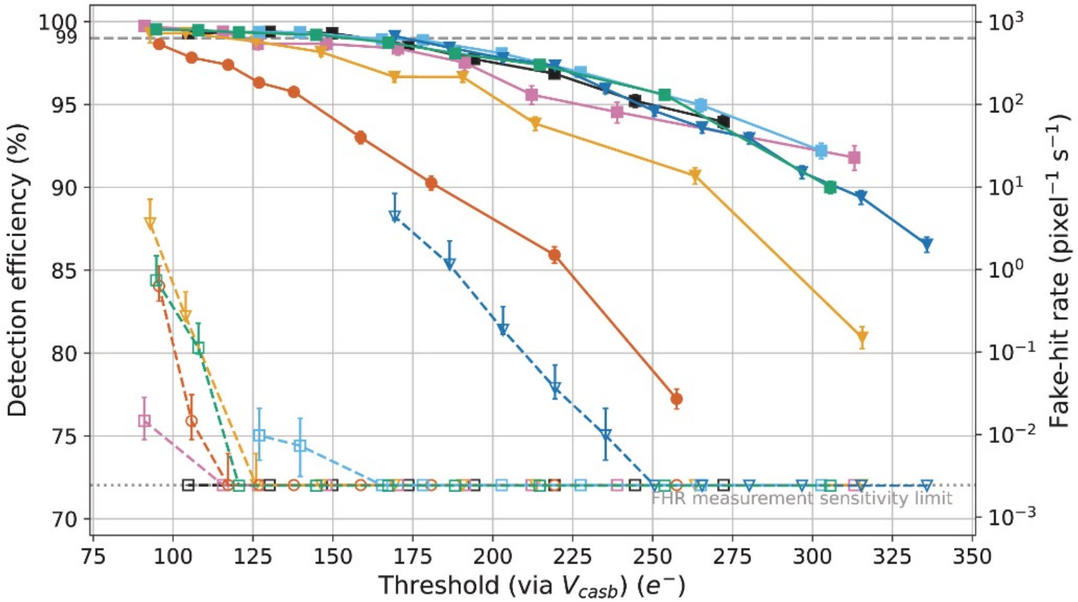


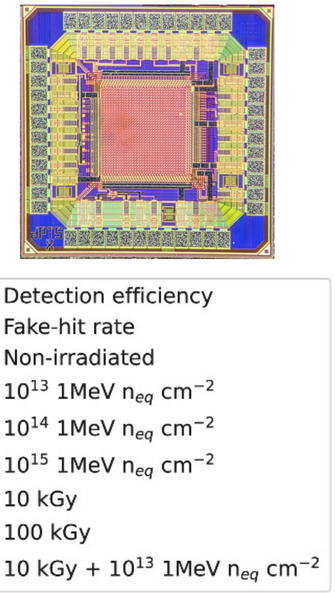
Read-out current: compare three process options

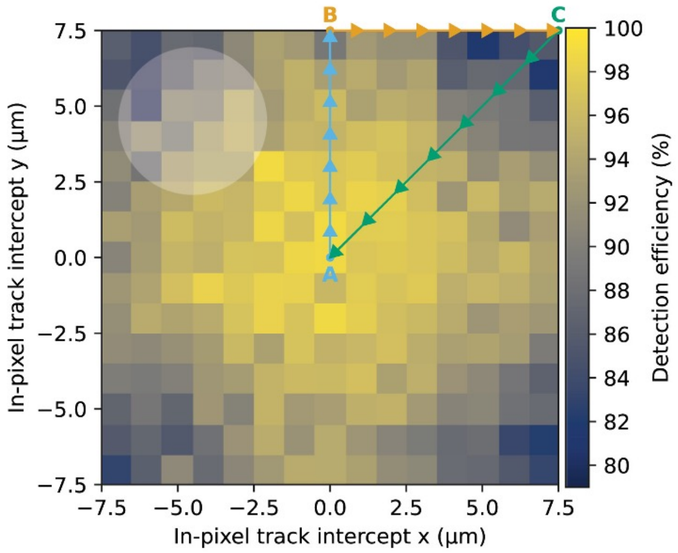
Recent results with Digital Pixel Test Structures

Synergies with DPTS characterization at CERN test beam facility within ALICE Collaboration

Characterization done up to 10^{15} 1 MeV n_{eq} cm^{-2}







Digital pixel test structures implemented in a 65 nm CMOS process
A Compact Front-End Circuit for a Monolithic Sensor in a 65-nm CMOS Imaging Technology

Current status of beam-background studies

D. Ntounis (2023)
G. Marchiori (2023)
TDAQ@Annecy2024

Similar tools and methodology between ILC & FCC within Key4HEP

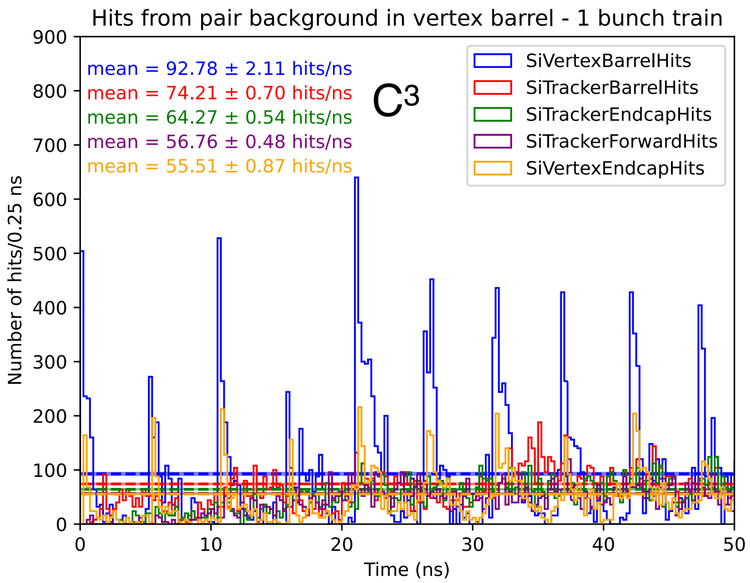
- ILC physics studies are based on full simulation data and some have been recently repeated for C³
  - Time distribution of hits per unit time and area on 1st layer ~ $4.4 \cdot 10^{-3}$ hits/(ns·mm²) ≃ 0.03 hits/mm² /BX
- CLD detailed studies @FCC show an overall occupancy of 2-3% in the vertex detector at the Z pole
  - assuming 10μs integration time

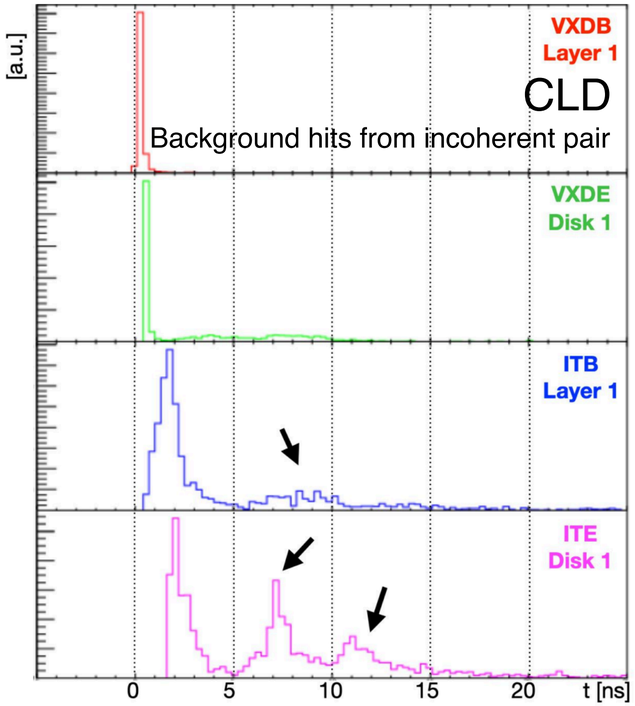
$$occupancy = hits/mm^2/BX \cdot size_{sensor} \cdot size_{cluster} \cdot safety$$

$$size_{sensor} = \frac{25\mu m \times 25\mu m\ (pixel)}{1mm \times 0.05mm\ (strip)} \qquad size_{cluster} = \frac{5\ (pixel)}{2.5\ (strip)} \qquad safety = 3$$

	Z	WW	ZH	Top
Bunch spacing [ns]	30	345	1225	7598
Max VXD occ. 1us	2.33e-3	0.81e-3	0.047e-3	0.18e-3
Max VXD occ.10us	23.3e-3	8.12e-3	3.34e-3	1.51e-3
Max TRK occ. 1us	3.66e-3	0.43e-3	0.12e-3	0.13e-3
Max TRK occ.10us	36.6e-3	4.35e-3	1.88e-3	0.38e-6

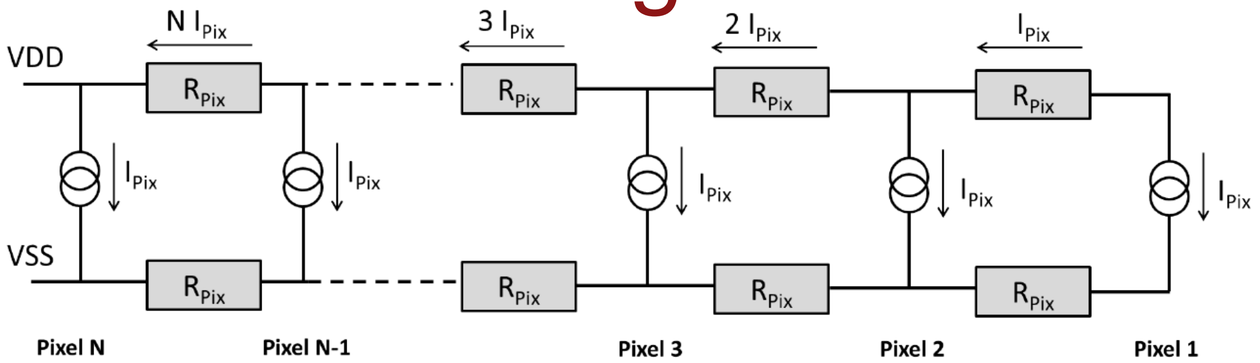
Occupancy in readout window (10μs)





Going Towards a Large Sensor → Challenge

$$\Delta V = I_{pix} \times R_{Pix} + 2 \times I_{Pix} \times R_{Pix} + 3 I_{Pix} \times R_{Pix} + ... + N \times I_{Pix} \times R_{Pix}$$
$$\Delta V = I_{Pix} \times R_{Pix}(1 + 2 + 3 + ... + N)$$
$$\Delta V = I_{Pix} \times R_{Pix} \times \frac{N(N+1)}{2}$$



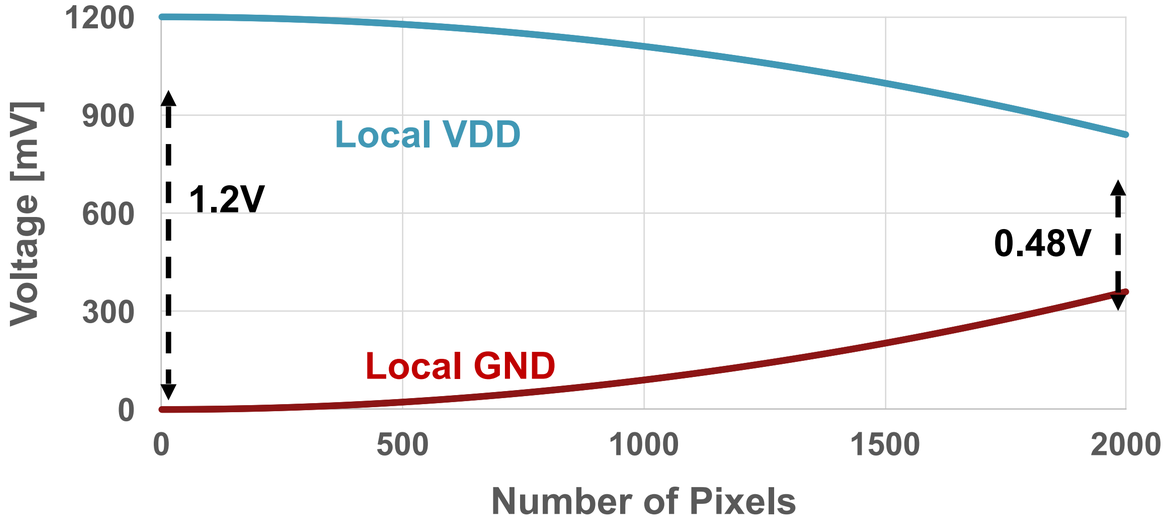
Assuming :I_{pix} = 600 nA and R_{pix} = 300 mΩ

Assuming pixel of 25 μm x 25 μm

A column of 10 cm would have 4000 pixels

Double sided powering

→ max drop length = 2000 pixels

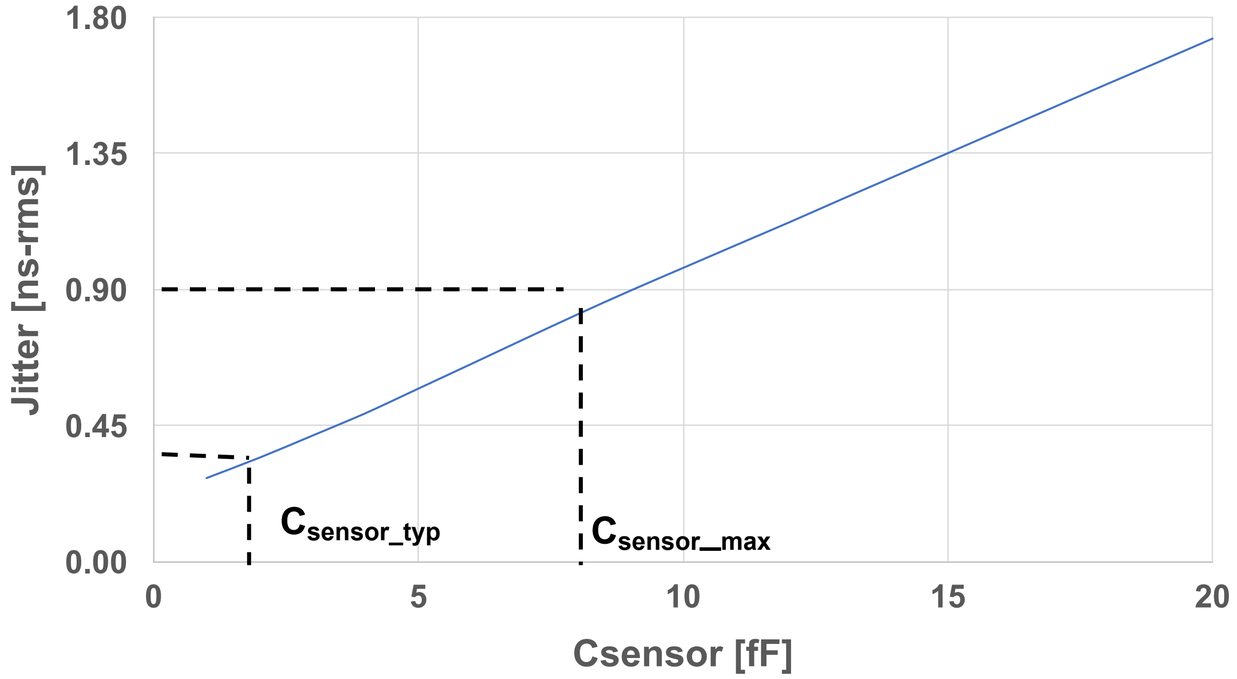


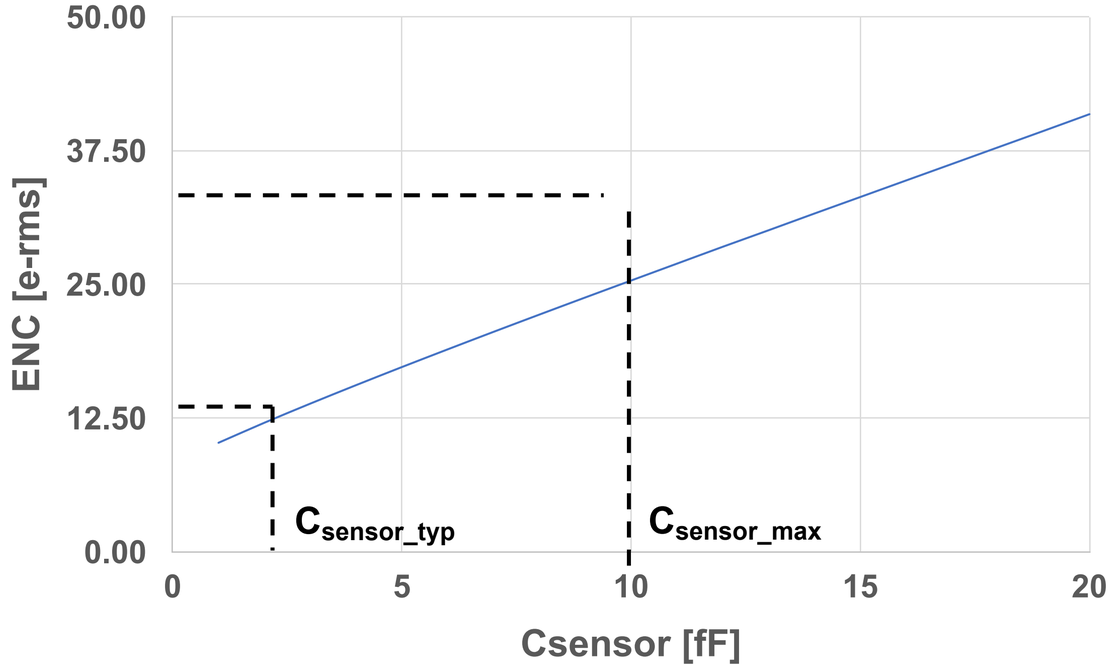
VDD-GND goes from 1.2 V near the power pads down to around 480 mV after 2000 pixels

The main limitation comes from large scale power distribution rather than cooling constraints

After 10^3 pixels (reticle, 2.5 cm), $V_{drop} \approx 0.1$ V
After 4 x 10^3 pixels (sensor, 10cm), V_{drop} = 1.5V !

Simulation of Jitter and ENC as a Function of C_{sensor}



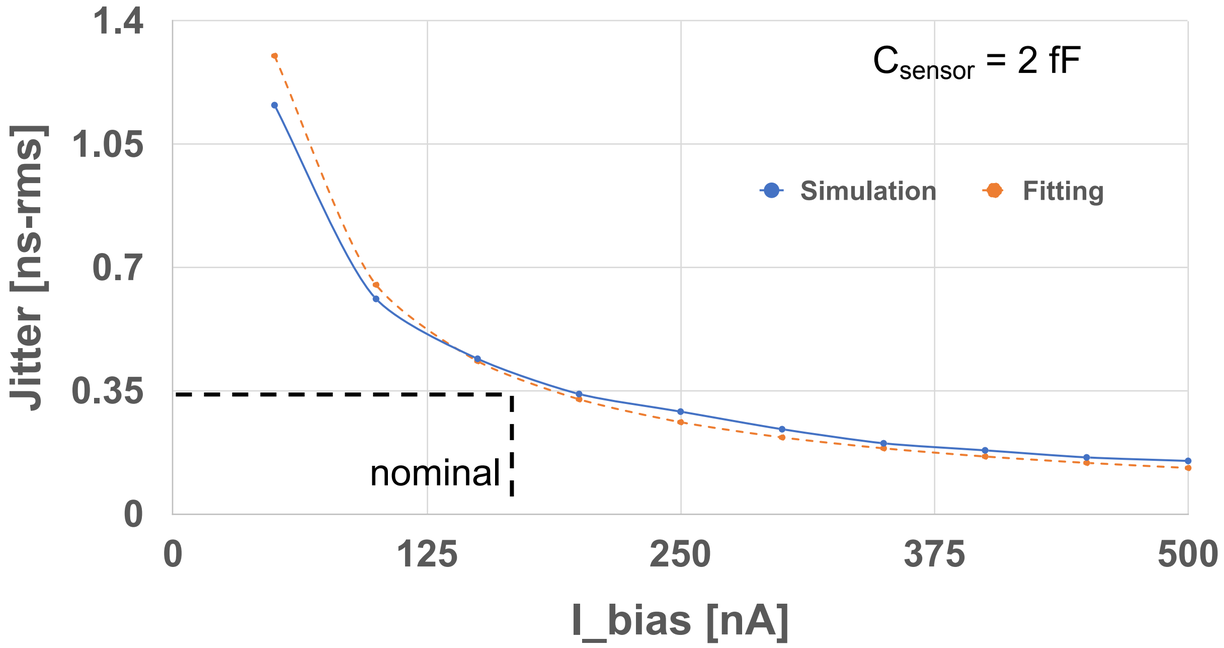


jitter = 400 ps for $C_{sensor\_typ} \approx 2$ fF → **Ok for Specs** ← **ENC = 13 e-rms for $C_{sensor\_typ} \approx 2$ fF**

These simulations are with a nominal pixel current of 600 nA → <Power density> = 115 mW/cm² x duty cycle
For e+e- machines such as ILC and C³, duty cycle is expected < 1%

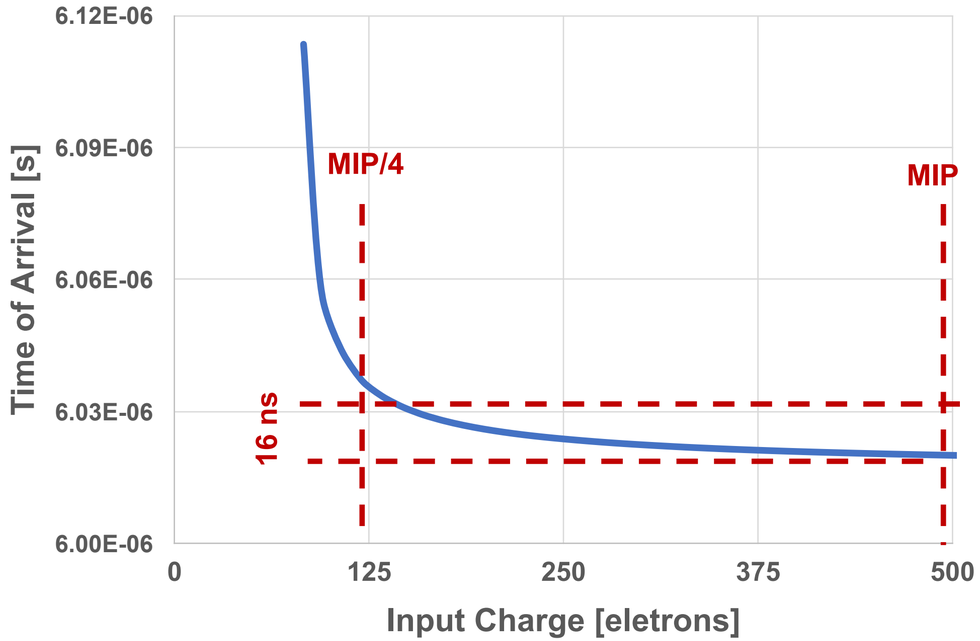
Simulation Results : Jitter and Time Walk

Jitter



I_bias = 200 nA ≡ pixel current = 600 nA
From theory we expect : $\sigma_{FE} \propto \frac{1}{(\mathrm{Power})^{\frac{1}{n}}}$ with $1 \leq n \leq 2$

Time Walk



Time walk for MIP → MIP/4 = 16 ns
Not negligible and must be corrected
(in pixel? In balcony? Offline? TBD)