Fermilab

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Tracking R&D at FNAL

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US Tracking Meeting BNL

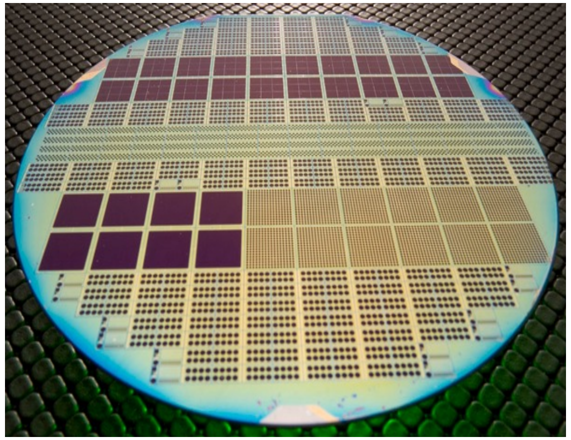
U.S. DEPARTMENT of ENERGY

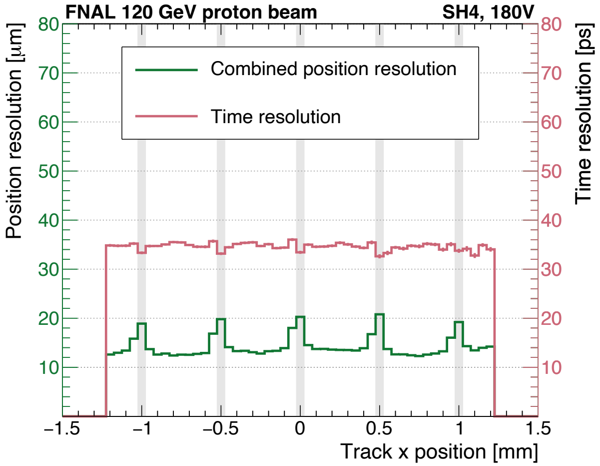
Fermi National Accelerator Laboratory is managed by FermiForward for the U.S. Department of Energy Office of Science

FERMI NATIONAL ACCELERATOR LABORATORY

Introduction

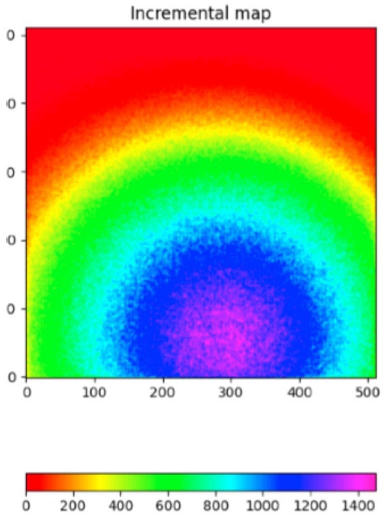
- Build on technologies developed at the for Tevatron, LHC, HL-LHC, EIC, and others
  - Unique resources of strong instrumentation groups
  - Expertise in physics simulations and tracking reconstruction
- Actively engaged in R&D on tracking detectors for FCC-ee
  - Sensor design, simulation studies, collaborations with vendors
  - Collaborative efforts with US and international universities

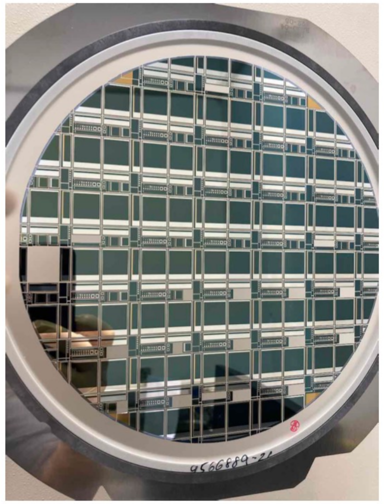


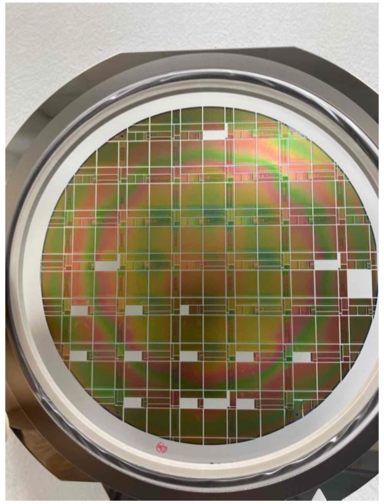


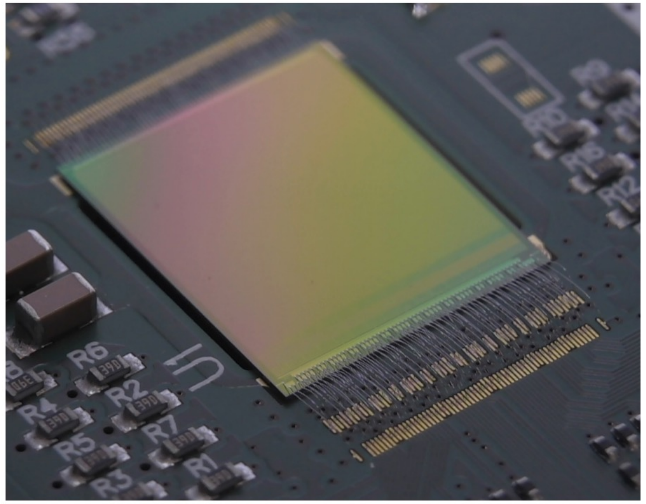
ARCADIA MAPS with LF110

- Sensor design and fabrication platform on LF11is technology
  - Developed for Future Lepton Colliders and Space Instruments
- Technology demonstrators
  - Main demonstrator (512 x 512 pixels) 25x25 µm^2 pixels
  - Several other demonstrators produced: pixel and strip test structures down to 10 μm pitch, small-scale demonstrator for fast timing, etc





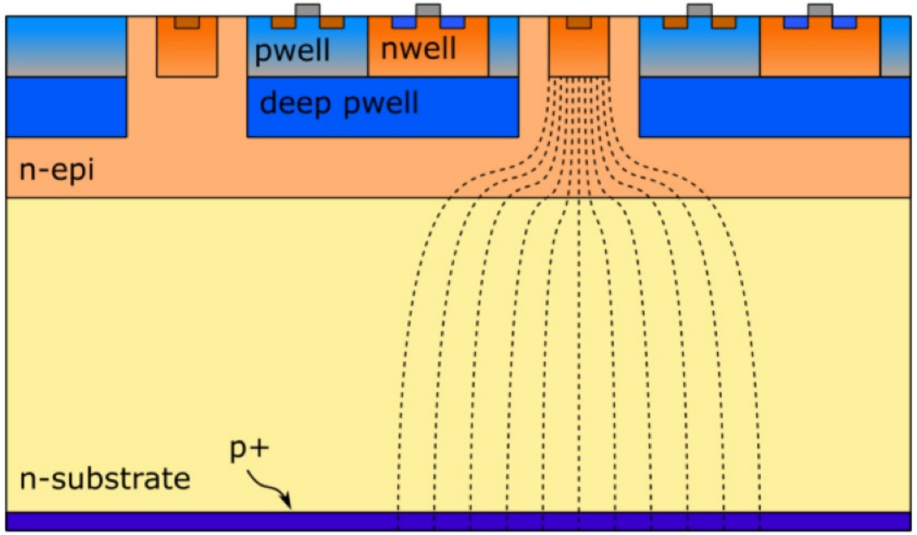




ARCADIA MAPS with LF110

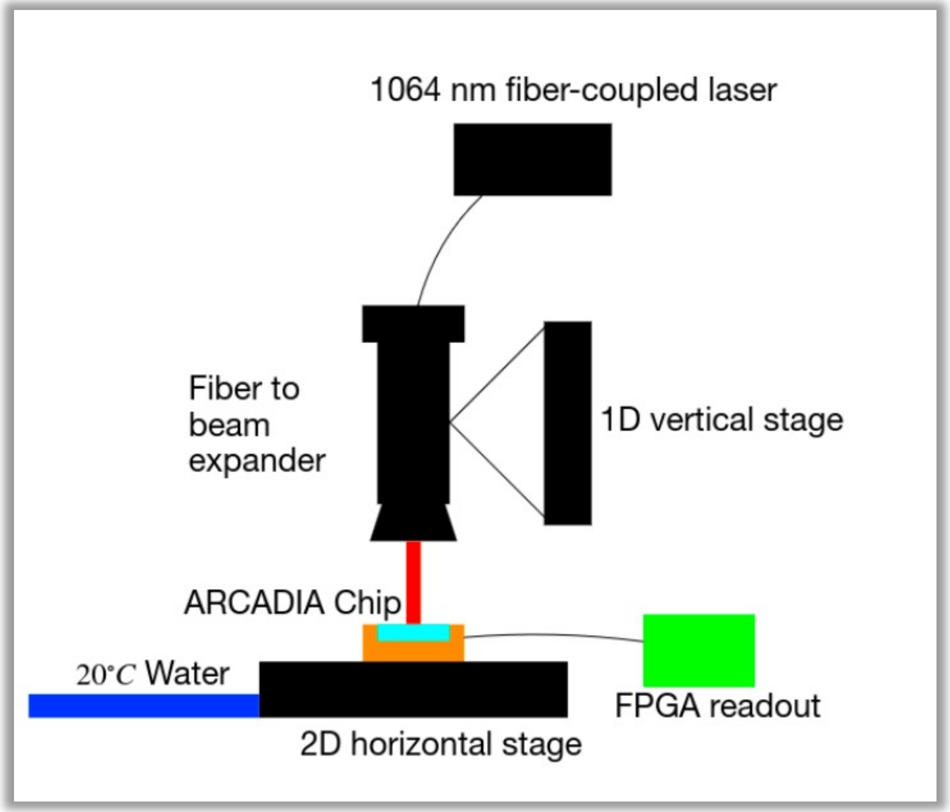
M. Rolo, VERTEX2023, https://agenda.infn.it/event/35597/contributions/211639/
L. Pancheri et al, 2019 JINST 14 C06016, DOI: 10.1088/1748-0221/14/06/C06016

- Sensor
  - n-type high resistivity active region (up to 500 μm)
  - backside p+ implantation: depletion from back to top
- Scalable readout architecture with ultra-low power capability O(10 mW/cm^2)
- Full chip demonstrator MD3
  - Pixel array 512×512 pixels, pitch 25 μm
  - Data-driven binary readout
  - Power consumption < 30 mW/cm^2 (down to 10 mW/cm^2 in low-rate mode)



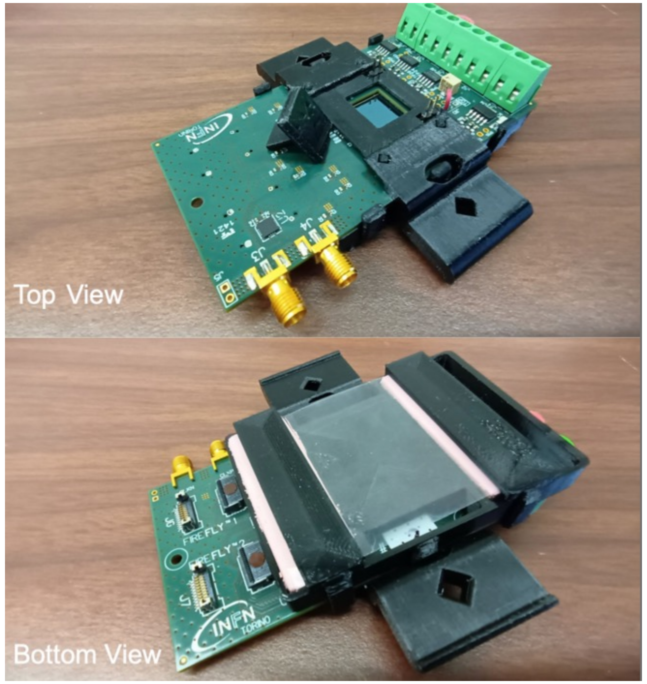
Measurements in the lab in HEERC

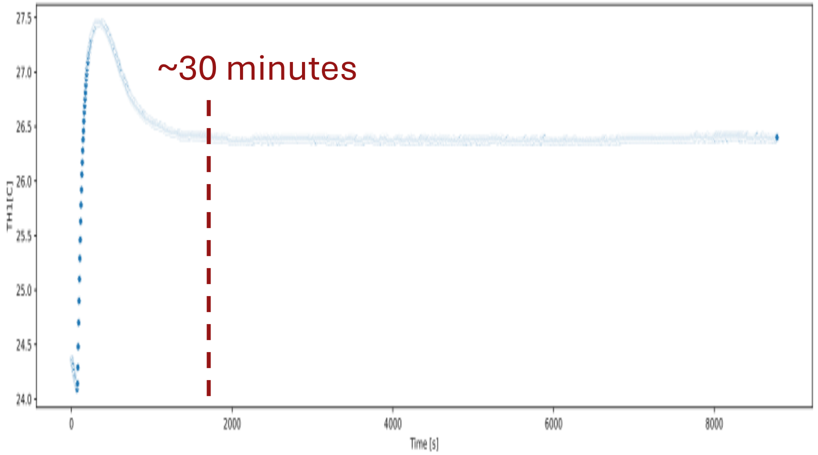
- Testing done in the new Precision Instrumentation and Timing (PIT) Lab at the Helen Edwards Engineering Center at Fermilab
  - Published in JINST 21 (***2026***) P04003



Measurements in the lab

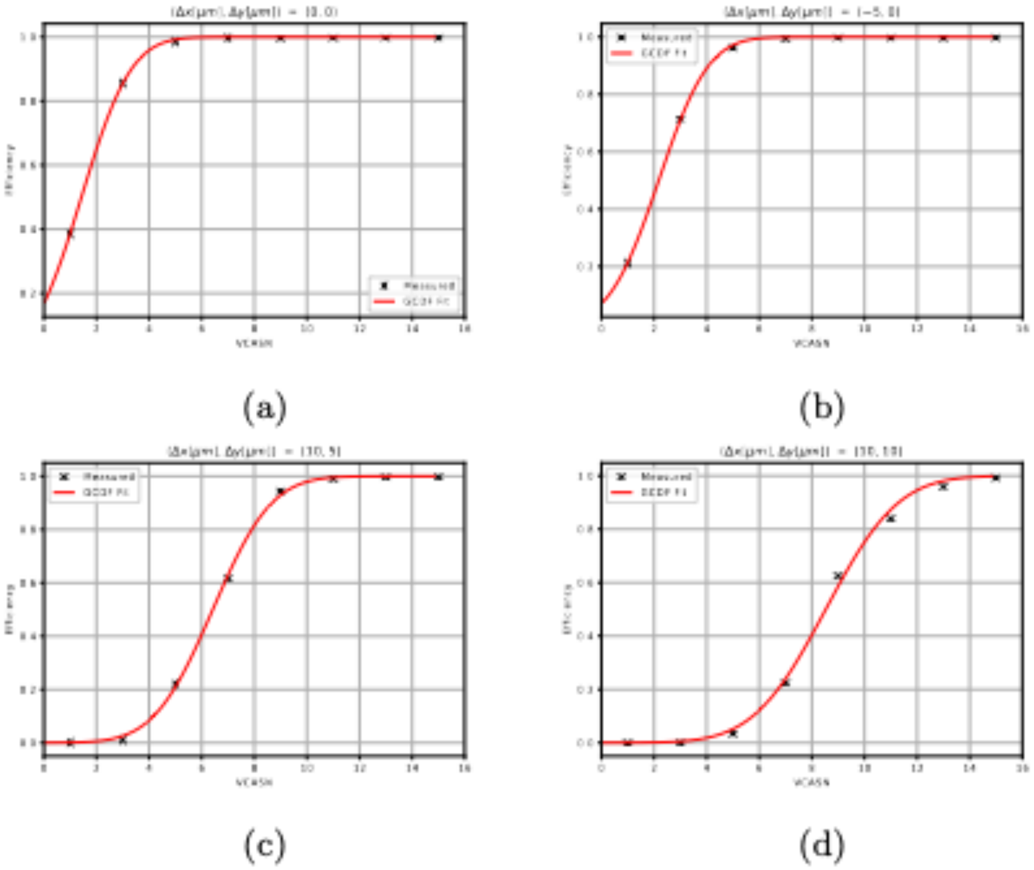
- Laser calibration:
  - Tune the intensity to reproduce a MIP signal
    - Use beta-source and cosmic muons for calibration
  - Achieve beam-spot around 10 µm FWHM
    - Edge scanning and dedicated CCD camera
  - Calibrate the laser power to monitor for output power changes : fiber split for monitoring
- Automatized control of motion stages to perform µm scans
  - Calibrate stage movement to account for rotations when moving in 2D directions
  - Temperature control: measurements performed at room temperature





Measurements in the lab

- An area of 6×10 pixels used to characterize cluster efficiency
  - Step size of 5µm is used across the scanning area
  - Total 25 scans per pixel.
  - Vary VCASN from 1 to 11, with steps of 2 to measure the efficiency.



Results of S-curve fits on scan points within pixel (0,0)

Measurements in the lab

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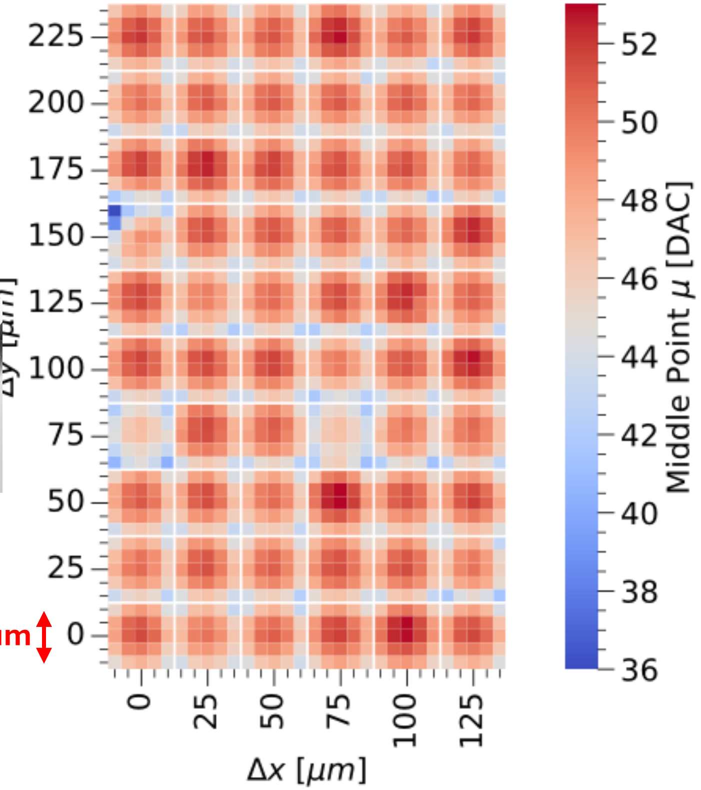
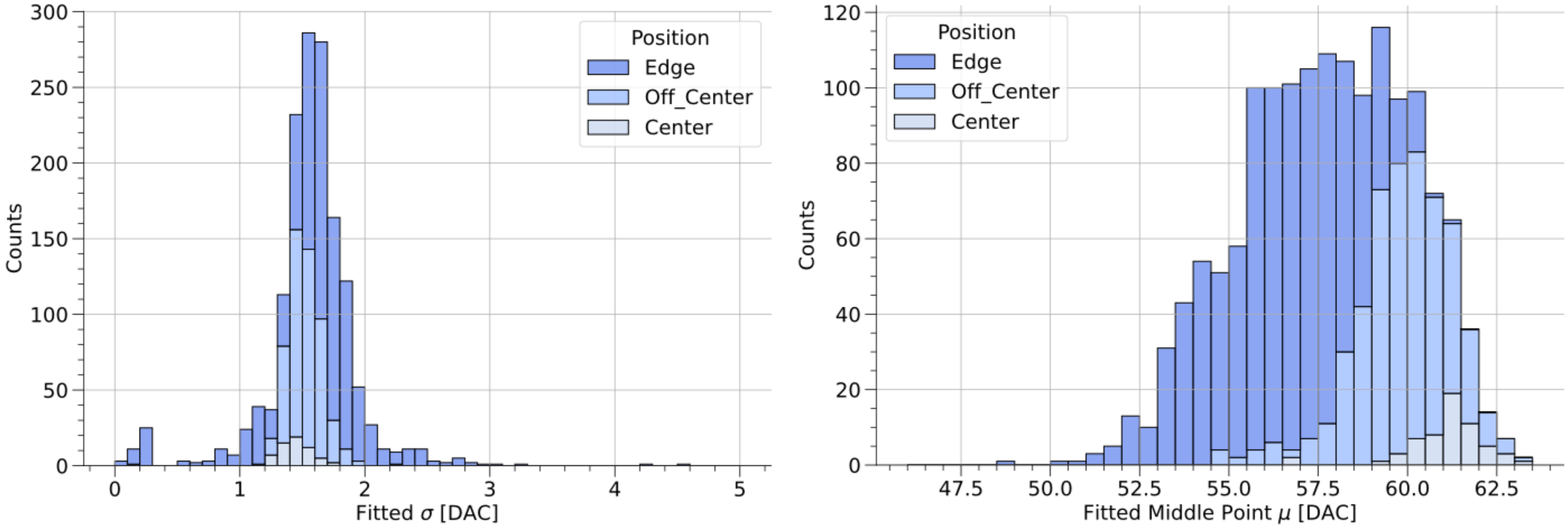


25 µm

- Due to charge sharing, the value of µ is lower at pixel edges and higher at the center

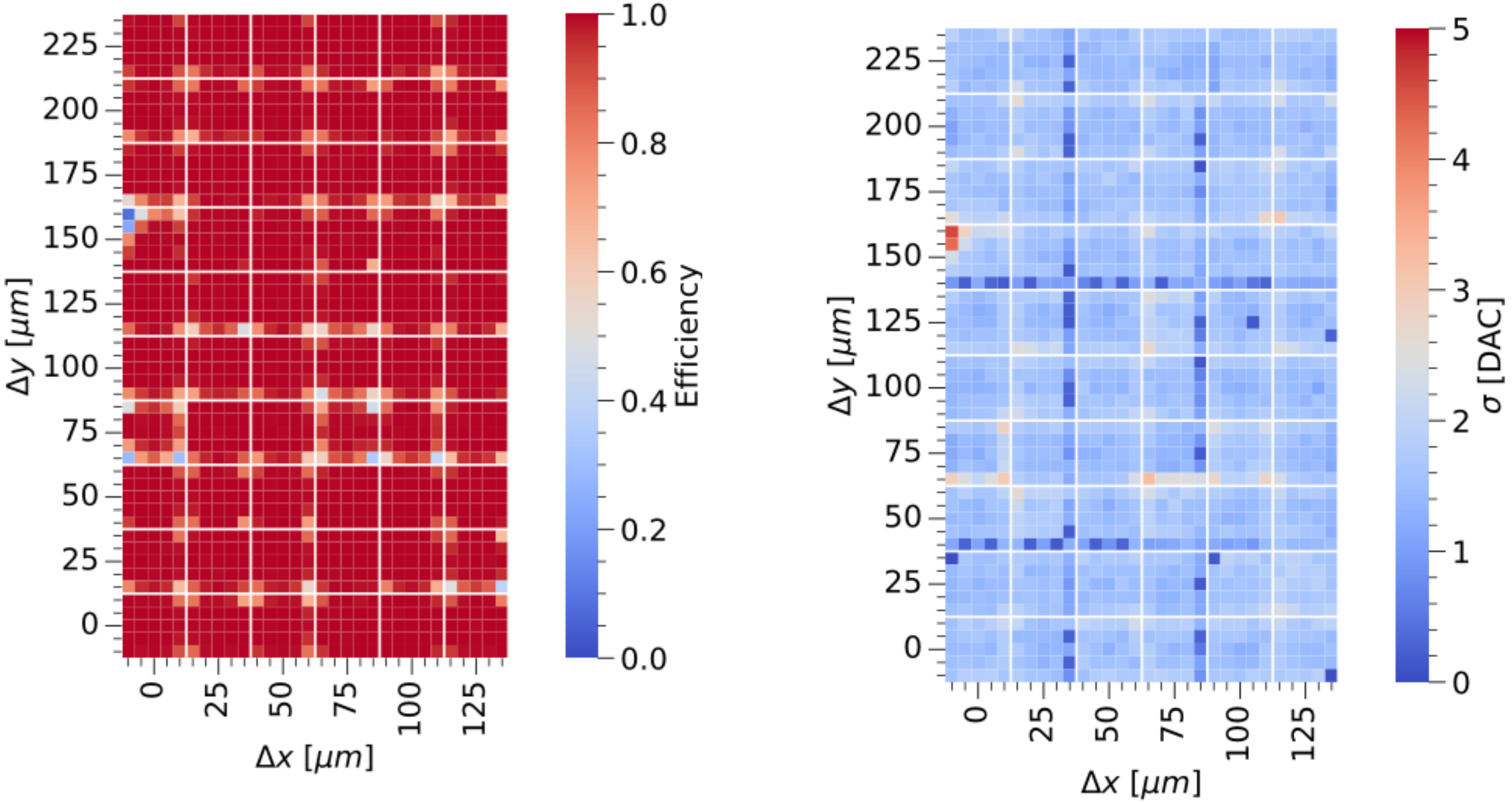
Measurements in the lab

- Excellent readout performance and response to laser scans
    - Lower charge threshold, and higher noise further away from the pixel center.
    - This behavior is largely due due to charge sharing between pixels



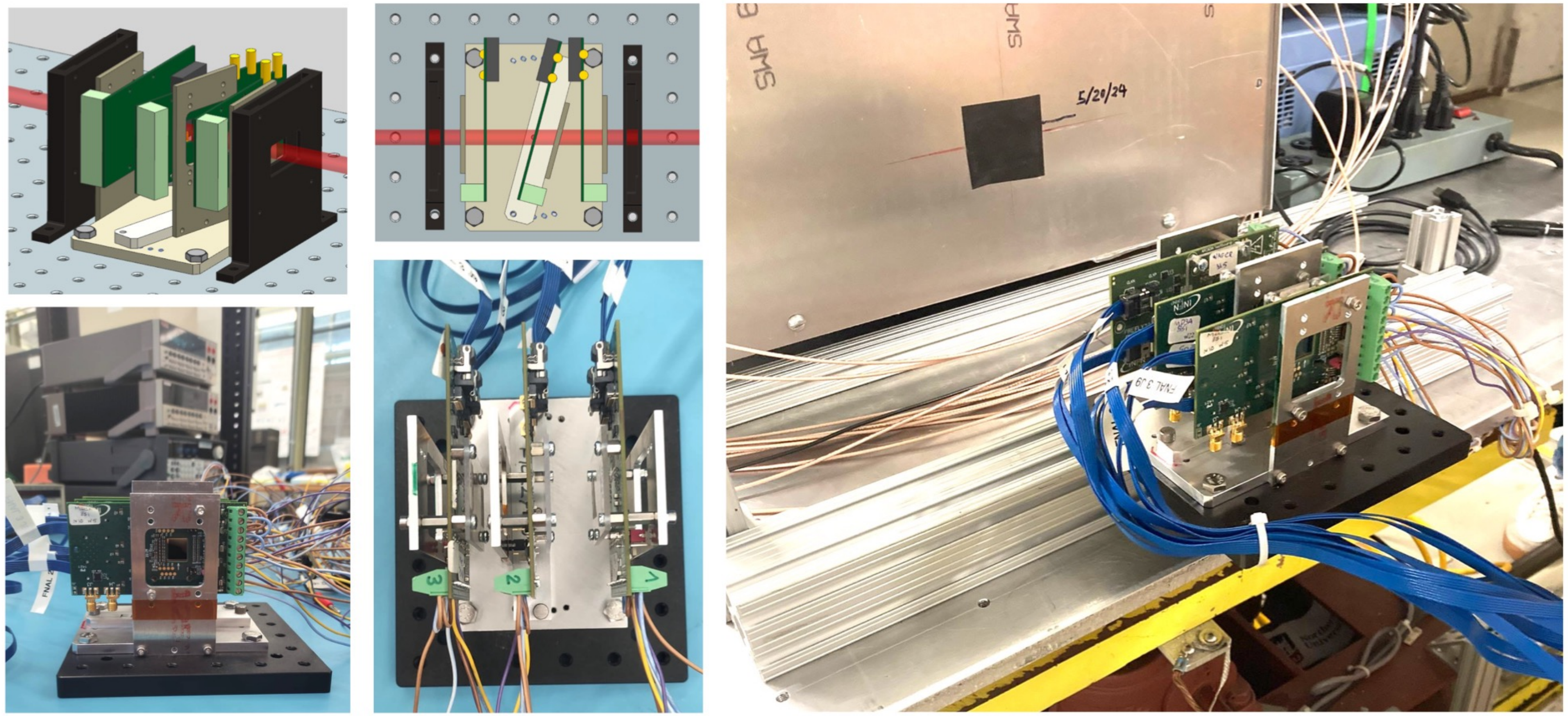
Measurements in the lab

- Excellent uniformity of detection efficiency across the pixel area
- Noise is mostly uniform across detector surface

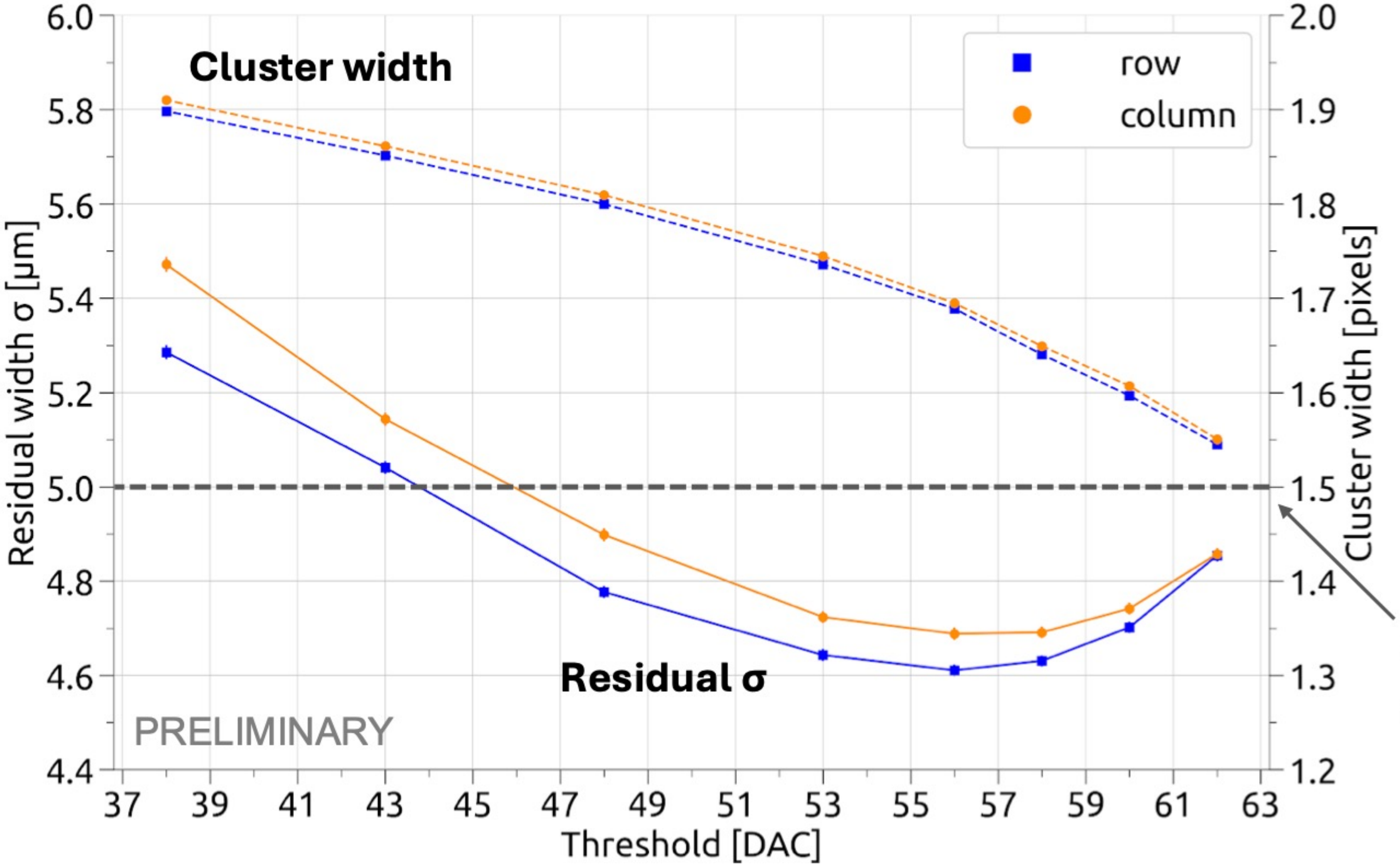


Measurements in beams

- Test beam at FNAL (120 GeV protons) in Summer 2024
  - Mini-telescope with 3 ARCADIA-MD3 sensors
  - Threshold, sensor HV and incidence angle parametrization: study of cluster size, collection efficiency, spatial resolution



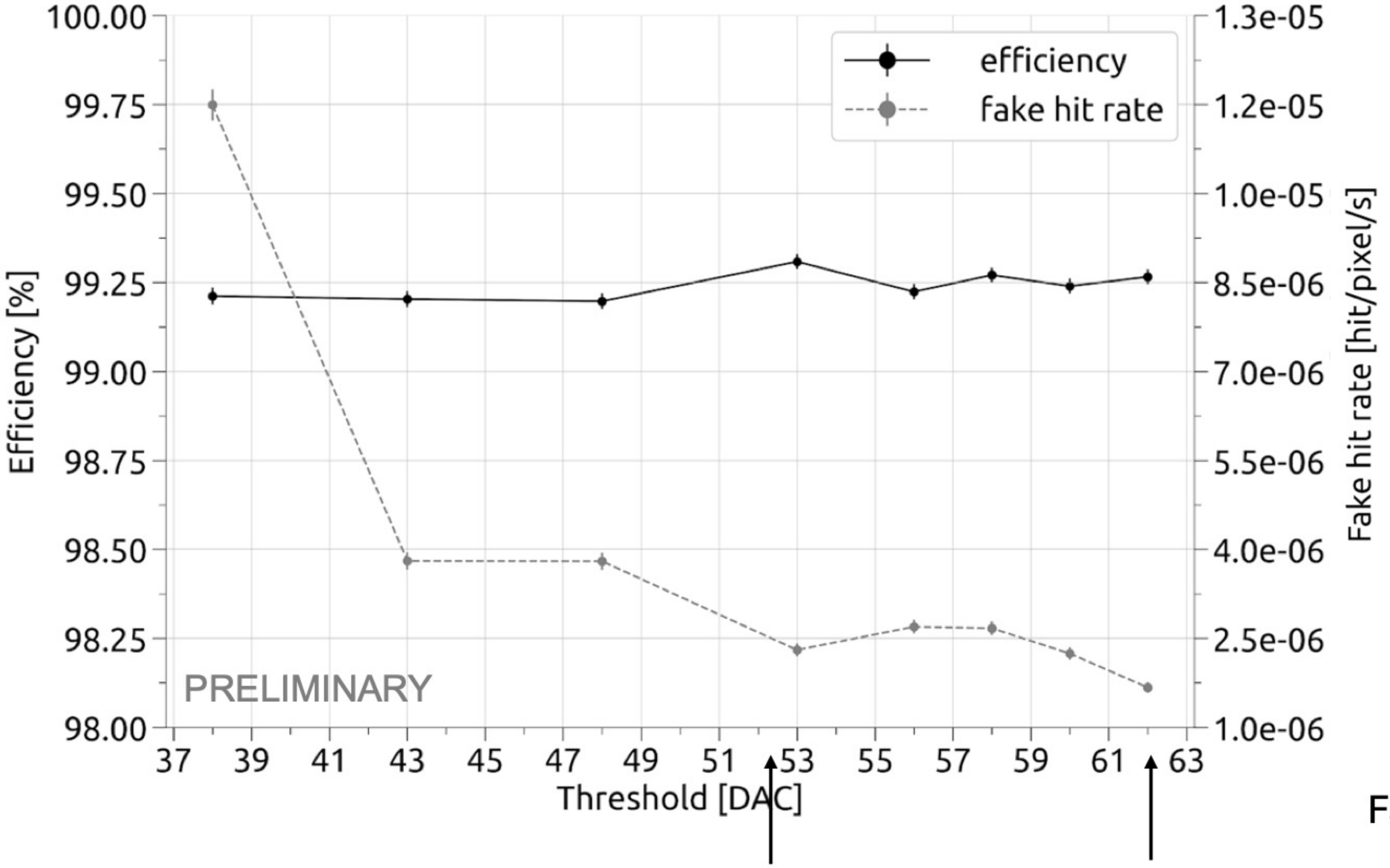
Measurements in beams



Cluster width always greater than 1.5 pixels

- Residual width always below the binary resolution (7.2 μm)

Measurements in beams



$1200\ e^-$

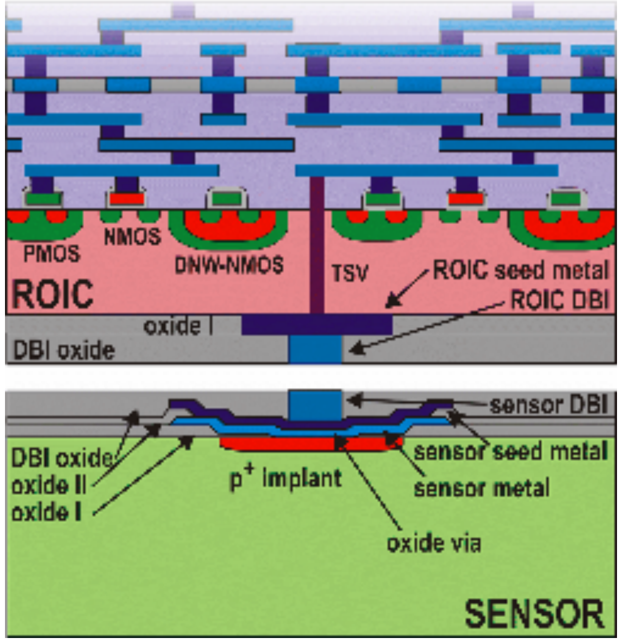
$2200\ e^-$

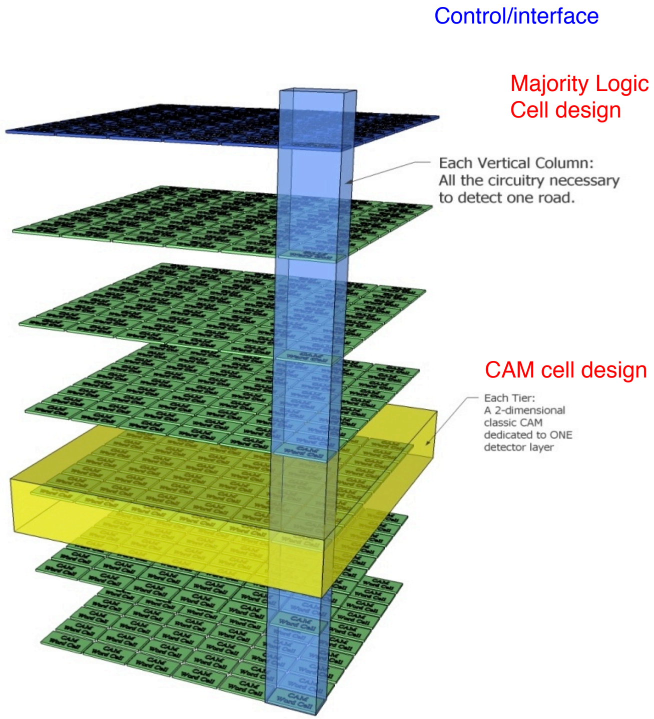
Fake hit rate measured
during no-beam time
12 masked pixels on the DUT

Advanced nodes, new technology

- Low-power, highly granular detectors in (***x***, *t*)
  - Implement in **TSMC 28-nm** technology node
  - Adopt **3D-integration** for HEP detectors

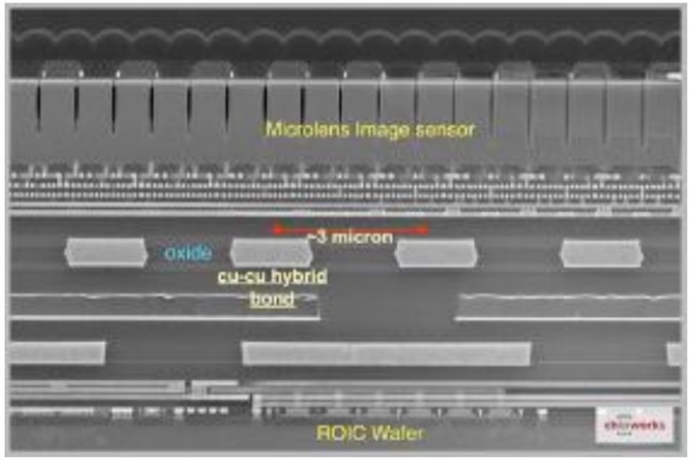
- Supported by DOE “Accelerated Innovation in Emerging Technologies”
  - Joint development effort of SLAC, FNAL and LLNL
  - Partner with industry leaders to implement new technologies
  - Design goal: position resolution ~5 µm, timing ~ 5-10 ps





3D project

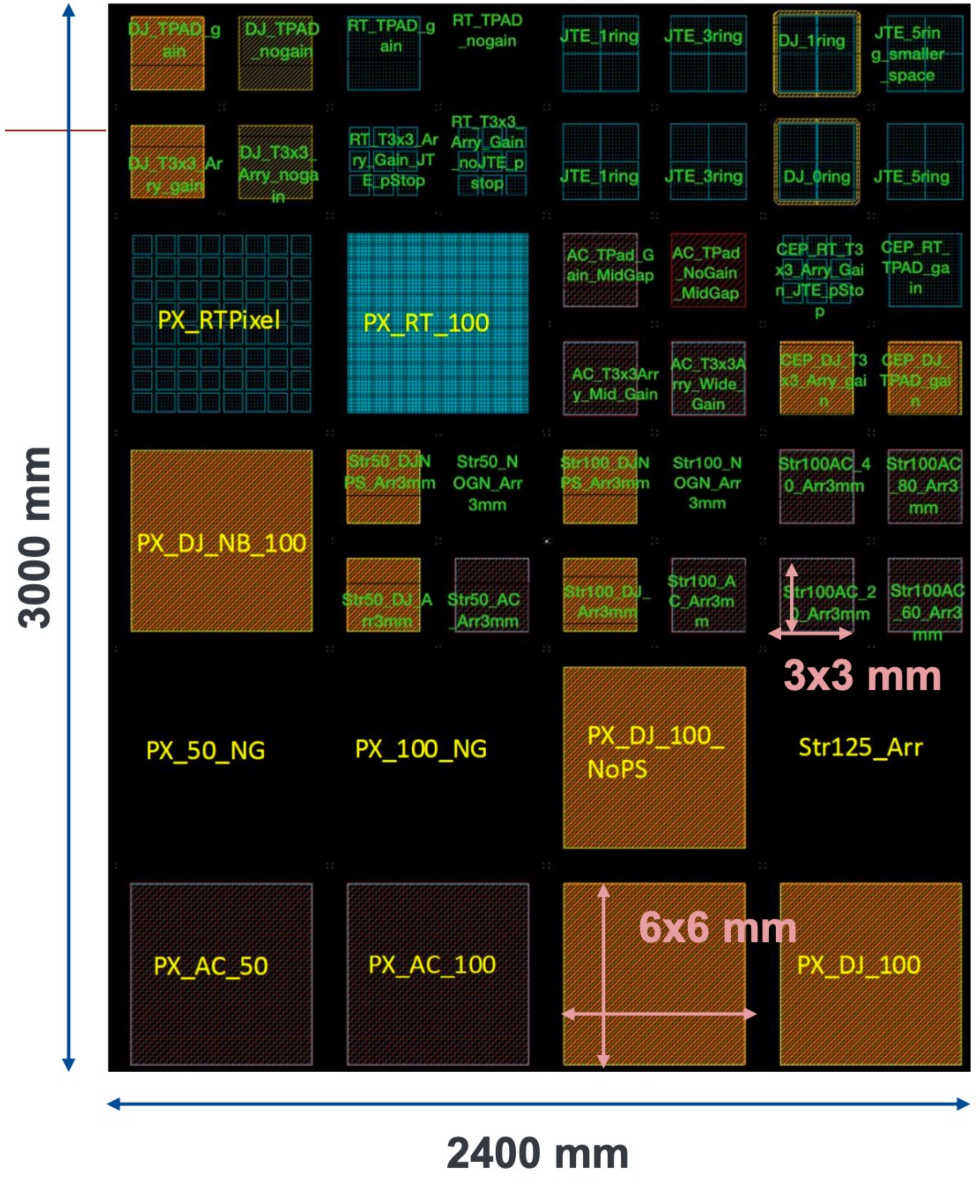
- The research program consists of three main thrusts towards developing the proposed detector:
  - **Thrust 1:** *Design and manufacture Low-Gain Avalanche Diodes (LGADs) devices compatible with* ***12" foundry processes :***
  - **Thrust 2:** *Design application specific integrated circuit (ASIC) techniques to meet various application needs for granularity, precision timing, and power*: ***28 nm design***
  - **Thrust 3:** *Enable a new generation of particle detectors that utilize* ***3D-integration****:*



Section of the Sony Exmor camera chip showing the hybrid bond interface

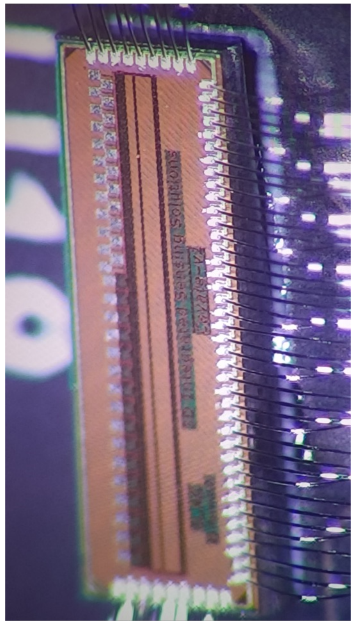
3D project : sensor development

- Development in partnership with Tower Semiconductor
  - Wafer run: 12” in 65nm process
  - **First LGAD process on 12” wafers**
- Optimize doses, energies, edge termination strategies
  - Standard CMOS process forces constraints on detector design
  - Define active regions to exclude STI, metal density and spacing, angles restricted to 45° and 90°, etc…

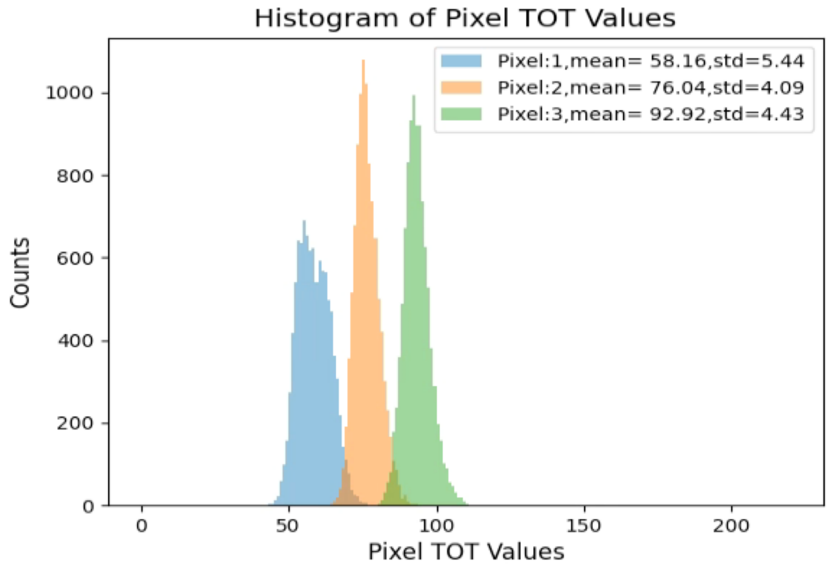


3D project: readout ASIC

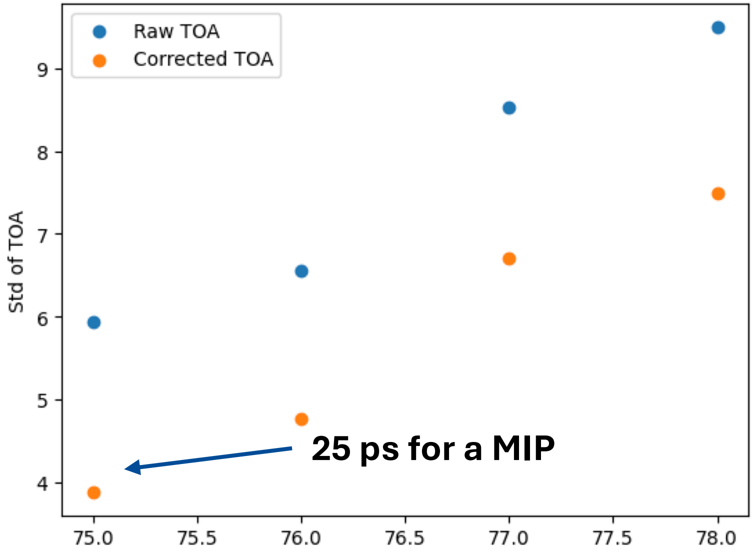
- First 28nm readout ASIC prototype (1x3 mm^2)
  - Variants of 50μm and 100μm size pixels
- Test main ingredients for full chip integration
  - TDC prototype demonstrated full system jitter around 10 ps
  - Measurements LGAD sensor: time resolution around 30 ps



First readout ASIC prototype, TSMC 28 nm



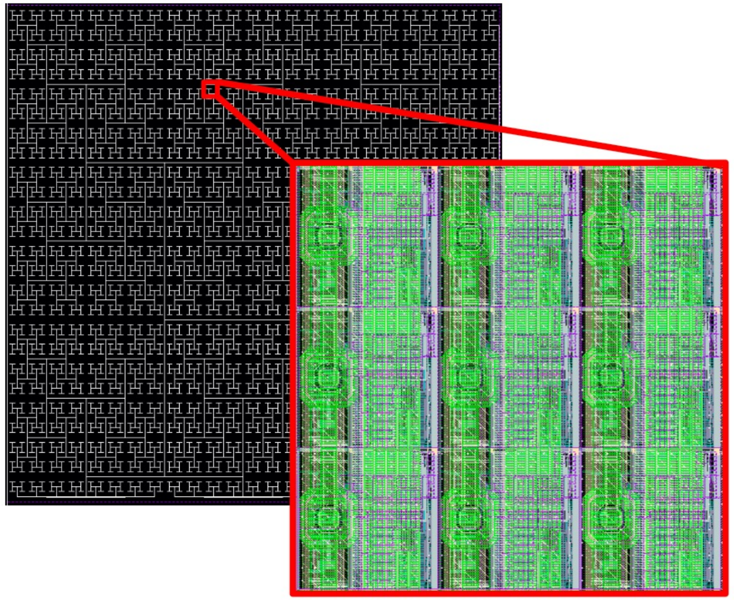
TOT of different channels of 50x50 μm^2 pixelated LGAD



Time resolution with 50x50 μm^2 pixelated LGAD

3D project: readout ASIC 2nd prototype

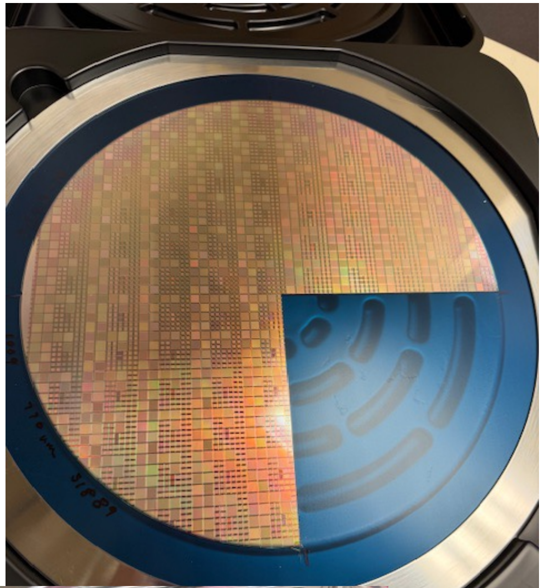
- 2nd prototype in 28nm submitted in September 2025
  - THRIGLAV: THRee-d InteGrated LgAd driVer
- (5x6 mm^2) with 100x100 array of 50μm pitch pixels
  - Optimization of pixel blocks based on feedback from MPW1
  - Digital control and readout logic design, fast IO driver.
  - First demonstration of 28nm readout chip bump-bonded to the prototype LGAD array with high-precision timing performance.
- For the next project phase, we would proceed to wafer-to-wafer bonding of 12” LGAD and 12” 28nm ASIC wafers.

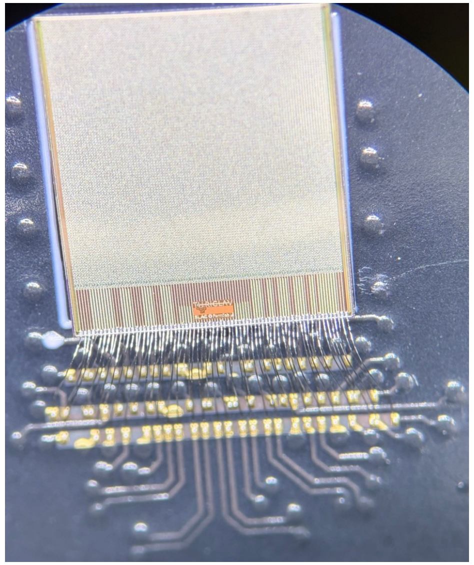


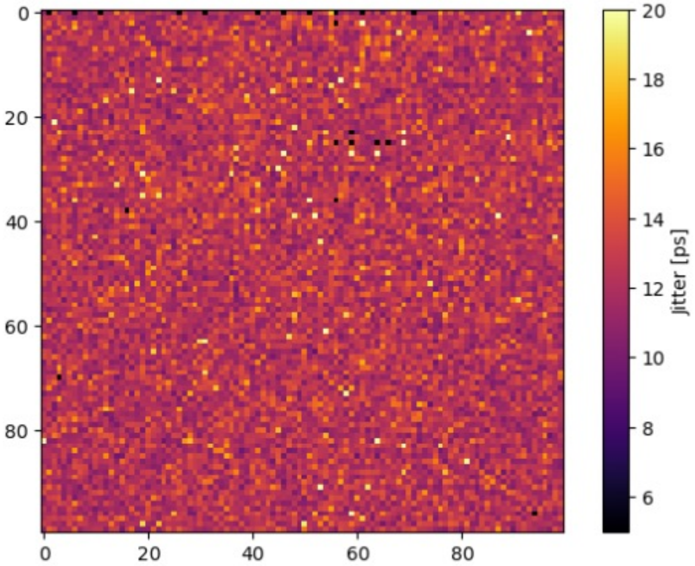
Layout of the pixel matrix highlighting the clock distribution three with zoom on 3x3 pixel region

3D project: MPW2 and 12” LGAD sensors

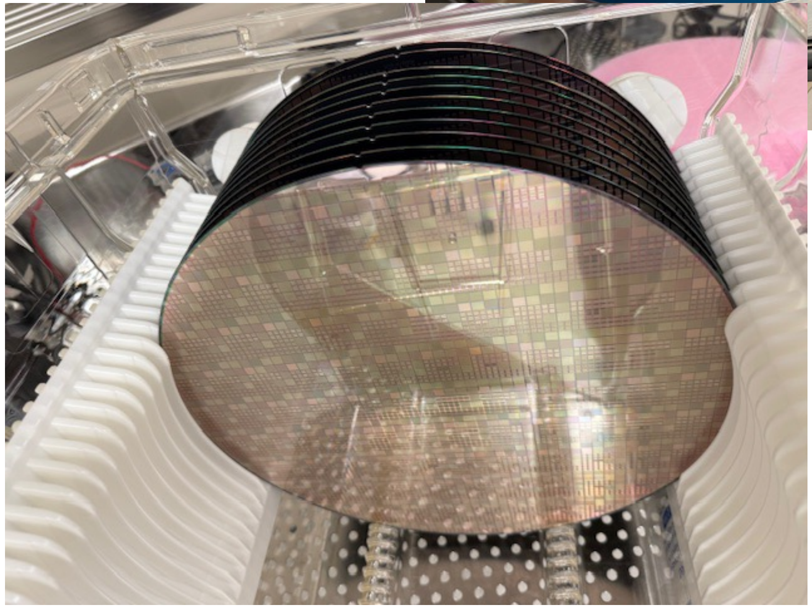
- First production of 12” LGAD sensors from Tower delivered
  - Sensors behave as expected, measure gain around 10-20
  - Extensive testing characterization is ongoing now
- MPW2 bump-bondable chip just received
  - Measurements of the FE+TDC jitter : around 12 ps
  - Bump-bonding with LGADs and test-beam characterization soon





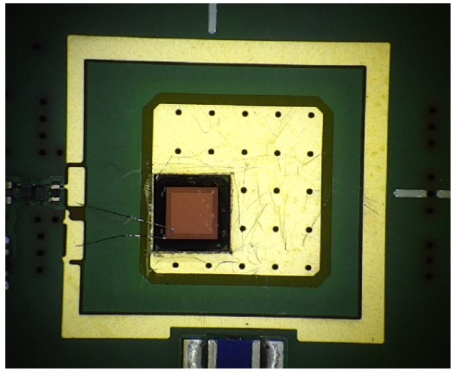


Average Standard Deviation: 12.54 ps

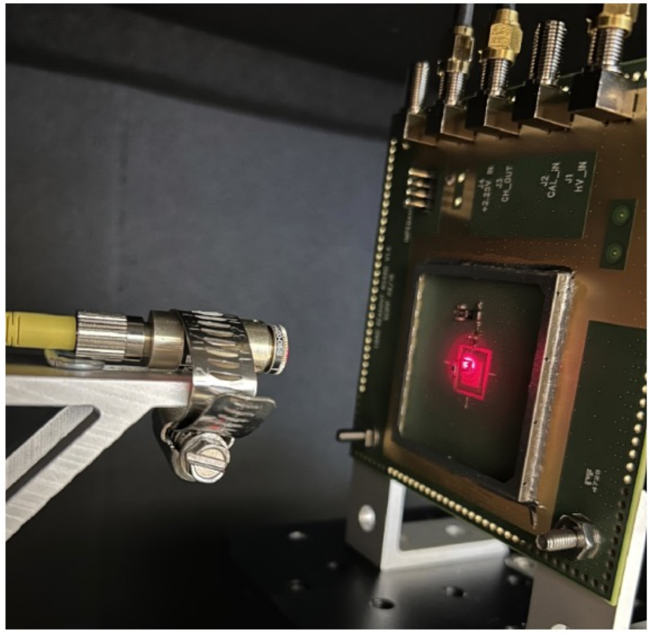


Measurements of performance

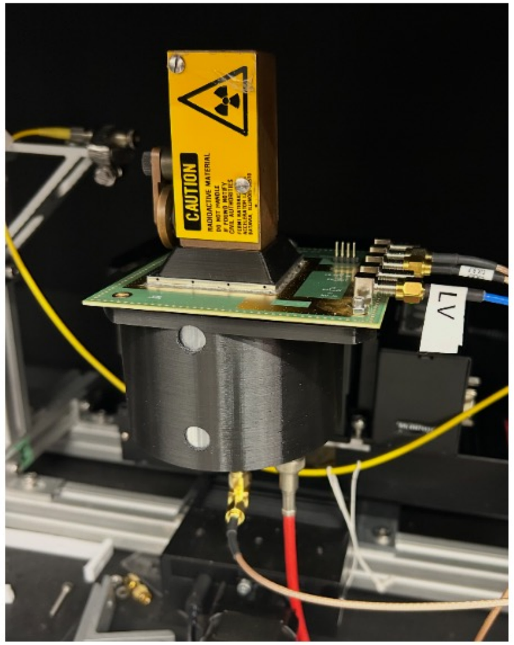
- Working on detailed characterization of performance of the sensors
- Measurements performed using either beta source, or IR-laser

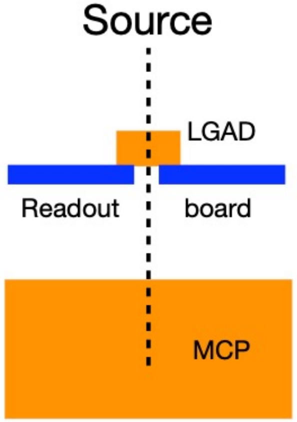


Laser setup



Beta source setup





Source

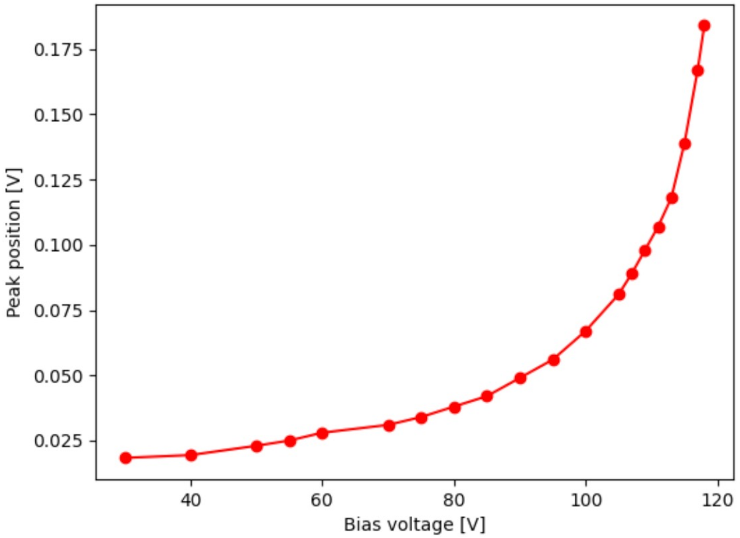
LGAD

Readout board

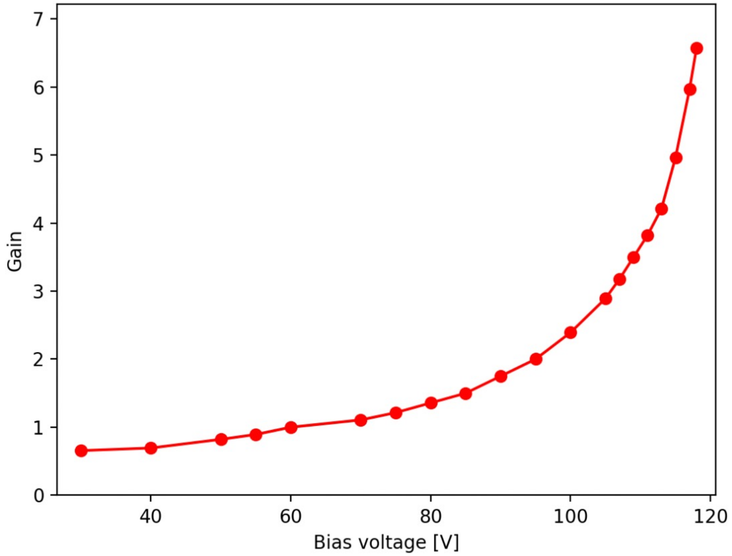
MCP

Performance characterization

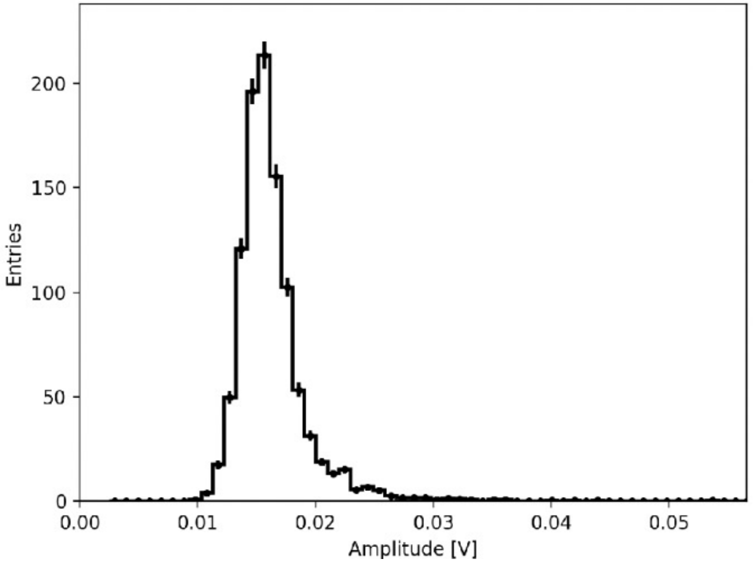
- Sensors behave very well, no early breakdown, gain performance as expected
- A few sensors have been tested so far, many more to be tested
- Time resolution studies are just starting, look very good so far



Signal MPV vs BV for DJ-LGAD, IR-laser



Signal Gain vs BV for DJ-LGAD, IR-laser



Signal MPV for AC-LGAD with beta-source

Summary

- Steady progress on multiple fronts in the development of tracking sensors for FCC
- Actively engaged in the international and US collaborations on detector R&D: DRD and RDC
- Unique facilities and expertise enable the community to perform cutting edge detector R&D
    - Many opportunities to make an impact on this R&D