Process fabrication III

E.G. Villani

Overview

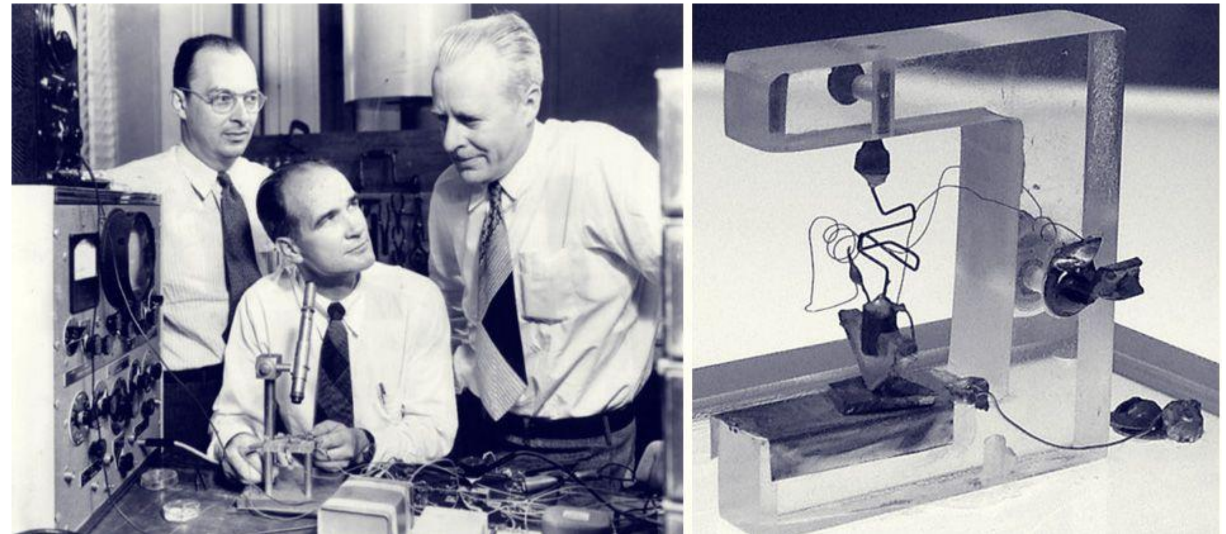
- **Semiconductor technology**
    - *Introduction*
    - *Moore's Law*
    - *Dennard's Law*
- Semiconductor fabrication process I
  - *Introduction*
  - *Silicon crystal growth*
  - *Fabrication process flow*
  - *Oxidation*
    - *Purpose*
    - *Tools/equipment*
    - *Deal-Grove model*

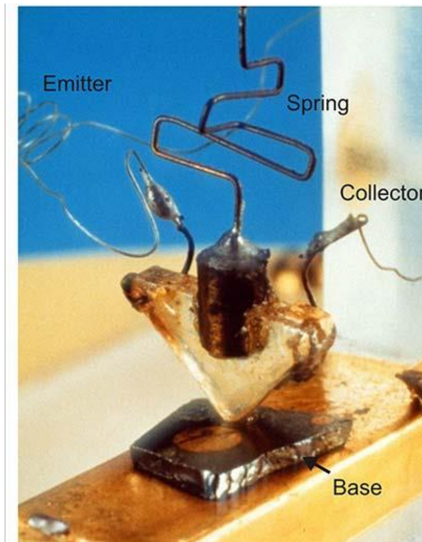
Introduction

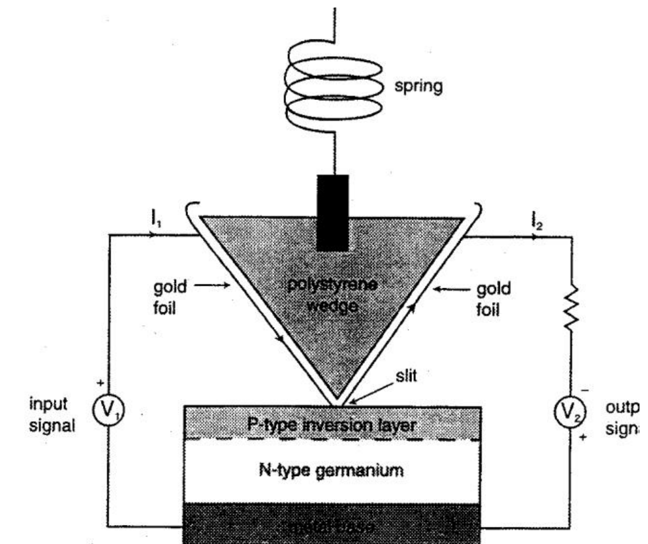
- First bipolar (PNP Ge) transistor invented in 1947 (*US patent 2569347A, 1948*)

- Research on solid state devices to replace vacuum tubes

- Resulted from failed attempts to build a field-effect transistor (FET)





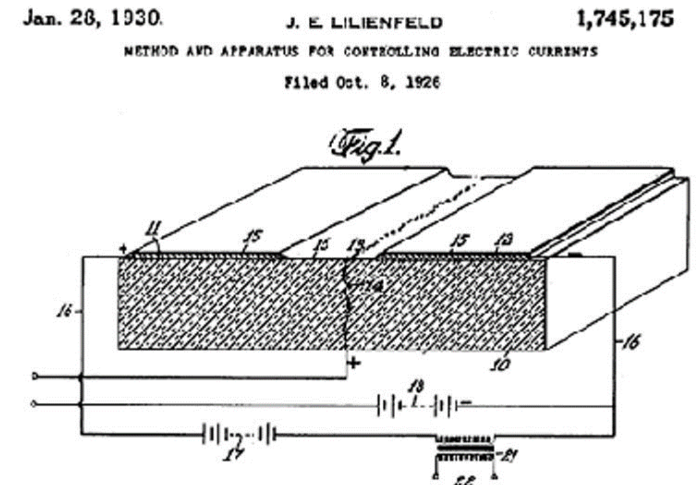


Introduction

- First FET (Field Effect Transistor) patented filed in 1930 (*US patent 1745175A,1930*)

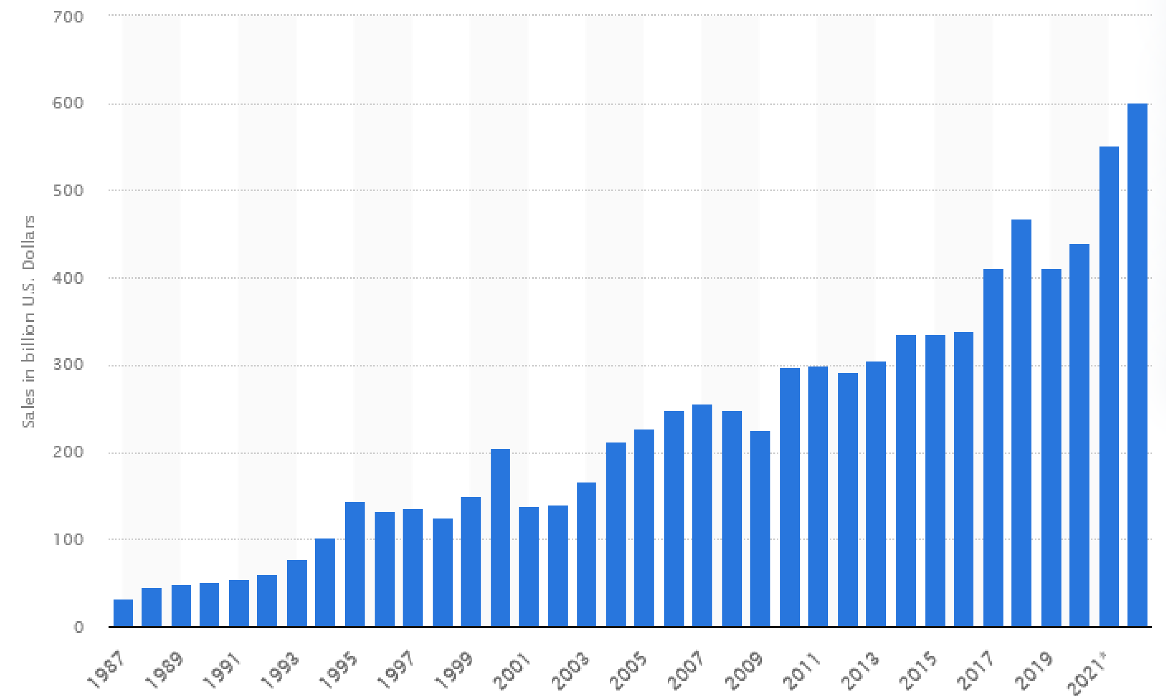
- Serious problems with surface states/ dielectric defects prevented the devices from working

- First practical working device invented in 1959, using SiO_2 as dielectric (MOSFET, Metal Oxide Silicon Field Effect Transistor)



Introduction

- MOSFETs by far the most widely used (99%) transistor device
- Estimated > 10^{22} devices produced since 1960 (> 10^{12} produced only in 2021)
- Sales of semiconductors in 2021 >550 10^9 USD



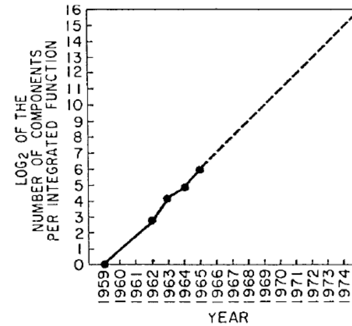
Semiconductor market size worldwide from 1987 to 2022

Moore’s Law

- Semiconductor industry started around 1960 (First hybrid:, Kilby, Jack S. "Miniaturized Electronic Circuits", U.S. Patent 3,138,743, February 1959)

- In 1965 G. Moore predicted a doubling number of integrated components every year, to promote the idea of integrating devices. From mid ‘70s the trend is doubling every ~2 years

- Such trend has been maintained for almost 60 years, leading to ~$2^{60/2}$= 10^9 transistors count on chip

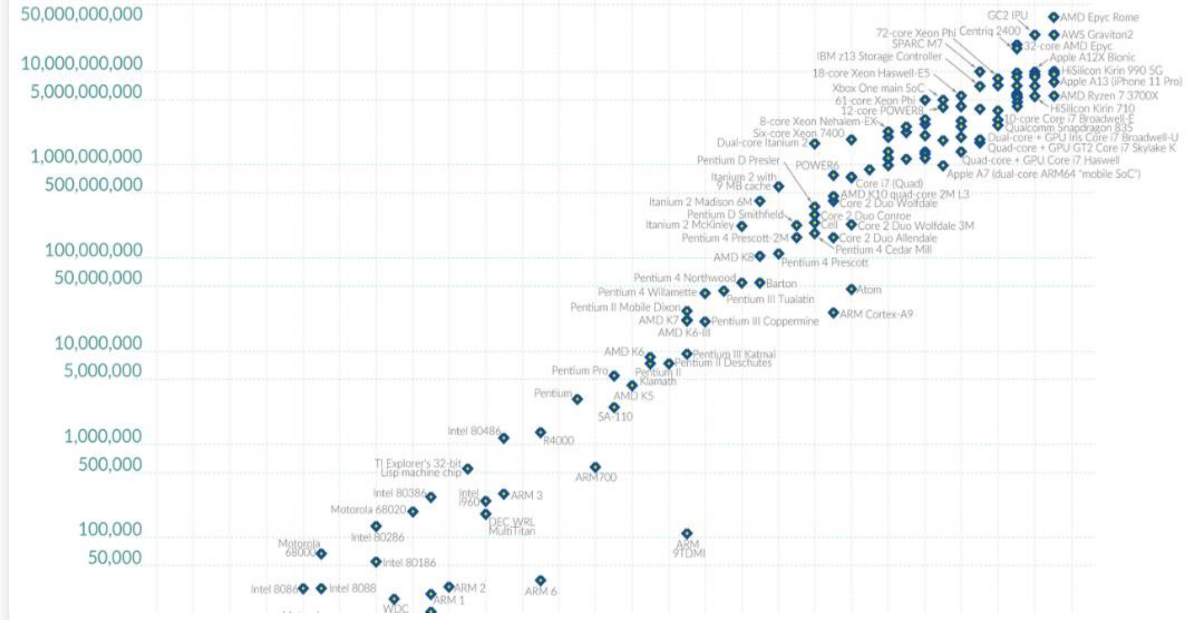


“With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65 000 components on a single silicon chip.”

G.E.Moore, “Cramming More Components onto Integrated Circuits”,Electronics Vol. 38, No. 8 Apr. 1965

Moore’s Law: The number of transistors on microchips doubles every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

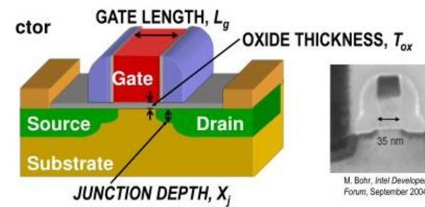


Moore's Law

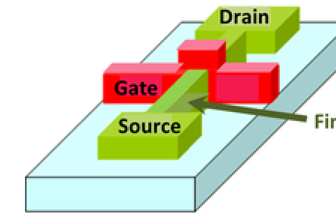
- Technology size referred to actual minimum MOS transistor gate length

- Since the advent of non-planar 3D structures the name of nodes means an equivalent gate length size of a planar device

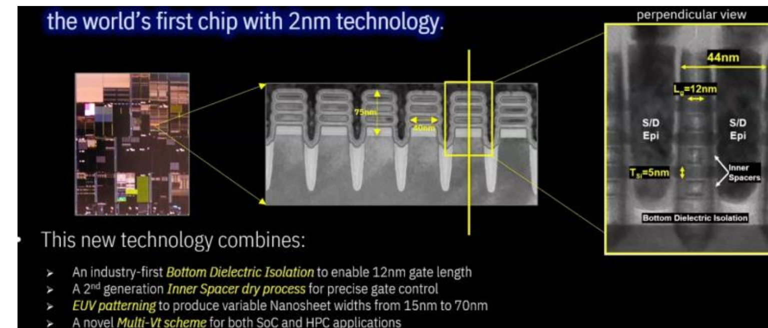
- Reducing the size of the devices requires considerable technological efforts and investments



Planar MOSFET. The gate material runs over the channel region



Non-planar Fin-MOSFET. The gate material wraps around the channel region and provides better control of the channel conductivity



Gate all around (GAA) MOSFET. The gate material surrounds the channel region on all sides. IBM announced 2 nm technology

Peak Quoted Transistor Densities (MTr/mm2)

AnandTech	IBM	TSMC	Intel	Samsung
22nm			16.50	
16nm/14nm		28.88	44.67	33.32
10nm		52.51	100.76	51.82
7nm		91.20	237.18*	95.08
5nm		171.30		
3nm		292.21*		
2nm	333.33			

Data from Wikichip, Different Fabs may have different counting methodologies
*** Estimated Logic Density**

https://www.anandtech.com/show/16823/intel-accelerated-offensive-process-roadmap-updates-to-10nm-7nm-4nm-3nm-20a-18a-packaging-foundry-emib-foveros

Dennard's Law of scaling

- From Dennard's 1974 paper: smaller feature size can only bring benefits
- Smaller -> Faster, Less power dissipation; Power density remains the same!

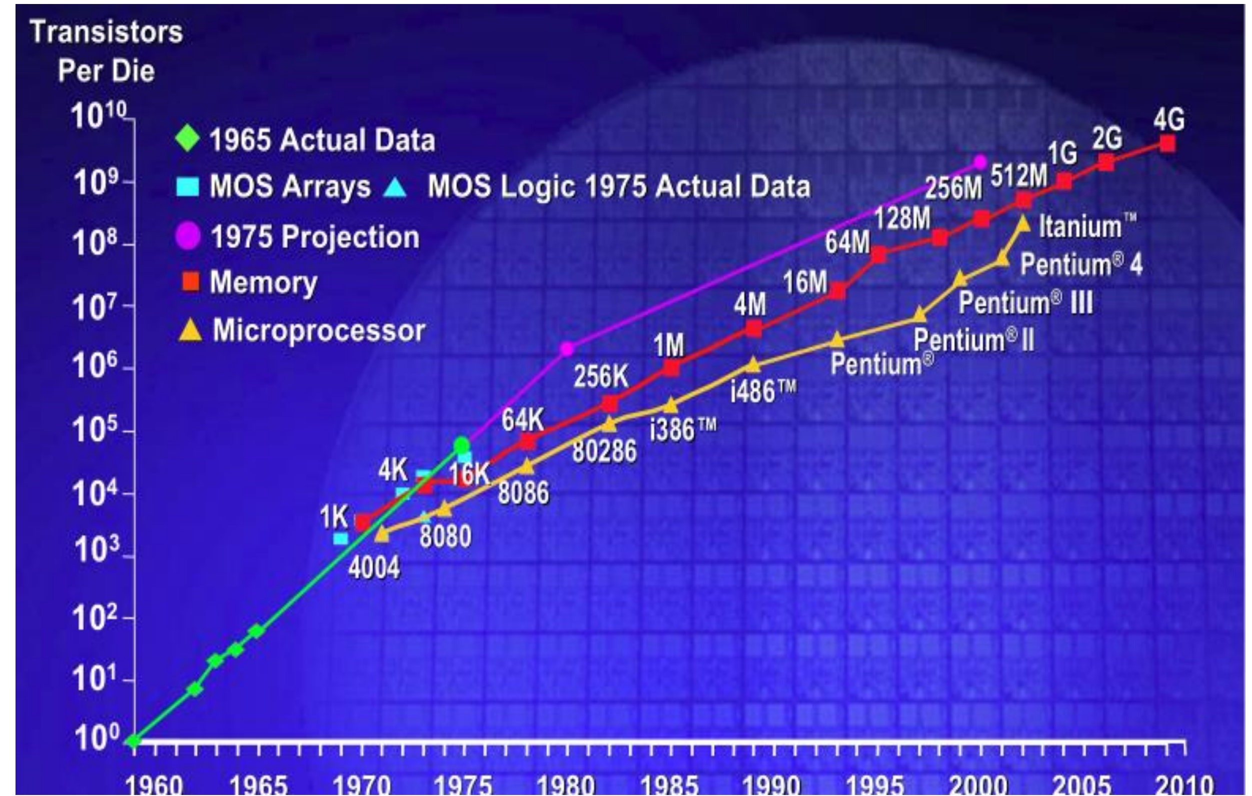
Device or Circuit Parameter	*Scaling Factor*
Device dimension t_{ox}, L, W	$1/k$
Doping concentration N_a	k
Voltage V	$1/k$
Current I	$1/k$
Capacitance eA/t	$1/k$
Delay time per circuit VC/I	$1/k$
Power dissipation per circuit VI	$1/k^2$
Power density VI/A	1

Table I: Scaling Results for Circuit Performance (from Dennard)

R. H. Dennard et al., "Design of ion-implanted MOSFET's with very small physical dimensions," Oct. 1974, doi: 10.1109/JSSC.1974.1050511

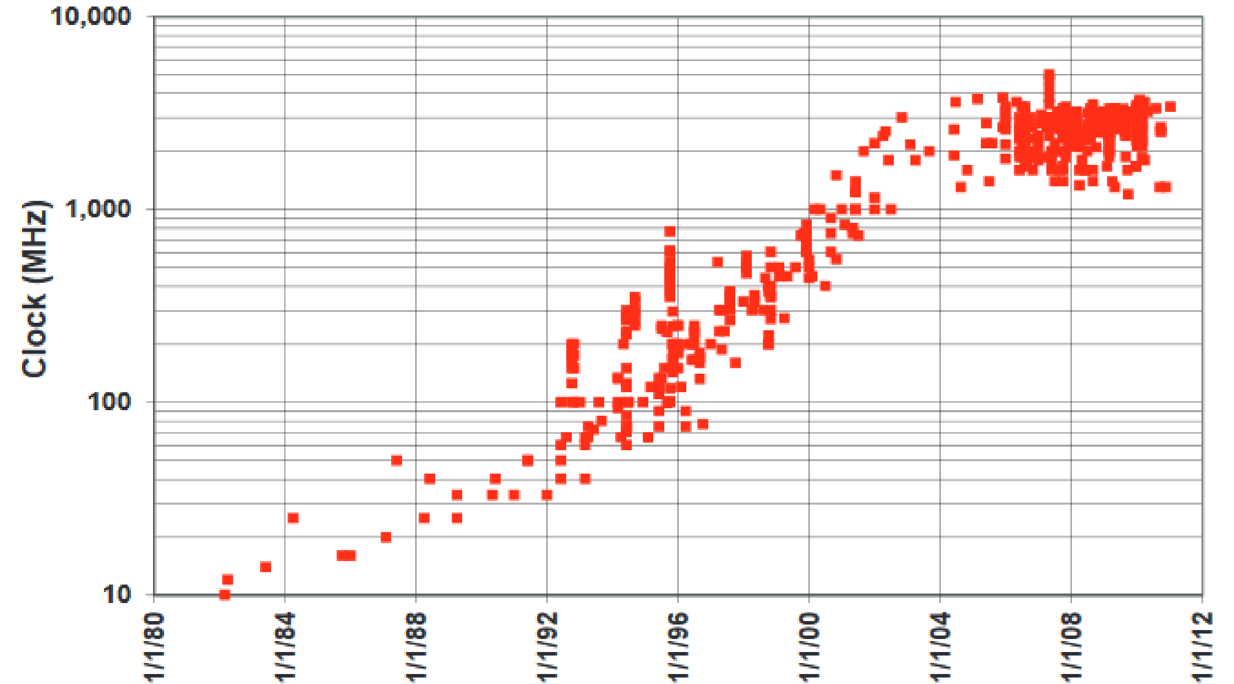
Dennard's and Moore's Law

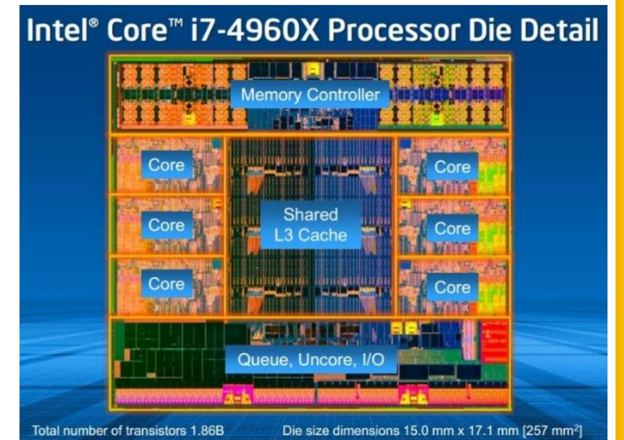
- By keeping the cost/area of chip constant:
  - More powerful chip for the same price
  - Same chip for a lower price: the scaling down of transistor area reduces the cost of a transistors by 30%/year.
  - This trend has continued for around 20-25 years (1975-2000)



Dennard’s Law of scaling

- This scaling ignores **quantum tunnelling** and **noise**, i.e. leakage current, which leads to power dissipation, and threshold voltage which do not scale with size (~1/√k)
- Power wall, limiting the frequency of processors to around 4 GHz since 2006





Dennard's and Moore's Law

- **Moore's law is not a physics law** per se: keeping the cost/area the same (for example increasing the wafer size) despite rising cost of fabrication is the result of human efforts.

- **Dennard's law is based on physics**, but it does not completely justify anymore the continuous trend in size reduction.

- Nowadays the main benefit to reduce the size of transistor is to reduce cost/function

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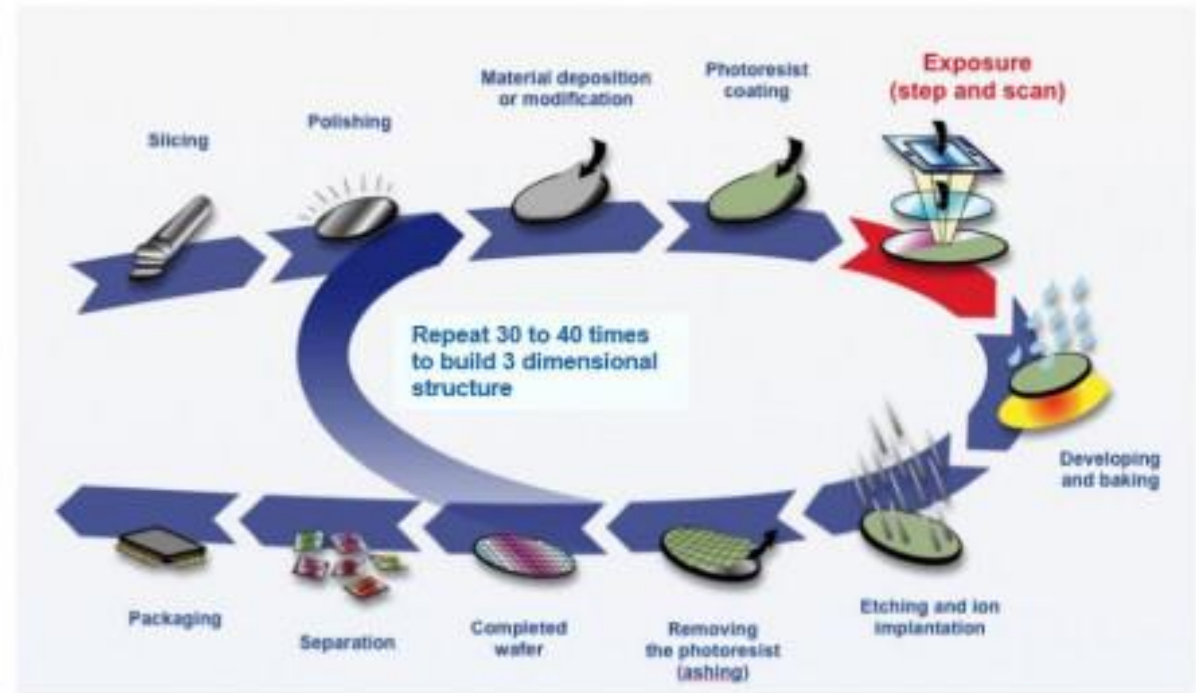
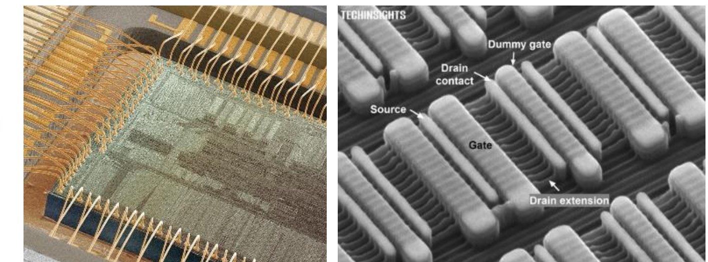
Introduction

- The fabrication of semiconductor devices is a rather complex process
- Many intermediate steps and manufacturing precision at atomic level
- A few of process steps (crystal growth, oxidation and implantation) will be described in some details here
- Other steps described in different lectures by **Andrew Blue**



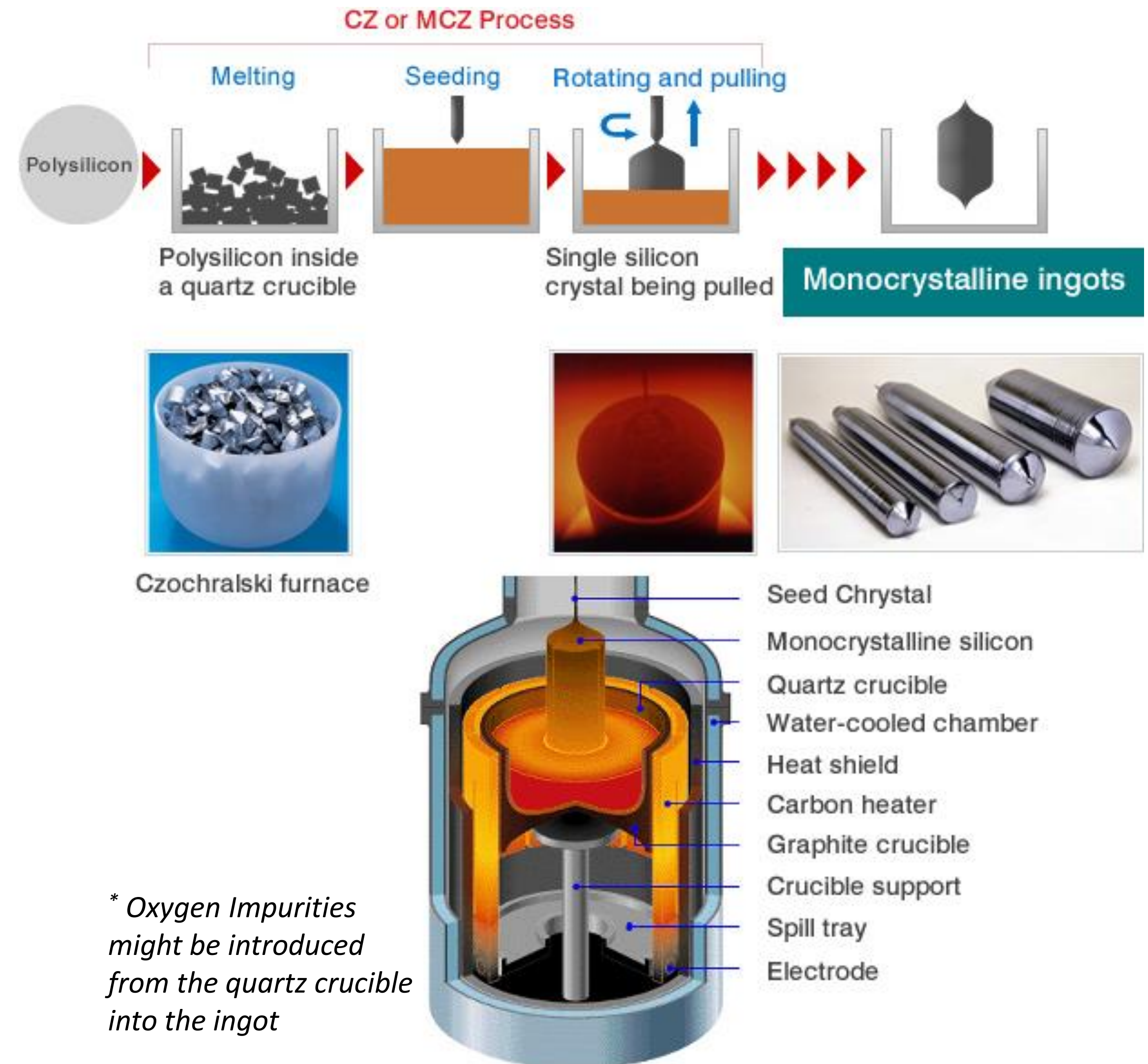


Silicon crystal growth
Czochralski

- The majority of ICs are made on single-crystal Si wafers grown in large ingots using **CZ** (Czochralski, 1915*) method

  1. High purity polysilicon (99.9999999% or 9N) crushed into powder, put into a quartz crucible and heated until it melts

  2. A seed crystal is dipped into liquid silicon. As the stick is rotated and slowly pulled up, an ingot of monocrystalline silicon is formed that has the same atomic arrangement as the seed crystal

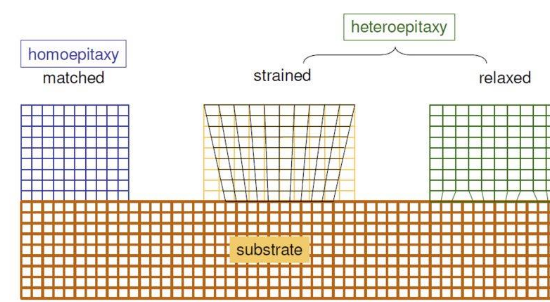


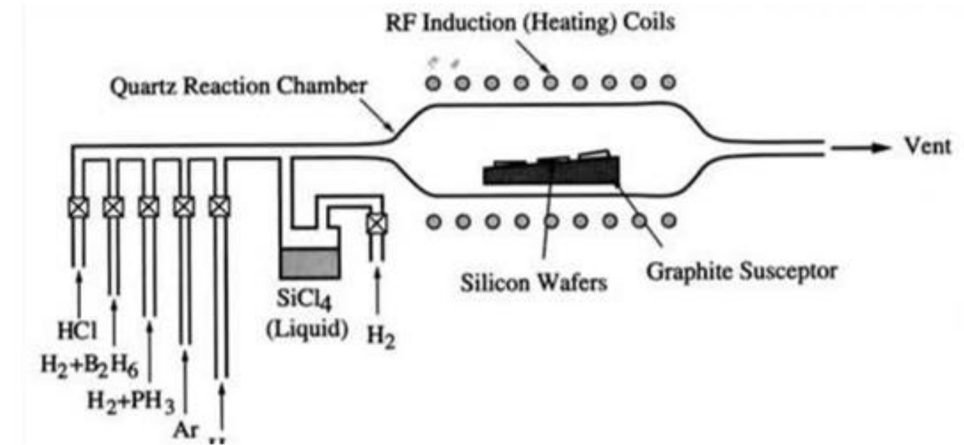
** Oxygen Impurities might be introduced from the quartz crucible into the ingot*

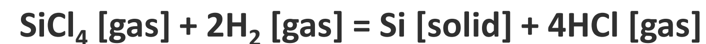
** Czochralski discovered this by accident: instead of dipping his pen into his inkwell, he dipped it in molten tin, and drew a tin filament, which later proved to be a single crystal*

Silicon crystal growth
Epitaxy

- Arrangement of atoms over existing planes of crystalline substrate, to form an extended crystal
- The deposited layer can have very different doping of the substrate, allowing doping profiles unattainable with implantation.
- Different materials can be grown (heteroepitaxy)
- The epitaxially grown layer can be oxygen free





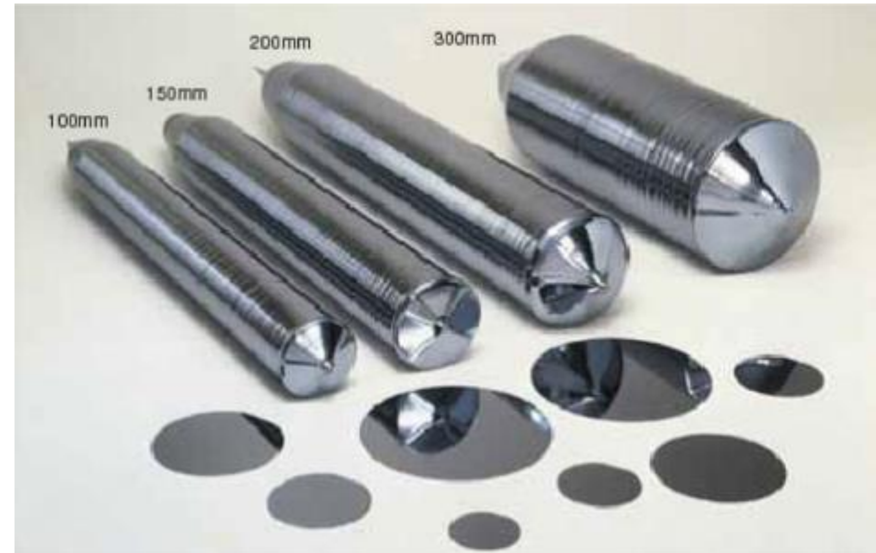


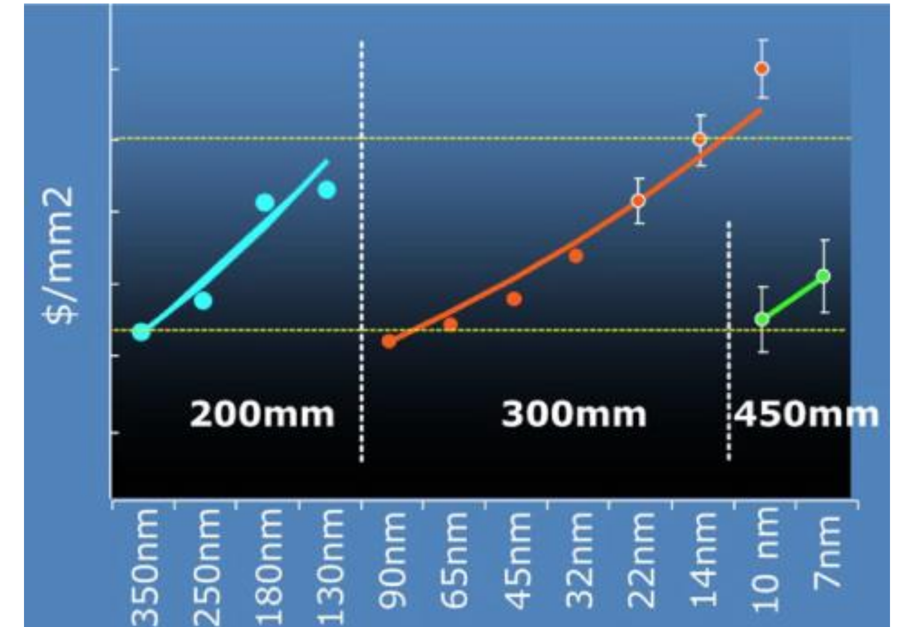
*Chemical Vapour Deposition (**CVD**) is the formation of solid films on a substrate by exploiting a chemical reaction of reactants in vapour phase.*

Reactants introduced in reaction chamber decompose and react with the heated surface to form the film

Silicon crystal growth

- The cylindrical ingot is sliced into thin circular wafers, polished, etched, and cleaned until their surface is almost roughness free (<< 1 nm)
- The diameter of Si ingots grew over the years: currently 300 mm diameter, driven by keeping the cost/area constant
- As per 2021, worldwide Si wafer area around 9×10^6 m^2 , for an approximate 1.15×10^{12} semiconductor units produced





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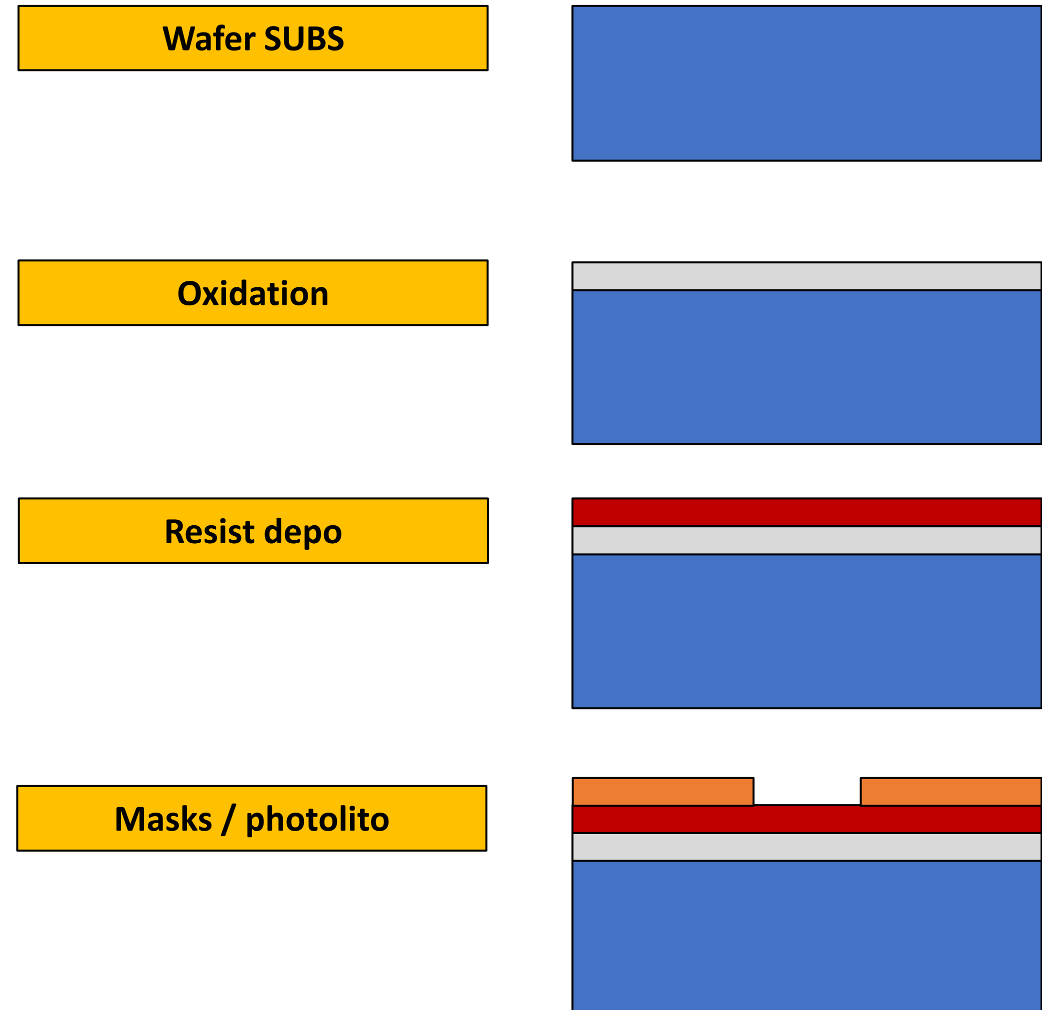
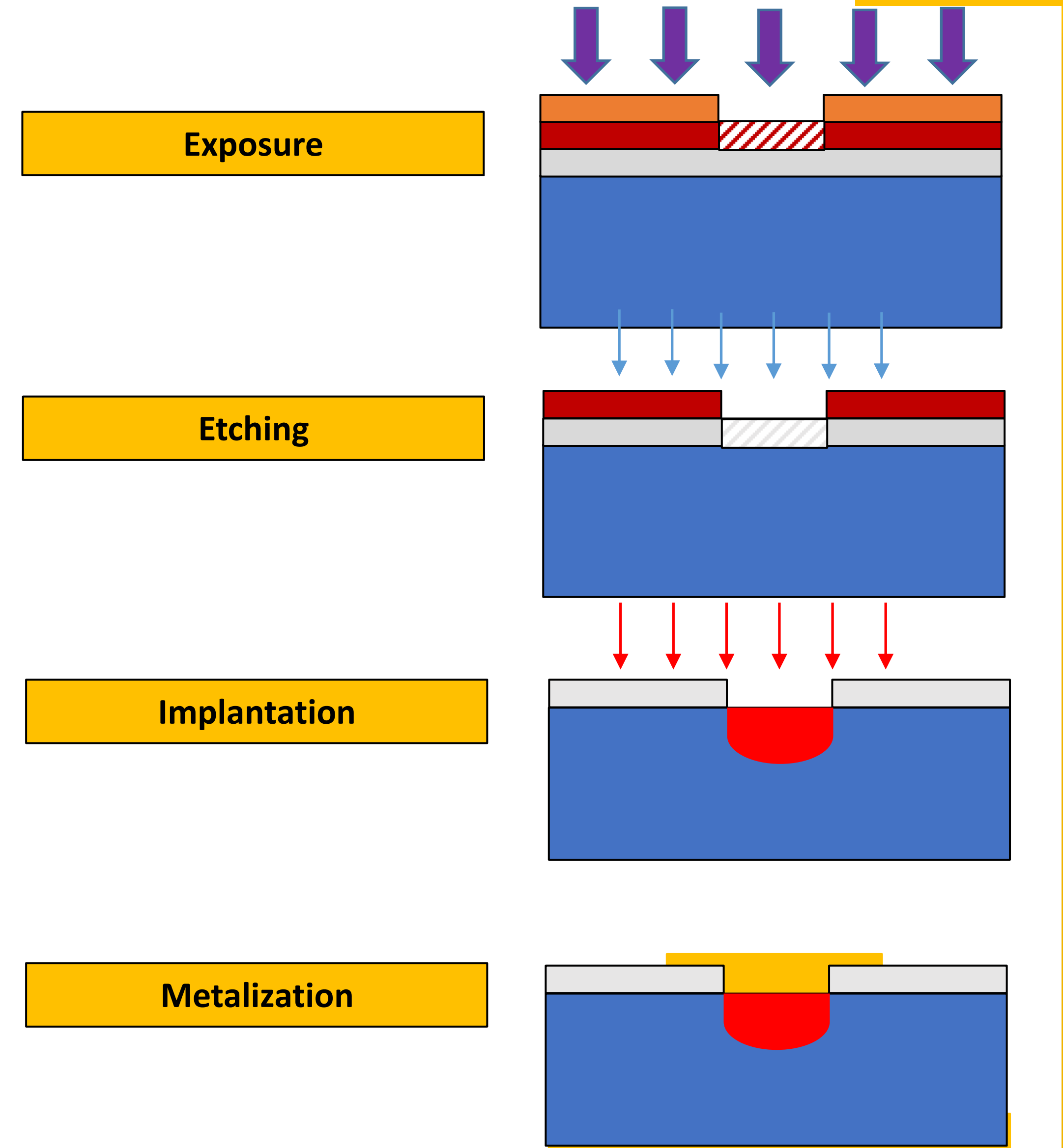
Silicon process fabrication example

- Start with Si wafer cleaned and polished
- The wafer top is covered by **insulating layer**, SiO_2
- Light -sensitive layer (photoresist) deposited
- A photomask with the desired pattern is aligned with the wafer



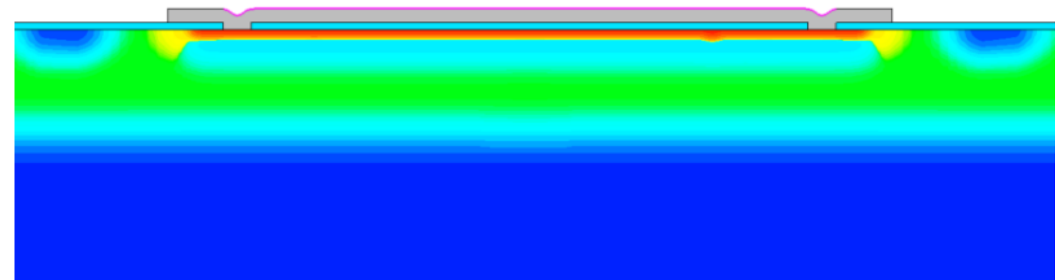
Silicon process fabrication example

- **Photolithography**: exposure to UV light makes the photoresist not covered by masks easily removable (stripping)
- The unprotected SiO_2 is then **etched**, using chemical process, resist is stripped
- The exposed areas of Silicon are then doped, via **implantation** or diffusion, e.g. to obtain PN junctions
- **Metallization** followed by similar photolithographic process to obtain a final device

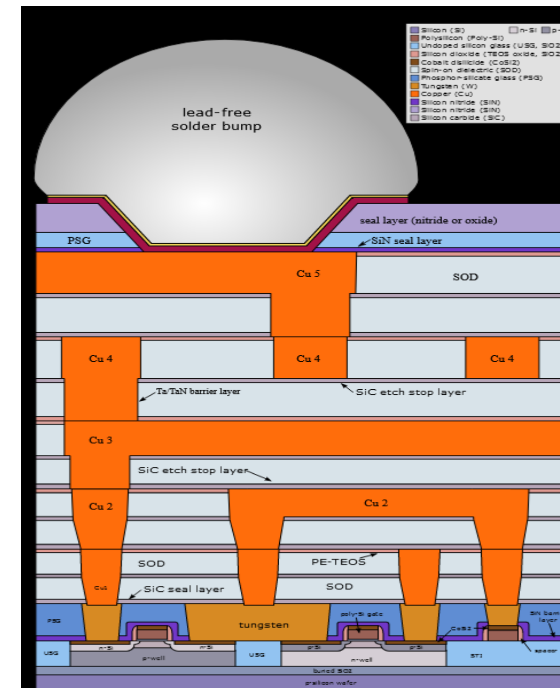


Silicon process fabrication example

- Additional layer of conducting or insulating materials can be added, to obtain multilayers structures
- > 10 layers in modern submicron CMOS process



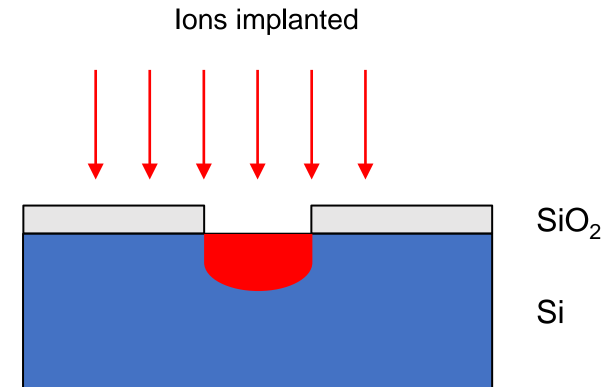
Example of cross section of LGAD devices – single Al layer

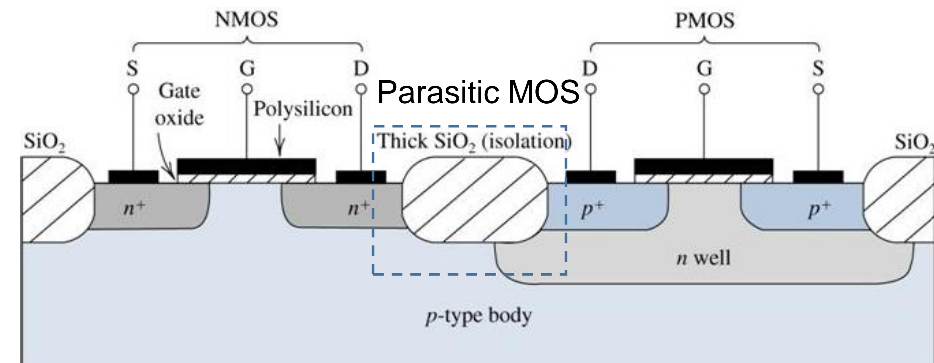


Example of cross section of modern CMOS IC – multiple metal layers (Cu to reduce resistivity of interconnections)

Oxidation fabrication process

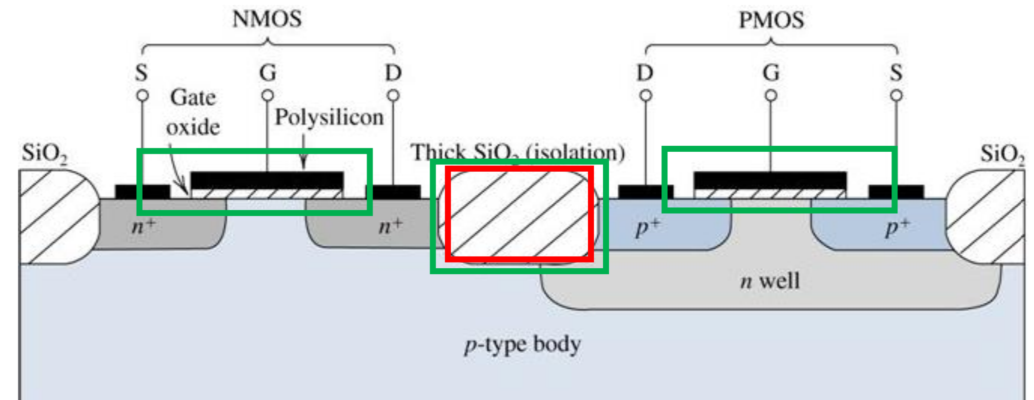
- The purpose of oxidation is essentially to provide **isolation**:
  - Barrier against dopants diffusion/implantation
  - Electrical insulator between devices (critical field ~ 10^7 V/cm)

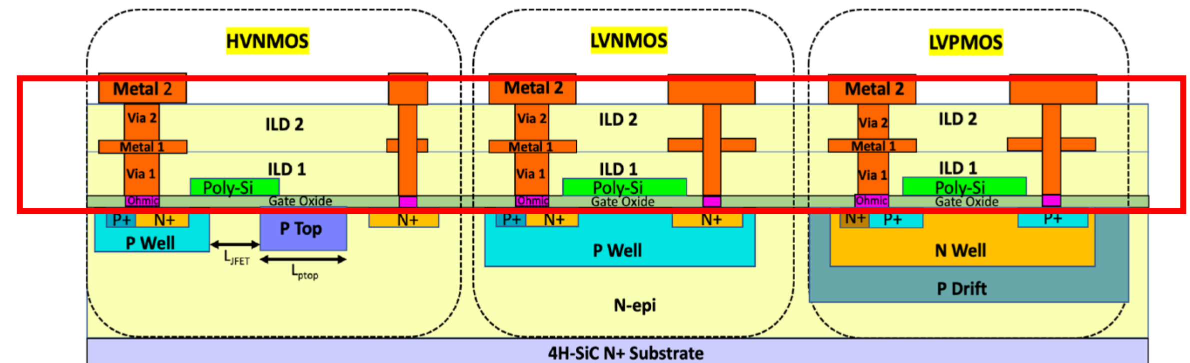




Oxidation fabrication process

- Two deposition methods:
  - **Thermal growth**
    - Dry: best quality, slow growth rate: used for **gate** oxide
    - Wet: lower quality, faster growth rate: used for **field** oxide (isolation)
  - **Chemical vapor deposition** (lower quality, fast)
    - Used when **no Si is available** for oxidation (Interlayer isolation)





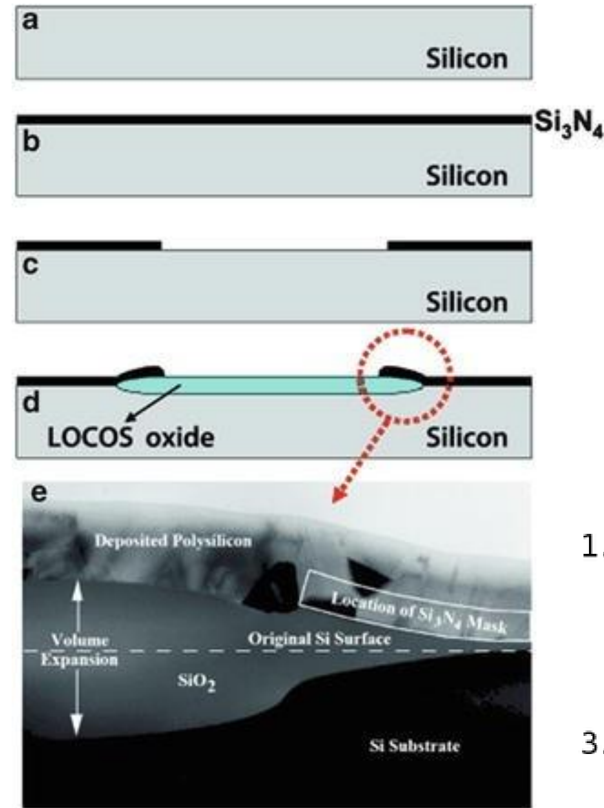
Oxidation fabrication process

- **LOCOS** (local Oxidation of Si) process, rarely used nowadays:

  Thermal oxide is grown in etched region: **bird's beak** means Si area loss

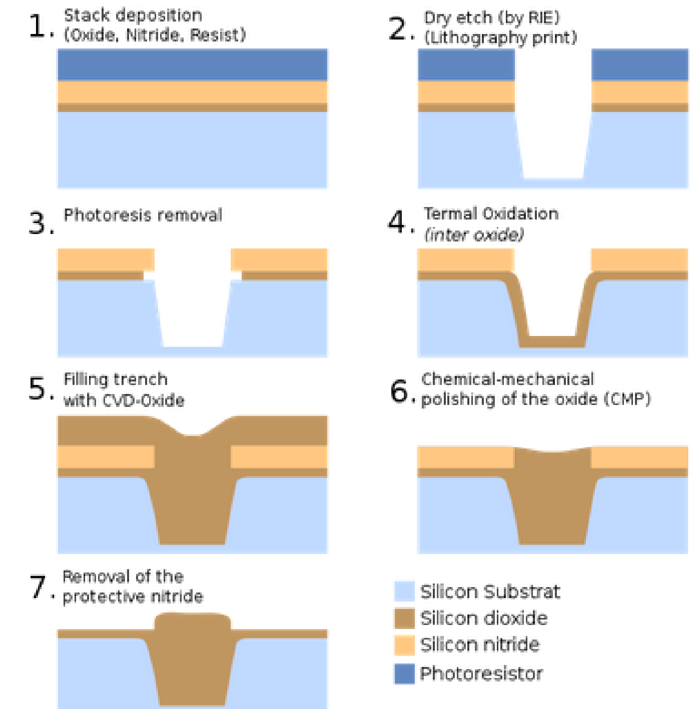
- **STI** (Shallow Trench Isolation) process: (<250 nm)

  CVD oxide is deposited in the etched region: reduced Si area loss



LOCOS process

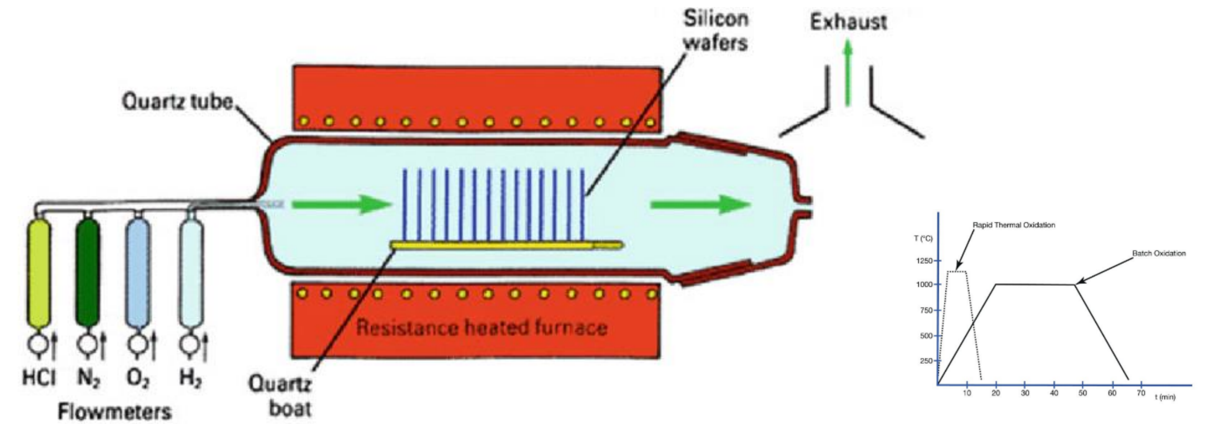
STI process



Oxidation process tools

- **Thermal oxidation:**
  oxide is grown at high temperature (~ 1000° C) by supplying oxygen that reacts with silicon wafer to form SiO_2 at the surface

- Wafers inserted on a suspended boat into a tubular reactor of quartz, heated by resistance



Dry oxidation: best quality, slow (10 nm/hr)

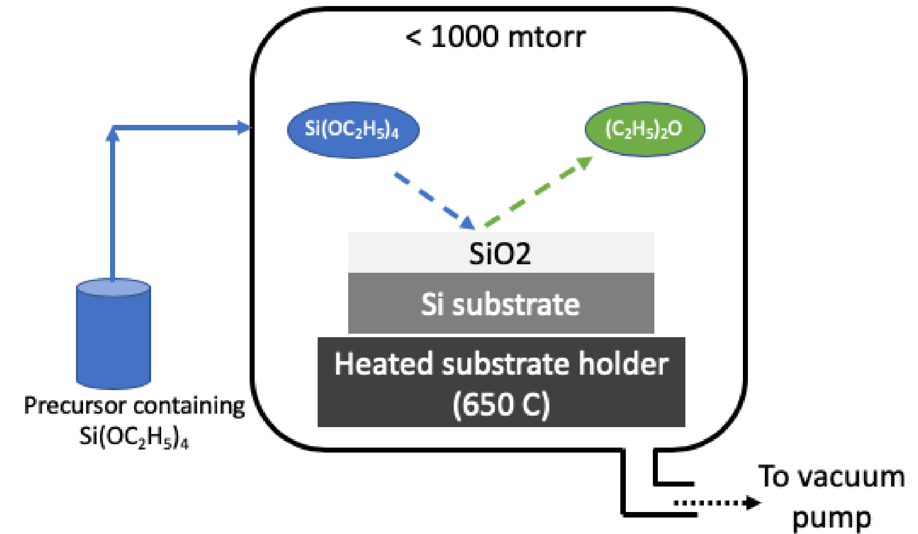
Wet oxidation: lower quality, faster (>x10)

Oxidation process tools

- **Chemical Vapor Deposition (CVD) :** reaction of vapor phase chemicals containing the material to deposit form the solid film on substrate. Reactant gases decompose and form the film.

  - SiO_2 growth rate >x10 compared to thermal oxide, but lower quality

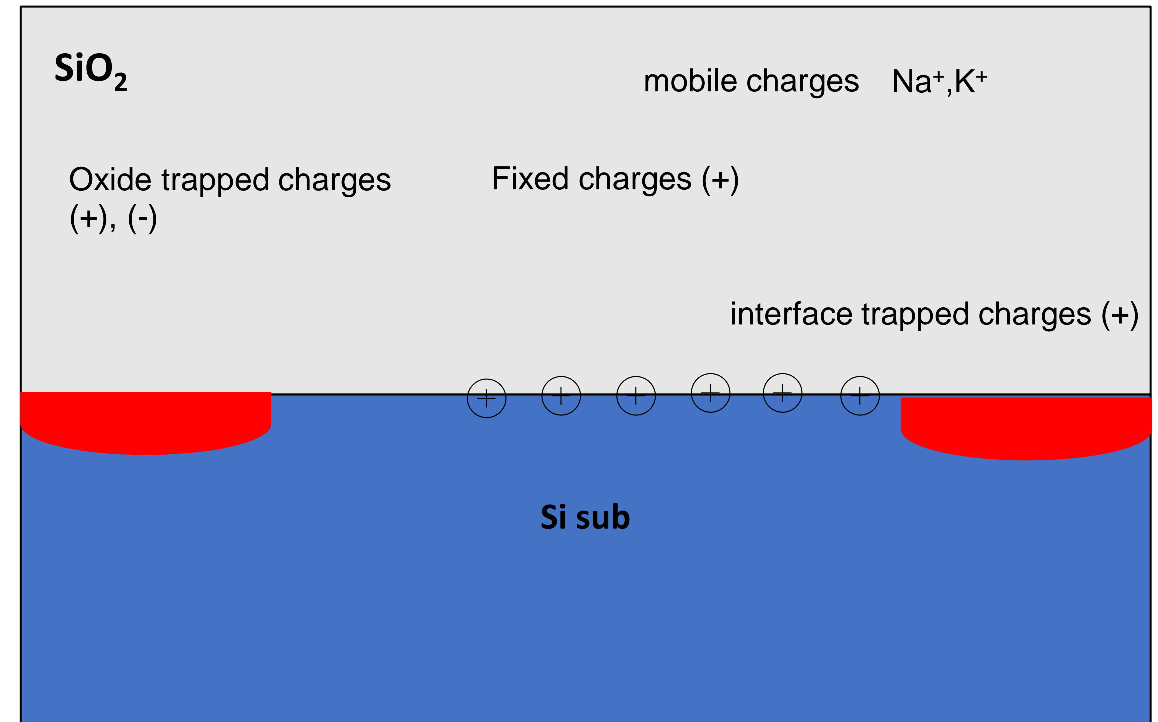
  - CVD is also used for growing dielectric materials of different electrical permittivity (high k/low k material)



Chemical reactions	Techniques
$SiH_4 + O_2 \xrightarrow{430\ °C,\ 1\ bar} SiO_2 + 2H_2$	Silane oxide CVD
$SiH_4 + O_2 \xrightarrow{430\ °C,\ 40\ bar} SiO_2 + 2H_2$	LTO CVD
$SiH_2Cl_2 + 2N_2O \xrightarrow{900\ °C,\ 40\ Pa} SiO_2 + Gas$	HTO CVD
$Si(OC_2H_5)_4 \xrightarrow{700\ °C,\ 40\ bar} SiO_2 + Gas$	TEOS CVD
$Si(OC_2H_5)_4 + O_2 \xrightarrow{400\ °C,\ 0.5\ bar} SiO_2 + Gas$	ACVD
$SiH_4 + 4N_2O \xrightarrow{350\ °C,\ Plasma\ 40\ Pa} SiO_2 + Gas$	PECVD

Oxide quality

- Mobile charges (contamination - make insulator conductive)
- Fixed charges (incompletely oxidized Si - create an extra electric field affecting the devices in Si)
- Oxide trapped charge (broken Si-O bonds, due to radiation)
- Interface trapped charges (dangling bonds – affect mobility and increase noise)



The Deal-Grove oxidation model

- The Deal Grove Model is a simple kinetic model for oxide thermal growth, wet and dry
- Developed by Andy Grove (Intel's CEO) and Bruce Deal in the 60's

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General Relationship for the Thermal Oxidation of Silicon

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(Received 10 May 1965; in final form 9 September 1965)

The thermal-oxidation kinetics of silicon are examined in detail. Based on a simple model of oxidation which takes into account the reactions occurring at the two boundaries of the oxide layer as well as the diffusion process, the general relationship $x_0^2+Ax_0=B(t+\tau)$ is derived. This relationship is shown to be in excellent agreement with oxidation data obtained over a wide range of temperature (700°–1300°C), partial pressure (0.1–1.0 atm) and oxide thickness (300–20 000 Å) for both oxygen and water oxidants. The parameters A, B, and τ are shown to be related to the physico-chemical constants of the oxidation reaction in the predicted manner. Such detailed analysis also leads to further information regarding the nature of the transported species as well as space-charge effects on the initial phase of oxidation.

1. INTRODUCTION

Owing to its great importance in planar silicon-device technology, the formation of silicon dioxide layers by thermal oxidation of single-crystal silicon has been studied very extensively in the past several years.[1–15] Now, with the availability of large amounts of experimental data, it appears that there is much contradiction and many peculiarities in the store of knowledge of silicon oxidation. For instance, reported activation energies of rate constants vary between 27 and 100 kcal/mole for oxidation in dry oxygen; pressure dependence of rate constants has been reported as linear as well as logarithmic. While most of the data on silicon oxidation have been evaluated using the parabolic rate law, certain authors have taken recourse to using empirical power-law dependence,[14] $x_0^n=kt$, where both n and k were complex functions of temperature, pressure, and oxide thickness.

The problems associated with the latter approach can be illustrated by considering Figs 1 and 2. These figures contain a summary of data obtained in these laboratories which are in good general agreement with the corresponding data of Fuller and Strieter[14] and of Evitts, Cooper, and Flaschen.[13] (The experimental methods are dealt with in detail later.) The plots are logarithm of oxide thickness vs the logarithm of oxidation time for dry and wet oxygen (95°C H_2O) at various temperatures. The slope of the lines corresponds to the exponent n in the above power law. These values are indicated at the limiting position of some of the curves. In the case of wet oxygen (Fig. 1), n ranges from 2 for thicker oxides at 1200°C to 1 for the thinner oxide region of the 920°C data. However, for dry oxygen (Fig. 2), the value of n at 1200° approaches 2 as the oxide thickness increases above 1.0 μ; but at lower temperatures and oxide thicknesses the value of n decreases only to about 1.5 and then appears to increase again. Obviously the data cannot be represented by a simple power law.

Most of the previous theoretical treatments of the kinetics of the oxidation of metals emphasize only two limiting types of oxidation mechanisms.[16] In one, the

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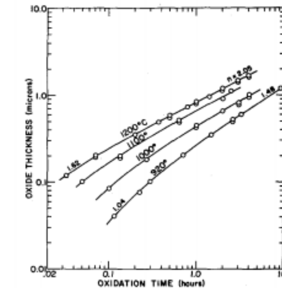
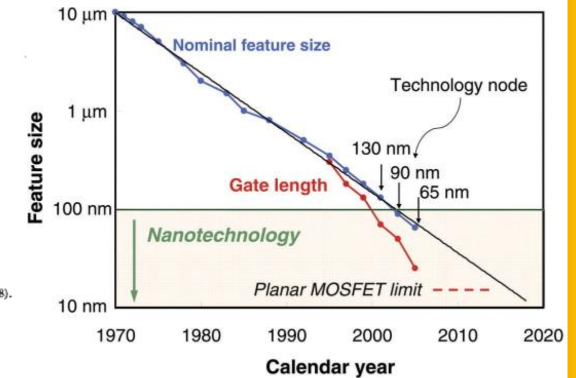


Fig. 1. Oxidation of silicon in wet oxygen (95°C H_2O).

[16] N. Cabrera and N. F. Mott, Rept. Progr. Phys. **12**, 163 (1948).



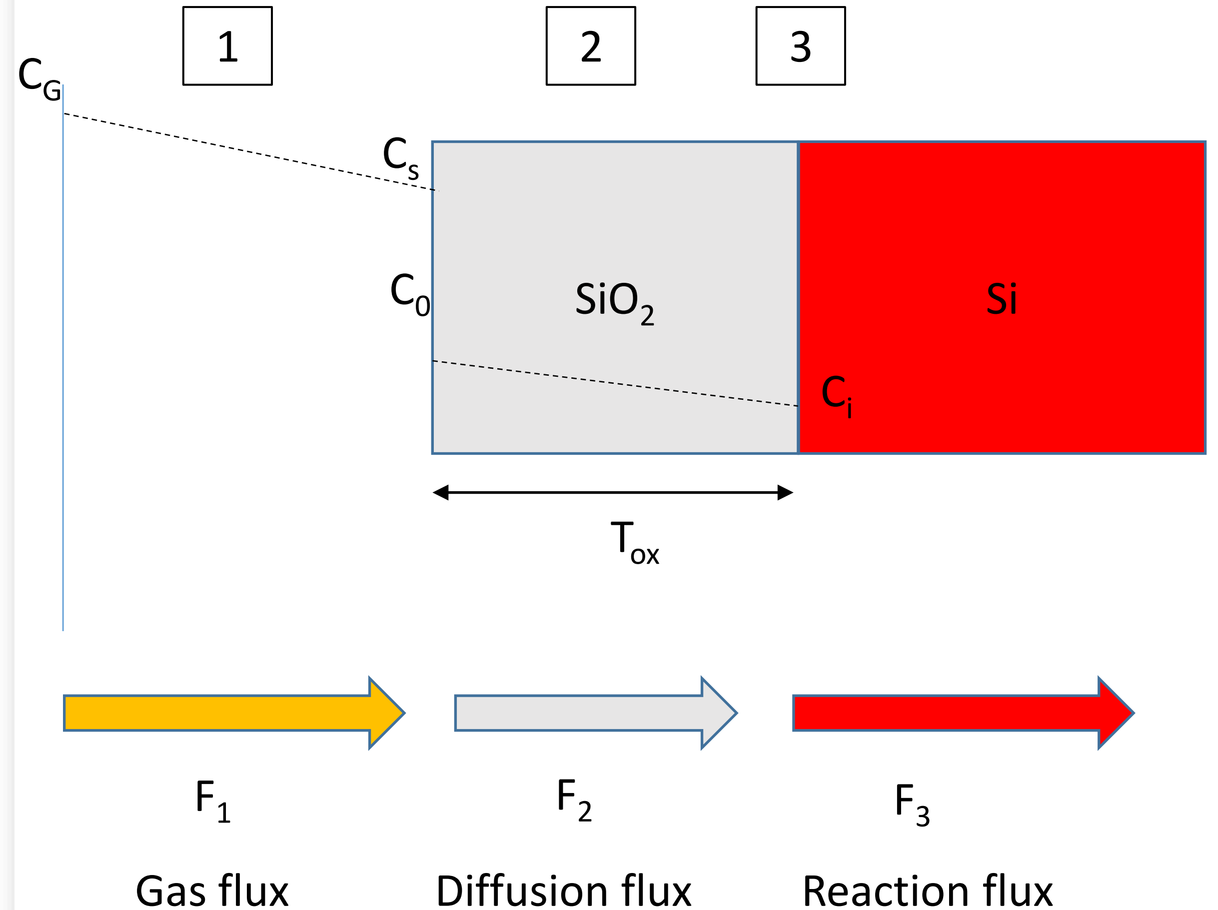
B. E. DEAL AND A. S. GROVE General Relationship for the Thermal Oxidation of Silicon, JOURNAL OF APPLIED PHYSICS VOLUME 36. NUMBER 12 DECEMBER 1965

The Deal-Grove oxidation model

1: Oxygen diffuses from bulk C_G to wafer surface C_S

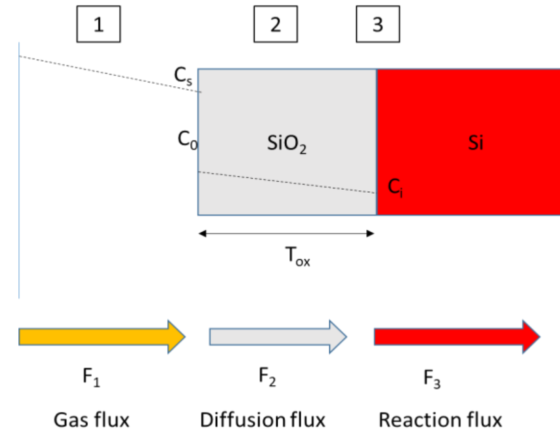
2: Oxygen diffuses from wafer surface C_O to Si surface C_i

3: Oxygen reacts with Si at interface to form SiO_2



The Deal-Grove oxidation model

- Oxygen diffusion through gas: Fick's 1st Law approximated as linear equation
- Adsorbed concentration C_o on surface ∝ partial pressure (Henry's Law)
- Oxygen diffusion through SiO_2 Fick's 1st Law approximated as linear equation
- 1st order reaction at Si interface



$$\mathbf{1}:\ F_1 = D\frac{dC}{dx} \approx \frac{D_g}{\delta}(C_g - C_s) = h_g(C_g - C_s)$$

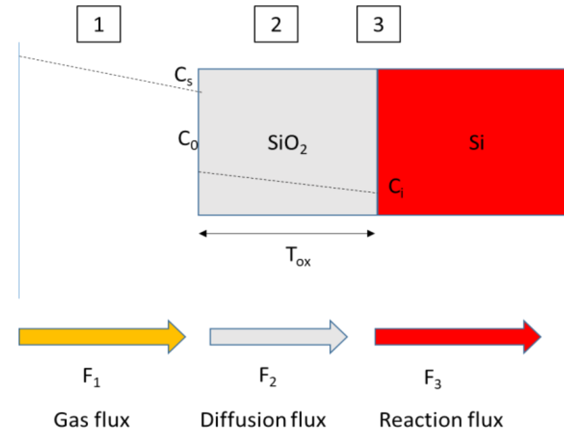
$$C_o = HP_s = HC_s kT$$

$$\mathbf{2}:\ F_2 = D\frac{dC}{dx} \approx \frac{D_{ox}}{t_{ox}}(C_o - C_i)$$

$$\mathbf{3}:\ F_3 = k_s C_i$$

$C_g = \frac{P_g}{kT}$	Reactant concentration
H	Henry's gas law coefficient
t_{ox}	SiO2 thickness
D_{ox}	Oxygen diffusivity in SiO2
h_g	Mass transfer coefficient

The Deal-Grove oxidation model



- Steady state: all fluxes are equal (Si interface reaction is the rate-limiting step)

$$F_1 = F_2 = F_3 = F_{OX}$$

$$F_{OX} = \frac{Hk_sP_g}{1+\frac{k_s}{h}+\frac{k_s t_{ox}}{D_{ox}}} = \frac{dt_{ox}}{dt} N_{ox} \qquad ; h = \frac{h_g}{HkT}$$

- Oxygen flux $F_{OX} = v_{ox} N_{ox}$

$$\frac{dt_{ox}}{dt} = \frac{Hk_sP_g}{1+\frac{k_s}{h}+\frac{k_s t_{ox}}{D_{ox}}} \frac{1}{N_{ox}}$$

The Deal-Grove oxidation model

- Integrating over t gives the expression for t_{ox} vs. time
- The model requires coefficients adjustments for different crystal orientations

$$t_{ox}^2 + At_{ox} = B(t+\tau)$$

$$A = 2D_{ox}\left(\frac{1}{h}+\frac{1}{k_s}\right)$$

$$B = \left(\frac{2D_{ox}HP_g}{N_{ox}}\right)$$

$$\tau = \left(\frac{t_0^2 + At_0}{B}\right)$$

Table 4.1 Oxidation coefficients for silicon

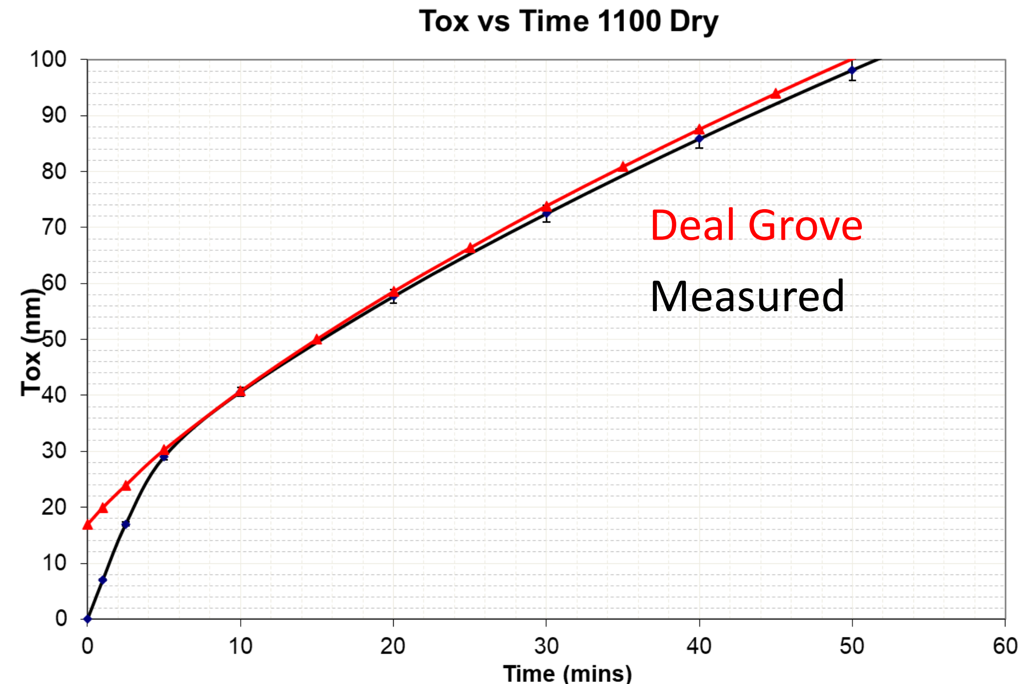
Temperature (°C)	Dry A (μm)	Dry B (μm²/hr)	Dry τ (hr)	Wet (640 torr) A (μm)	Wet (640 torr) B (μm²/hr)
800	0.370	0.0011	9	—	—
920	0.235	0.0049	1.4	0.50	0.203
1000	0.165	0.0117	0.37	0.226	0.287
1100	0.090	0.027	0.076	0.11	0.510
1200	0.040	0.045	0.027	0.05	0.720

The τ parameter is used to compensate for the rapid growth regime for thin oxides. *(After Deal and Grove.)*

<111> Si

The Deal-Grove oxidation model

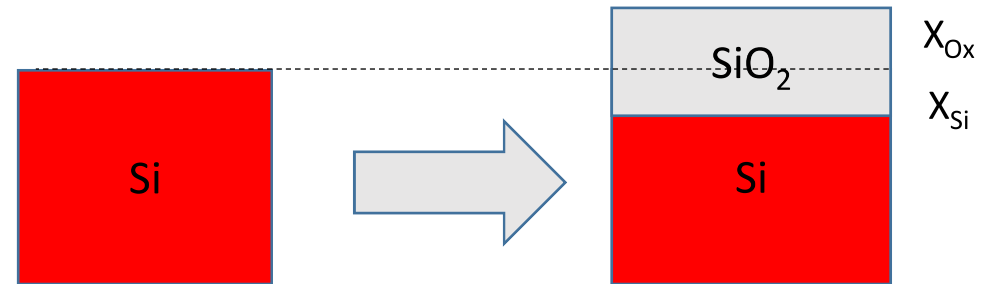
- Comparison of Deal-Grove model with <u>measured</u> oxide thickness (Dry oxide)
- With the correct coefficients (P,T, crystal) the Deal-Grove model works nicely for single crystal silicon (~%'s accuracy). Model extensions to 3D exist
- Additional tweaking needed for high doping Si
- The model fails for Polysilicon



* Self-limiting growth of native oxide saturates at around 2-3 nm
'**Growth of native oxide on a silicon surface'** Journal of Applied Physics, Volume 68, Issue 3, August 1, 1990, pp.1272-1281

The Deal-Grove oxidation model

- The oxide grows at the expense of Silicon: during oxidation around half of Silicon is consumed



$$X_{Si}\ N_{Si} = X_{Ox}\ N_{Ox} \rightarrow X_{Si} = \frac{X_{Ox}\ N_{Ox}}{N_{Si}} \equiv X_{Ox} \frac{2.3\ 10^{22}}{5\ 10^{22}} = X_{Ox}\ 0.46$$

$N_{Ox} = molecular\ density\ SiO_2$
$N_{Si} = atomic\ density\ Si$

Process fabrication III Summary

Thank you

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- Introduction to Semiconductor technology
- Differences between Moore's (economic) and Dennard's (physics) law, miniaturization and Power wall

- Process fabrication I, Introduction and typical process flow
- Silicon wafer
- Oxidation: purpose, tools. Modeling (Deal-Groove)