Transistor layout: 250 – 28 nm, FinFETs

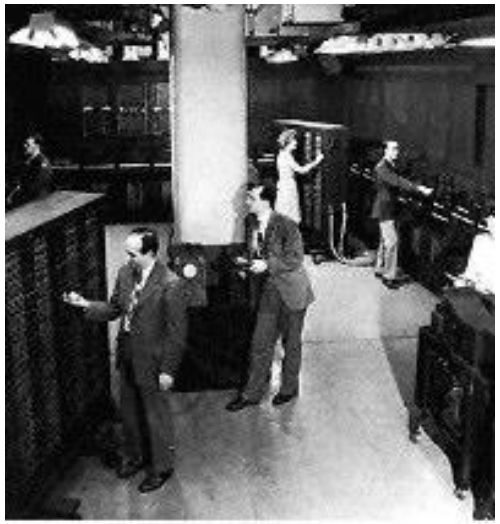
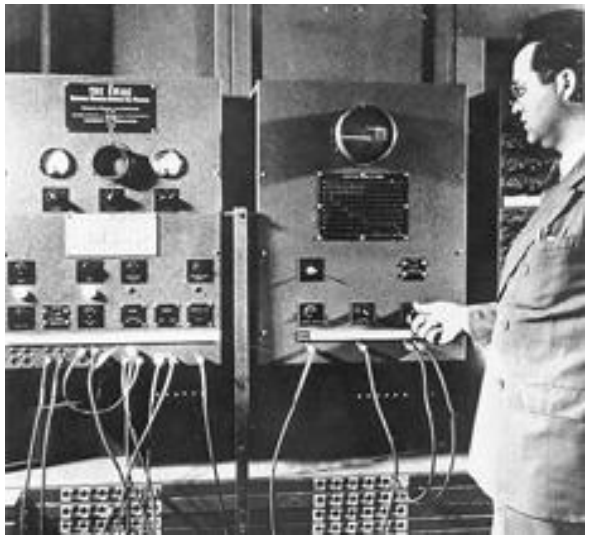
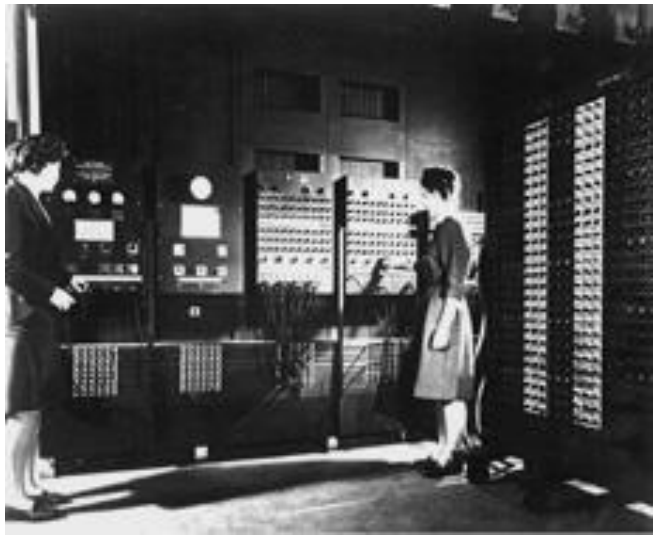
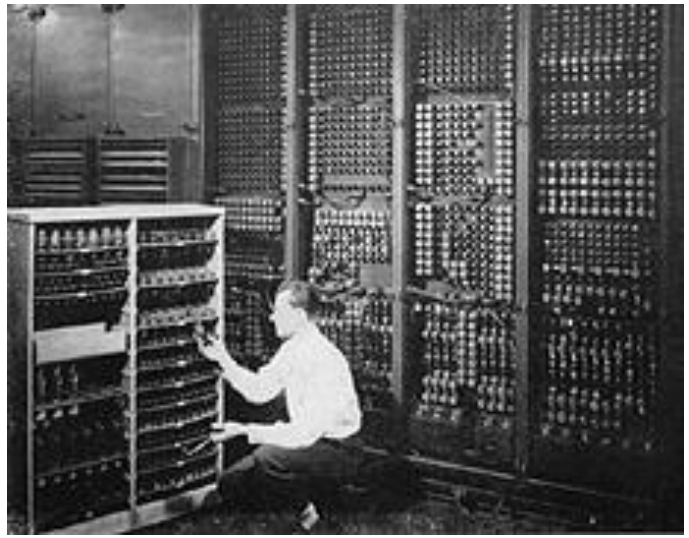
Eva Vilella

University of Liverpool

vilella@hep.ph.liv.ac.uk

ENIAC (1946 – 1954)

ELECTRONIC NUMERICAL INTEGRATOR AND COMPUTER

- 17,468 vacuum valves
- 27,000 Kg
- 450 m^3
- 174 kW

- It had extremely high costs

Birth of Microelectronics

1947

is considered the date of birth of Microelectronics

W. Shockley

J. Bardeen

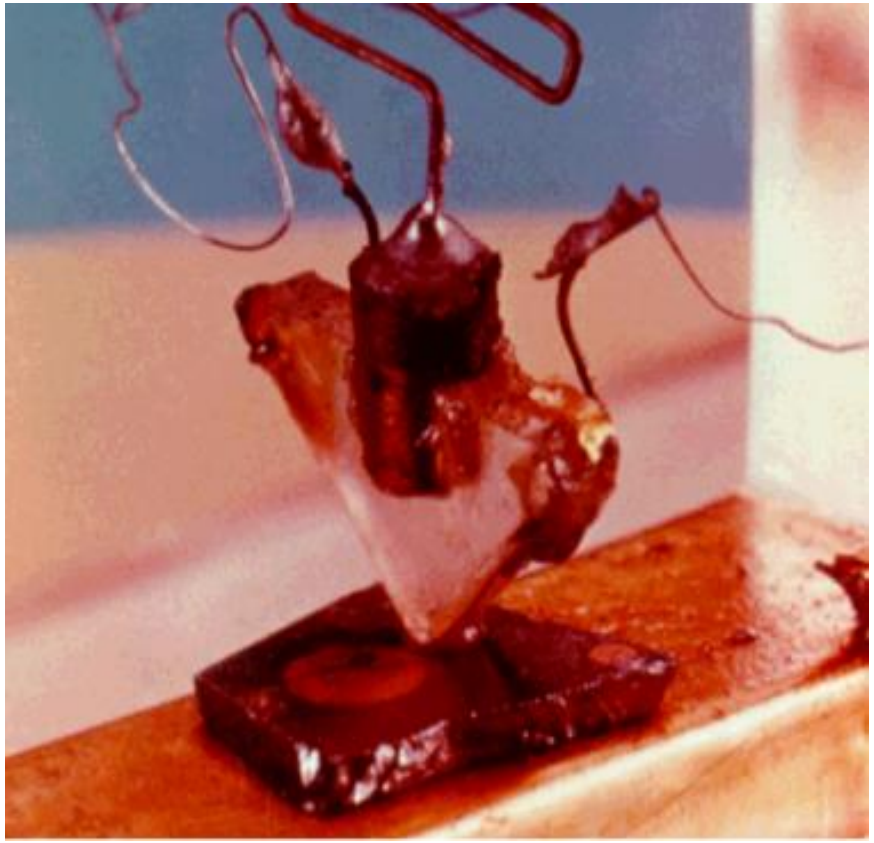
W. Brattain

They discovered the transistor effect in Germanium

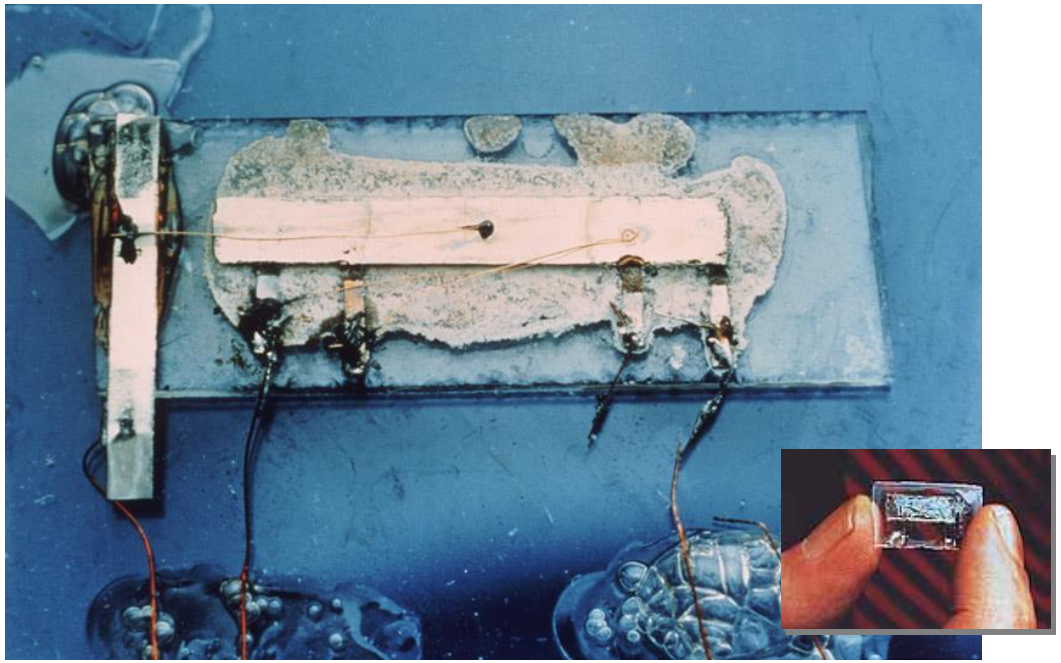
They invented the Bipolar Junction Transistor (BJT)

First transistor

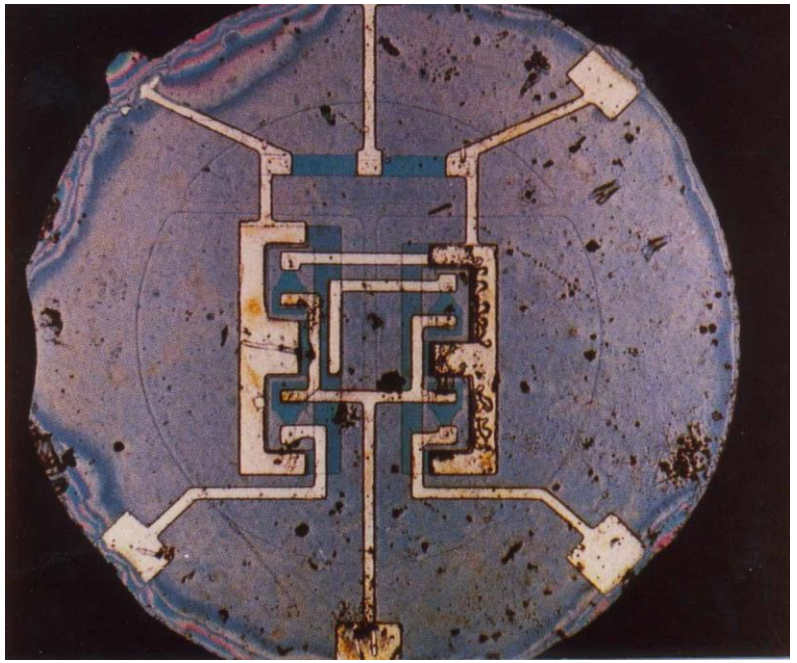
- Original device
  - Bipolar transistor
  - Germanium N
  - 3 electrodes
  - 2 contacts metal-semiconductor like those used for rectifiers and another large area at the base



Integrated circuit



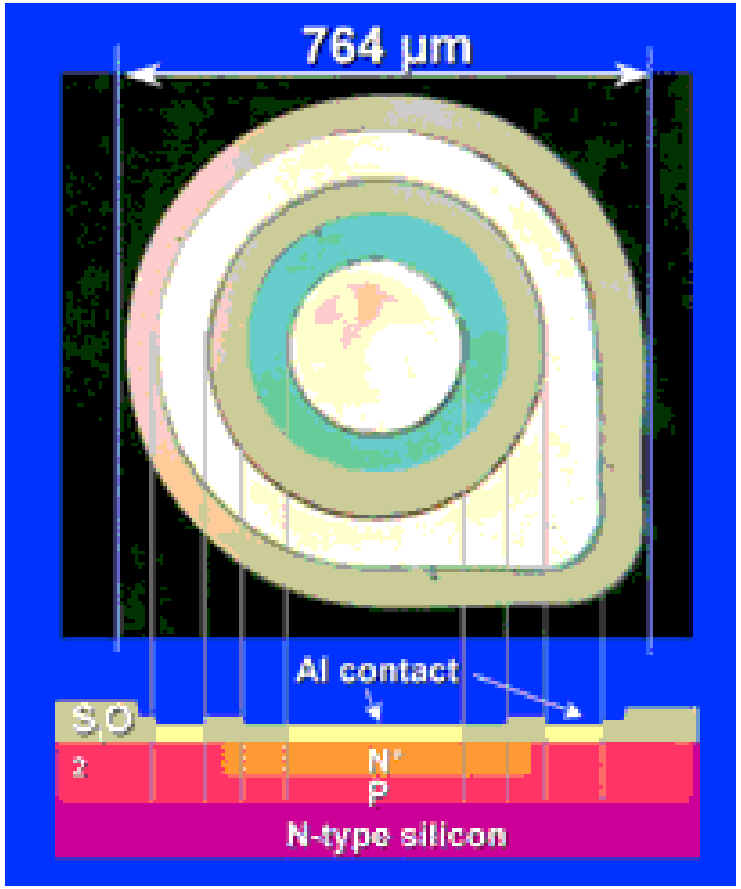
- J. Kilby, Texas Instruments, 1958
- Circuit with transistors connected by metallic wires (by hand)



- R. N. Noyce, Fairchild Semiconductors, 1959
- First monolithic integrated circuit with devices isolated by reverse biased PN junctions and interconnected with aluminium lines

Planar technology – 1958

- Process to produce a large number of devices simultaneously on a wafer
  - Diffusion, oxidation, deposition, photolithography
- Reduced cost
- Birth of Silicon Valley
  - Fairchild Semiconductors (1957)
  - Intel (1970)
  - …

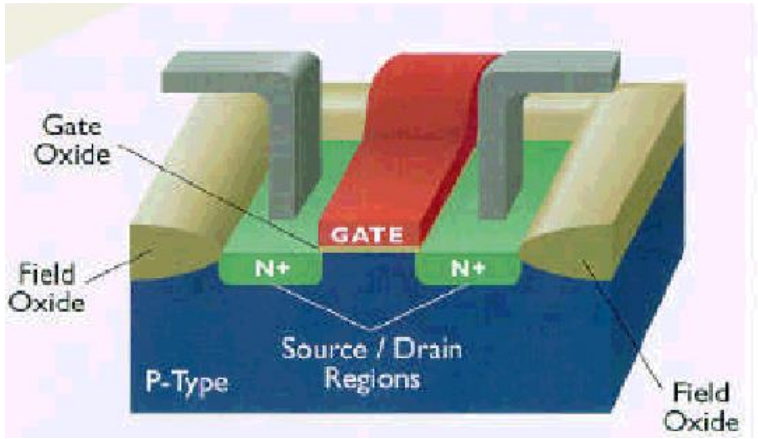


First applications

- 1961 – Fairchild Micrologic devices were designed into the AC Spark Plug MAGIC and Martin MARTAC 420 computers, but NASA's Apollo Guidance Computer (AGC) was the most significant early project. Designed by MIT in 1962 and built by Raytheon, each system used about 4,000 "Type-G" (3-input NOR gate) circuits. Consuming 200,000 units at $20-30 each, the AGC was the largest user of ICs through 1965.
- 1962 – Texas Instruments won a contract from the Autonetics Division of North American Aviation to design 22 custom circuits for the Minuteman II missile guidance system.
  - The Minuteman project by 1965 overtook NASA's Apollo procurement as the largest single consumer of integrated circuits.

MOS transistors

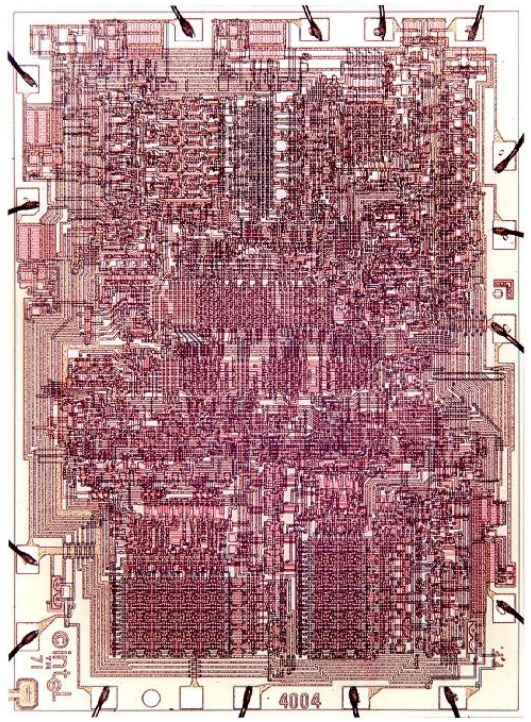
- Many failed attempts at achieving a field effect device system
  - A capacitor-type device to modulate the carrier concentration in a semiconductor
  - The problem was the existence of too many shallow states, which prevented an electric field on the surface of the semiconductor
  - SiO_2 reduces the concentration of shallow states
- 1960 – M. M. Atalla and D. Khang fabricate the first MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor)
- Comparison MOSFET - bipolar
  - Less power consumption to control the same current
  - Less area
  - Allows for larger complexity
  - Slower

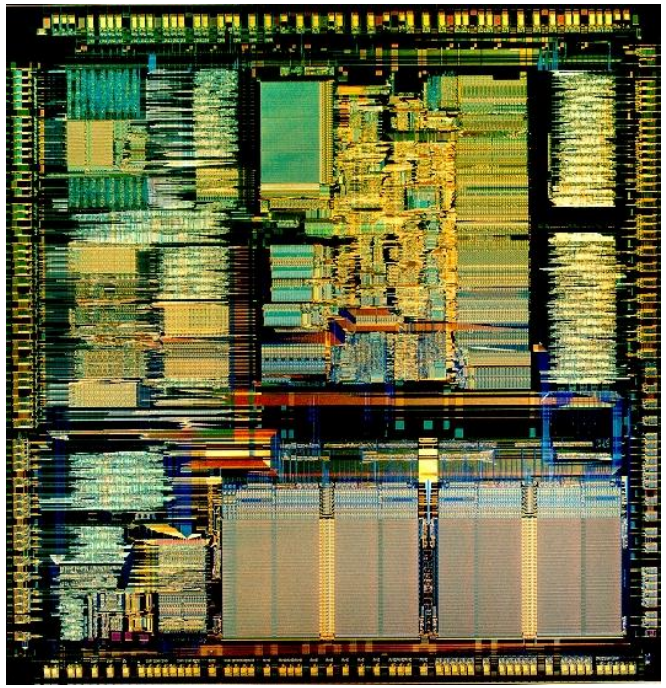


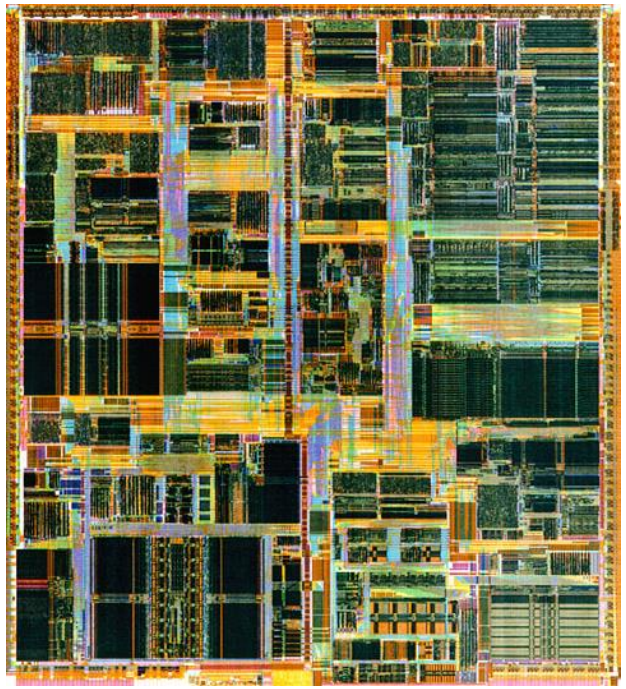
Microprocessors and memories

- MOSFETs offered large potential
- 1970 – R. Noyce, G. Moore and A. Grove left Fairchild and started Intel
  - 1970 – They presented the first semiconductor chip (a memory)
    - 1k DRAM
    - Basic cell consisted of 3 transistors
    - pMOS technology only
  - 1971 – F. Faggin and E. Hoff, from Intel, fabricated the first 4004 microprocessor
    - 4 bits
    - 45 instructions
    - pMOS technology only
    - 3.6 mm x 2.8 mm
    - 2,3000 transistors
  - (4004 microprocessor + memory + I/O chip + clock = computer)

Evolution of microprocessors







Pictures not to scale

First μP 4004 (1971)
2,300 gates

μP 80386 (1984)
275,000 gates

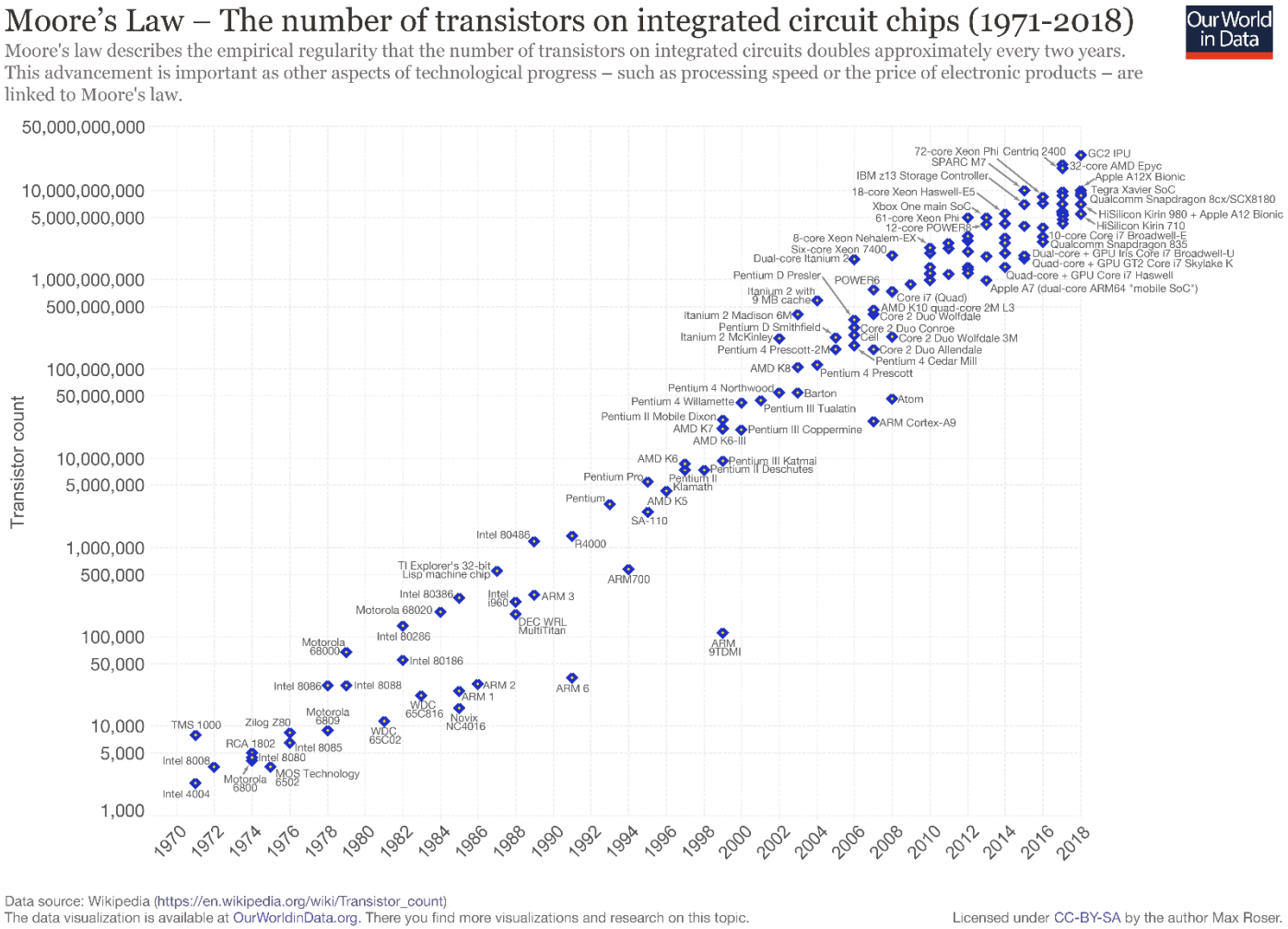
μP Pentium III (1999)
9,500,000 gates

The invention of the integrated circuit was a revolution as humankind discovered the technology to produce electronic circuits in mass volumes

Evolution

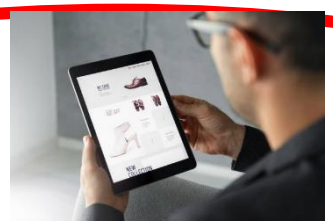
- Race to increase the complexity of integrated circuits since the 1970s
  - Faster microprocessors
  - More complex memories

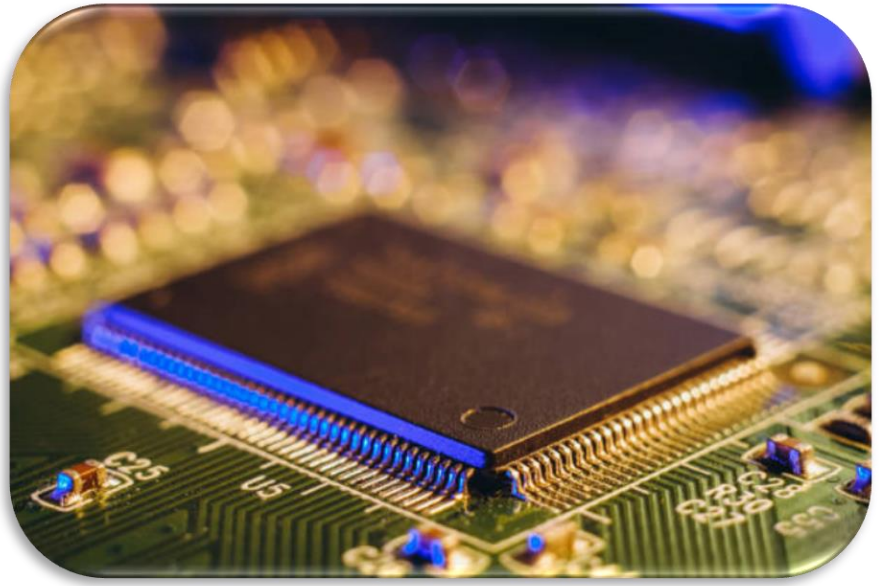
Moore's law (1965) → The number of transistors in a dense integrated circuit (IC) doubles about every two years

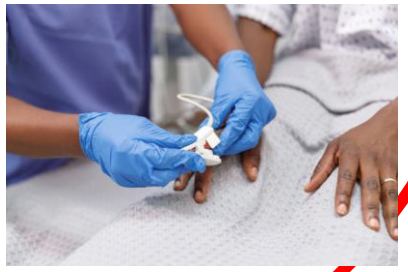


Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Today's applications







Device structure

MOSFET = Metal-Oxide-Semiconductor Field-Effect Transistor

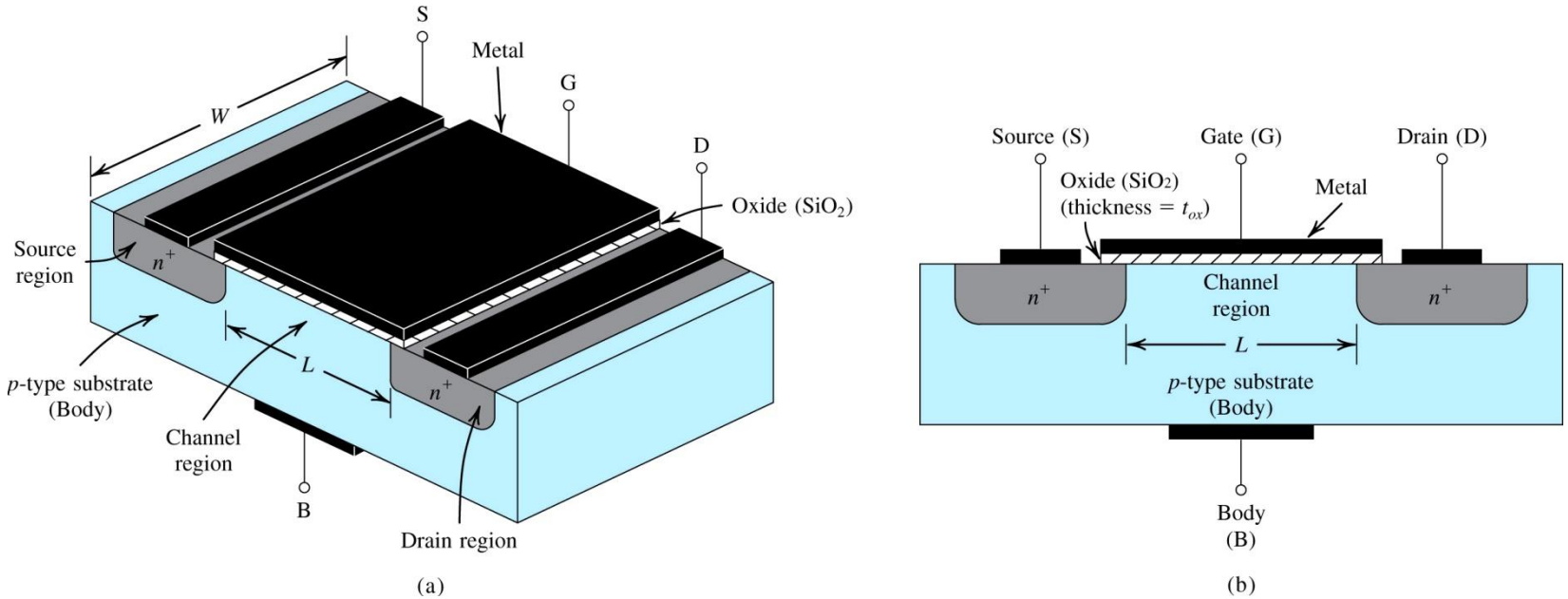


Figure 1: Physical structure of an NMOS transistor: **(a)** perspective view, **(b)** cross-section.

Device structure

two *n*-type doped regions (drain, source)

layer of SiO_2 separates source and drain

metal, placed on top of SiO_2, forms gate electrode

one *p*-type doped region

MOSFET = Metal-Oxide-Semiconductor Field Effect Transistor

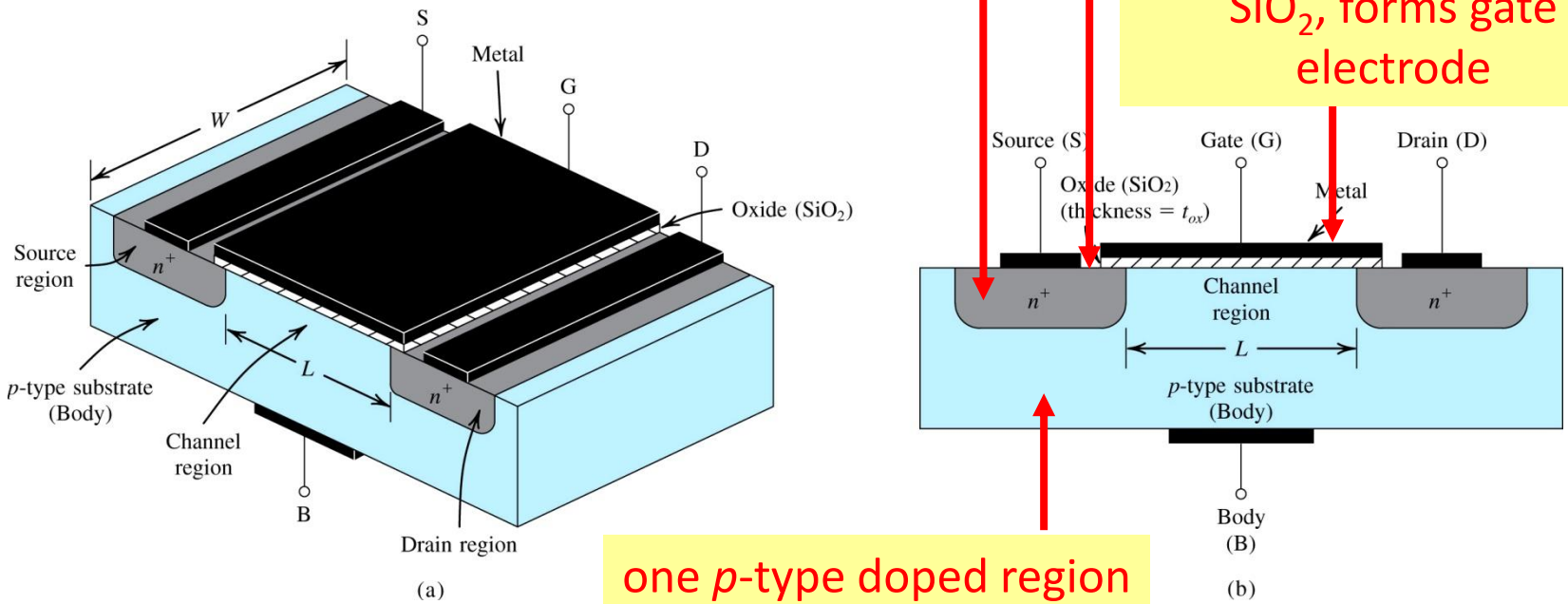
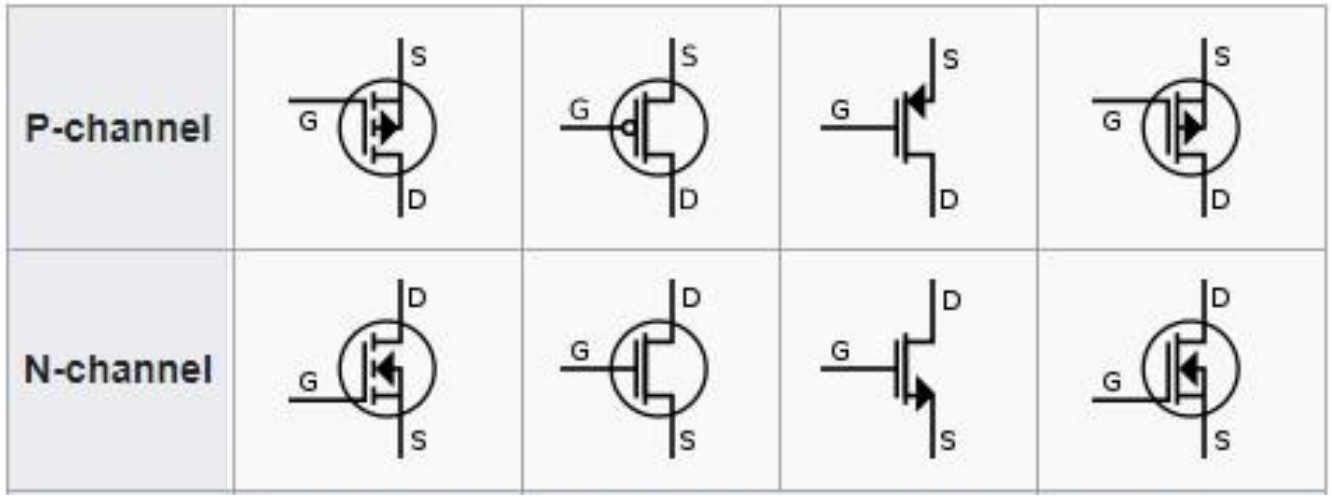


Figure 1: Physical structure of an NMOS transistor: **(a)** perspective view, **(b)** cross-section.

Symbols

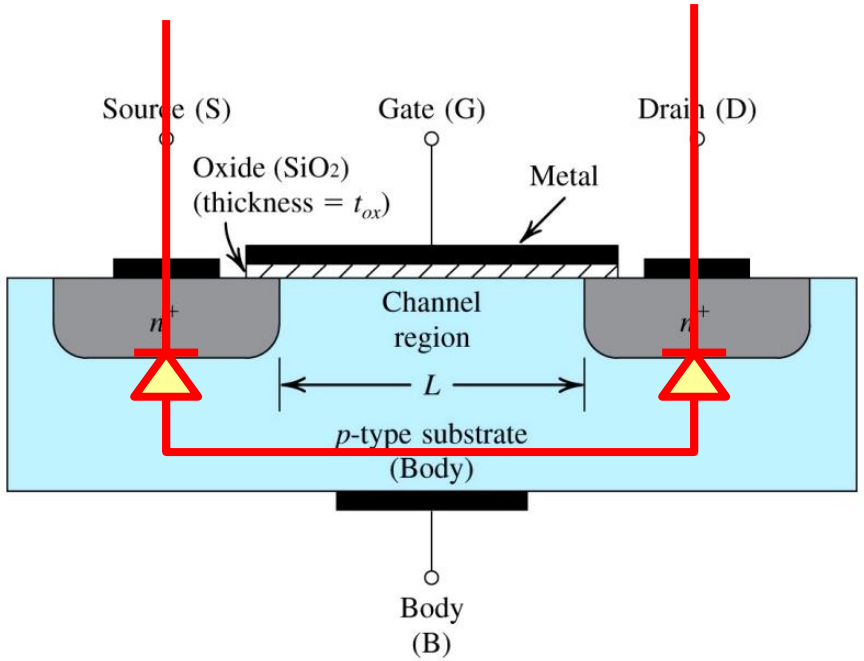


There are four terminals:

drain (D), gate (G), bulk (B), and source (S).

Operation

- **Zero Gate Voltage**
  - With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
  - "They" prevent current conduction from drain to source when a voltage v_{DS} is applied.
  - Yielding very high resistance ($10^{12} ohms$)



Physical structure of MOSFET

Operation

- **Creating a Channel for Current flow**
  - **Q:** What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate?
  - **step #1:** v_{GS} is applied to the gate terminal, causing a positive build up of positive charge along metal electrode.
  - **step #2:** This "build up" causes free holes to be repelled from region of *p*-type substrate under gate.

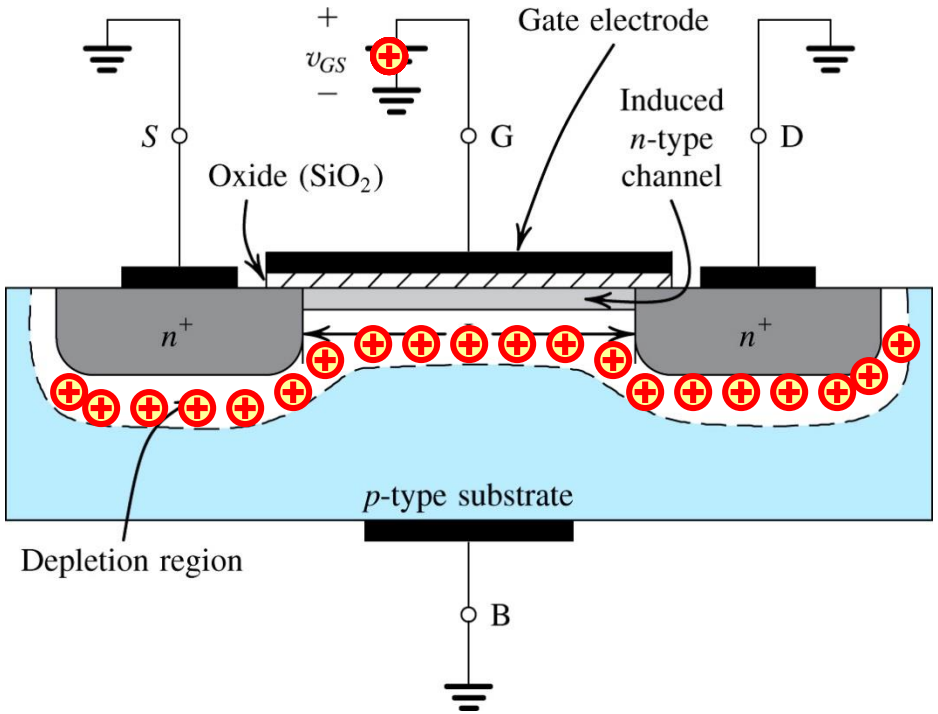


Figure 2: NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Operation

- **Creating a Channel for Current flow**
  - **Q:** What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate? Refer to figure to right.
  - **step #3:** This "migration" results in the uncovering of negative **bound charges**, originally neutralized by the free holes
  - **step #4:** The positive gate voltage also attracts electrons from the n^+ source and drain regions into the channel.

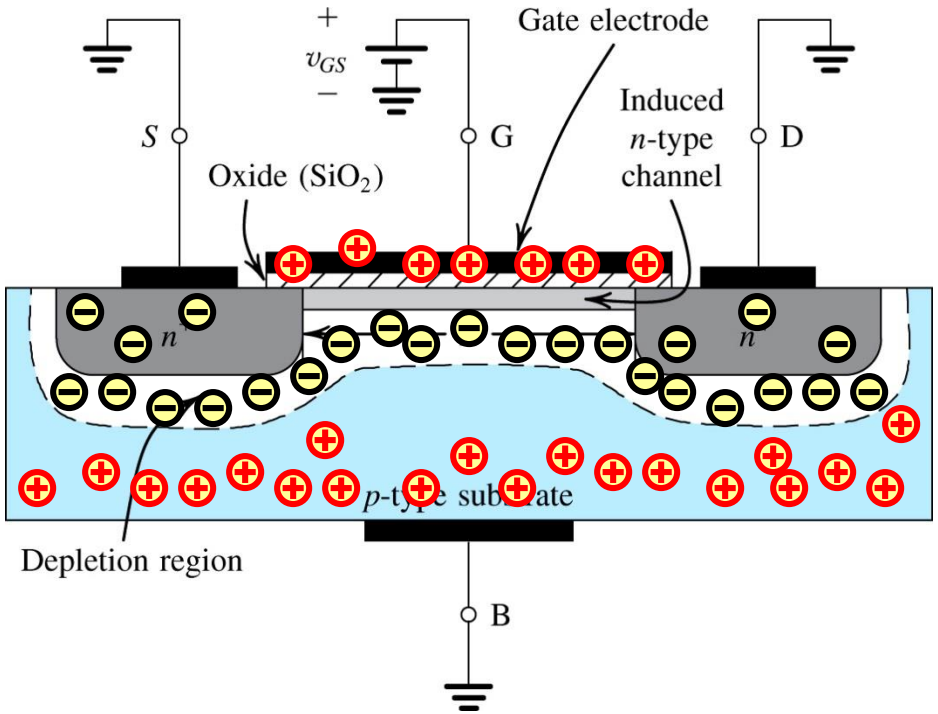


Figure 2: NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Operation

- **Creating a Channel for Current flow**
  - **Q:** What happens if (1) source and drain are grounded and (2) positive voltage is applied to gate?
  - **step #5:** Once a sufficient number of "these" electrons accumulate, an *n*-region is created…
    …connecting the source and drain regions
  - **step #6:** This provides path for current flow between *D* and *S.*

this induced channel is also known as an **inversion layer**

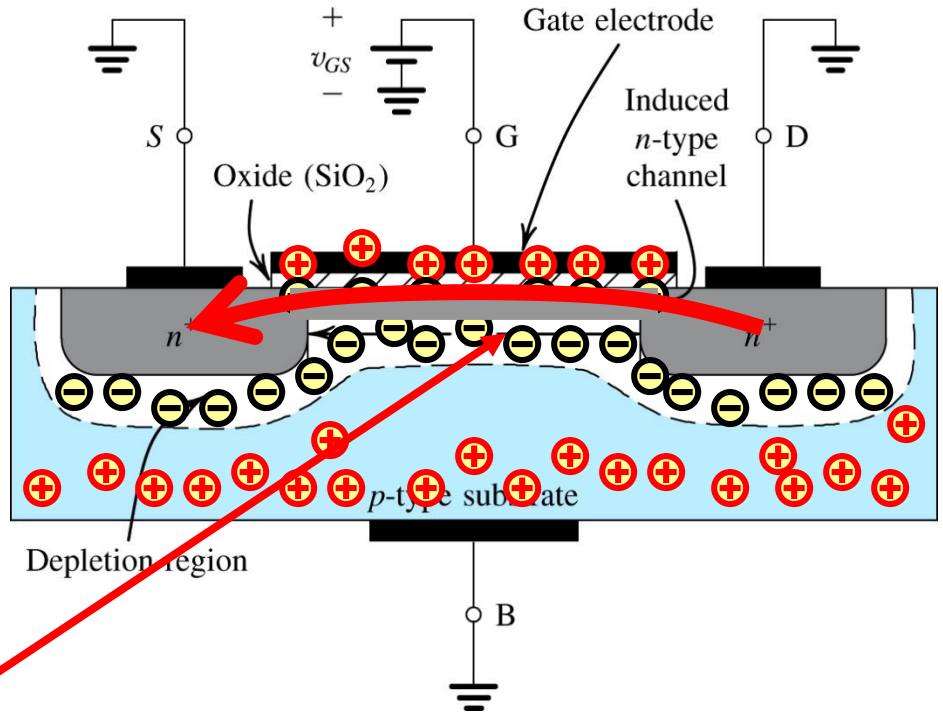
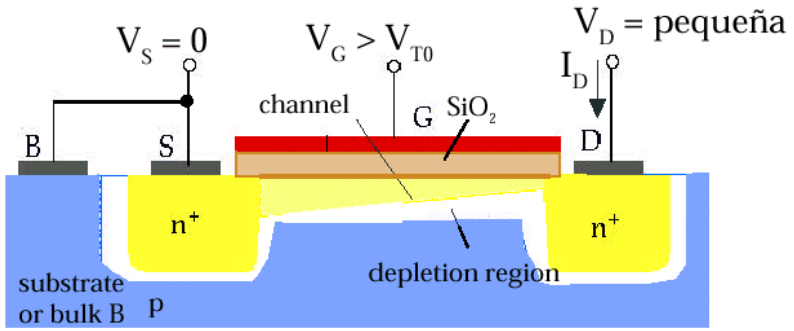
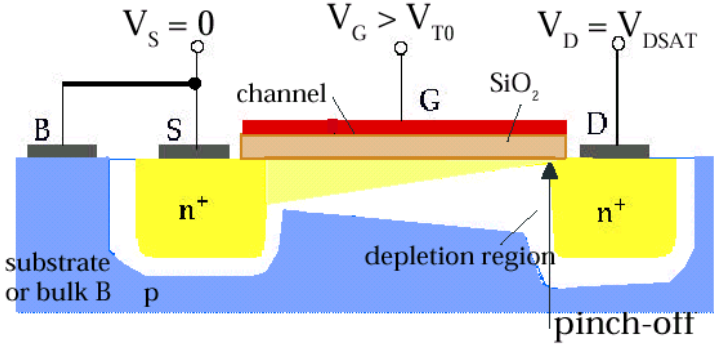
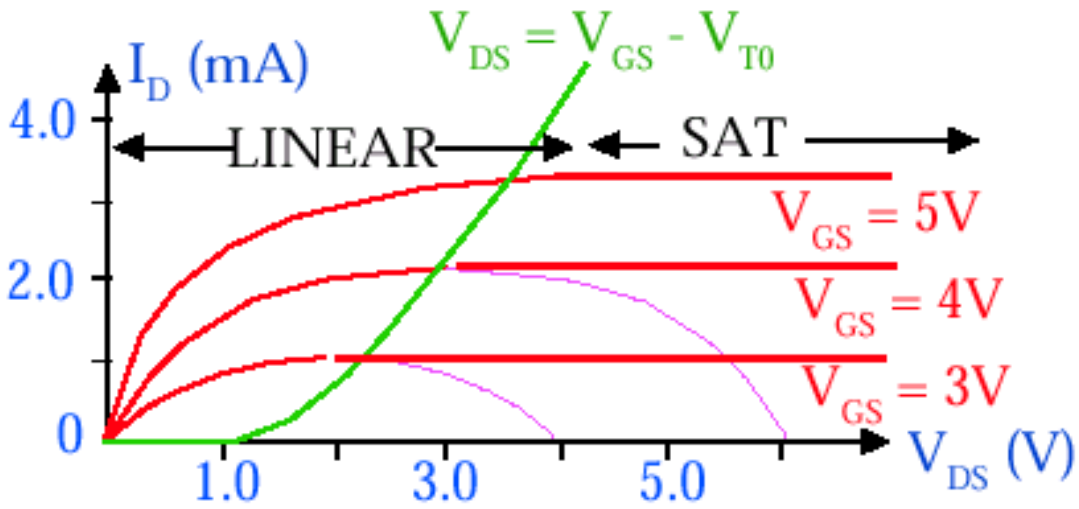


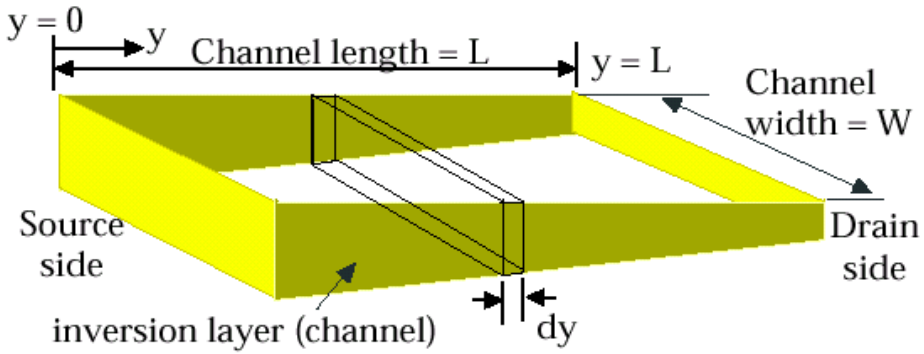
Figure 2: NMOS transistor with a positive voltage applied to the gate. An *n* channel is induced at the top of the substrate beneath the gate.

Operation





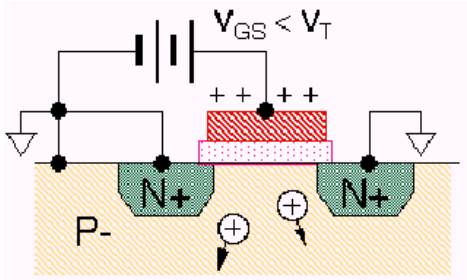


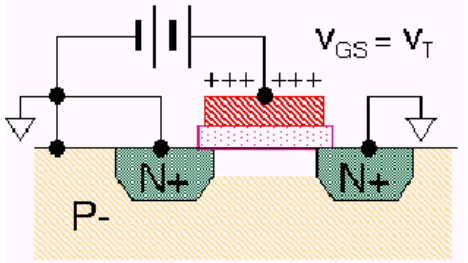


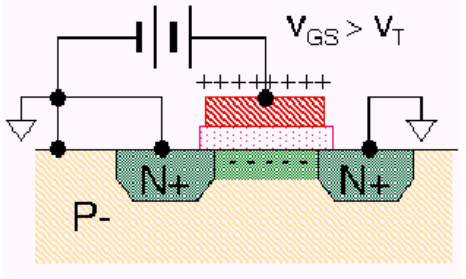
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS} - V_{T0})V_{DS} - V_{DS}^2]$$

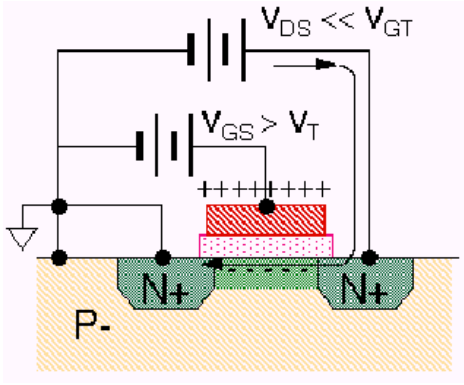
$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{T0})^2$$

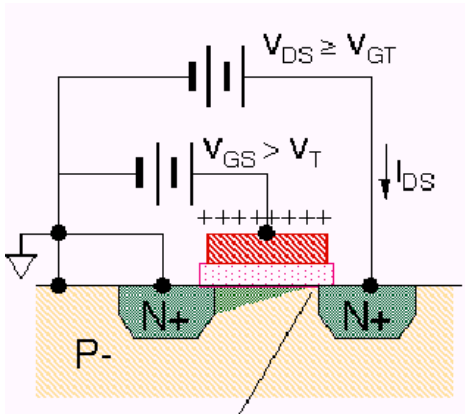
Operation











Cut-off region

$V_{GS} < V_T$

Linear region

$V_{DS} \leq V_{GS} - V_T$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} [2(V_{GS} - V_{T0}) V_{DS} - V_{DS}^2]$$

$$I_D = k'_n \, W/L \, [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2]$$

Transconductance

$k'_n = \mu_n C_{ox} = \mu_n \varepsilon_{ox}/t_{ox}$

$k_n = k'_n \, W/L$

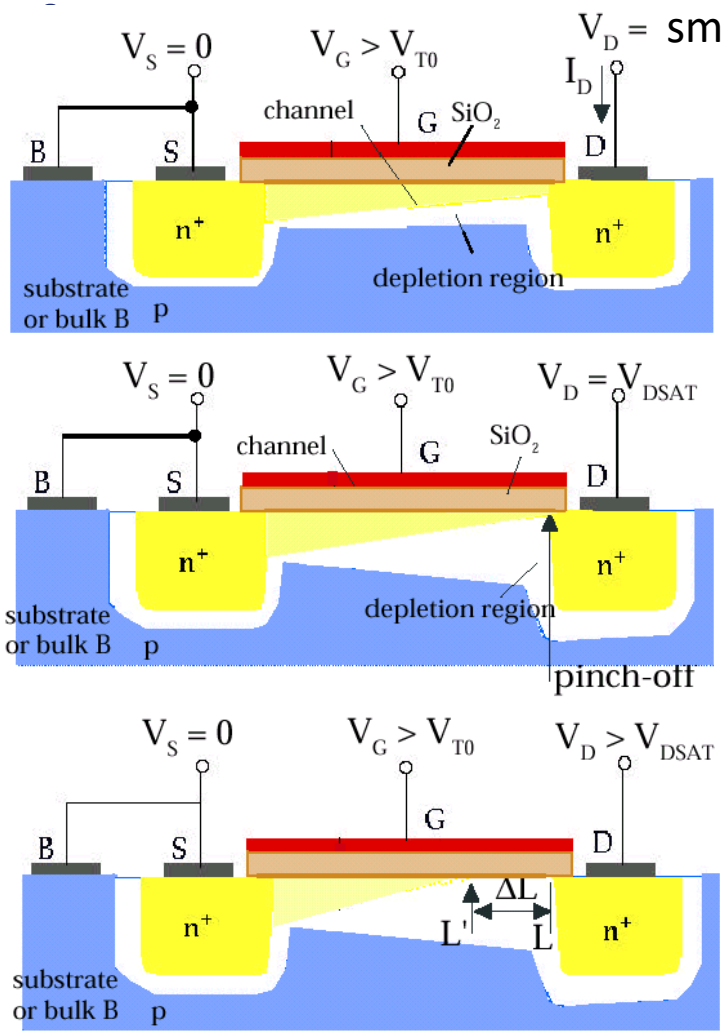
Saturation region

$V_{DS} \geq V_{GS} - V_T$

$$I_D(sat) = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{T0})^2$$

$$I_D = k'_n/2 \, W/L \, [(V_{GS} - V_T)^2]$$

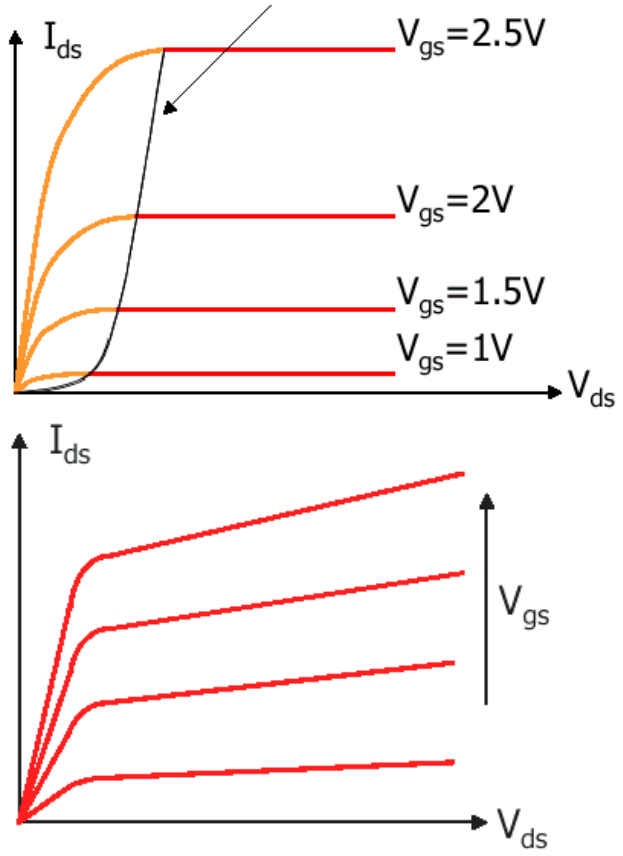
Opera



$$I_D = k'_n/2\ W/L\ [(V_{GS} - V_T)^2]$$

$$I_D' = I_D(1 + \lambda V_{DS})$$

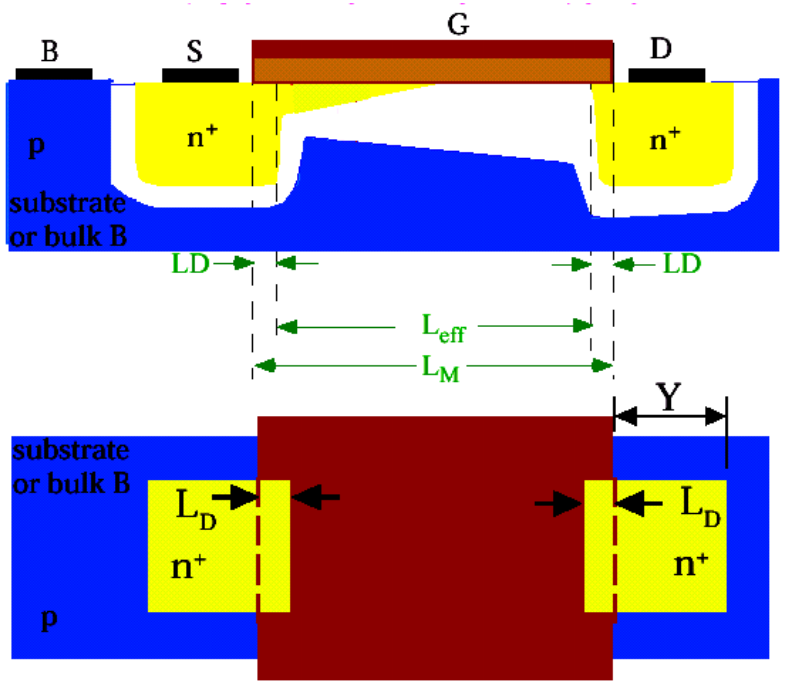
Saturation

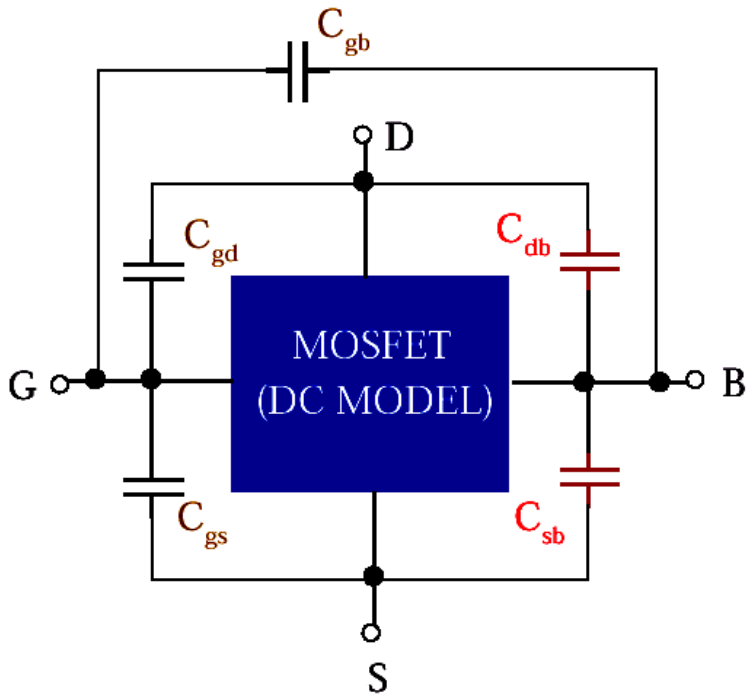


λ Channel length modulation

$$I_D(sat) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

Capacitances





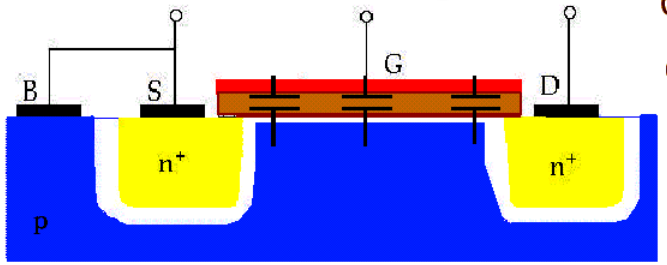
C_{gd}, C_{gs}, C_{gb} -> Oxide capacitances

C_{db}, C_{sb} -> Junction capacitances

Capacitances

b. Gate - Channel

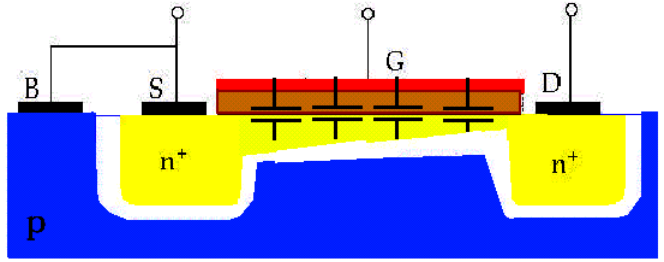
MOSFET - Cut-off Region



$C_{gb} = C_{ox} W L$

$C_{gs} = C_{gd} = 0$

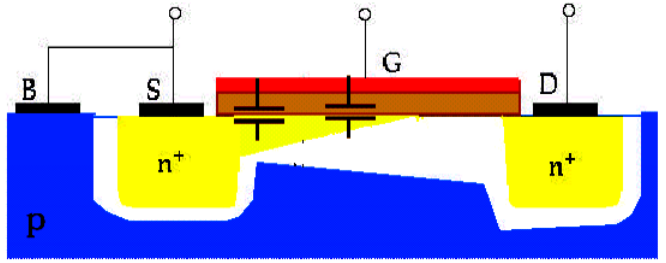
MOSFET - Linear Region



$C_{gb} = 0$

$C_{gs} = (1/2)\, C_{ox} W L$

$C_{gd} = (1/2)\, C_{ox} W L$

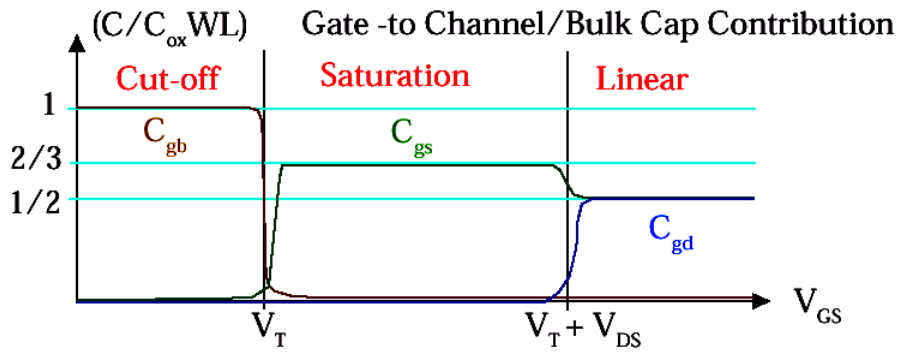


$C_{gb} = 0$

$C_{gs} = (2/3)\, C_{ox} W L$

$C_{gd} = 0$

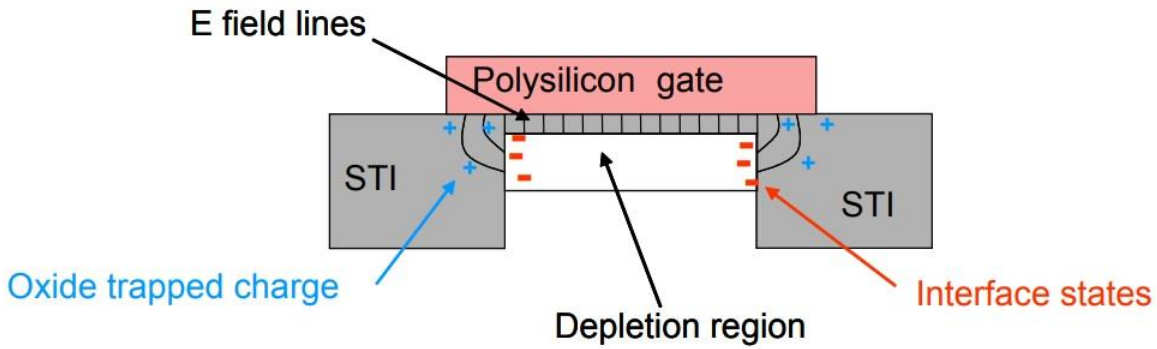
Capacitance	Cut-off	Linear	Saturation
C_{gb}(total)	$C_{ox}WL$	0	0
C_{gd}(total)	$0 + C_{ox}WL_D$	$0.5C_{ox}WL + C_{ox}WL_D$	$0 + C_{ox}WL_D$
C_{gs}(total)	$0 + C_{ox}WL_D$	$0.5C_{ox}WL + C_{ox}WL_D$	$(2/3)C_{ox}WL + C_{ox}WL_D$

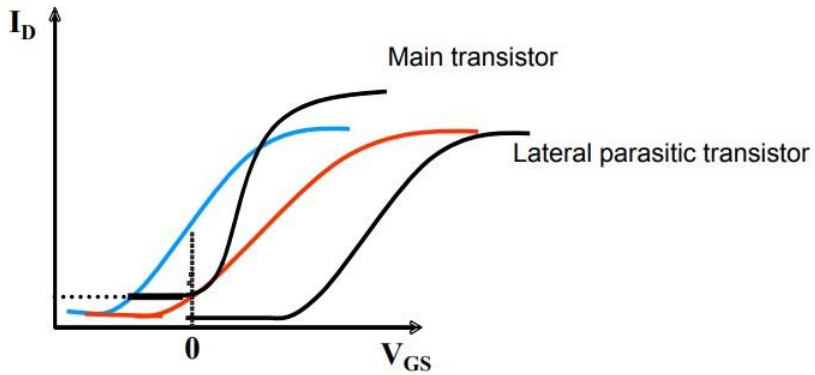


TID effects – Consequences – Leakage current

- **Increase of leakage current**

The leakage current in NMOS is due to the accumulation of defects in the lateral Shallow Trench Isolation (STI) oxide

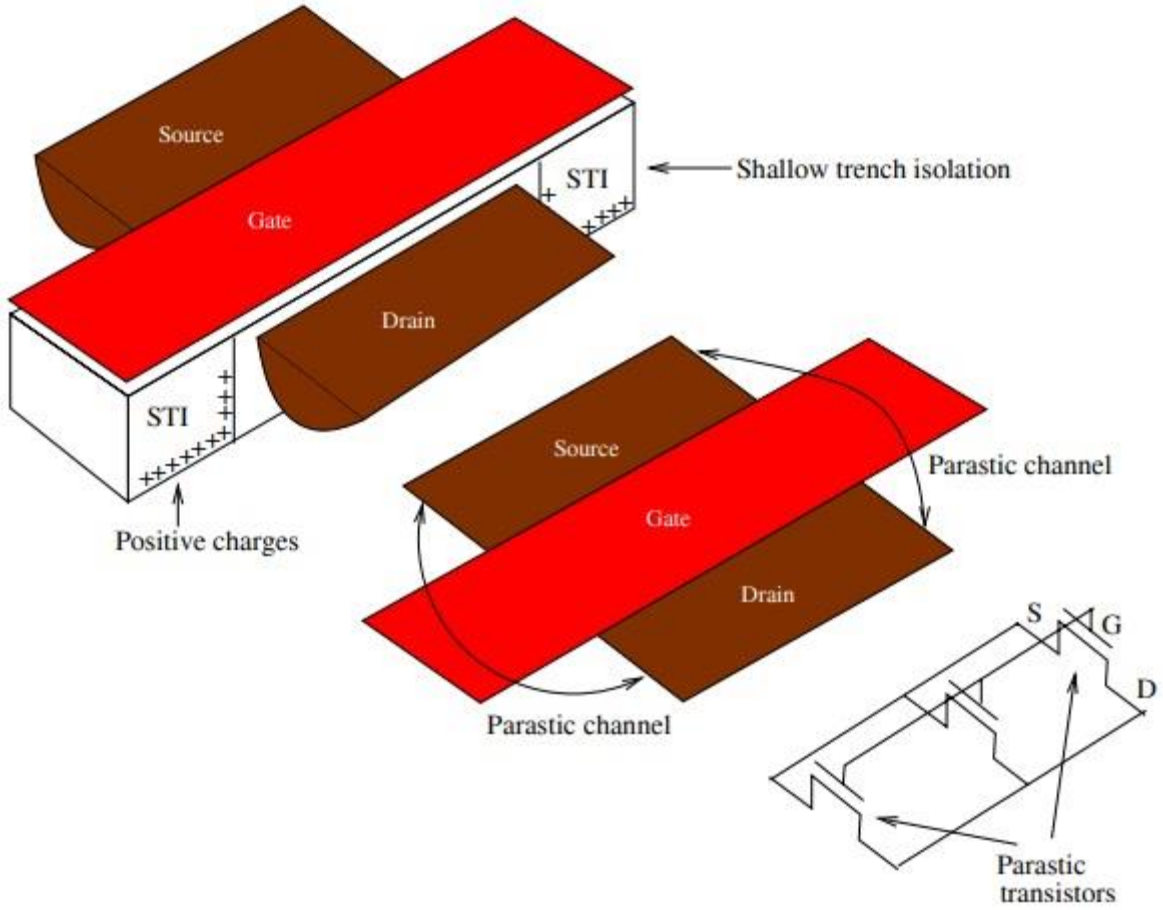




F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

TID effects – Consequences – Leakage current

- **Increase of leakage current**



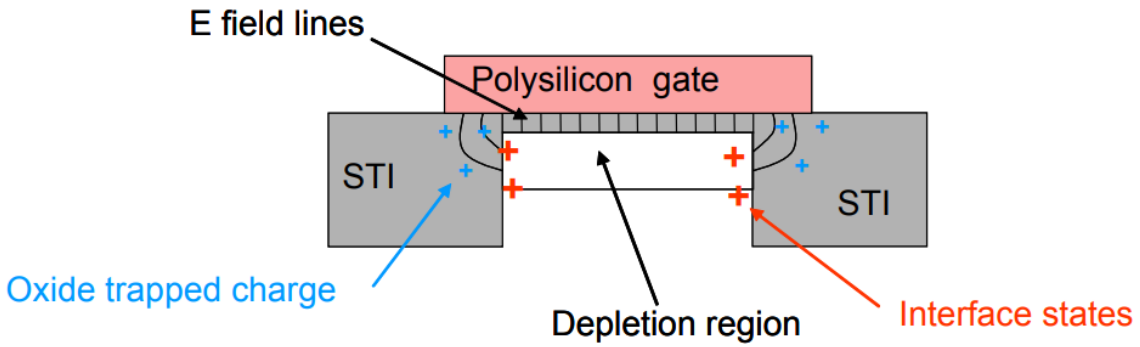
Leakage current also appears between adjacent n-type diffusions

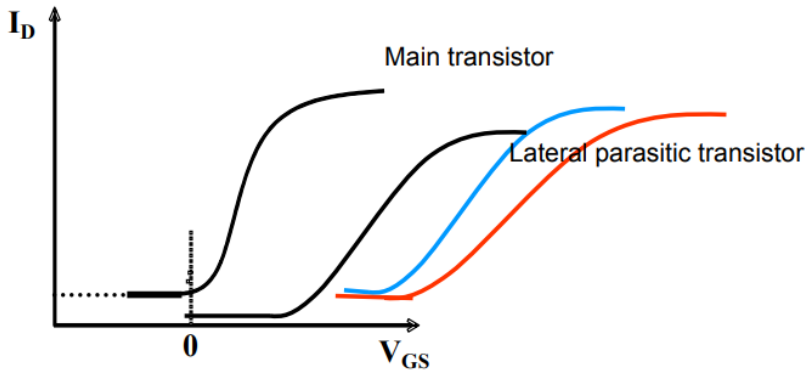
L. Chen, Radiation tolerant design with 0.18-micron CMOS technology, PhD thesis

TID effects – Consequences – Leakage current

- **Increase of leakage current**

In PMOS both type of defects increase the threshold of the parasitic lateral transistor, and no leakage current can be observed

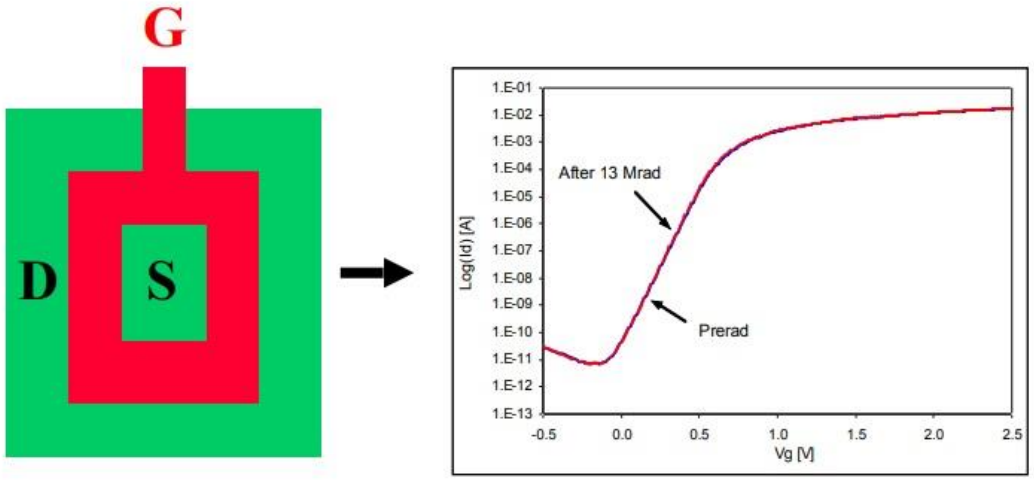




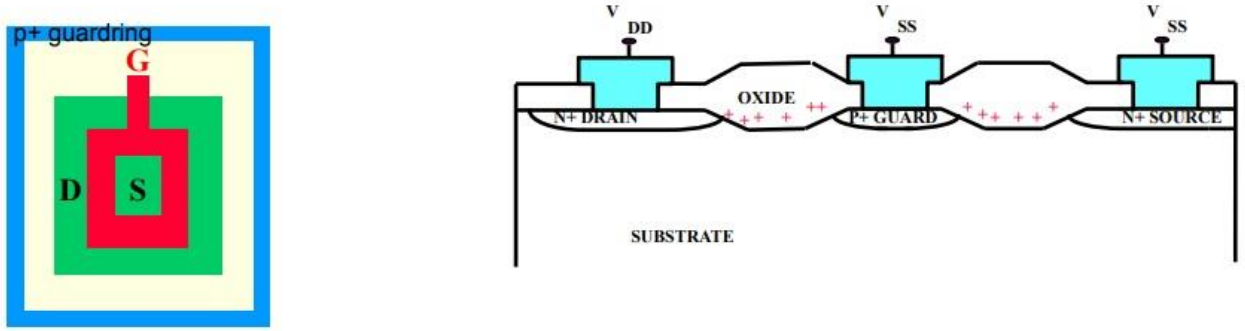
F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

Enclosed Layout Transistors

Source-Drain leakage is eliminated by the Enclosed Layout Transistor (ELT)…



Inter-diffusion leakage is eliminated by p+ guard rings…

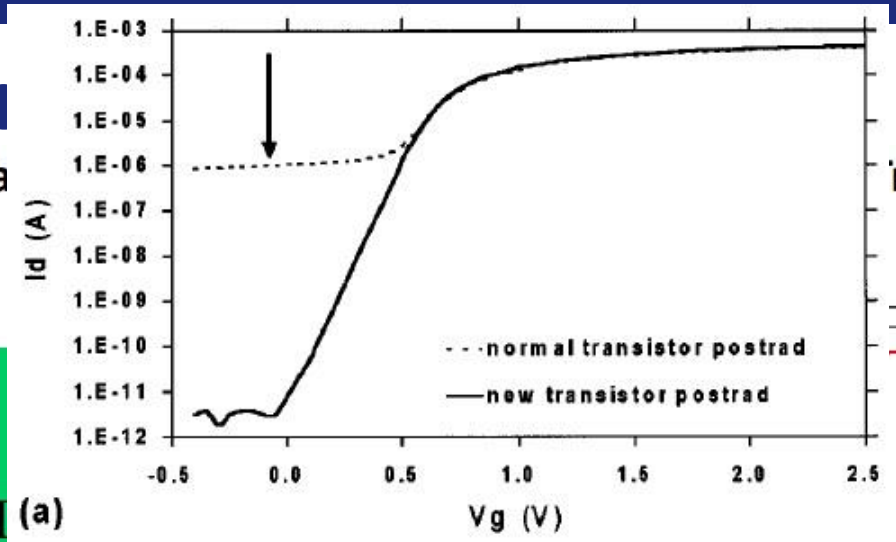


F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

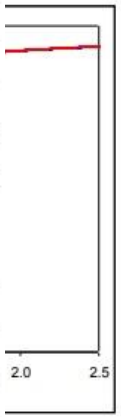
Enclosed Layout Tr

Source-Drain lea

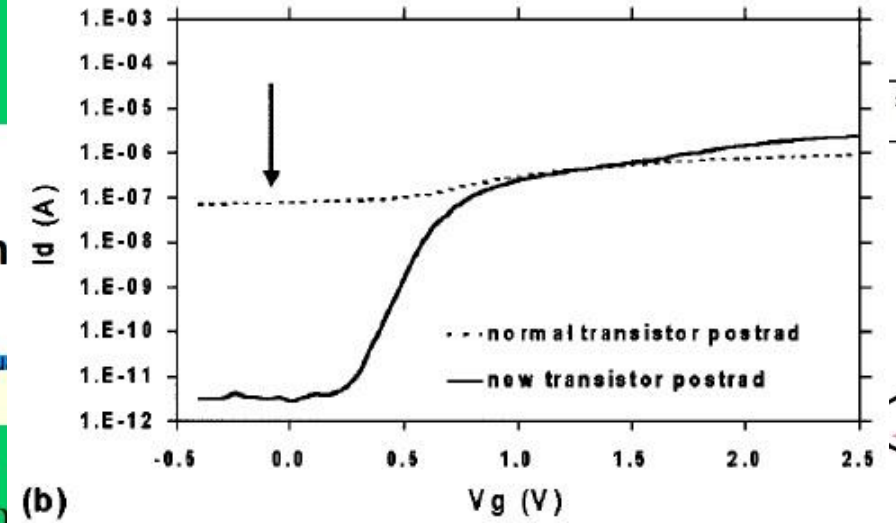
ransistor (ELT)...



(a)



Inter-diffusion



(b)

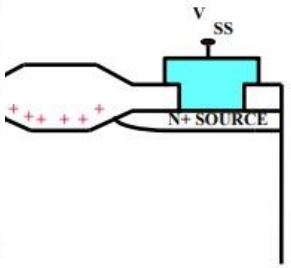
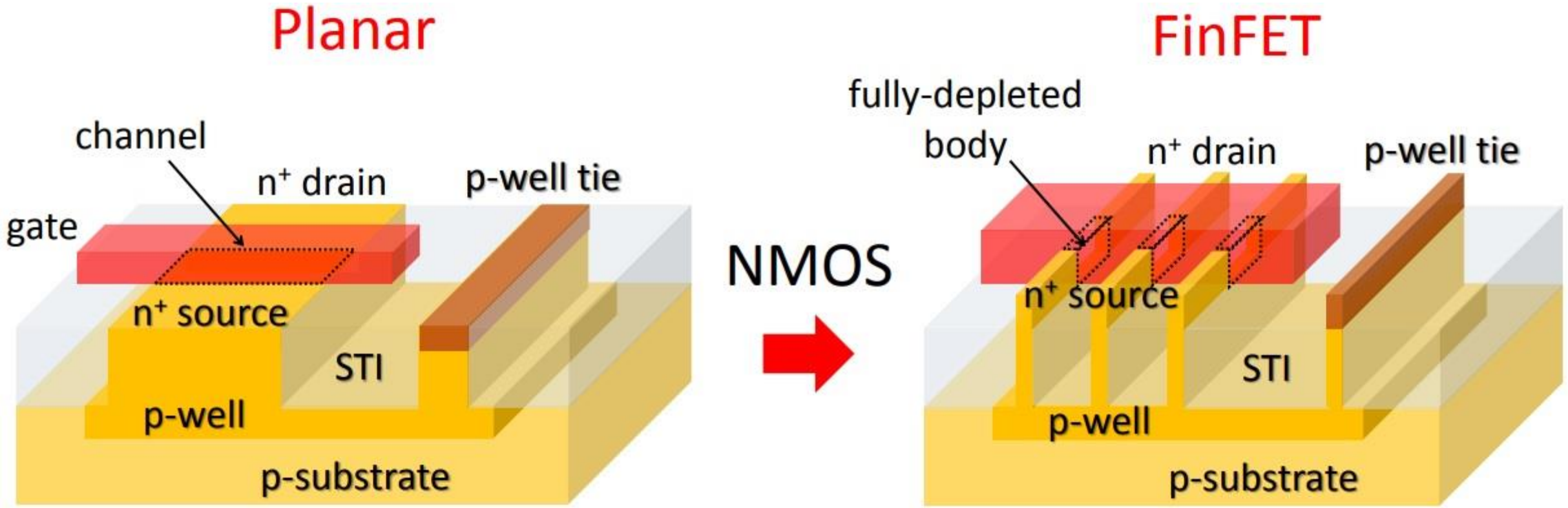


Fig. 10. (a) Transistor measurements after irradiation [dose 40 Mrad(SiO_2)] W/L = 10 μm/0.28 μm. (b) W/L = 0.64 μm/10 μm. The normal transistor shows severe post-irradiation leakage (arrow). The behavior of the new transistor is virtually unaffected by the irradiation. The turning on of the channel underneath the poly of the opposite type remains present and can be observed for the long transistor (around 1.6 V and up).

F. Faccio, upgrades

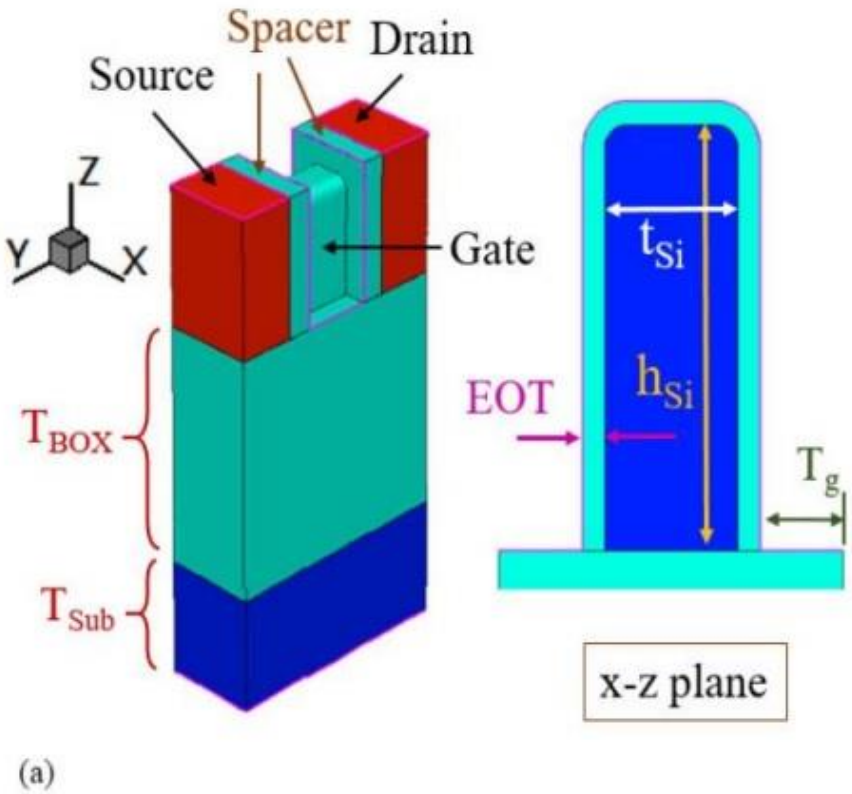
Planar nMOS vs FinFET

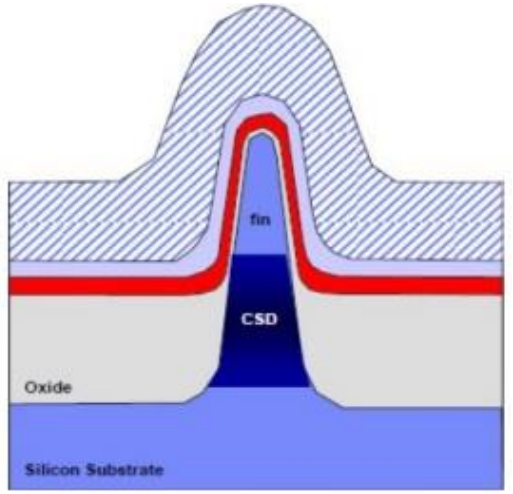


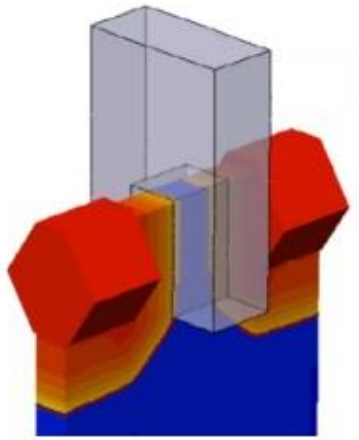
M. Campbell & F. Faccio, Future ASIC technologies in HEP experiments

FinFETs

- Most commercial fabs have migrated to FinFETs below 20-nm gate length feature sizes
- FinFETs exhibit improved electrostatic control of the channel and improved reliability compared to equivalent scaled planar CMOS





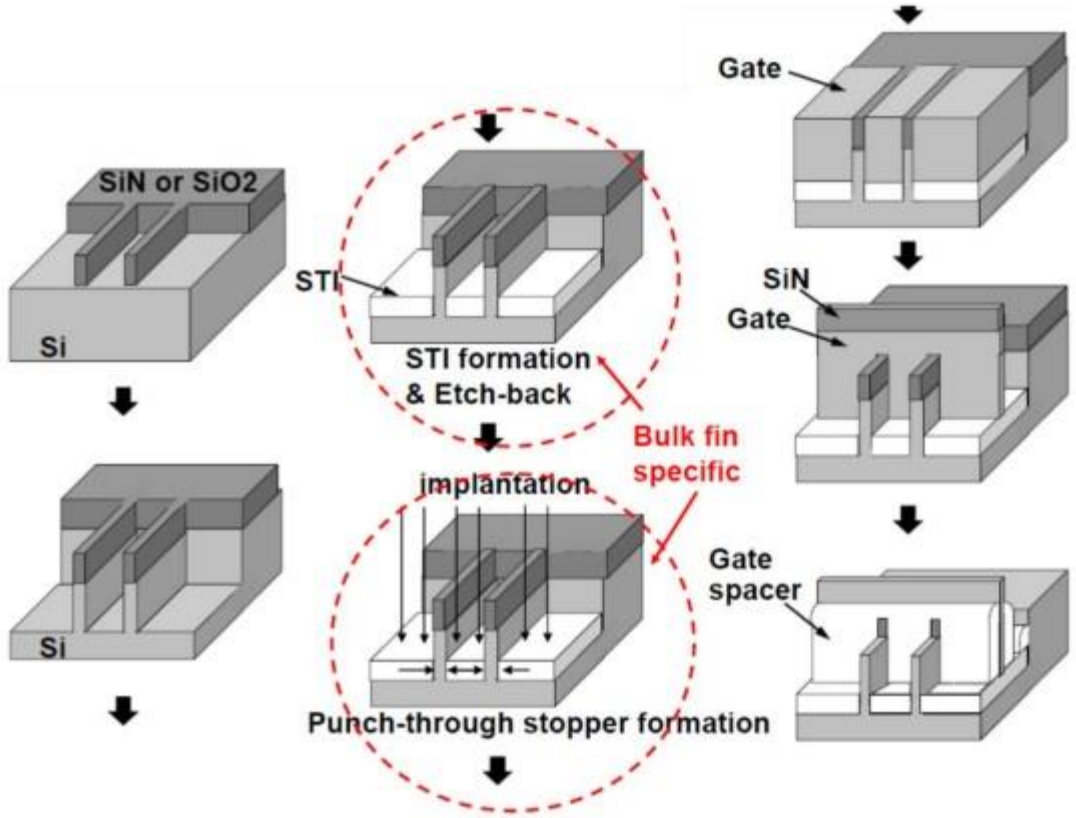


T. Hook, FDSOI Conference, Taiwan, 2013

M. Campbell & F. Faccio, Future ASIC technologies in HEP experiments

FinFET processing technology

- Increasing processing complexity
- More challenging lithography
  - Quad patterning
  - Soon EUV
- Line edge roughness
- Isolation steps
  - STI
  - CSD/SSRW



A. Yagishita (Toshiba), SOI Short Course (2009)

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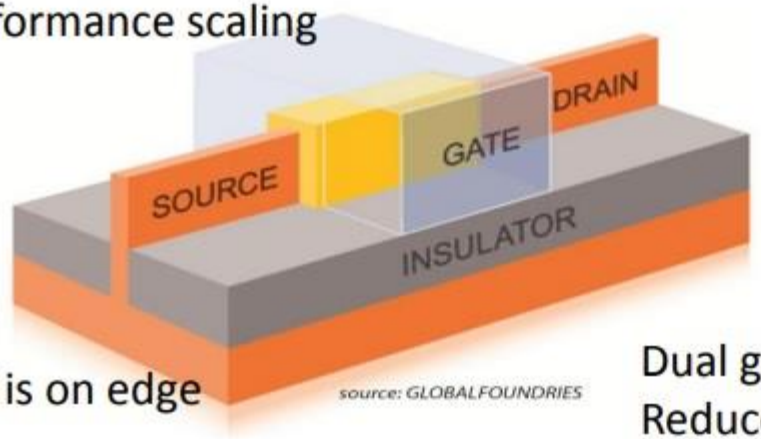
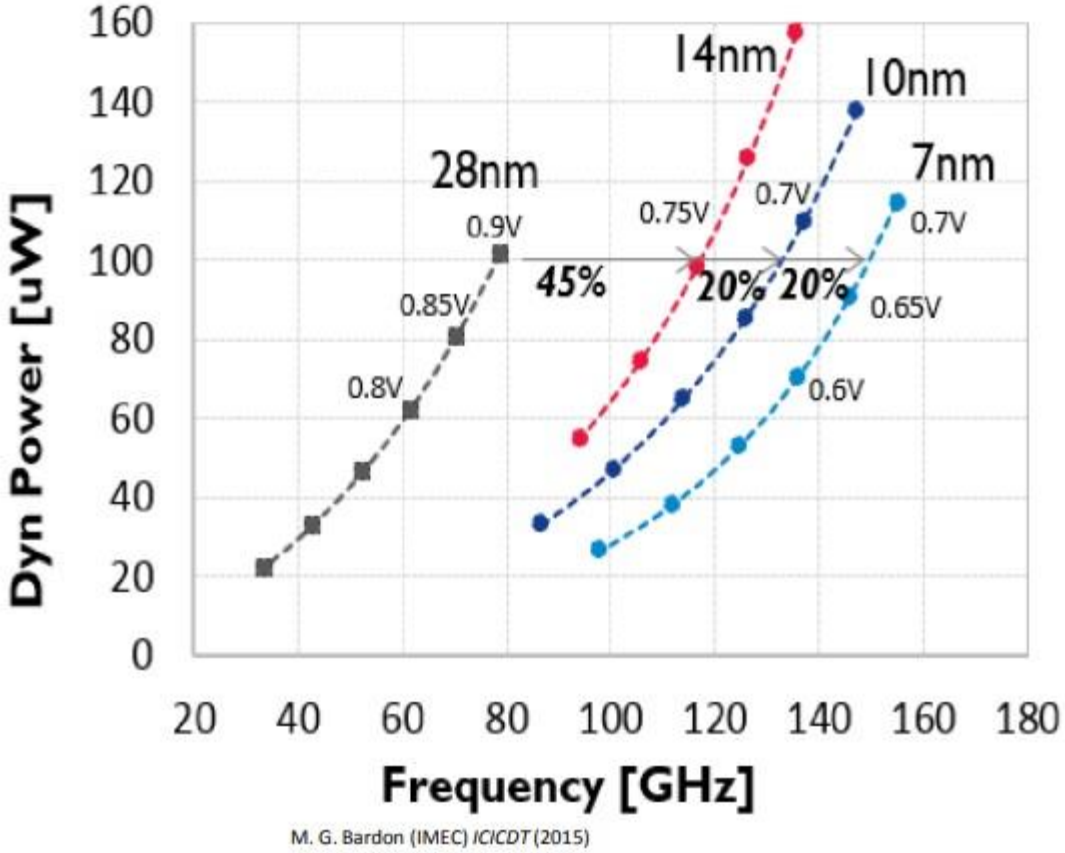
FinFET – Advantages / challenges

Gate length shrink
Performance scaling



FET is on edge

Dual gate
Reduces I_{off}

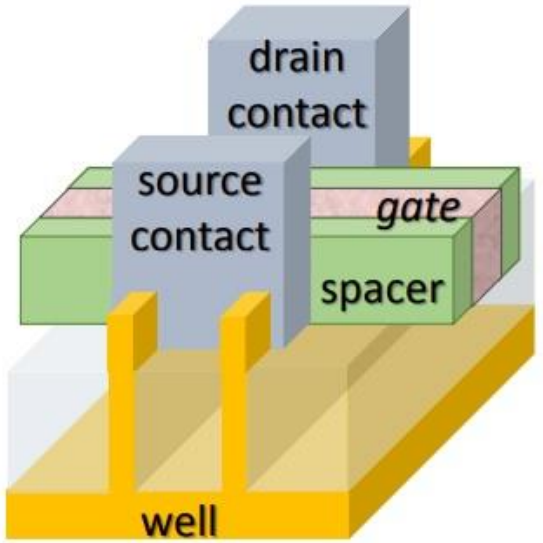


M. G. Bardon (IMEC) *ICICDT* (2015)

M. Campbell & F. Faccio, Future ASIC technologies in HEP experiments

FinFET – Design

- More drive current for given footprint
- Quantized channel width
  - Challenge for logic & SRAM
  - OK for analog, enough g_m granularity
- Less DIBL → better r_{out}, 3× intrinsic gain
- Essentially no body effect ($\Delta V_T < 10mV$)
- Higher R_s & R_d spreading resistance
- Lower C_j but higher C_{gd} & C_{gs} coupling
- Higher R_{well} (R_{diode}, latch-up)
- Mismatch depends on fin geometry, MG grains, gate density, stress, less on RDF



Sheu, TSMC [18]
Hsueh *et al.*, TSMC [19]

Slide courtesy of Alvin Loke, Qualcomm

Thank you for your attention