UK Advanced Instrumentation Training

Circuit Design 3 & 4
Simulation LTspice 1 & 2

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2022 Apr 19

Circuit Design, Noise, Grounding

- Workflow
  - Analyze -> Block Diagram, Specs
  - Schematic -> Circuit topology, Constraints
  - Layout -> GERBER, BOM, Assembly-files
  - Manufacturing (fabrication, population, assembly)
  - Debug, Characterization -> Reports
  - (Revision)
- Simulation

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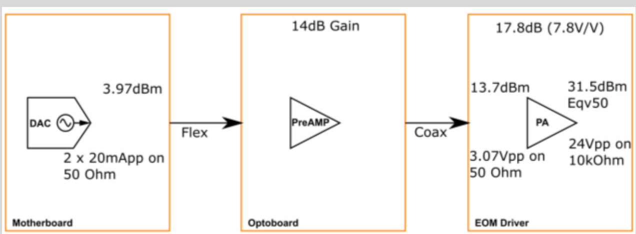
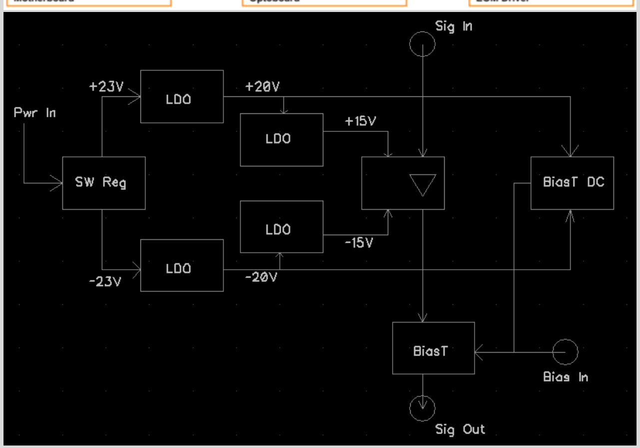
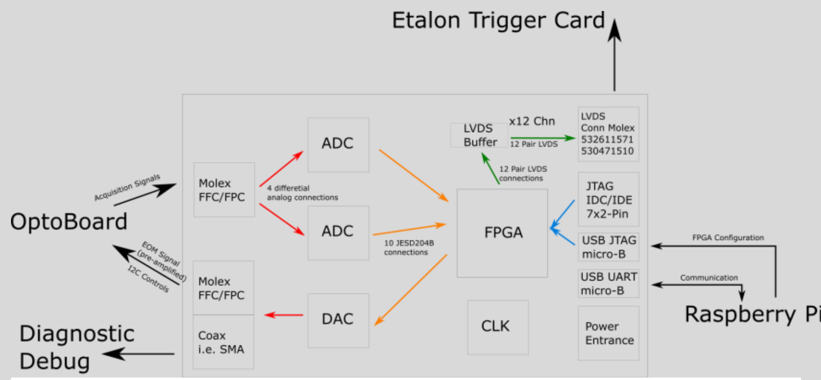
Circuit Design, Noise, Grounding

- Workflow
  - Analyze -> Block Diagram, Specs





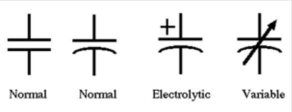


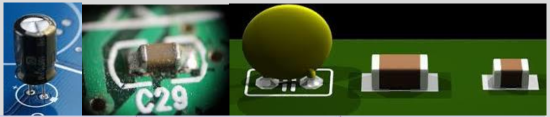
Recalculated Power Consumption at 3.8.9.2:

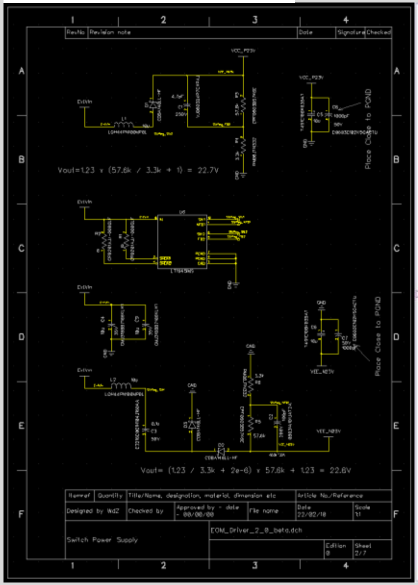
	Layer	Power Supply Net Name	Voltage (V)	Consumer	Current Input (mA)
ADP2384	1	VDD3V8	3.8	DAC + CLK	454
				Total	454
MAX15301	1	VDD3V3	3.3	LVDS + USB	155
		VDD3V3	3.3	FPGA Fabric	TBD (Max725)
		VDD3V3	3.3	DAC + CLK	5.7
		VDD3V3	3.3	ADC	801
				Total	1686.7
MAX15301	1	VDD1V8	1.8	DAC + CLK	767
		VDD1V8	1.8	2 ADCs	1572
		VDD1V8	1.8	FPGA MGT	2983
		VDD1V8	1.8	FPGA Fabric	2938
				Total	8260
MAX15301	1	VCCINT	0.95	FPGA Fabric	10262
				Total	10262

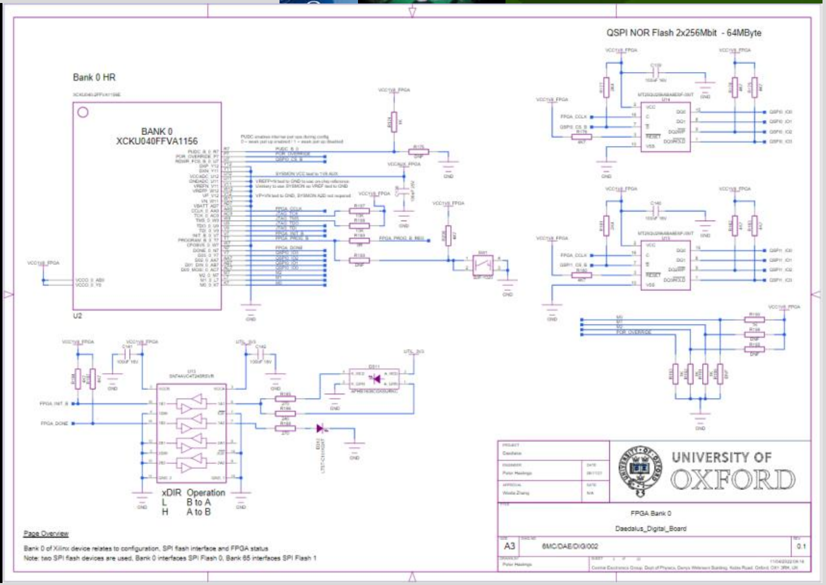
Circuit Design, Noise, Grounding

- Workflow
  - Schematic -> Circuit topology, Constraints









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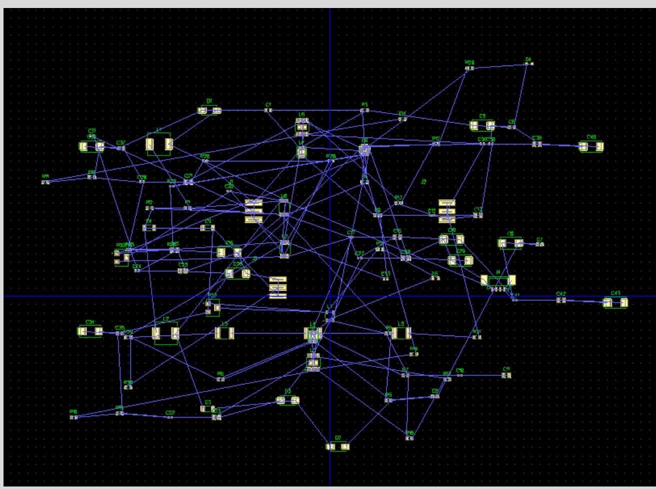
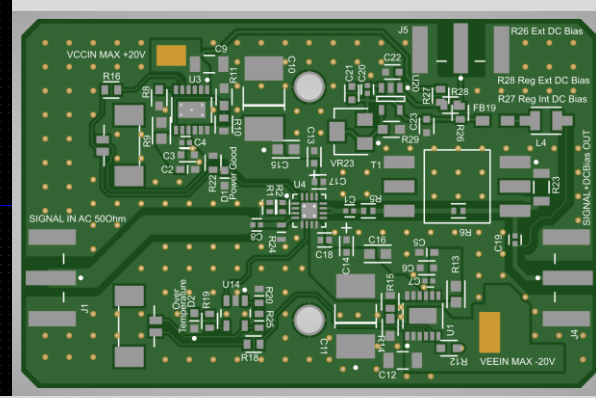
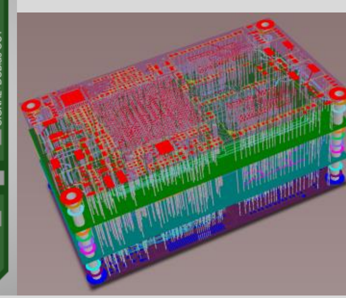
Circuit Design, Noise, Grounding

- Workflow
    - Layout -> GERBER, BOM, Assembly-files



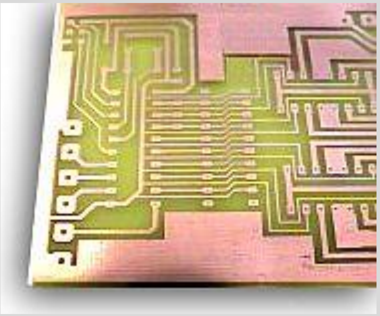


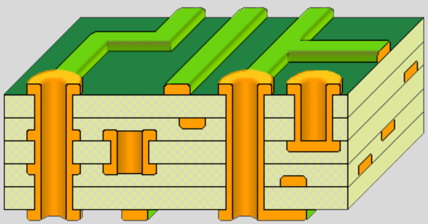


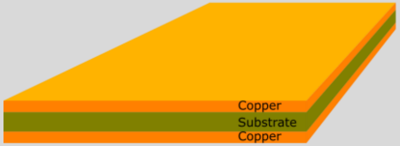
Source: https://www.wellpcb.com/

Circuit Design, Noise, Grounding

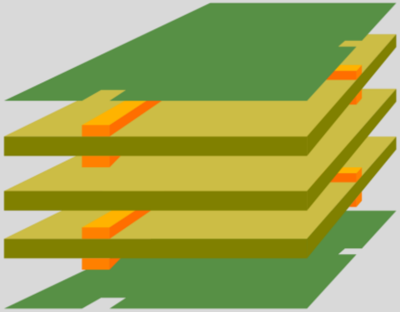
- Workflow
  - Manufacturing (fabrication, population, assembly)

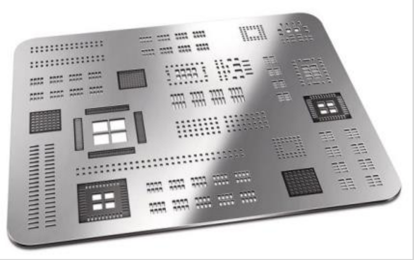






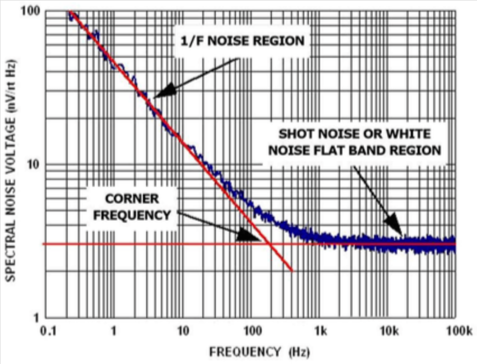
Core

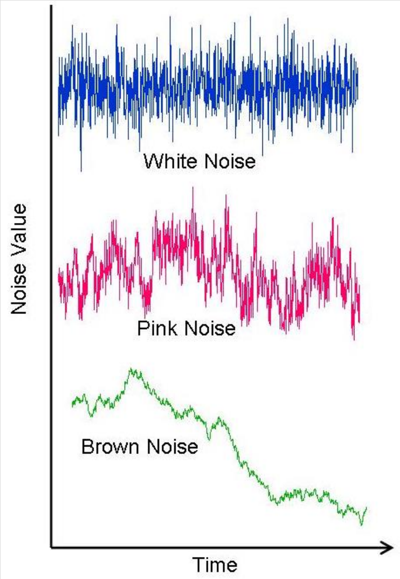




Circuit Design, Noise, Grounding

- Noise
  - Thermal ~ quasi-white, Gaussian, $4kTR$; Conductor
  - Shot ~ white, Gaussian, $2e|I|$; Semiconductor
  - $1/f$, flicker ~ f-depend; Anything
  - Burst ~ 2-value, f-depend; Semiconductor





Circuit Design, Noise, Grounding

- Interference/Crosstalk
  - Data/Clock dependent ~ non-stationary, f-depend
- Systematic
  - Harmonics, Spurs ~ f-depend; Amp-linearity, ADC, DAC
  - Quantization Noise ~ quasi-white, uniform; ADC
  - Aliasing/Mirror Noise~ Signal x Sinc, uniform; ADC, DAC
  - Clock Phase Noise ~ $1/f^{\alpha}$; resonant, quartz, PLL

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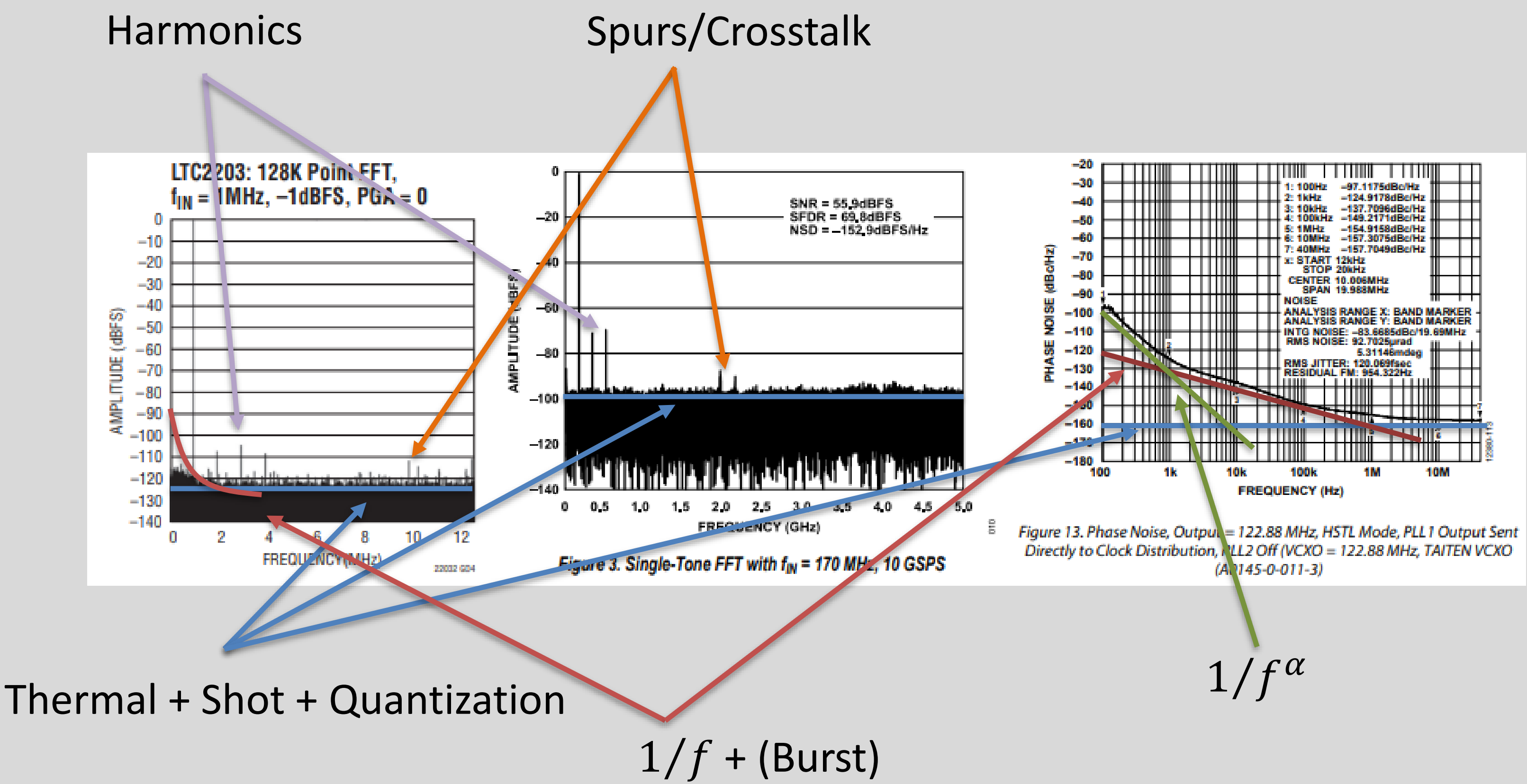
Circuit Design, Noise, Grounding



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Circuit Design, Noise, Grounding

- Noise
  - Units PSD vs PSD

$$\bar{P} = \lim_{T \to \infty} \frac{1}{T} \int_{-T/2}^{T/2} \frac{x^2(t)}{R} \mathrm{d}t$$

x is the random variable of noise, with the unit of voltage
Resistivity R is sometimes ignored to 1, $\bar{P}$ is average power

$$\bar{P} = \int_0^B S_x(f) \mathrm{d}f$$

B is the bandwidth, S_x is the power spectrum density, with the unit of Power per Bandwidth, i.e. dBm/Hz

$$x_{\mathrm{RMS}} = \sqrt{\bar{P}R}$$

x_{RMS} is the root-mean-square of the noise, with the unit of voltage

$$v_n(f) = \sqrt{\overline{S_x(f)}R} = \sqrt{\frac{\bar{x}^2}{RB}}$$

This is only in white noise, $v_n(f)$ is the voltage spectrum density, with the unit of $\mathrm{V}/\sqrt{\mathrm{Hz}}$

Circuit Design, Noise, Grounding

- Noise
  - Conversion
    - 0dBm = 0.632V_{PP} = 0.233 V_{RMS}
  - Quantify and Comparison

$$x_{\mathrm{RMS}} = \sqrt{\bar{P}R}$$

$$v_n(f) = \sqrt{\overline{S_x(f)}R} = \sqrt{\frac{\bar{x}^2}{RB}}$$

ADA4099-1/ADA4099-2

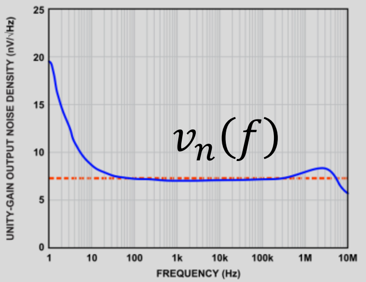


Figure 42. Unity-Gain Output Noise Density vs. Frequency

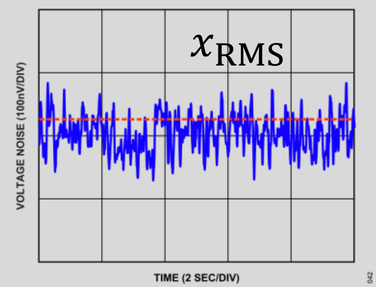


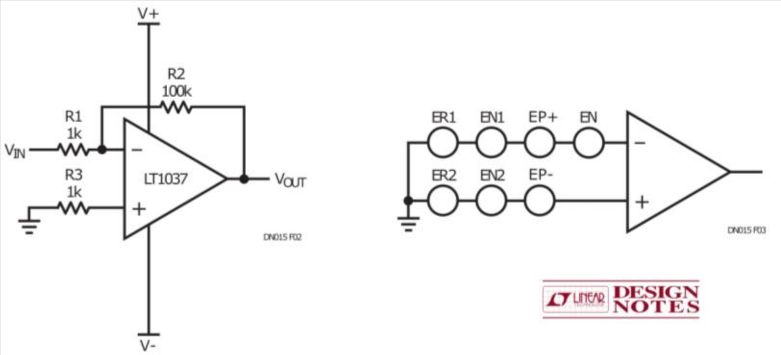
Figure 43. 0.1 Hz to 10 Hz Noise

analog.com

- v_n as a number gives floor
- x_{RMS} at low frequency tells flicker

NOISE PERFORMANCE				
Input Voltage Noise	f = 0.1 Hz to 10 Hz	150	150	nV p-p
	1/f noise corner	6	6	Hz
	f = 100 Hz	7	7	nV/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > +V_S	8	8	nV/√Hz
Input Current Noise	f = 100 Hz	0.5	0.5	pA/√Hz
Over-The-Top	f = 100 Hz, V_{CM} > +V_S	5	5	pA/√Hz

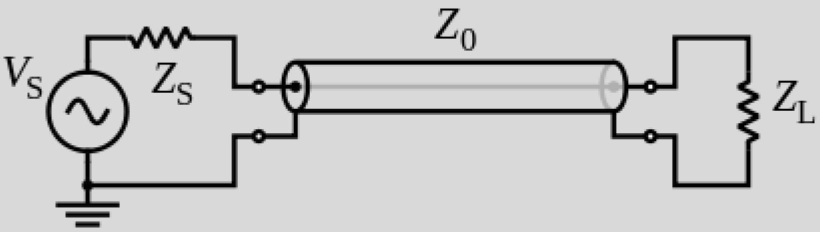
Circuit Design, Noise, Grounding

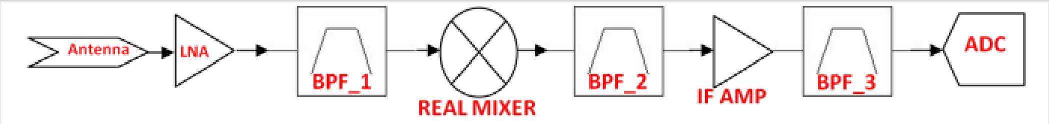


- Noise
  - Paths
    - Signal Input
    - Resistive Components
    - Semiconductor Devices
    - Non-Linear (not LTI)
    - Power Supplies
    - Indirect Coupling

Circuit Design, Noise, Grounding

- Noise
  - Paths
    - Signal Input
      - Antenna, transducer -> matching network
      - Previous Stage of Amps -> termination



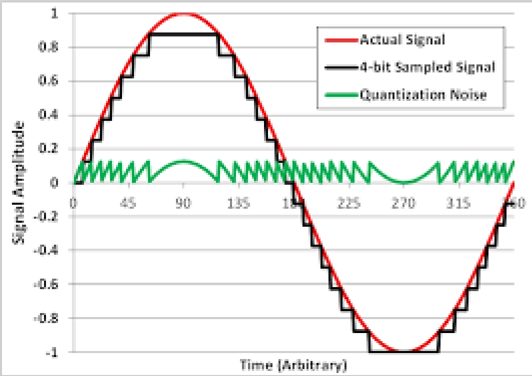


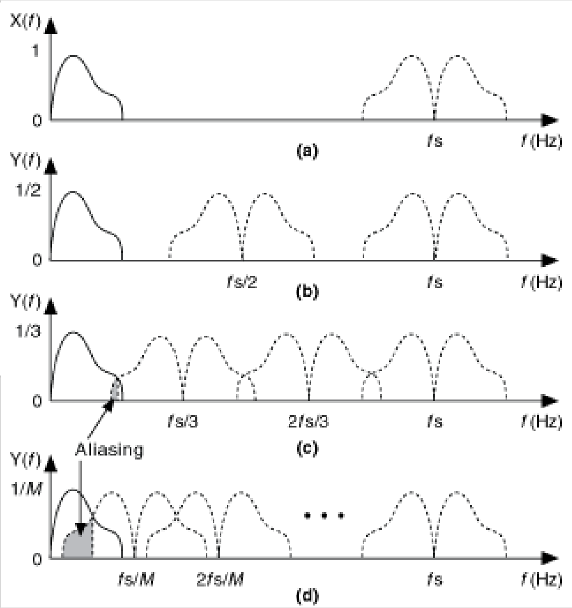
Source: Texas Instruments

$$F_n = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots$$

Circuit Design, Noise, Grounding

- Noise
  - Paths
    - Signal Input
      - ADC
        - Quantization ENOB
        - Aliasing

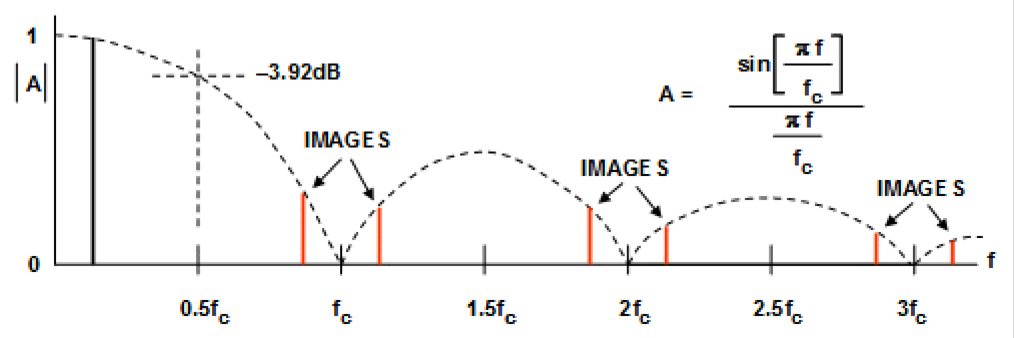




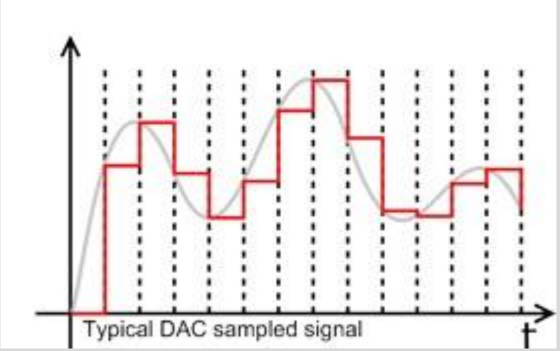
$$x[n] = \sum_n \int s(t)\delta(t - nT_S)\mathrm{d}t$$

Circuit Design, Noise, Grounding

- Noise
  - Paths
    - Signal Input
      - DAC
        - Quantization ENOB
        - Mirror/Image

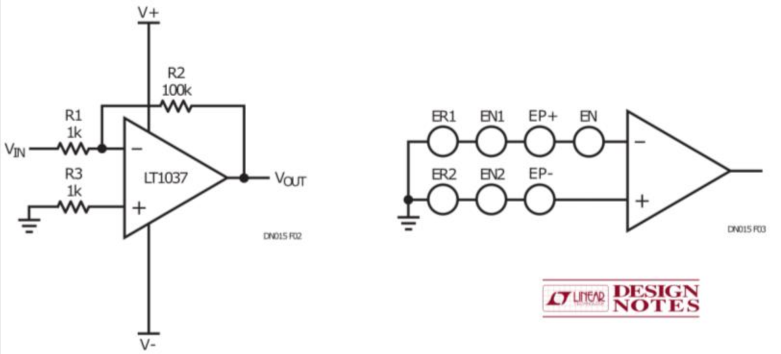


$$s(t) = \sum_n x[n] * \mathrm{rect}\left(\frac{t}{T_S}\right)$$



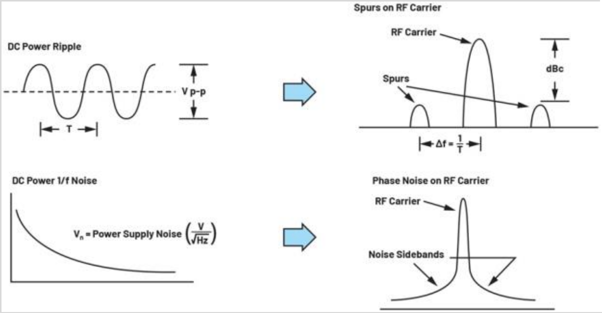
Circuit Design, Noise, Grounding

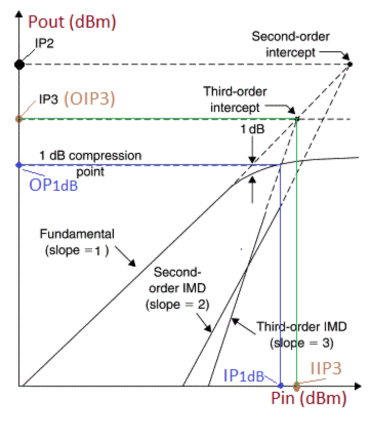
- Noise
  - Paths
    - Resistive Components
    - Semiconductor Devices

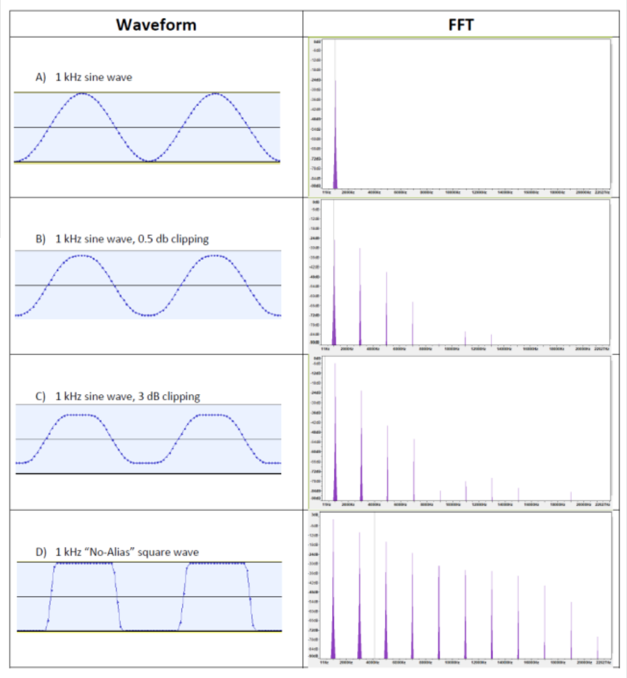


Circuit Design, Noise, Grounding

- Noise
  - Paths
    - Non-Linear (not LTI)







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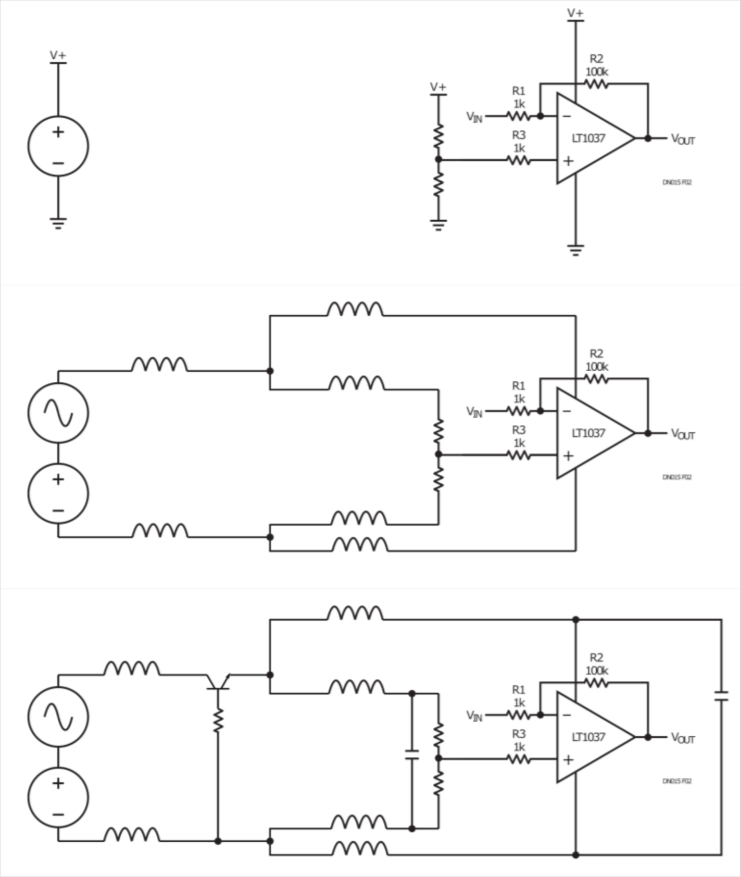
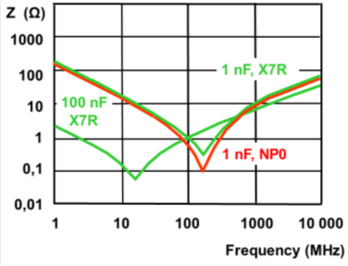
Circuit Design, Noise, Grounding

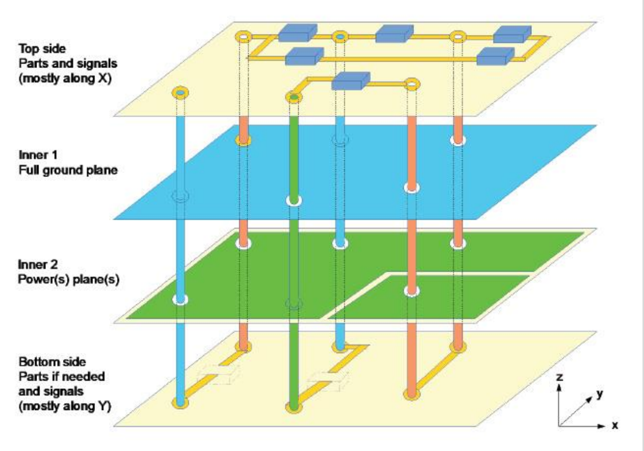
- Noise
  - Paths
    - Power Supplies
    - Indirect Coupling
    - Power integrity

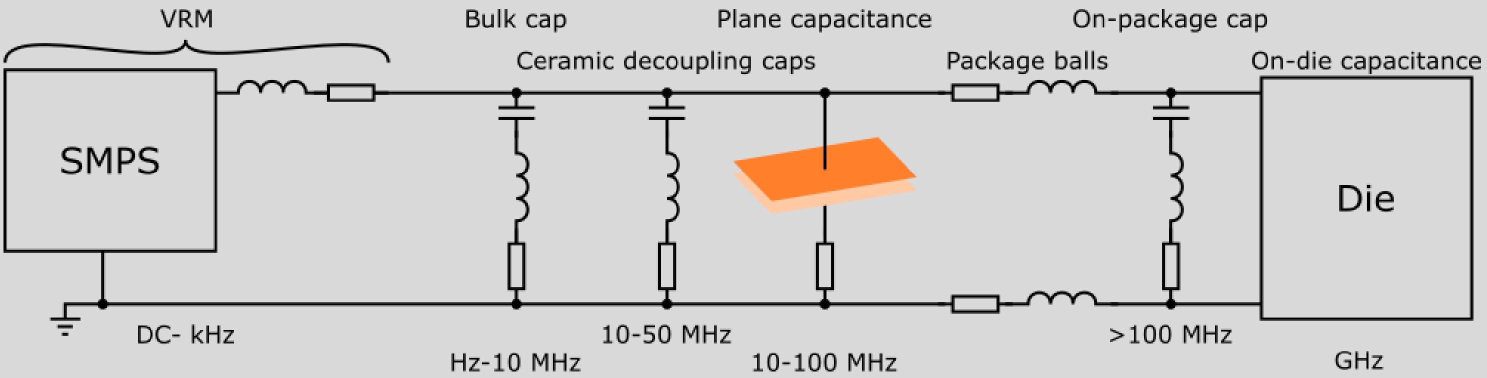


Circuit Design, Noise, Grounding

- Noise
  - Paths
    - Power Supplies
    - Indirect Coupling

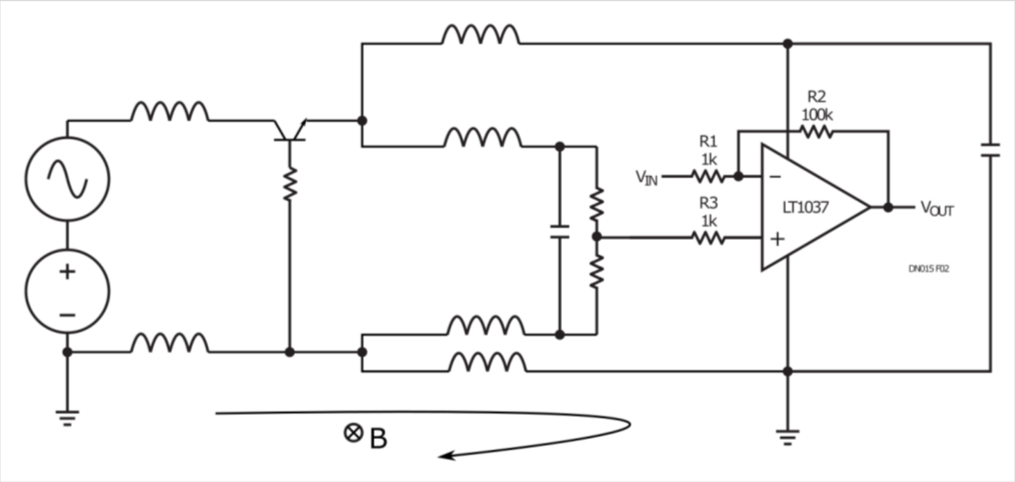






Circuit Design, Noise, Grounding

- Grounding



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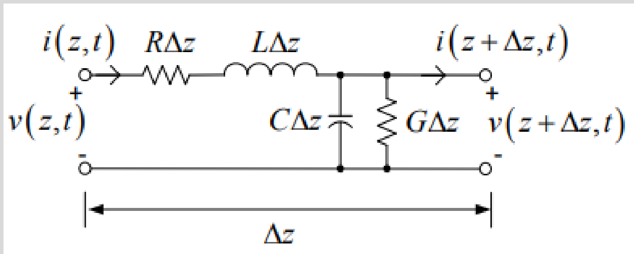
Circuit Design, Amplifier, Clock

- Transmission Line Theory

$$v(z,t) = L\Delta z \frac{\partial i(z,t)}{\partial t} + v(z+\Delta z,t)$$

$$i(z,t) = C\Delta z \frac{\partial v(z+\Delta z,t)}{\partial t} + i(z+\Delta z,t)$$



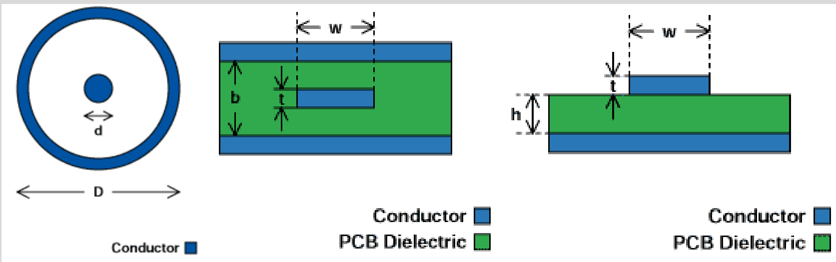
$$\frac{\partial v(z,t)}{\partial z} = -L\frac{\partial i(z,t)}{\partial t}$$

$$\frac{\partial i(z,t)}{\partial z} = -C\frac{\partial v(z,t)}{\partial t}$$

$$\frac{\partial^2 V}{\partial t^2} - u^2\frac{\partial^2 V}{\partial x^2} = 0$$

$$\frac{\partial^2 I}{\partial t^2} - u^2\frac{\partial^2 I}{\partial x^2} = 0$$

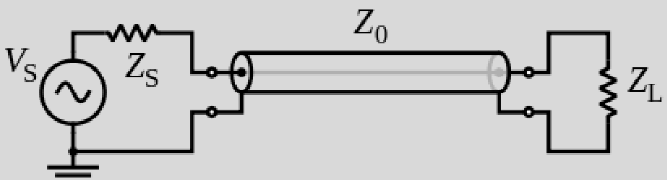
$$u = \frac{1}{\sqrt{LC}}$$



$$V(x) = V_1 e^{-jkx} + V_2 e^{+jkx}$$

$$I(x) = \frac{V_1}{Z_0} e^{-jkx} - \frac{V_2}{Z_0} e^{+jkx}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$



Circuit Design, Amplifier, Clock

- Signal Integrity
  - Designing and Maintaining Trace Structure
  - Termination

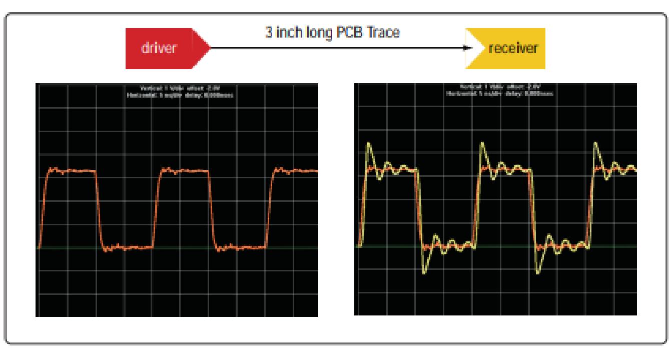
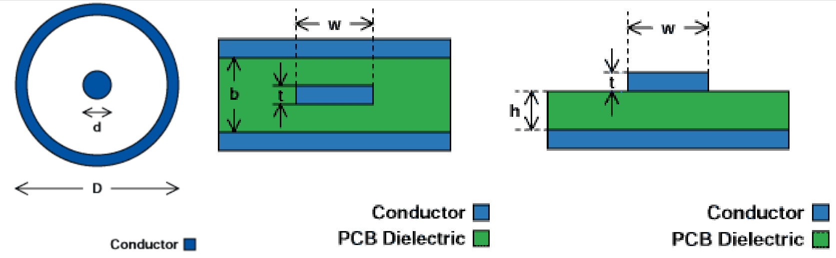
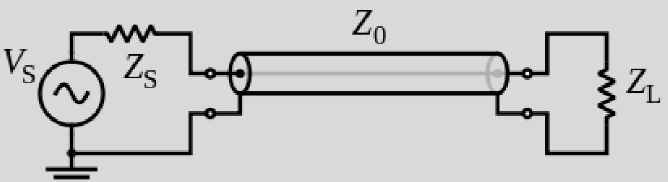


Figure 1. A signal as it emerges from the driver chip (left) is distorted by multiple reflections from impedance discontinuities at both ends (right).

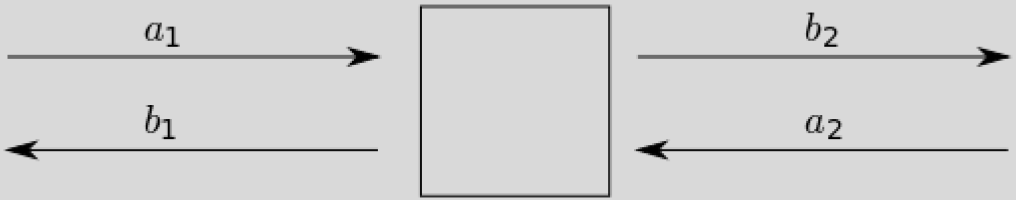
Source: Keysight





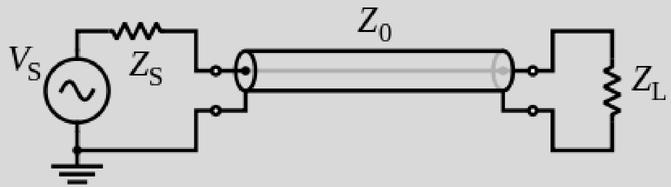
Circuit Design, Amplifier, Clock

- Scattering Parameter (S-Parameter)



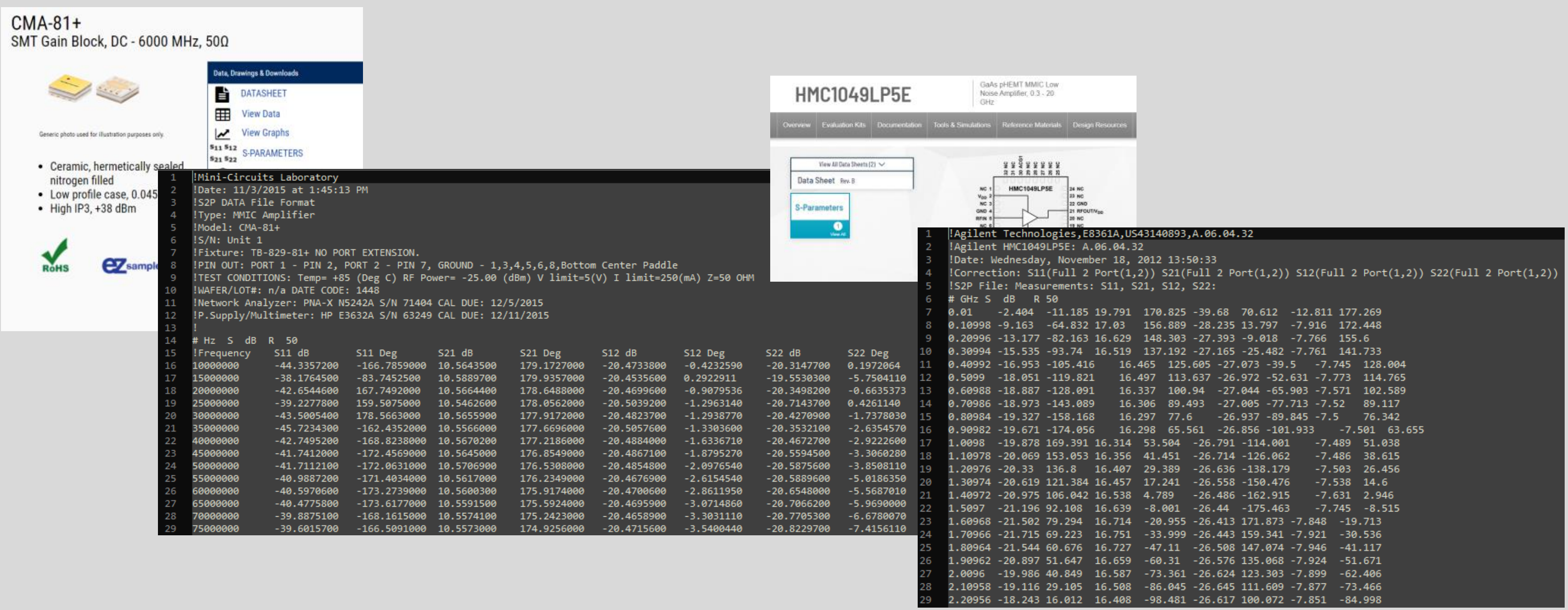
$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}.$$

S_{11} is the input port voltage reflection coefficient
S_{12} is the reverse voltage gain
S_{21} is the forward voltage gain
S_{22} is the output port voltage reflection coefficient.



Circuit Design, Amplifier, Clock

- Scattering Parameter (S-Parameter)




```
!Mini-Circuits Laboratory
!Date: 11/3/2015 at 1:45:13 PM
!S2P DATA File Format
!Type: MMIC Amplifier
!Model: CMA-81+
!S/N: Unit 1
!Fixture: TB-829-81+ NO PORT EXTENSION.
!PIN OUT: PORT 1 - PIN 2, PORT 2 - PIN 7, GROUND - 1,3,4,5,6,8,Bottom Center Paddle
!TEST CONDITIONS: Temp= +85 (Deg C) RF Power= -25.00 (dBm) V limit=5(V) I limit=250(mA) Z=50 OHM
!WAFER/LOT#: n/a DATE CODE: 1448
!Network Analyzer: PNA-X N5242A S/N 71404 CAL DUE: 12/5/2015
!P.Supply/Multimeter: HP E3632A S/N 63249 CAL DUE: 12/11/2015
!
# Hz  S  dB  R  50
!Frequency    S11 dB       S11 Deg      S21 dB       S21 Deg      S12 dB       S12 Deg      S22 dB       S22 Deg
10000000      -44.3357200  -166.7859000 10.5643500  179.1727000  -20.4733800  -0.4232590   -20.3147700  0.1972064
15000000      -38.1764500  -83.7452500  10.5889700  179.9357000  -20.4535600  0.2922911    -19.5530300  -5.7504110
20000000      -42.6544600  167.7492000  10.5664400  178.6488000  -20.4699600  -0.9079536   -20.3498200  -0.6635373
25000000      -39.2277800  159.5075000  10.5462600  178.0562000  -20.5039200  -1.2963140   -20.7143700  0.4261140
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35000000      -45.7234300  -162.4352000 10.5566000  177.6696000  -20.5057600  -1.3303600   -20.3532100  -2.6354570
40000000      -42.7495200  -168.8238000 10.5670200  177.2186000  -20.4884000  -1.6336710   -20.4672700  -2.9222600
45000000      -41.7412000  -172.4569000 10.5645000  176.8549000  -20.4867100  -1.8795270   -20.5594500  -3.3060280
50000000      -41.7112100  -172.0631000 10.5706900  176.5308000  -20.4854800  -2.0976540   -20.5875600  -3.8508110
55000000      -40.9887200  -171.4034000 10.5617000  176.2349000  -20.4676900  -2.6154540   -20.5889600  -5.0186350
60000000      -40.5970600  -173.2739000 10.5600300  175.9174000  -20.4700600  -2.8611950   -20.6548000  -5.5687010
65000000      -40.4775800  -173.6177000 10.5591500  175.5924000  -20.4695900  -3.0714860   -20.7066200  -5.9690000
70000000      -39.8875100  -168.1615000 10.5574100  175.2423000  -20.4658900  -3.3031110   -20.7705300  -6.6780070
75000000      -39.6015700  -166.5091000 10.5573000  174.9256000  -20.4715600  -3.5400440   -20.8229700  -7.4156110
```

```
!Agilent Technologies,E8361A,US43140893,A.06.04.32
!Agilent HMC1049LP5E: A.06.04.32
!Date: Wednesday, November 18, 2012 13:50:33
!Correction: S11(Full 2 Port(1,2)) S21(Full 2 Port(1,2)) S12(Full 2 Port(1,2)) S22(Full 2 Port(1,2))
!S2P File: Measurements: S11, S21, S12, S22:
# GHz S  dB   R 50
0.01    -2.404  -11.185 19.791  170.825 -39.68  70.612  -12.811 177.269
0.10998 -9.163  -64.832 17.03   156.889 -28.235 13.797  -7.916  172.448
0.20996 -13.177 -82.163 16.629  148.303 -27.393 -9.018  -7.766  155.6
0.30994 -15.535 -93.74  16.519  137.192 -27.165 -25.482 -7.761  141.733
0.40992 -16.953 -105.416    16.465  125.605 -27.073 -39.5   -7.745  128.004
0.5099  -18.051 -119.821    16.497  113.637 -26.972 -52.631 -7.773  114.765
0.60988 -18.887 -128.091    16.337  100.94  -27.044 -65.903 -7.571  102.589
0.70986 -18.973 -143.089    16.306  89.493  -27.005 -77.713 -7.52   89.117
0.80984 -19.327 -158.168    16.297  77.6    -26.937 -89.845 -7.5    76.342
0.90982 -19.671 -174.056    16.298  65.561  -26.856 -101.933    -7.501  63.655
1.0098  -19.878 169.391 16.314  53.504  -26.791 -114.001    -7.489  51.038
1.10978 -20.069 153.053 16.356  41.451  -26.714 -126.062    -7.486  38.615
1.20976 -20.33  136.8   16.407  29.389  -26.636 -138.179    -7.503  26.456
1.30974 -20.619 121.384 16.457  17.241  -26.558 -150.476    -7.538  14.6
1.40972 -20.975 106.042 16.538  4.789   -26.486 -162.915    -7.631  2.946
1.5097  -21.196 92.108  16.639  -8.001  -26.44  -175.463    -7.745  -8.515
1.60968 -21.502 79.294  16.714  -20.955 -26.413 171.873 -7.848  -19.713
1.70966 -21.715 69.223  16.751  -33.999 -26.443 159.341 -7.921  -30.536
1.80964 -21.544 60.676  16.727  -47.11  -26.508 147.074 -7.946  -41.117
1.90962 -20.897 51.647  16.659  -60.31  -26.576 135.068 -7.924  -51.671
2.0096  -19.986 40.849  16.587  -73.361 -26.624 123.303 -7.899  -62.406
2.10958 -19.116 29.105  16.508  -86.045 -26.645 111.609 -7.877  -73.466
2.20956 -18.243 16.012  16.408  -98.481 -26.617 100.072 -7.851  -84.998
```

Circuit Design, Amplifier, Clock

- Matching Network

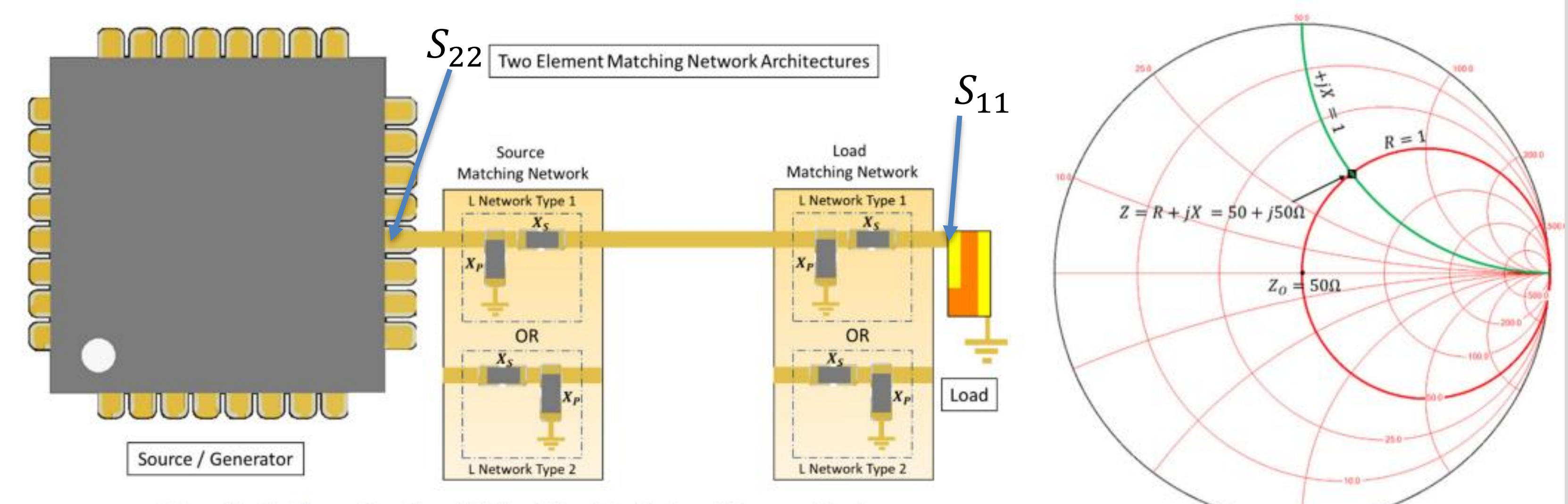

Figure 4.1. Two Element Impedance Matching Network Architecture at Source and Load

Source: SiLabs

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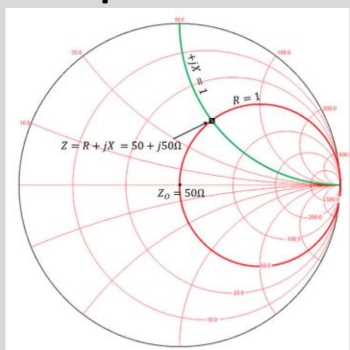
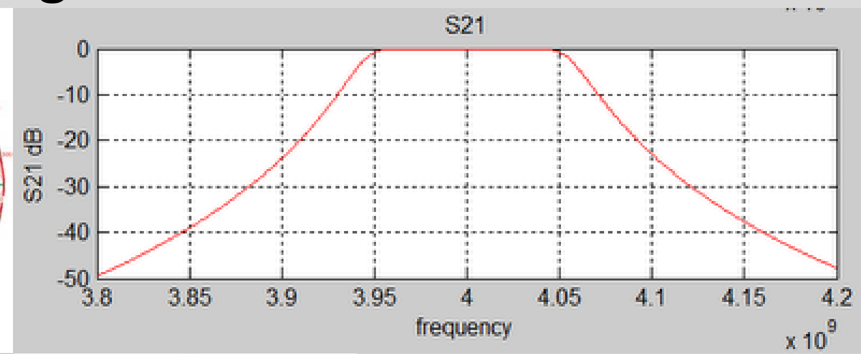
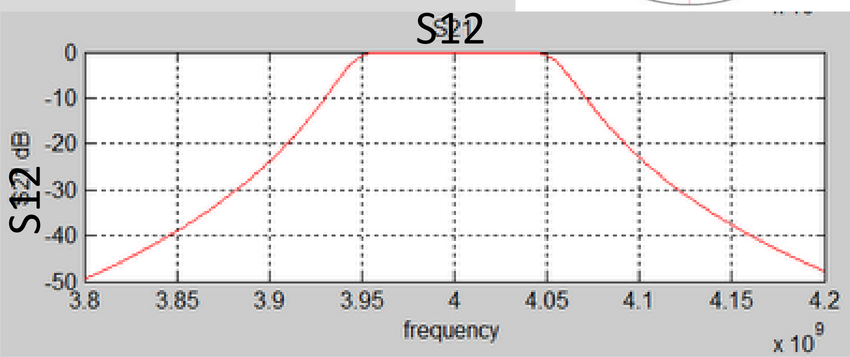
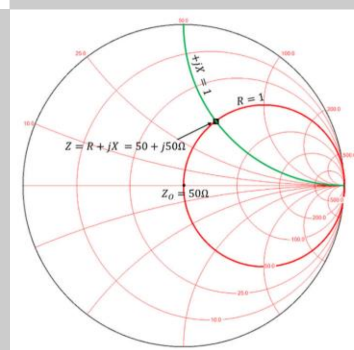
Circuit Design, Amplifier, Clock

- Simulation of Amplifier Design



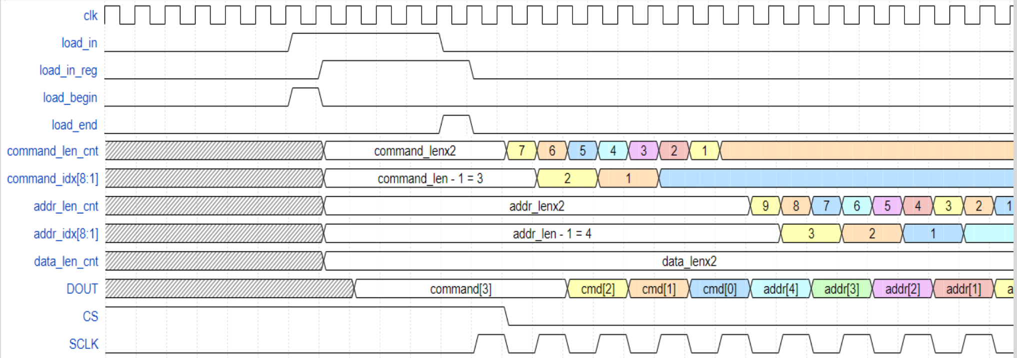


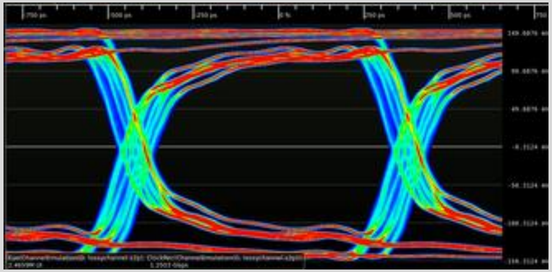




Circuit Design, Amplifier, Clock

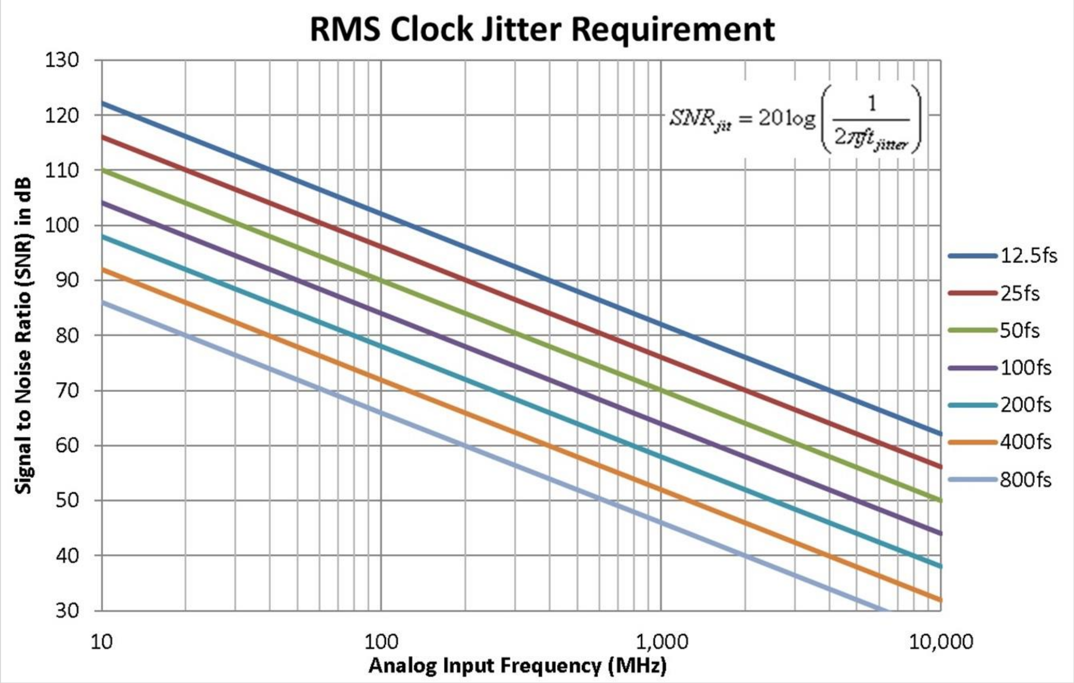
- Clock Jitter/Phase noise in Digital System/Comms





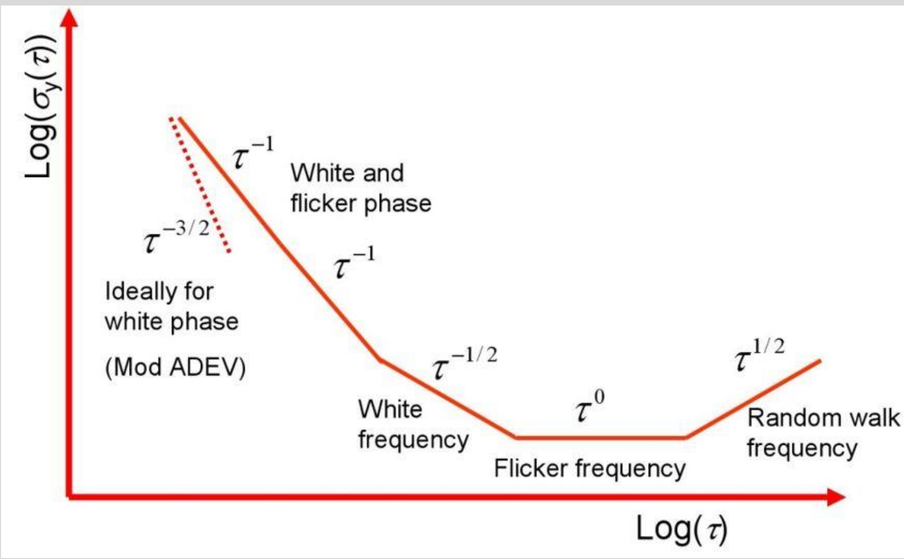
Circuit Design, Amplifier, Clock

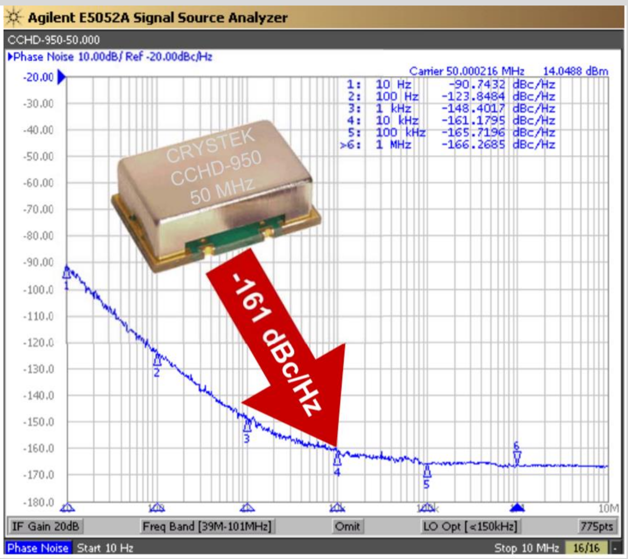
- Clock Jitter/Phase noise in DAQ



Circuit Design, Amplifier, Clock

- Clock Jitter/Phase noise

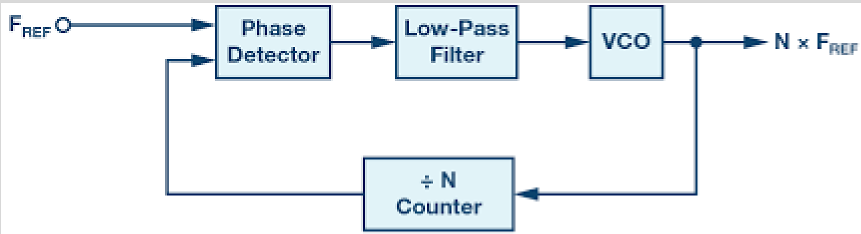


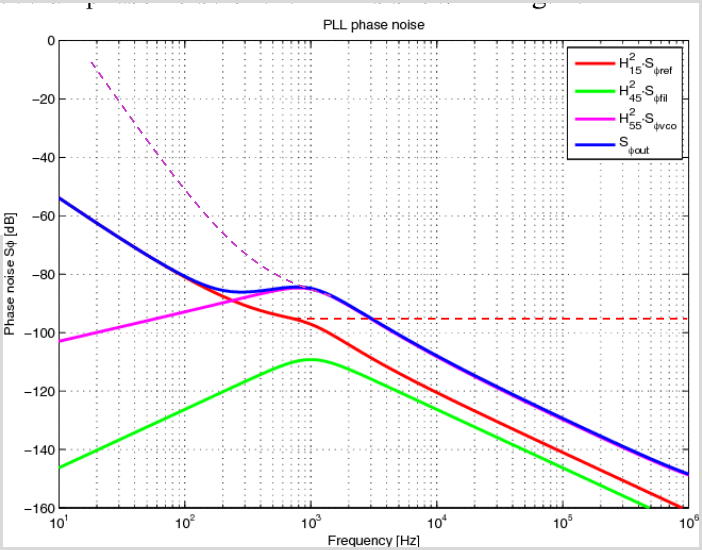


Source: NIST

Circuit Design, Amplifier, Clock

- Phase Locked Loop





Circuit Design, Amplifier, Clock

- How to read datasheet

Data Sheet **HMC1049LP5E**

FEATURES

Low noise figure: 1.8 dB
P1dB output power: 14.5 dBm
P_{SAT} output power: 17.5 dBm
High gain: 15 dB
Output IP3: 29 dBm
Supply voltage: V_{DD} = 7 V at 70 mA
50 Ω matched input/output (I/O)
32-lead, 5 mm × 5 mm LFCSP package: 25 mm²

APPLICATIONS

Test instrumentation
High linearity microwave radios
VSAT and SATCOM
Military and space

FUNCTIONAL BLOCK DIAGRAM

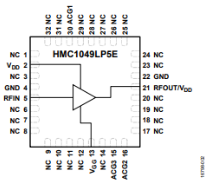


Figure 1.

GENERAL DESCRIPTION

The HMC1049LP5E is a GaAs MMIC low noise amplifier (LNA) that operates between 0.3 GHz and 20 GHz. This LNA provides 15 dB of small signal gain, 1.8 dB noise figure, and an IP3 output of 29 dBm, yet requires only 70 mA from a 7 V supply. The P1dB output power of 14.5 dBm enables the LNA to function as a local oscillator (LO) driver for balanced, I/Q, or image rejection mixers. V_{DD} can also be applied to Pin 21, although Pin 21 requires a bias tee with V_{DD} = 4 V. The HMC1049LP5E amplifier I/Os are internally matched to 50 Ω, and the device is supplied in a compact, leadless 5 mm × 5 mm LFCSP package.

Data Sheet **HMC1049LP5E**

SPECIFICATIONS

T_A = 25°C, V_{DD} = 7 V, I_{DD} = 70 mA[1].

Table 1.

Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
FREQUENCY RANGE	0.3		1	1		14	14		20	GHz
GAIN	13.5	16.5		12	15		10	13		dB
Gain Variation Over Temperature		0.006			0.019			0.017		dB/°C
NOISE FIGURE		2.5	3.5		1.8	2.5		2.7	4.0	dB
RETURN LOSS										
Input		15			13			14		dB
Output		8			15			13		dB
OUTPUT										
Output Power for 1 dB Compression (P1dB)		15			14.5			13		dBm
Saturated (P_{SAT})		18			17.5			16		dBm
Output Third-Order Intercept (IP3)[2]		31			29			26		dBm
TOTAL SUPPLY CURRENT		70			70			70		mA

[1] Adjust V_{GG} between −2 V to 0 V to achieve I_{DD} = 70 mA typical.
[2] Measurement taken at P_{OUT}/tone = 8 dBm.

HMC1049LP5E Data Sheet

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD})	10 V
Drain Bias Voltage (RF Out/V_{DD})	7 V
RF Input Power	18 dBm
Gate Bias Voltage, V_{GG}	−2 V to +0.2 V
Channel Temperature	175°C
Continuous P_{DISS} (T = 85°C) (Derate 37.1 mW/°C Above 85°C)	3.34 W
Thermal Resistance (Channel to Ground Paddle)	26.9°C/W
Temperature	
Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C
ESD Sensitivity (HBM)	Class 1A

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 3. Typical Supply Current vs. V_{DD}

V_{DD} (V)	I_{DD}[1] (mA)
5	70
6	70
7	70

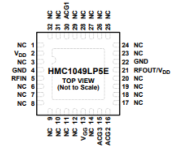
[1] Adjust V_{GG} to achieve I_{DD} = 70 mA.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Data Sheet **HMC1049LP5E**

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THESE PINS ARE NOT CONNECTED INTERNALLY; HOWEVER, ALL DATA WAS MEASURED WITH THESE PINS CONNECTED TO RF/DC GROUND EXTERNALLY.
2. EXPOSED PAD. THE EXPOSED GROUND PADDLE MUST BE CONNECTED TO RF/DC GROUND.

Figure 2. Pin Configuration Diagram

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description[1]
1, 3, 6 to 12, 14, 17 to 20, 23 to 29, 31, 32	NC	No Connect. These pins are not connected internally; however, all data was measured with these pins connected to RF/dc ground externally (see the Typical Performance Characteristics section for data plots).
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω.
2	V_{DD}	Power Supply Voltage for the Amplifier. External bypass capacitors (100 pF and 0.01 μF) are required.
30	ACG1	Low Frequency Termination. An external bypass capacitor of 100 pF is required.
21	RFOUT/V_{DD}	RF Output/Alternate Power Supply Voltage for the Amplifier. An external bias tee is required when used as alternative V_{DD}. This pin is dc-coupled and matched to 50 Ω.
15, 16	ACG2, ACG3	Low Frequency Termination. External bypass capacitors of 100 pF are required.
13	V_{GG}	Gate Control for Amplifier. Adjust the voltage to achieve I_{DD} = 70 mA. External bypass capacitors of 100 pF, 0.01 μF, and 4.7μF are required.
4, 22	GND	Ground. Connect Pin 4 and Pin 22 to RF/dc ground.
0	EP	Exposed Pad. The exposed ground paddle must be connected to RF/dc ground.

[1] See the Interface Schematics section for pin interfaces.

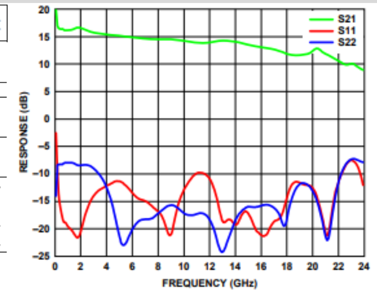


Figure 10. Broadband Gain and Return Loss

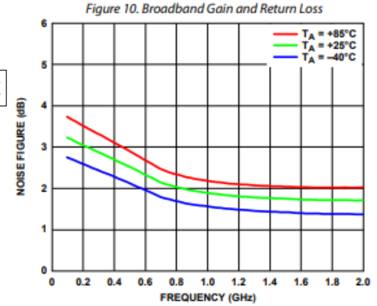


Figure 15. Noise Figure vs. Temperature, Low Frequency

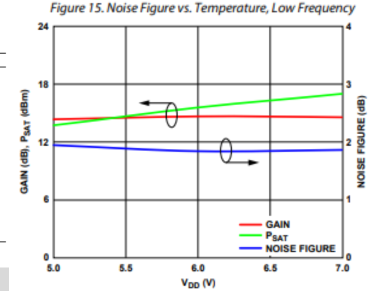


Figure 27. Gain, P_{SAT}, and Noise Figure vs. V_{DD} at 12 GHz

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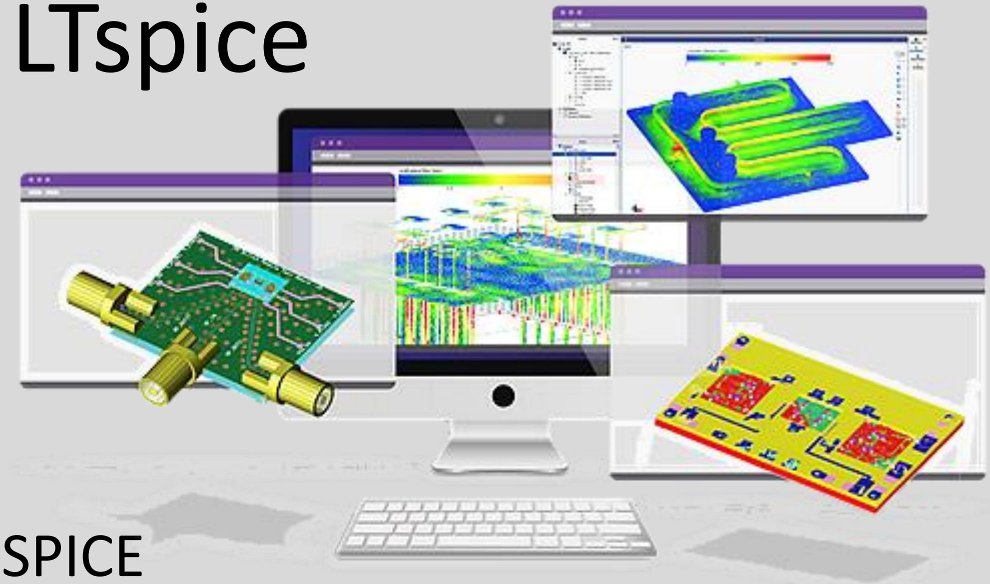
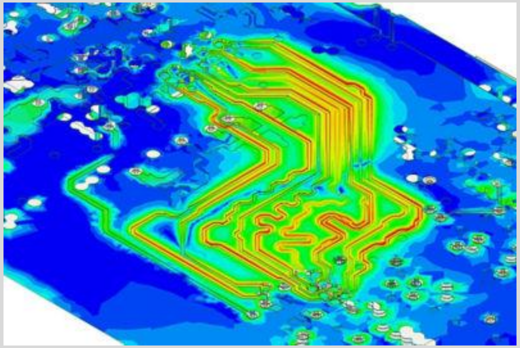
Simulation - LTspice



- Schematic Level
- Layout Level

- Structural model – SPICE
- Behavioral model – IBIS
- Scattering model – S-parameter

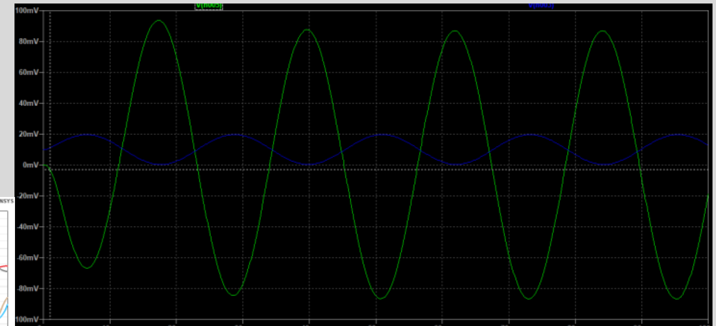


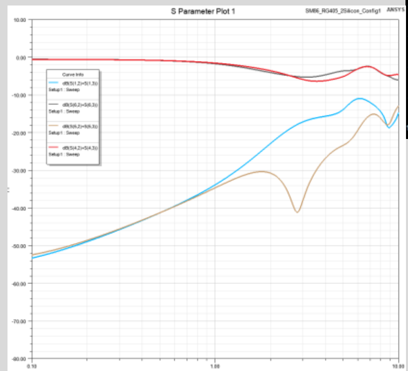
Simulation - LTspice

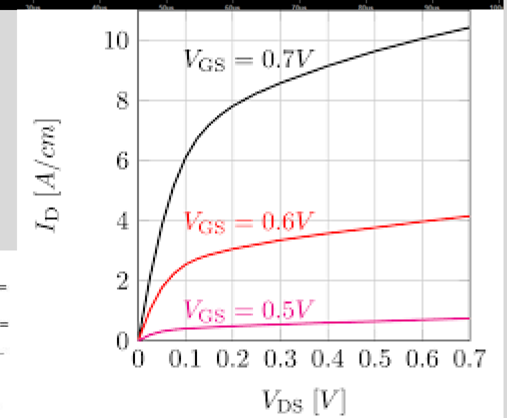
- ADS by Keysight
- Electronics Desktop by Ansys
- LTspice by Analog Devices
- Qucs (under GPL license)

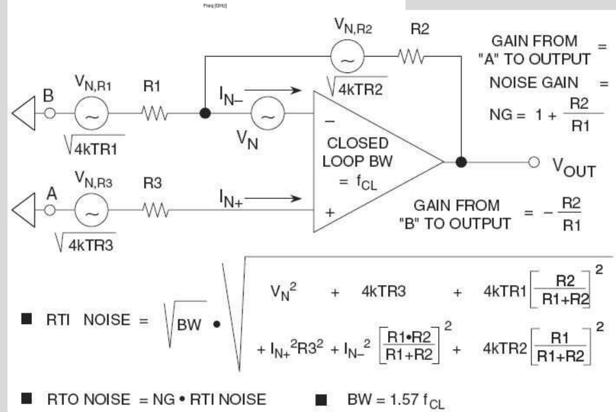
Simulation - LTspice

- Transient
- AC
- DC Sweep
- Noise



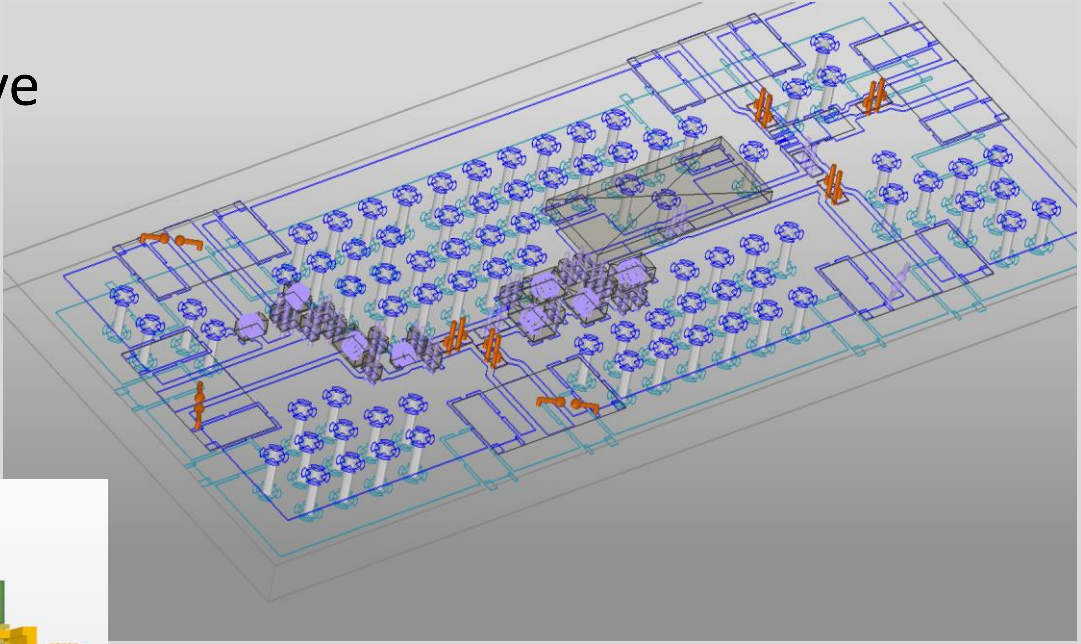


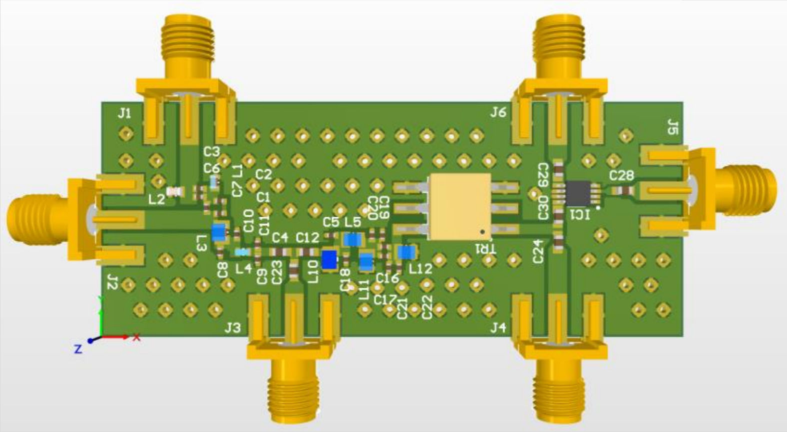




Simulation - LTspice

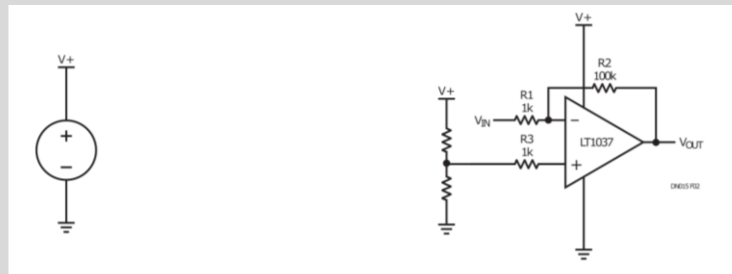
- Layout Level - SIwave

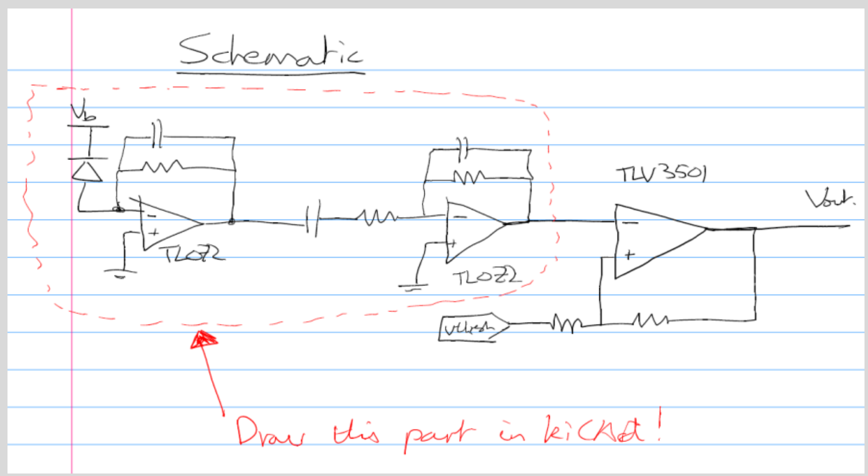




Simulation - LTspice

- Transient
- AC
- Noise





Thanks to Daniel Weatherill