Transistor layout: 250 – 28 nm, FinFETs

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Radiation damage

- **Cumulative effects**
  - Accumulating during the whole lifetime of the experiment
  - Due to the energy deposited by radiation in the electronics
  - Leads to device degradation or even failure
  - Two types:
    - **Ionisation → Total Ionising Dose (TID)** = Measurement of the energy dose deposited by radiation in the material in the form of ionising radiation, typically measured in rad or Gray (100 rad = 1 Gray)
    - **Non-ionisation → Displacement or fluence**, expressed in particles/cm^2

- **Single Event Effects (SEEs)**
  - Very localised event induced by a single particle
  - Due to the energy deposited by one single particle in the electronic device
  - Leads to failure, at any moment
  - Two types:
    - **Single Event Upset (SEU)** –Transient effect
    - **Single Effect Latch-up (SEL**) –Catastrophic SEE, Permanent effect

F. Faccio, Radiation effects in the electronics for CMS

Radiation damage

This lecture

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F. Faccio, Radiation effects in the electronics for CMS

Radiation damage – Total Ionising Dose (TID)

Ionisation in SiO_2

↓

Creation of electron-hole pairs

↓

Build-up of charge/defects

↓

Device degradation

F. Faccio, Radiation effects in the electronics for CMS

Total Ionising Dose (TID) effects on MOS transistors

- TID mechanism = Hole trapping in oxides

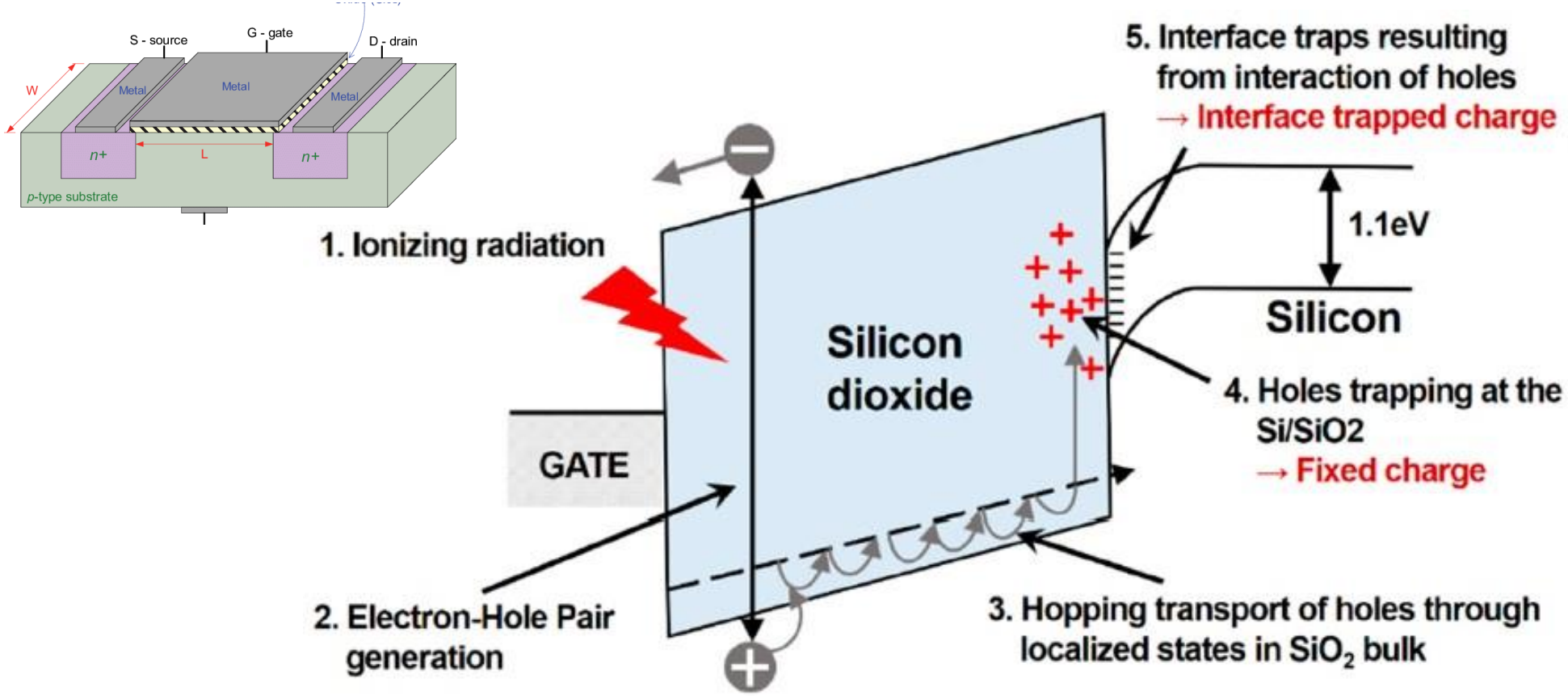


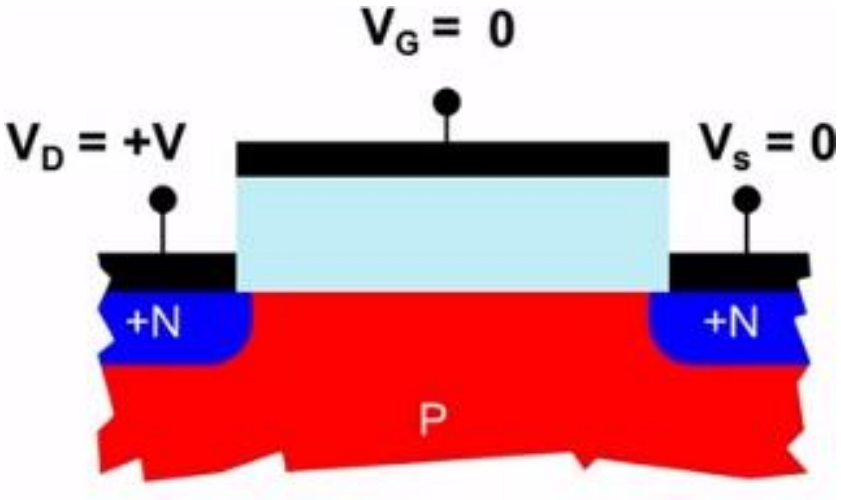
Fig. 1. Band diagram of an MOS capacitor with a positive gate bias. Illustrated are the main processes for radiation-induced charge generation.

M. Lee, doi.org/10.3390/Electronics10080887, 2021

Trapped holes →
Threshold voltage shift, leakage current increase, fast formation, annealing

Interface states →
Threshold voltage shift, transconductance, slow formation, no annealing below 400°C

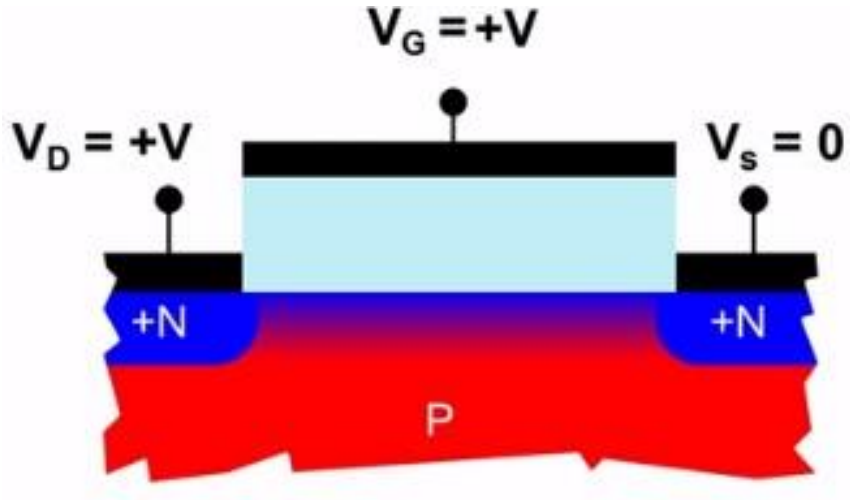
TID effects – Trapped charge – nMOS transistors



N-channel (nMOS)

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – nMOS transistors

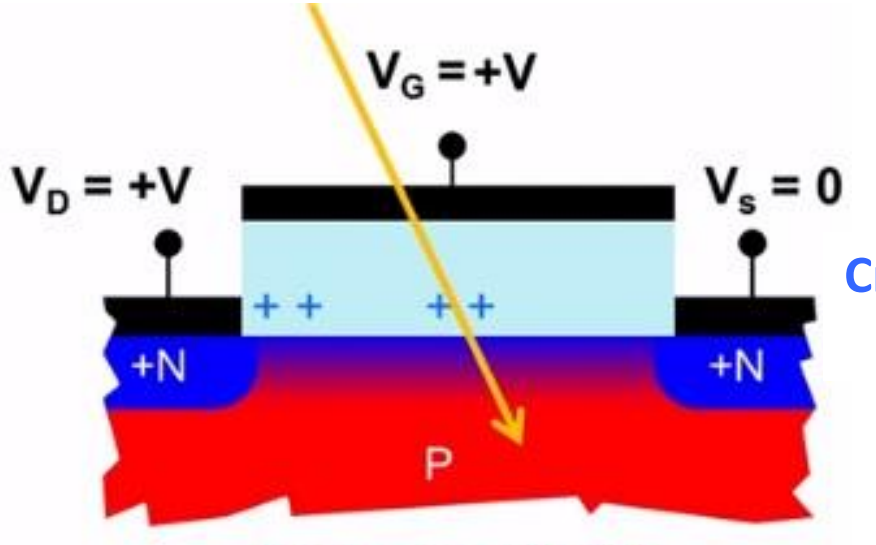


N-channel (nMOS)
"ON" (channel conducting)

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – nMOS transistors

Radiation event

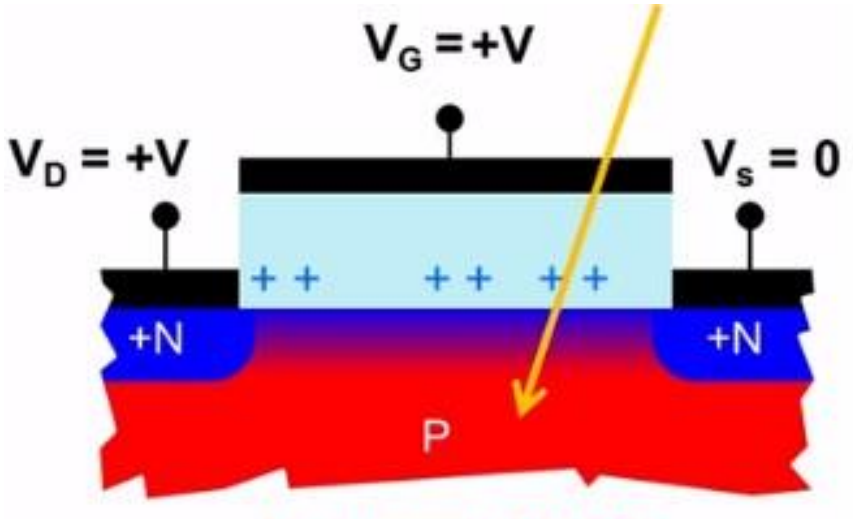


Creation of positive charge in the oxide region

N-channel (nMOS)

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – nMOS transistors



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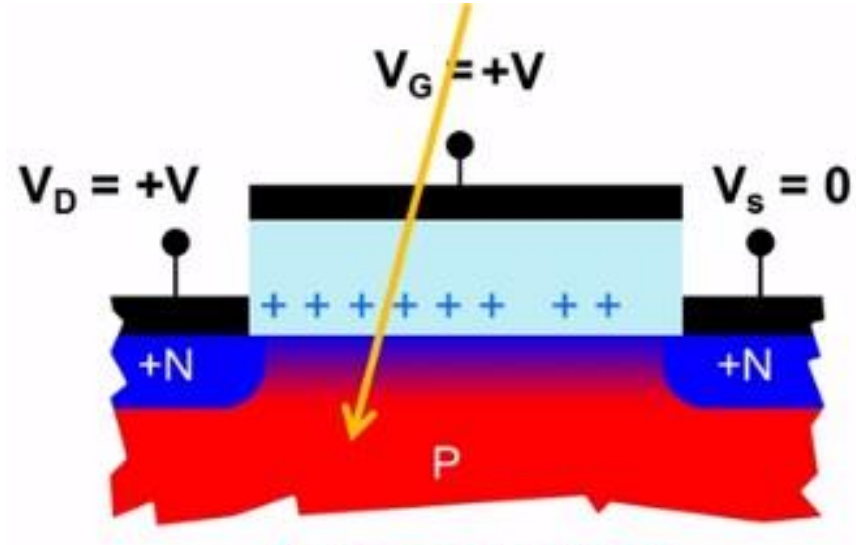
TID effects – Trapped charge – nMOS transistors



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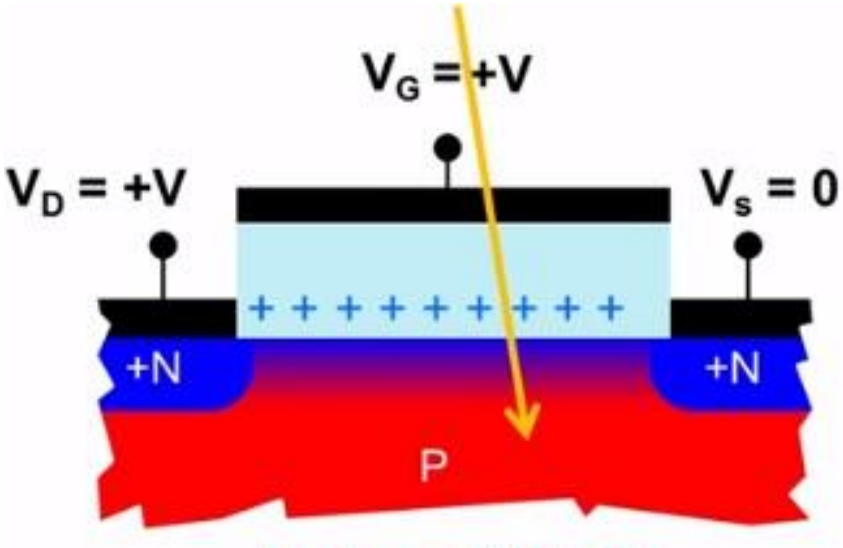

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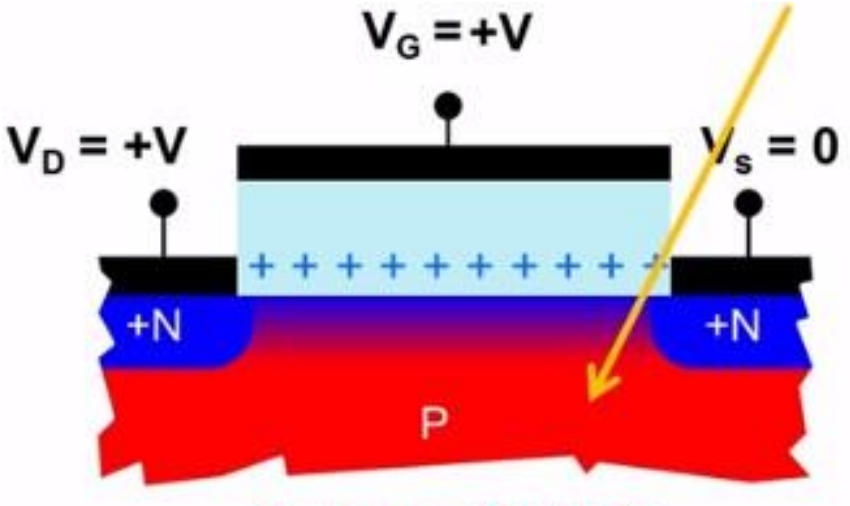

N-channel (nMOS)

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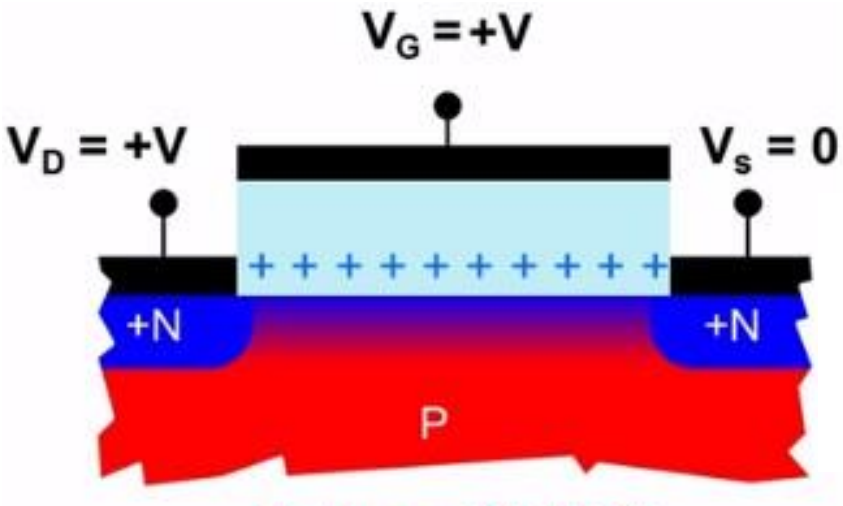
TID effects – Trapped charge – nMOS transistors

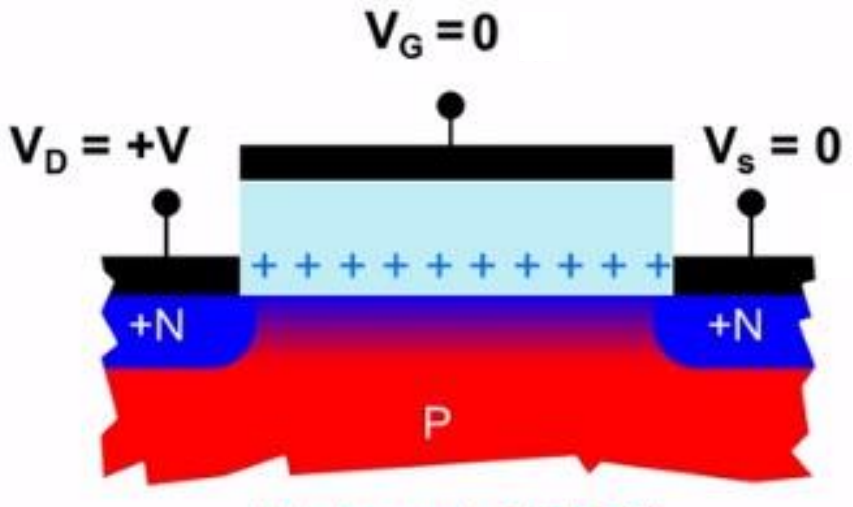


N-channel (nMOS)

The positive charge attracts more electrons, equivalent to applying a small $V_G > 0$ V

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – nMOS transistors



Leakage current ↑↑

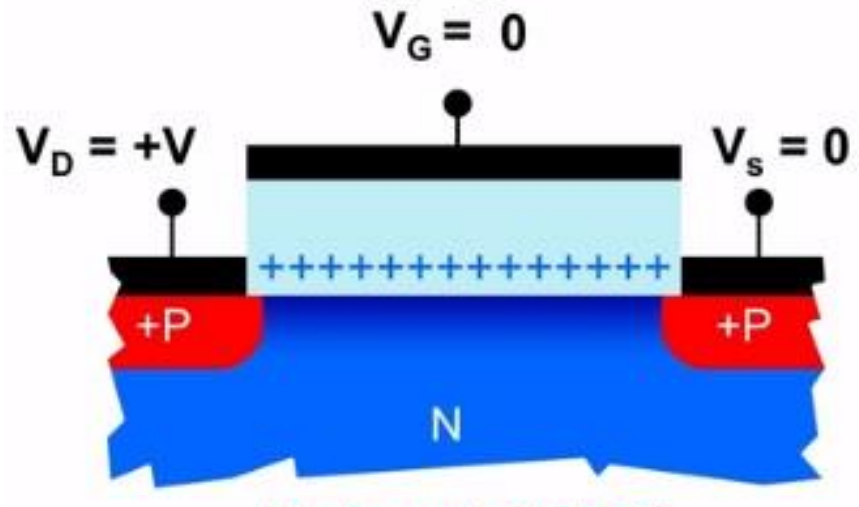
N-channel (nMOS)
still "ON" with V_G

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – nMOS transistors

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – pMOS transistors



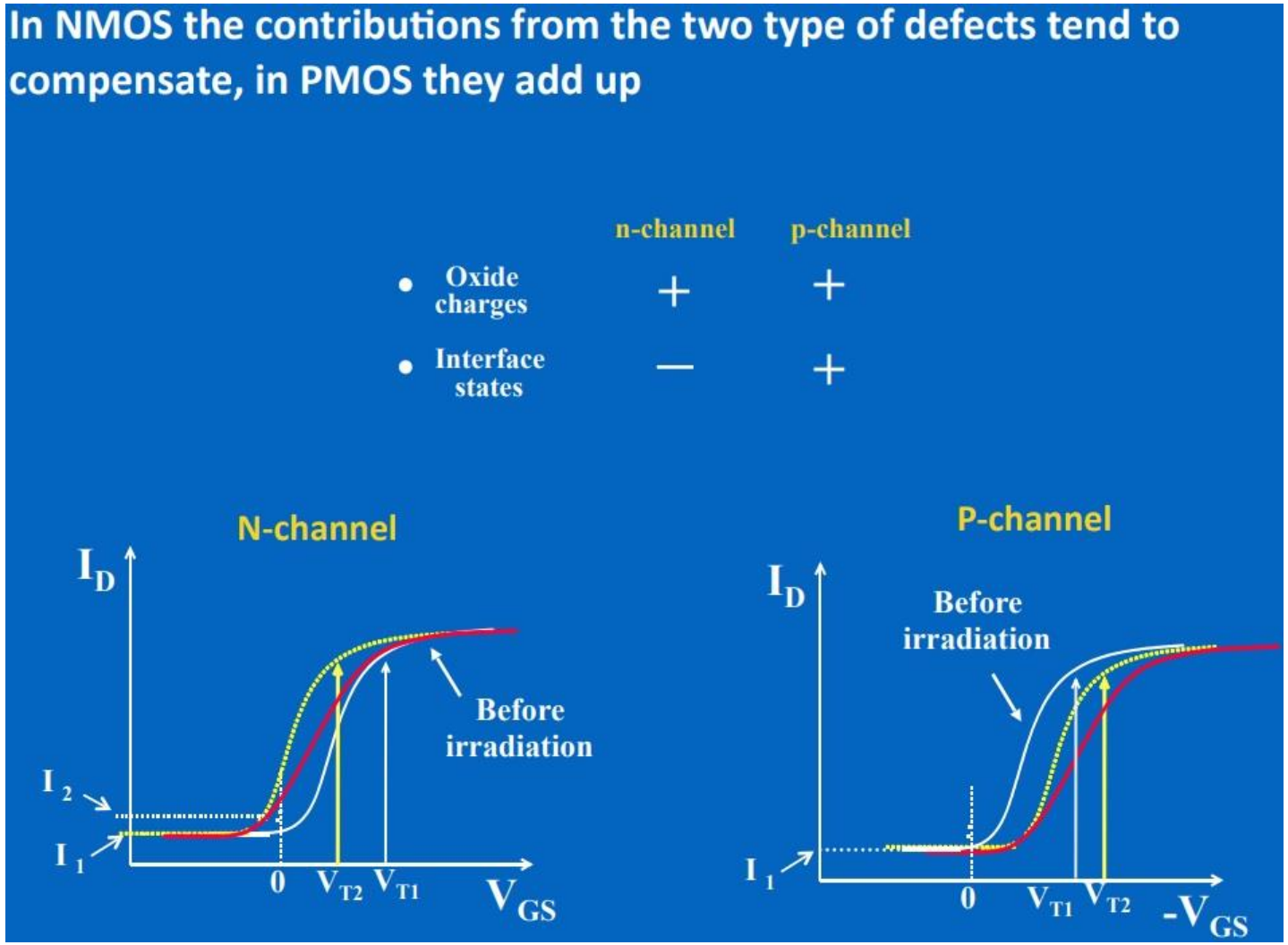
P-channel (pMOS)
"OFF" even with V_G

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Trapped charge – pMOS transistors

Texas Instruments training & videos, https://training.ti.com/total-ionizing-dose-effects-mosfets

TID effects – Consequences – Threshold voltage shift



F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

TID effects – Consequences – Threshold voltage shift

- **Threshold voltage shift** = $\Delta V_T = f(\Delta V_{OX}, \Delta V_{IT})$
  - **Due to charged trapped in the oxide,** ΔV_{OX}
    - In an nMOS transistor, the trapped positive charge causes negative shifts of the threshold voltages
    - The positive charge trapped in the oxide repels the holes in the channel = To re-create the same inversion condition the gate requires a less positive voltage
    - For a pMOS transistor, it is the opposite

These trapped holes give rise to a threshold voltage shift, ΔV_{ox}, given by:

$$\Delta V_{ox} = -\frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho(x) dx = -\left(\frac{q}{\varepsilon_{ox}}\right) t_{ox} \Delta N_{ot}, \qquad (2.1)$$

where q is the electron charge, $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the oxide capacitance, ε_{ox} is the dielectric constant of SiO_2 and t_{ox} is the thickness of the oxide, $\rho(x)$ is the spatial distribution of the oxide charge density, and ΔN_{ot} is the trapped charge density referred to the SiO_2-Si interface.

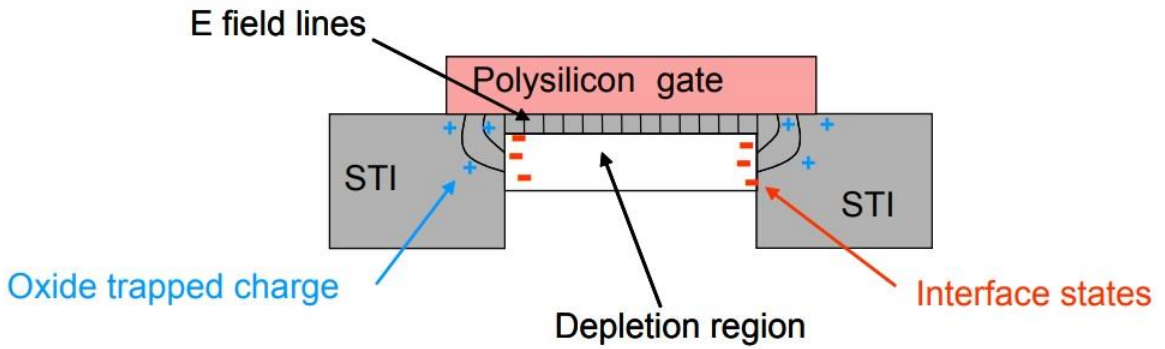
  - **Due to charged trapped in the interface,** ΔV_{IT}
    - Threshold voltage shift due to increasing charged trapped at the interface region is a relatively slower phenomenon than the build-up of positive charge in the oxide. ΔV_{IT} can be slower than ΔV_{OX}.
  - The threshold voltage shift for nMOS transistors as a function of the total dose can be negative at the beginning and become positive at a later time (rebound effect).

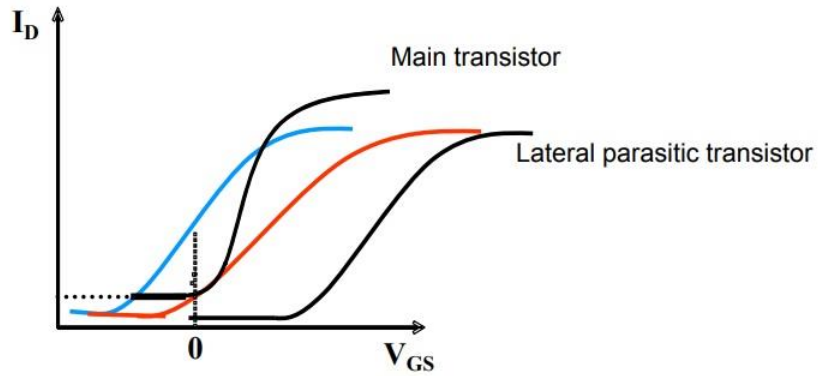
L. Chen, Radiation tolerant design with 0.18-micron CMOS technology, PhD thesis

TID effects – Consequences – Leakage current

- **Increase of leakage current**

The leakage current in NMOS is due to the accumulation of defects in the lateral Shallow Trench Isolation (STI) oxide

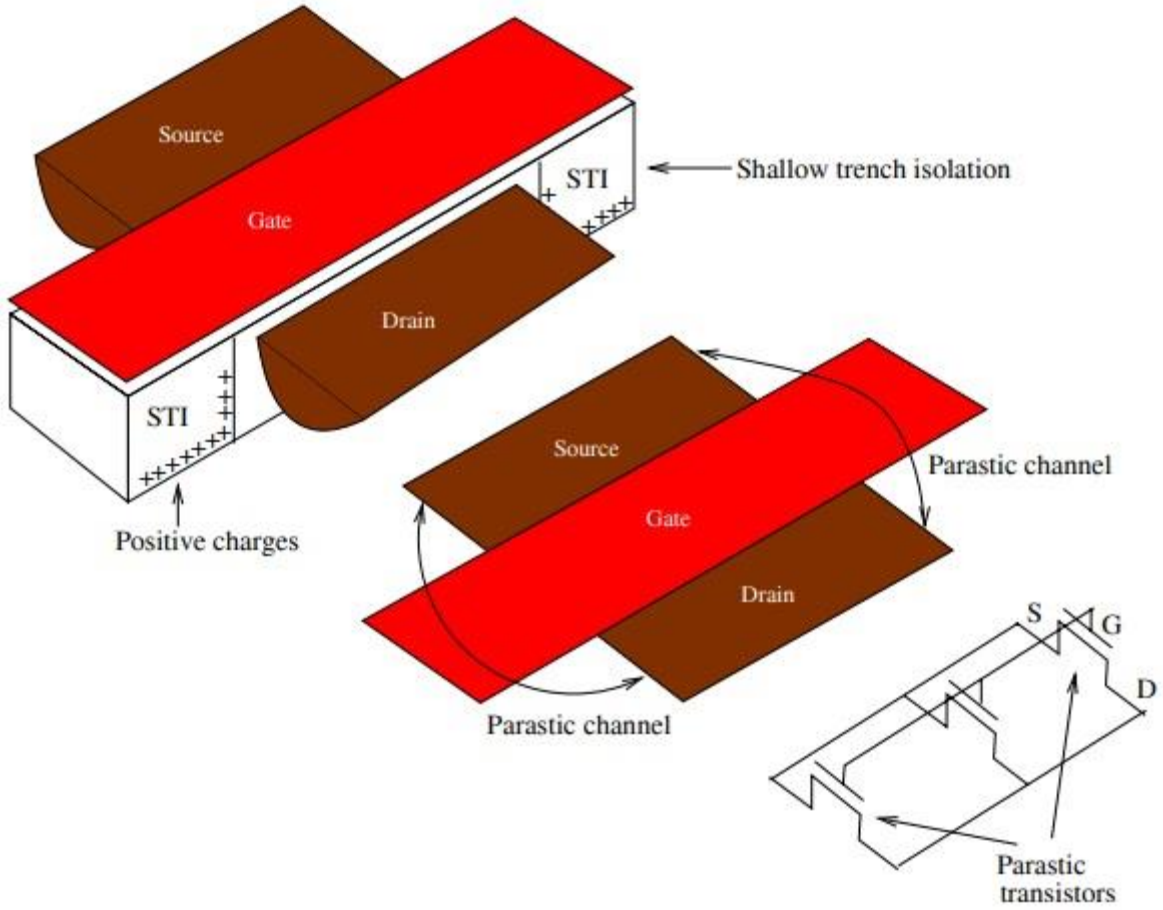




F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

TID effects – Consequences – Leakage current

- **Increase of leakage current**



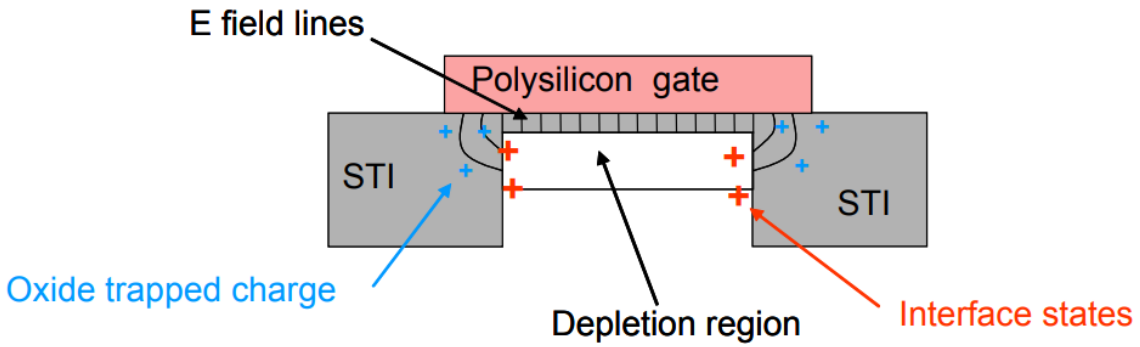
Leakage current also appears between adjacent n-type diffusions

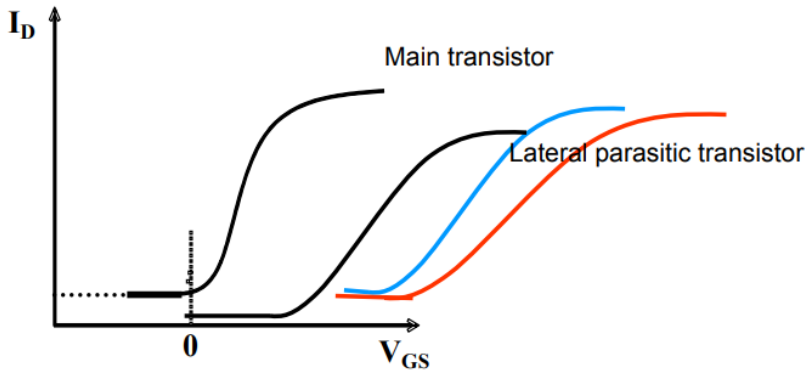
L. Chen, Radiation tolerant design with 0.18-micron CMOS technology, PhD thesis

TID effects – Consequences – Leakage current

- **Increase of leakage current**

In PMOS both type of defects increase the threshold of the parasitic lateral transistor, and no leakage current can be observed

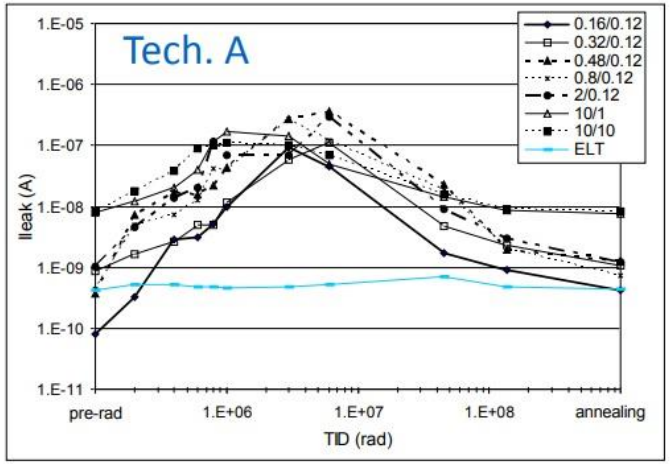


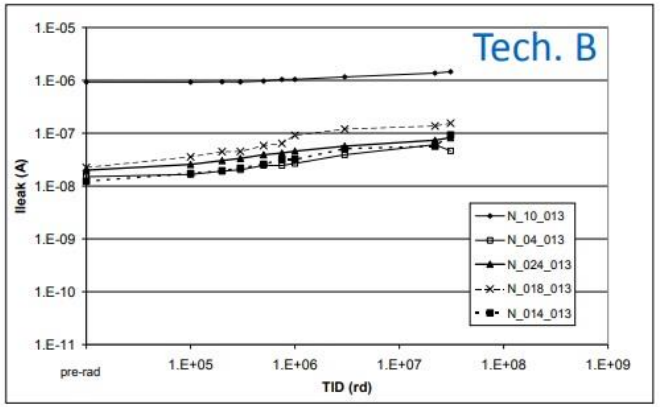


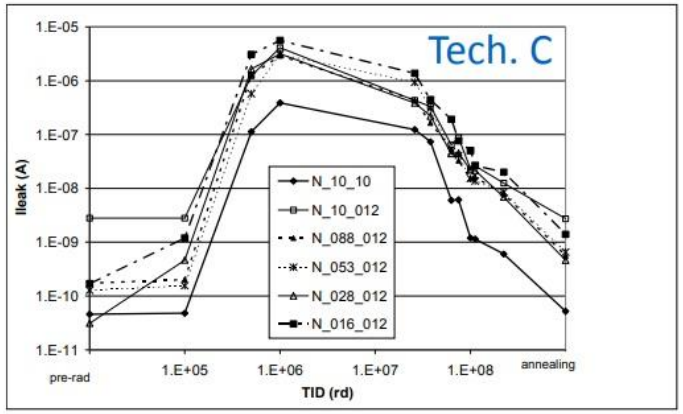
F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

TID effects – Consequences – Leakage current

The leakage paths are technology dependent
(here this is shown for source-drain leakage currents in NMOS)







F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

TID effects – Consequences – Mobility decrease

- **Decrease of mobility and transconductance**
  - Due to increase of the interface traps (conduction in MOS transistors is due to carrier motion close to the SiO_2-Si interface)
  - Mobility trend as a function of the trap increase expressed as:

$$\mu = \frac{\mu_0}{1 + \alpha \cdot \Delta N_{it}}, \qquad (2.5)$$

where μ_0 is the pre-irradiation mobility, ΔN_{it} is the increase of the interface traps and α is a parameter whose value depends on the technology. The degradation of the mobility gives origin to degradation in the transconductance, which is proportional to μ in the linear region and to $\mu^{1/2}$ in saturation. This decreases the driving capability of the device.

L. Chen, Radiation tolerant design with 0.18-micron CMOS technology, PhD thesis

TID effects – Consequences – Noise increase

- **Noise increase**
  - Increase in white noise (frequency independent)
  - Increase in 1/f noise (flicker noise)
  - Due to the increase of the concentration of the interface traps and the traps in the oxide near the interface

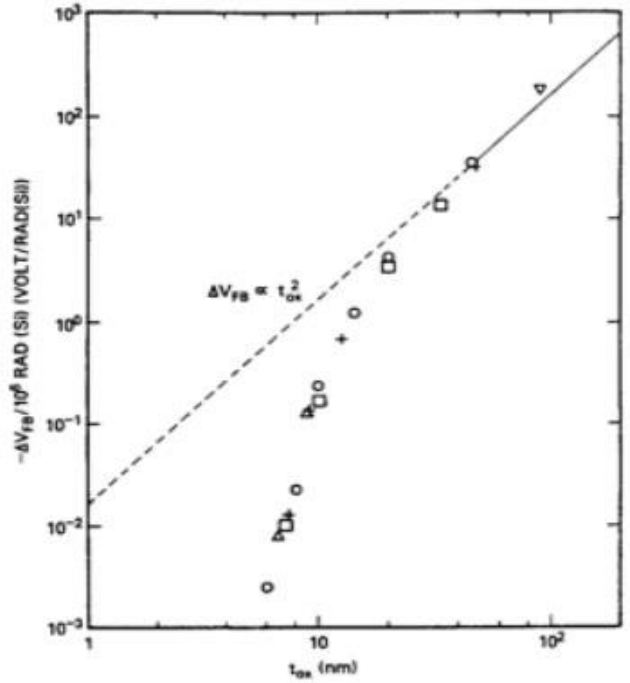
L. Chen, Radiation tolerant design with 0.18-micron CMOS technology, PhD thesis

Can we mitigate (some of) these problems?

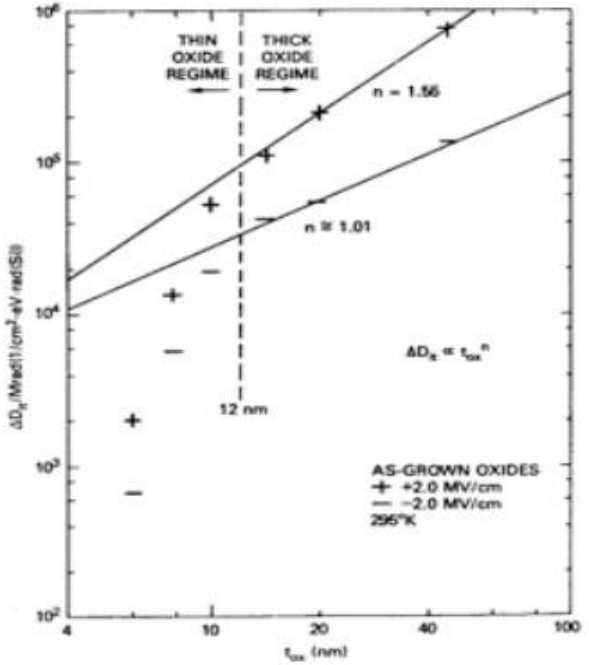
TID effects – Solutions

The accumulation of both type of 'defects' decreases with the thickness of the oxide

Oxide trapped charge



Interface states

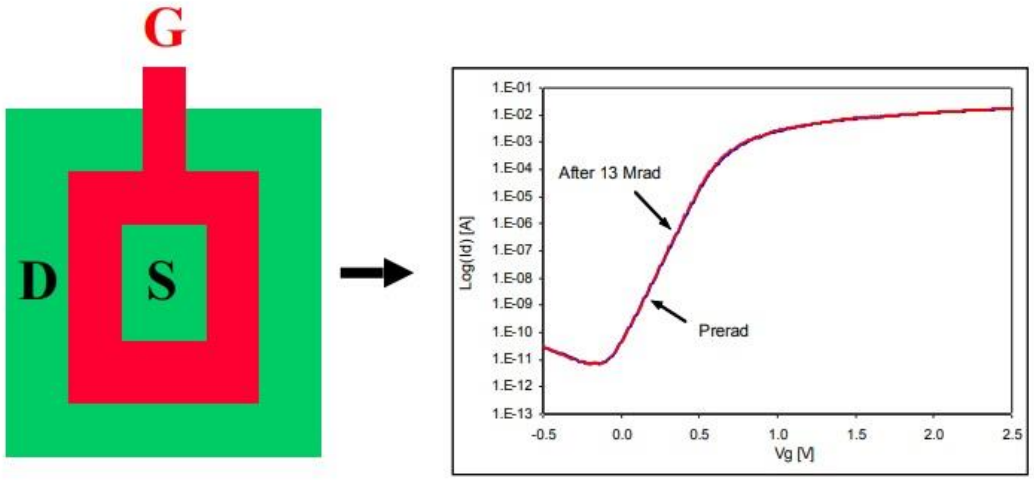


N.S. Saks et al., IEEE TNS, Dec. 1984 and Dec. 1986

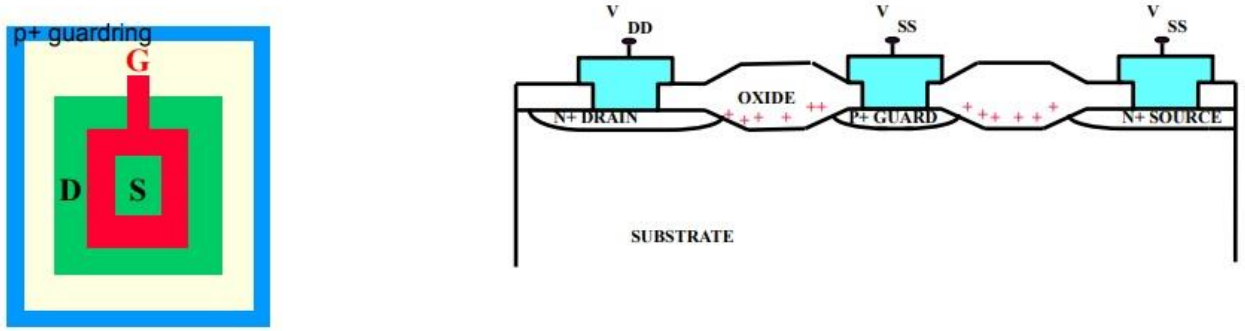
F. Faccio, Radiation effects in CMOS technologies for the LHC upgrades

TID effects – Solutions

Source-Drain leakage is eliminated by the Enclosed Layout Transistor (ELT)…



Inter-diffusion leakage is eliminated by p+ guard rings…



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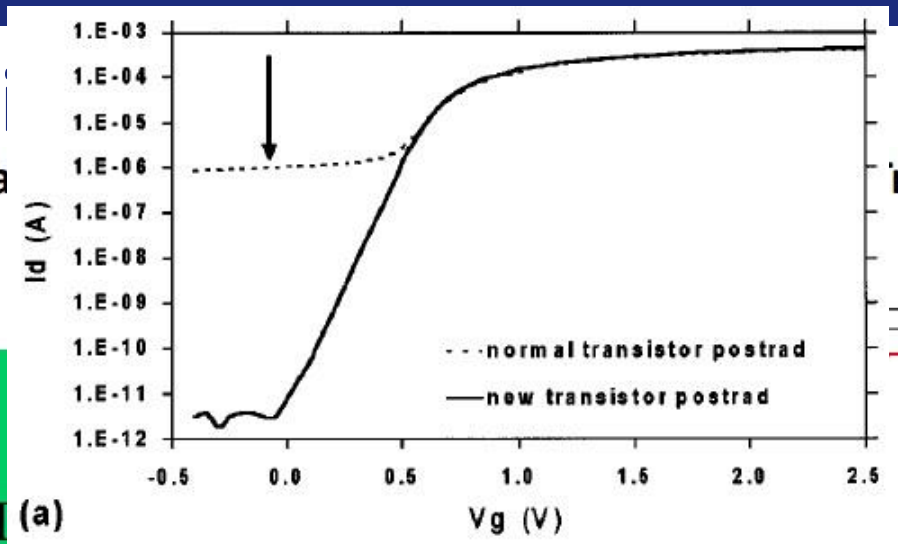
TID effects – Soluti

Source-Drain lea

ransistor (ELT)...

Inter-diffusion



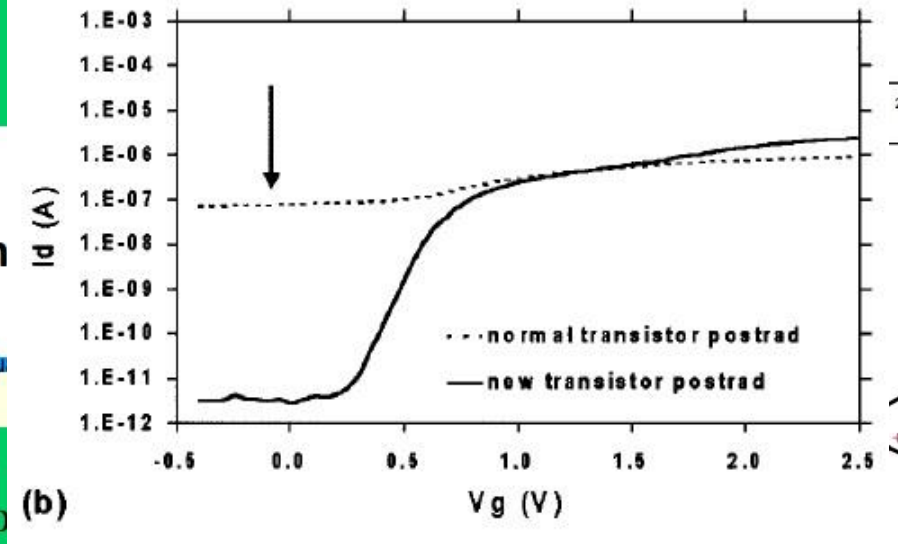
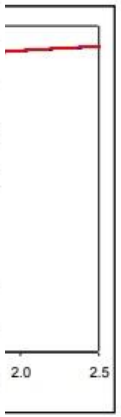
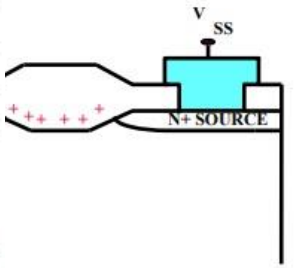


Fig. 10. (a) Transistor measurements after irradiation [dose 40 Mrad(SiO_2)] W/L = 10 μm/0.28 μm. (b) W/L = 0.64 μm/10 μm. The normal transistor shows severe post-irradiation leakage (arrow). The behavior of the new transistor is virtually unaffected by the irradiation. The turning on of the channel underneath the poly of the opposite type remains present and can be observed for the long transistor (around 1.6 V and up).





W. Snoeys, A new nMOS layout structure for radiation tolerance, 2002

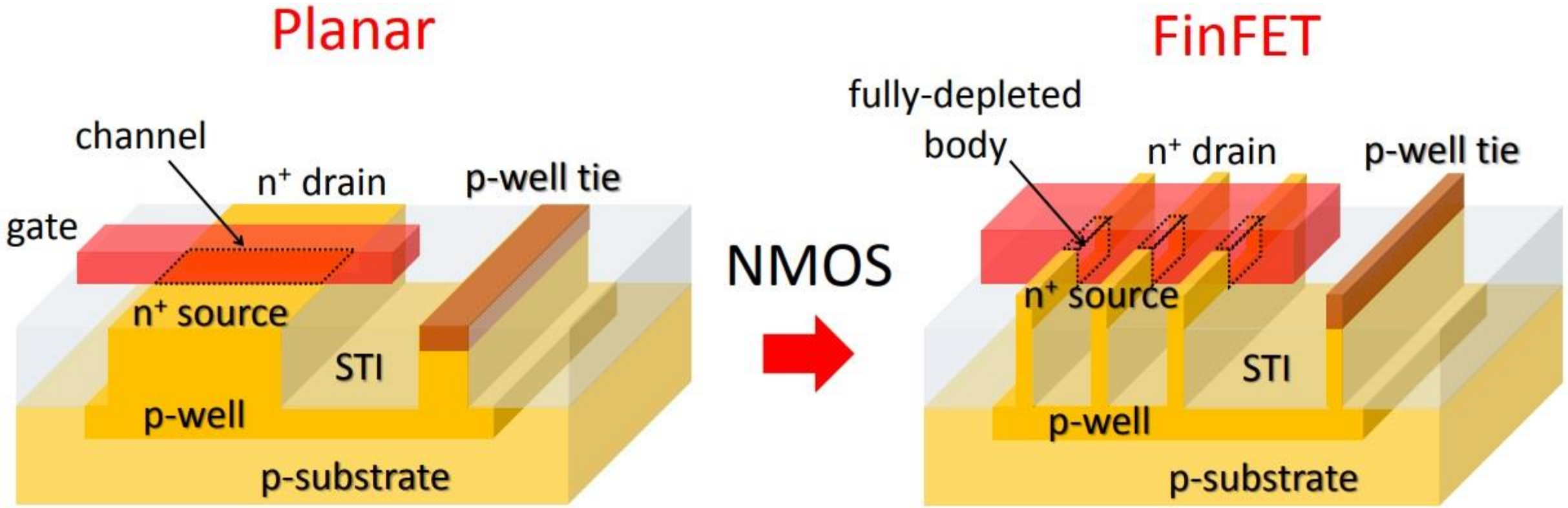
TID effects – Solutions

- **Enclosed Layout Transistors… Very nice, but…**
  - They tend to occupy more area than the conventional linear transistors, for the same (W/L)
  - Not all (W/L) combinations are possible
  - They do not exist in design libraries provided by foundries (usually)
  - Not recognised by verification tools typically used to verify designs before submission for fabrication

Recipe to mitigate TID effects

- **Use a technology with a small technology node (e.g. 65 nm is better than 180 nm)**
- **Use Enclosed Layout Transistors**
  - For nMOS transistors only
  - For critical transistors
    - in the analogue readout electronics –yes!
    - in the digital readout electronics, the designers need to evaluate if it is really necessary, benefits…
- **Use as many guard rings as possible**

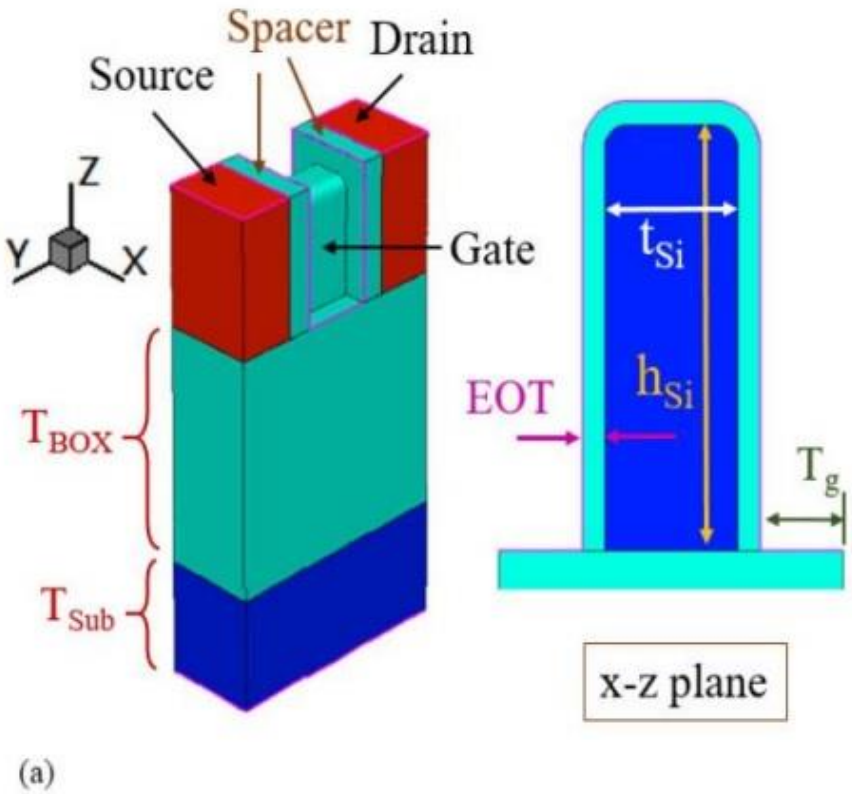
Planar nMOS vs FinFET

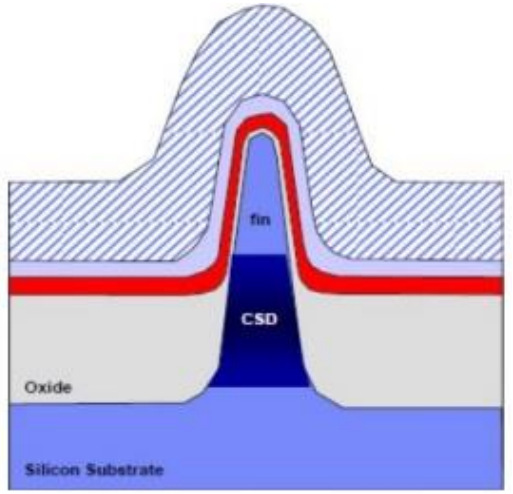


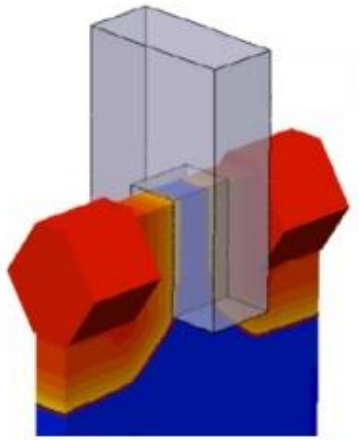
M. Campbell & F. Faccio, Future ASIC technologies in HEP experiments

FinFETs

- Most commercial fabs have migrated to FinFETs below 20-nm gate length feature sizes
- FinFETs exhibit improved electrostatic control of the channel and improved reliability compared to equivalent scaled planar CMOS





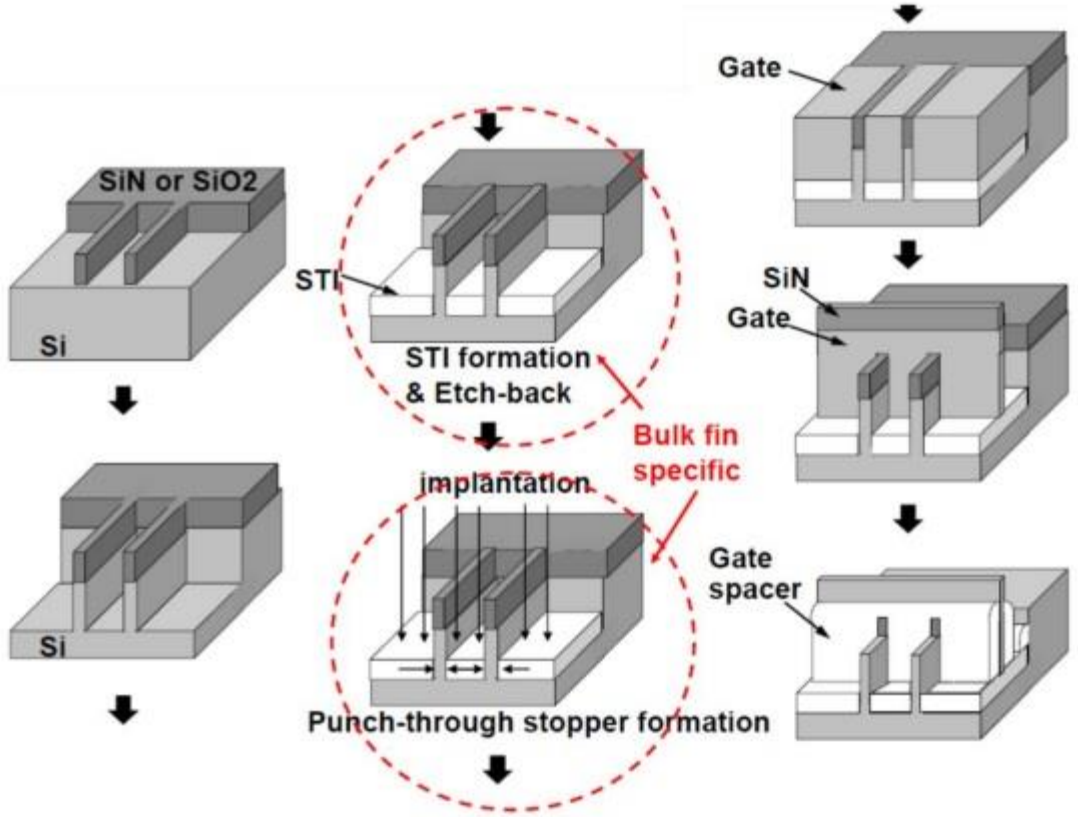


T. Hook, FDSOI Conference, Taiwan, 2013

M. Campbell & F. Faccio, Future ASIC technologies in HEP experiments

FinFET processing technology

- Increasing processing complexity
- More challenging lithography
  - Quad patterning
  - Soon EUV
- Line edge roughness
- Isolation steps
  - STI
  - CSD/SSRW



A. Yagishita (Toshiba), SOI Short Course (2009)

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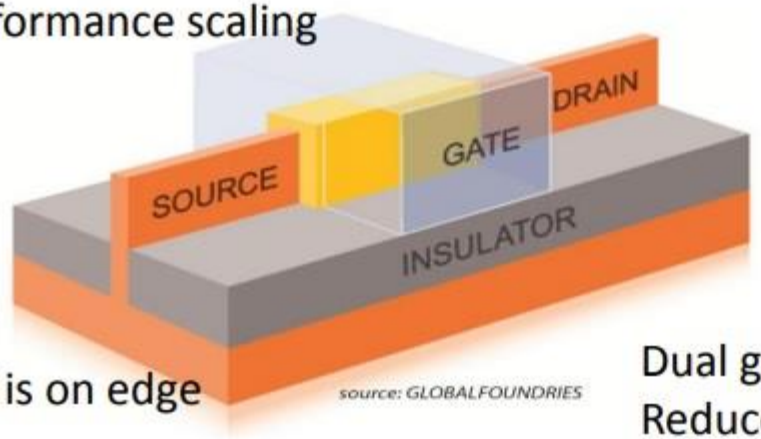
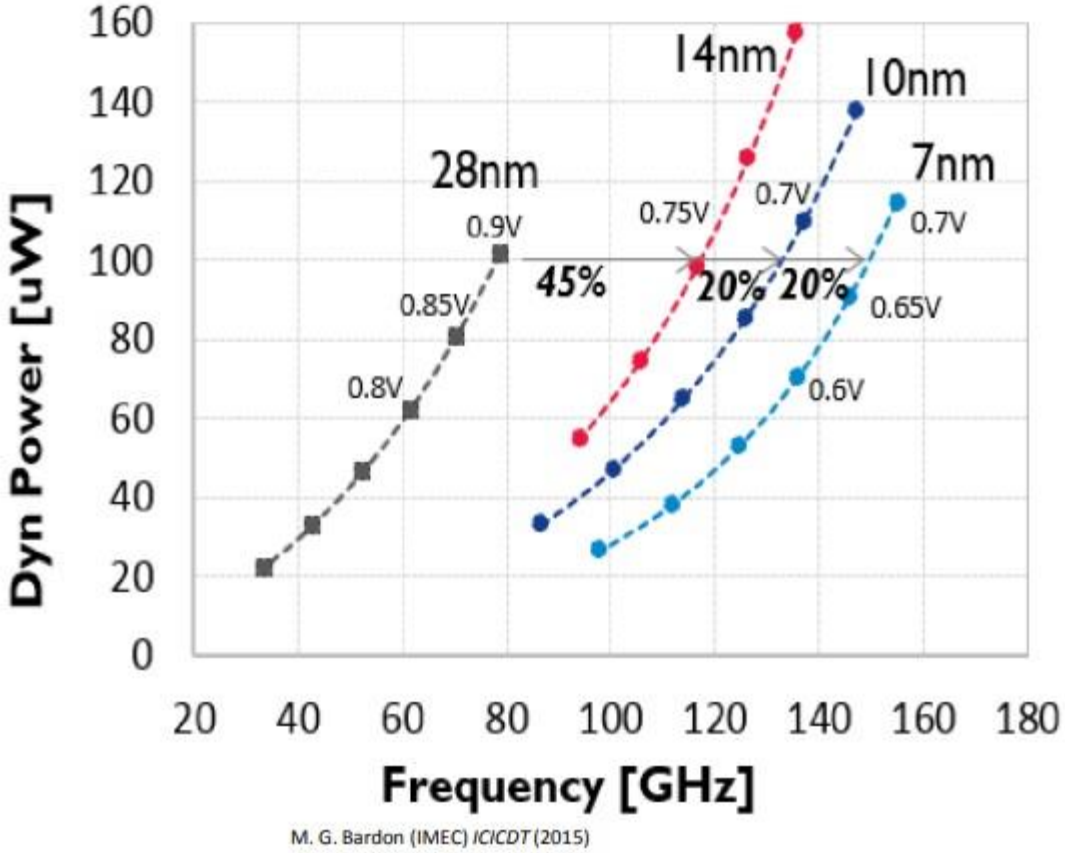
FinFET – Advantages / challenges

Gate length shrink
Performance scaling



FET is on edge

Dual gate
Reduces I_{off}

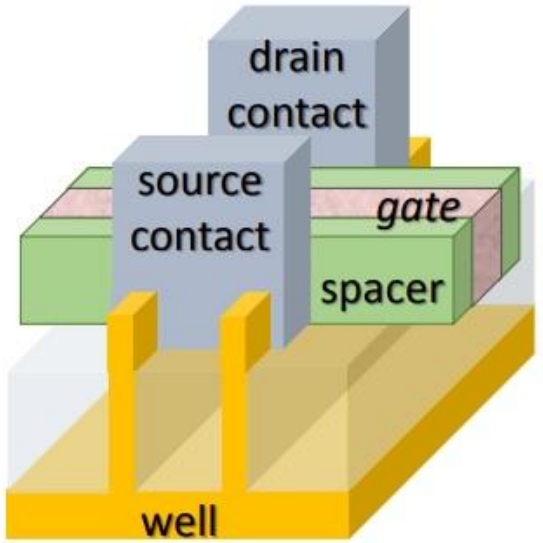


M. G. Bardon (IMEC) *ICICDT* (2015)

M. Campbell & F. Faccio, Future ASIC technologies in HEP experiments

FinFET – Design

- More drive current for given footprint
- Quantized channel width
  - Challenge for logic & SRAM
  - OK for analog, enough g_m granularity
- Less DIBL → better r_{out}, 3× intrinsic gain
- Essentially no body effect ($\Delta V_T < 10mV$)
- Higher R_s & R_d spreading resistance
- Lower C_j but higher C_{gd} & C_{gs} coupling
- Higher R_{well} (R_{diode}, latch-up)
- Mismatch depends on fin geometry, MG grains, gate density, stress, less on RDF



Sheu, TSMC [18]
Hsueh *et al.*, TSMC [19]

Slide courtesy of Alvin Loke, Qualcomm

Thank you for your attention