Device structures: monolithic

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Eva Vilella – Who I am…

2009 BSc Electronic Engineer @ Uni Barcelona

2010 MSc Electronic Engineer @ Uni Barcelona

2013 PhD Engineering and Advanced Technologies @ Uni Barcelona

Universitat de Barcelona

2014 Postdoc @ Uni Liverpool – HV-CMOS R&D

UNIVERSITY OF LIVERPOOL

2017 Started HV-CMOS Working Group within CERN-RD50 collaboration

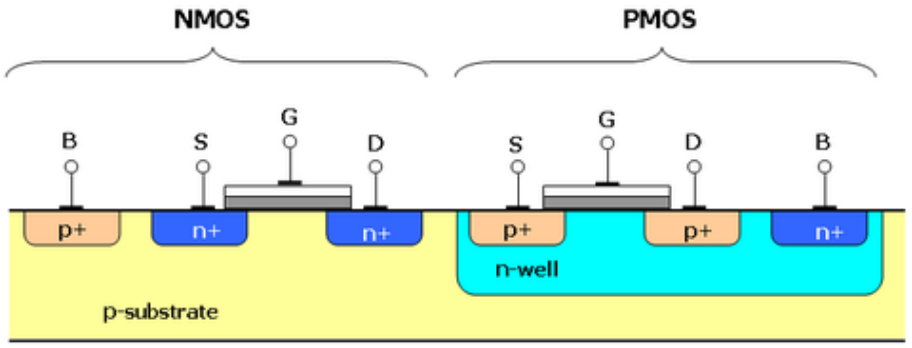
2018 Co-proposed using HV-CMOS sensors for the LHCb Mighty Tracker upgrade

2019 UKRI Future Leaders Fellow – HV-CMOS R&D Group Leader

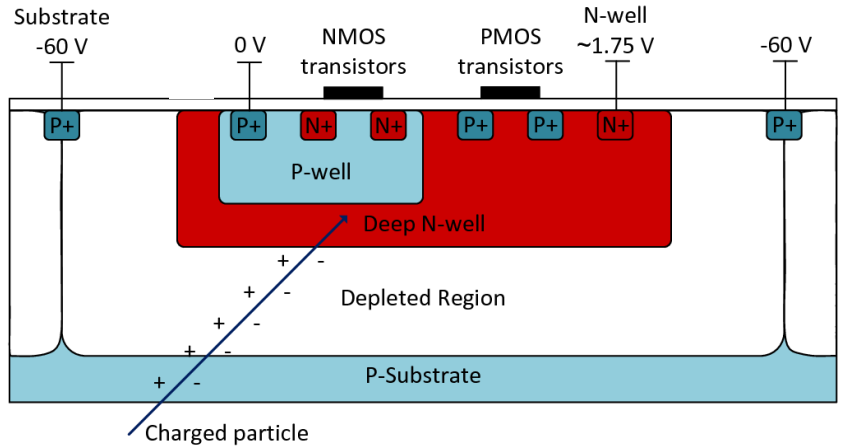
AIDA innova UK Research and Innovation UNIVERSITY OF LIVERPOOL

Device structures: monolithic

- Monolithic refers to detectors that integrate the *sensing element* and *readout chip* in a single layer of silicon:
  - **CMOS**
  - **HV-CMOS**
- Both CMOS and HV-CMOS are *the* industry standard fabrication processes for MOSFET transistors used in integrated circuits (IC) chips:
  - **CMOS (Low Voltage)**
    - Image sensors
    - Microprocessors
    - Microcontrollers
    - Memories
    - Transceivers for communication
  - **HV-CMOS = CMOS + High Voltage substrate biasing & additional wells to isolate the electronics from the substrate**
    - Display and motor drivers



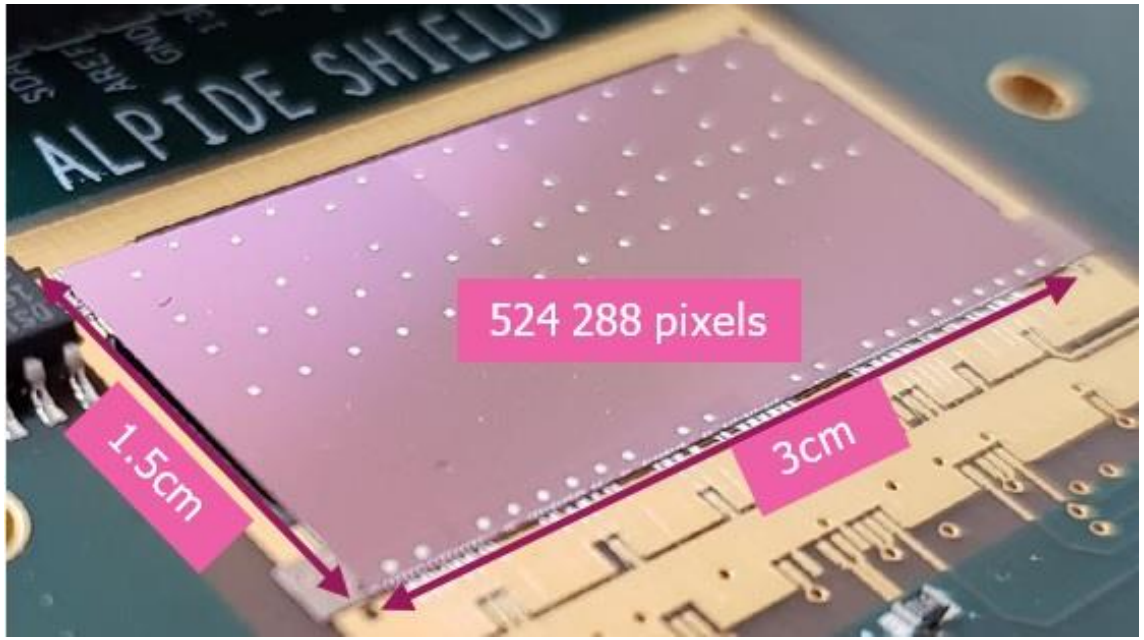
Wikipedia



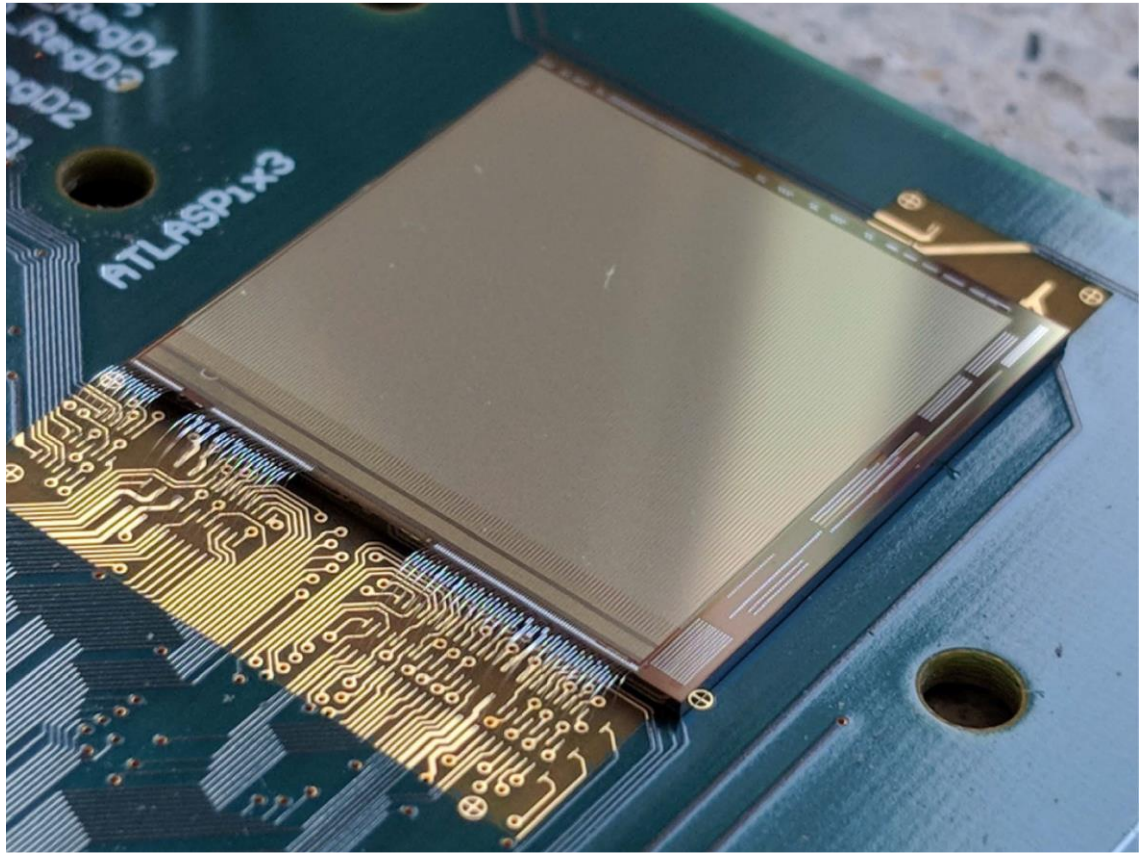
I. Kremastiotis, arXiv:1706.04470v2, 2017

Device structures: monolithic

- Can we use CMOS and HV-CMOS processes to fabricate detectors for physics experiments?
  - **Absolutely yes!!!**



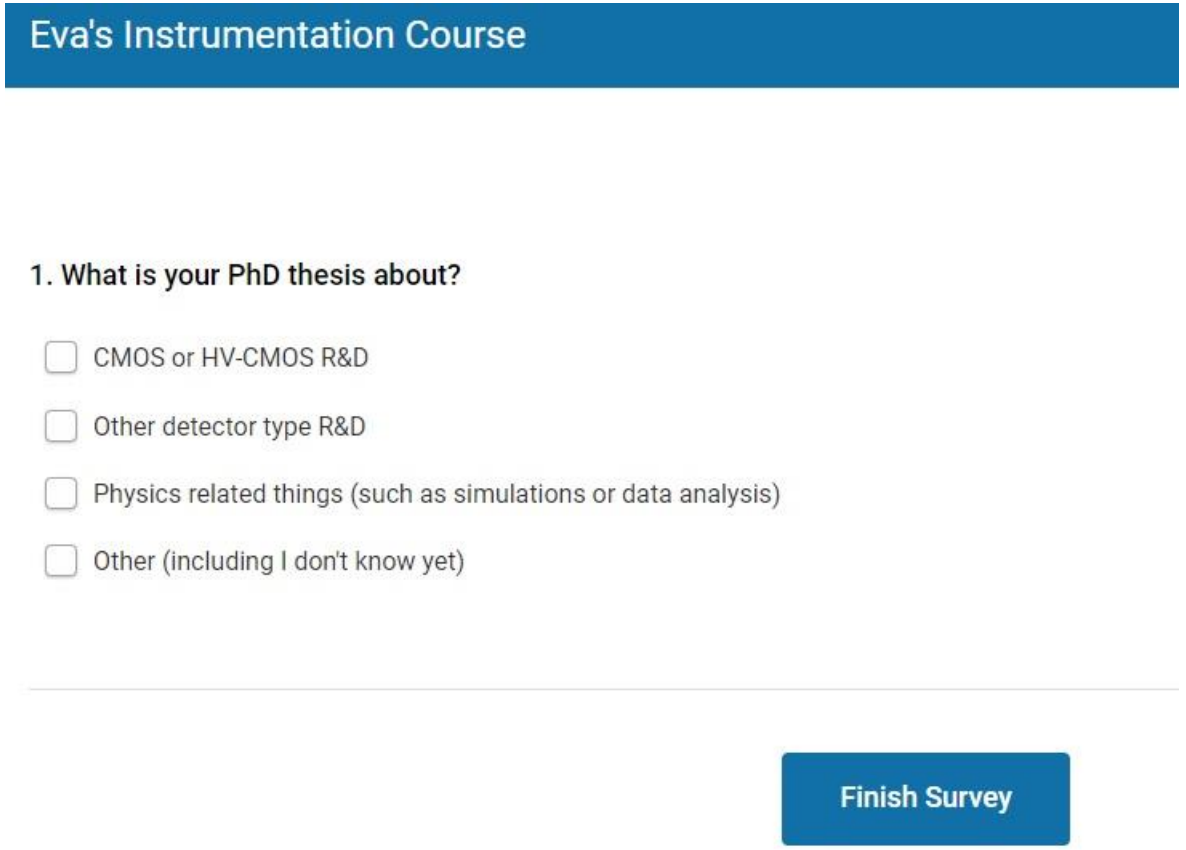
M. Mager, NIM-A: 824 434-438, 2016



I. Peric, 10.1109/JSSC.2021.3061760, 2021

Who are you?

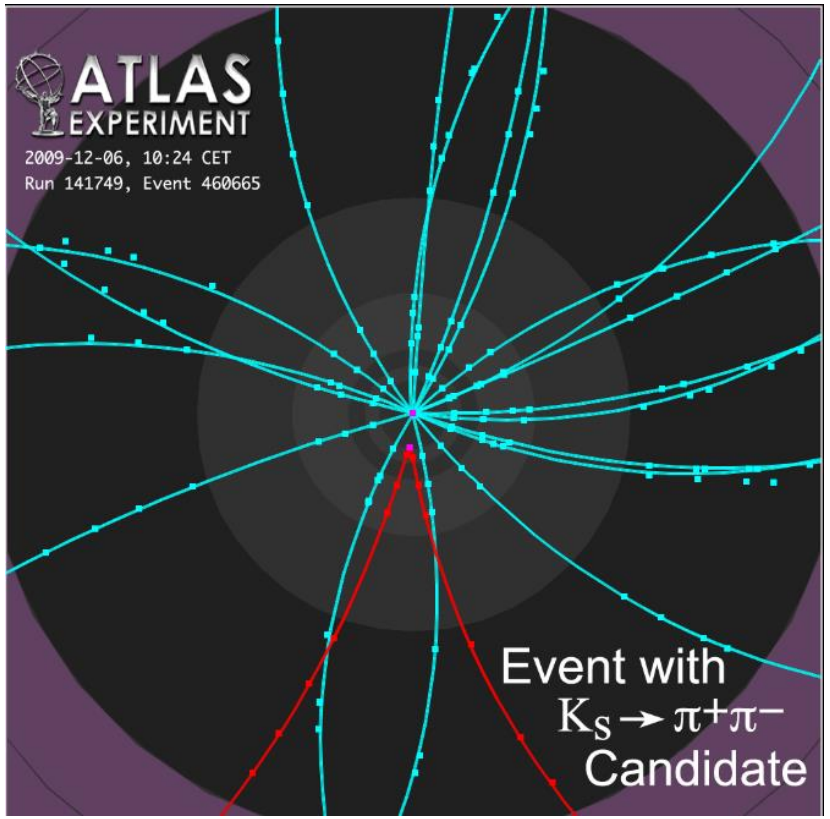
https://www.smartsurvey.co.uk/s/12T2Q7/



Particle tracking

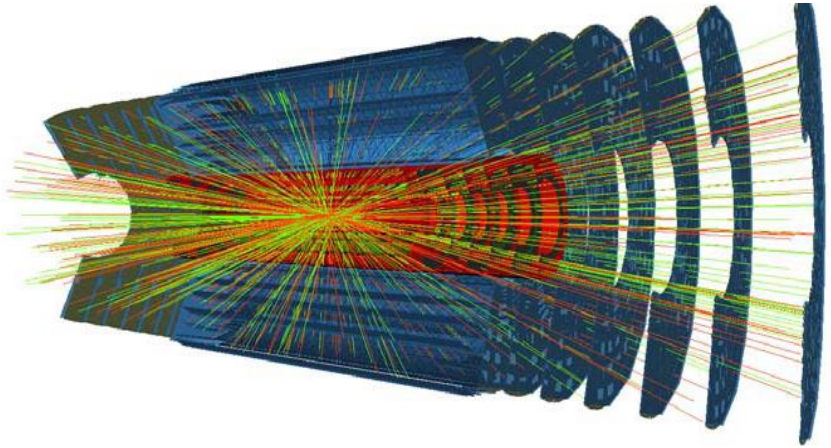
Follow the tracks of an animal and identify it from its footprint

Measure particle trajectories from hits they leave in silicon detectors

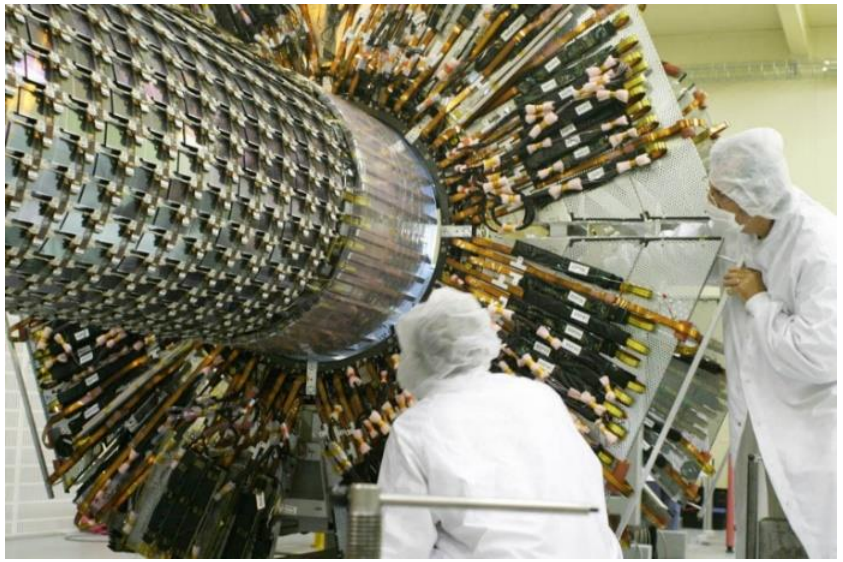


Connecting the dots: The **tracks** provide crucial information on a particle's direction, charge and energy.

The technological challenge



Billions of collisions per second produce 100's of billions of particles.
Above picture shows **one 25 ns frame with 1000s of particles**.

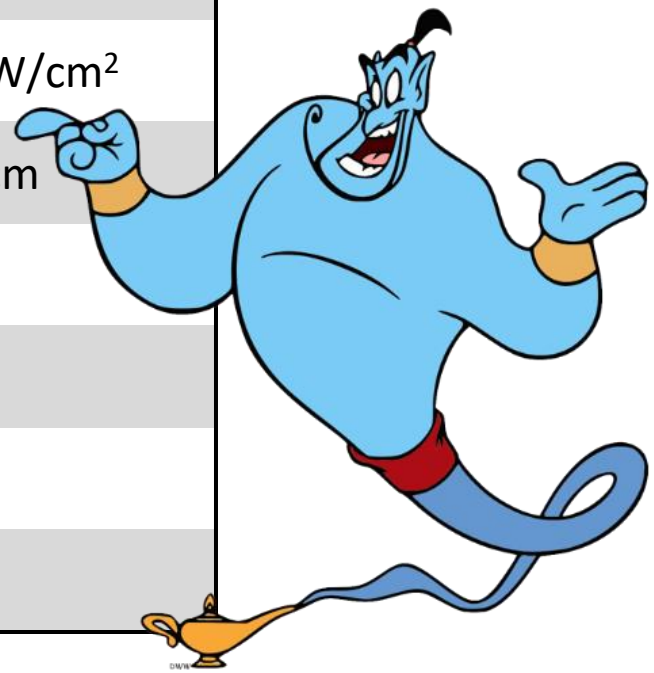


Detectors: Layers of thin silicon sensors measure accurate **hit points** along the particles' trajectories.

- Physics experiments require ever more precise and fast detectors to make high precision measurements in high intensity environments.
- Radiation tolerance is critical as detectors have to survive many years of operation.

Silicon tracking detectors – Specifications

Pixel size	Small	~ µm x µm
Time resolution	Excellent	< 100 ps
Radiation tolerance	High	> 10^{17} 1 MeV n_{eq}/cm^2
Material budget	Minimal	< 50 µm
Power consumption	Minimal	~10-100 mW/cm^2
Reticle size	Large	> 2 cm x 2 cm
Noise	Minimal	
Assembly process	As easy as possible	
Yield	High	
Price	Cheap	

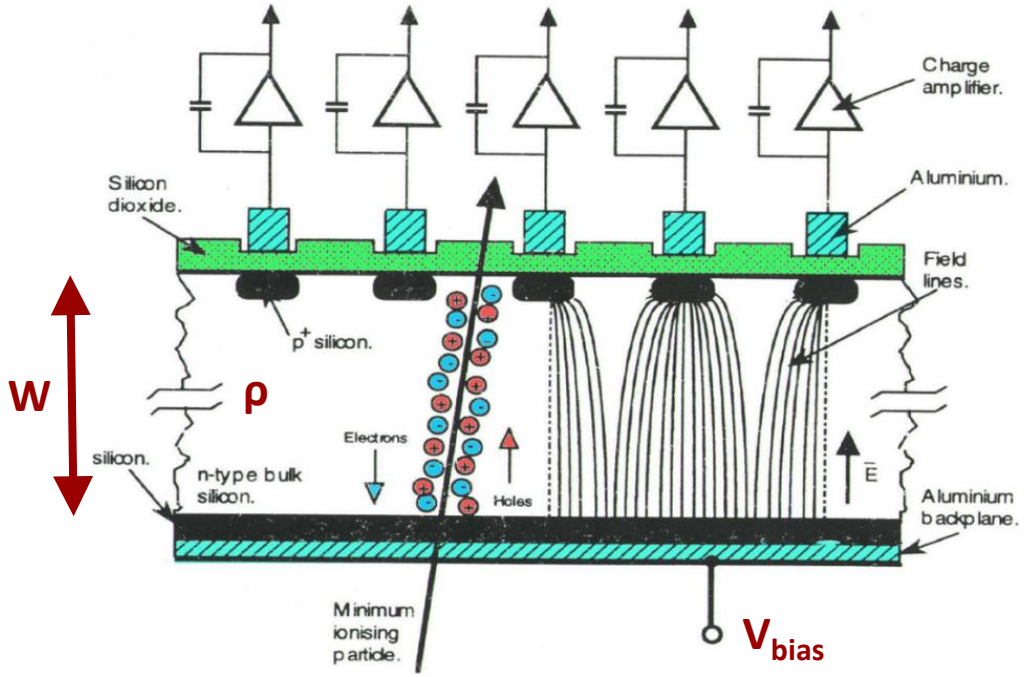


Sensor – Detection principle

- Silicon p-n diode in reverse bias
- A traversing particle creates e^-/h^+ pairs by ionization
- The electric field separates the e^-/h^+ pairs, which move to the detector electrodes where they generate signal
- Basic requirements:
  - **Large bias voltage (V_{bias})**
    - Larger W → larger signal
    - Faster charge collection
    - Better radiation tolerance
  - **High resistivity silicon bulk (ρ)**

  } ➔ $W = \sqrt{\rho \cdot V_{bias}}$

  - **Backside biasing**
    - More uniform electric field lines
    - Improved charge collection efficiency

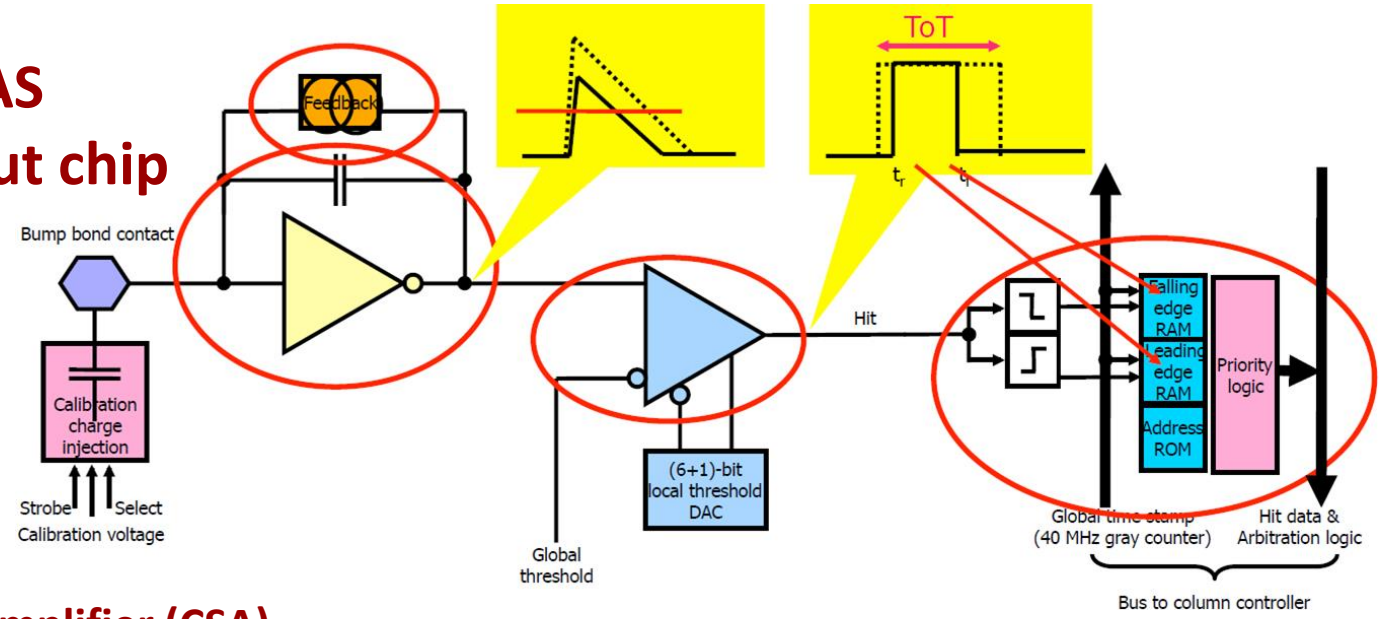


On average 80 electron-hole-pairs/µm of depleted region for a MIP

- The signal is amplified, discriminated and digitized by the readout electronics

Readout electronics – The integrated circuit

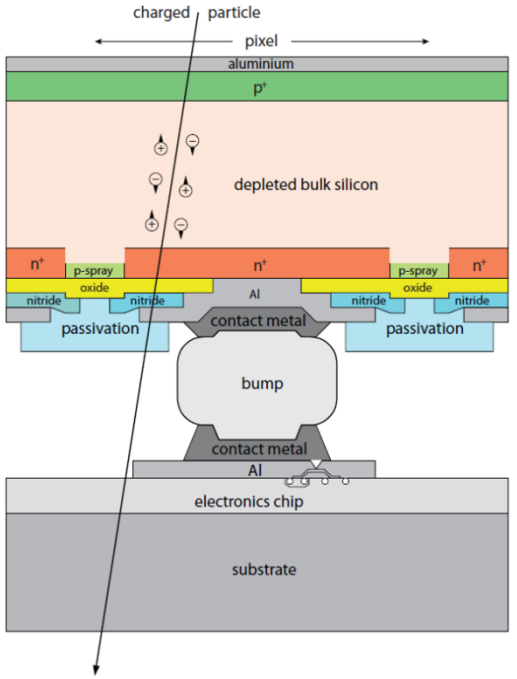
FE-I3 – ATLAS pixel readout chip

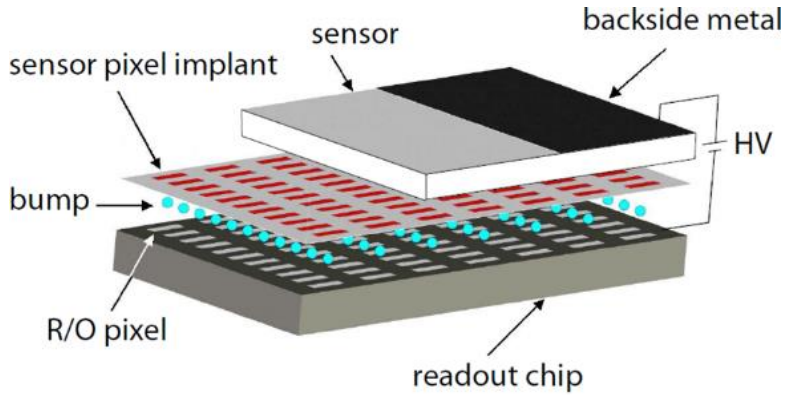


- **Charge Sensitive Amplifier (CSA)**
  - Signal charge integration
  - Pulse shaping (feedback capacitor with constant current)
- **Comparator with DAC for local threshold voltage compensation**
  - Pulse digitization
  - Length of digital pulse determined by time at which the rising and falling edges cross the comparator threshold voltage (Time over Threshold or ToT)
- **RAM and ROM memories** to store time-stamps and pixel address
- In deep sub-micron technologies for high density of integration

Hybrid pixel detectors

- Sensor and readout electronics on separate wafers
- **Best technology for the sensor and the readout electronics**
  - Very fast charge collection by drift (1 ns)
  - Fully depleted bulk (large signal)
  - Radiation tolerant (10^{16} 1MeV n_{eq}/cm^2)
  - Capability to cope with high data rates
- **1-to-1 connection between sensor and readout chip via tiny conductive bumps using bumping and flip-chip technology**
  - Limited pixel size (55 µm x 55 µm)
  - Substantial material thickness (300 µm)
  - Limited fabrication rate (bump-bonding and flip chipping is complex)
  - Expensive (> £1M/m^2) – custom wafers and processing
- **State-of-the-art for high rate experiments**

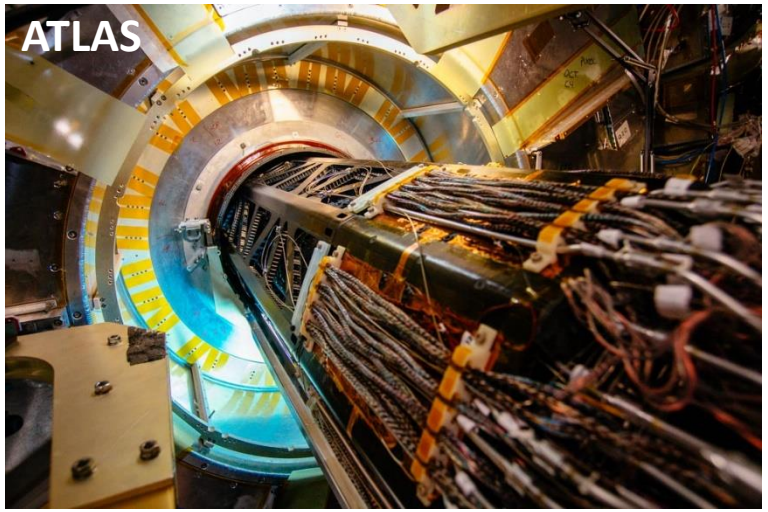


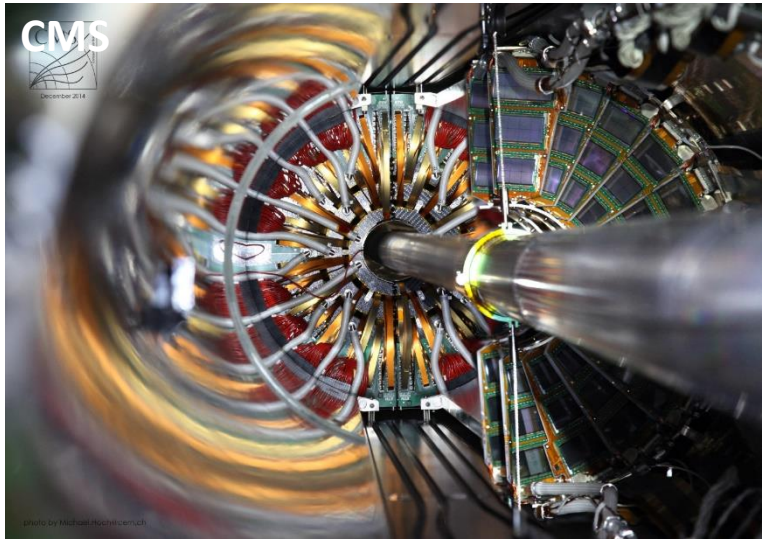


M. Garcia-Sciveres, arXiv:1705.10150v3, 2018

Hybrid pixel detectors in particle physics

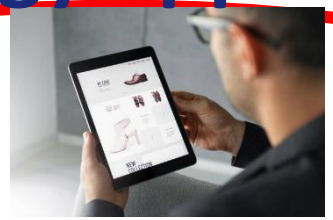
- **ATLAS, CMS and ALICE** use hybrid pixel detectors near the interaction point
- Complemented by hybrid strip detectors at larger radii
- Largest detector systems ever built in HEP (several m^2)

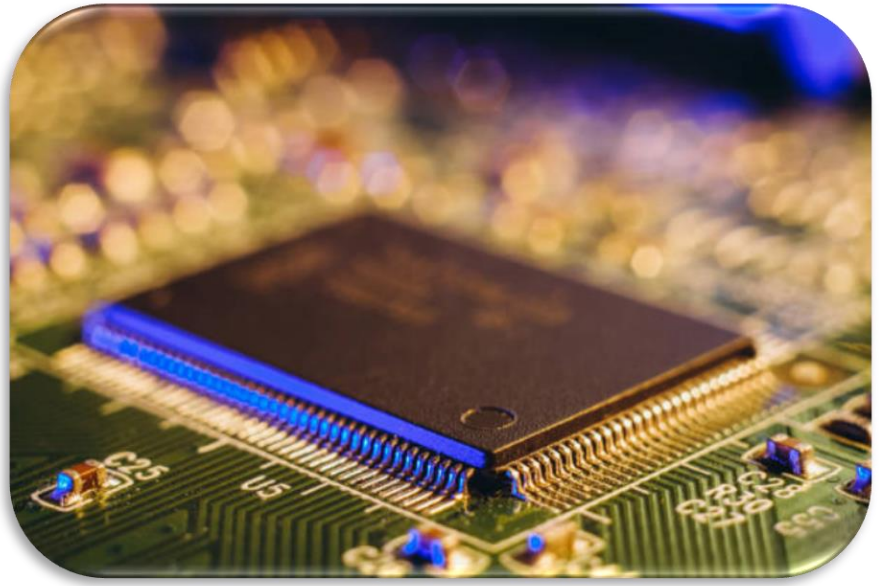


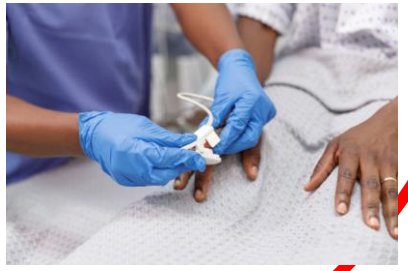


CMOS/HV-CMOS technology applications





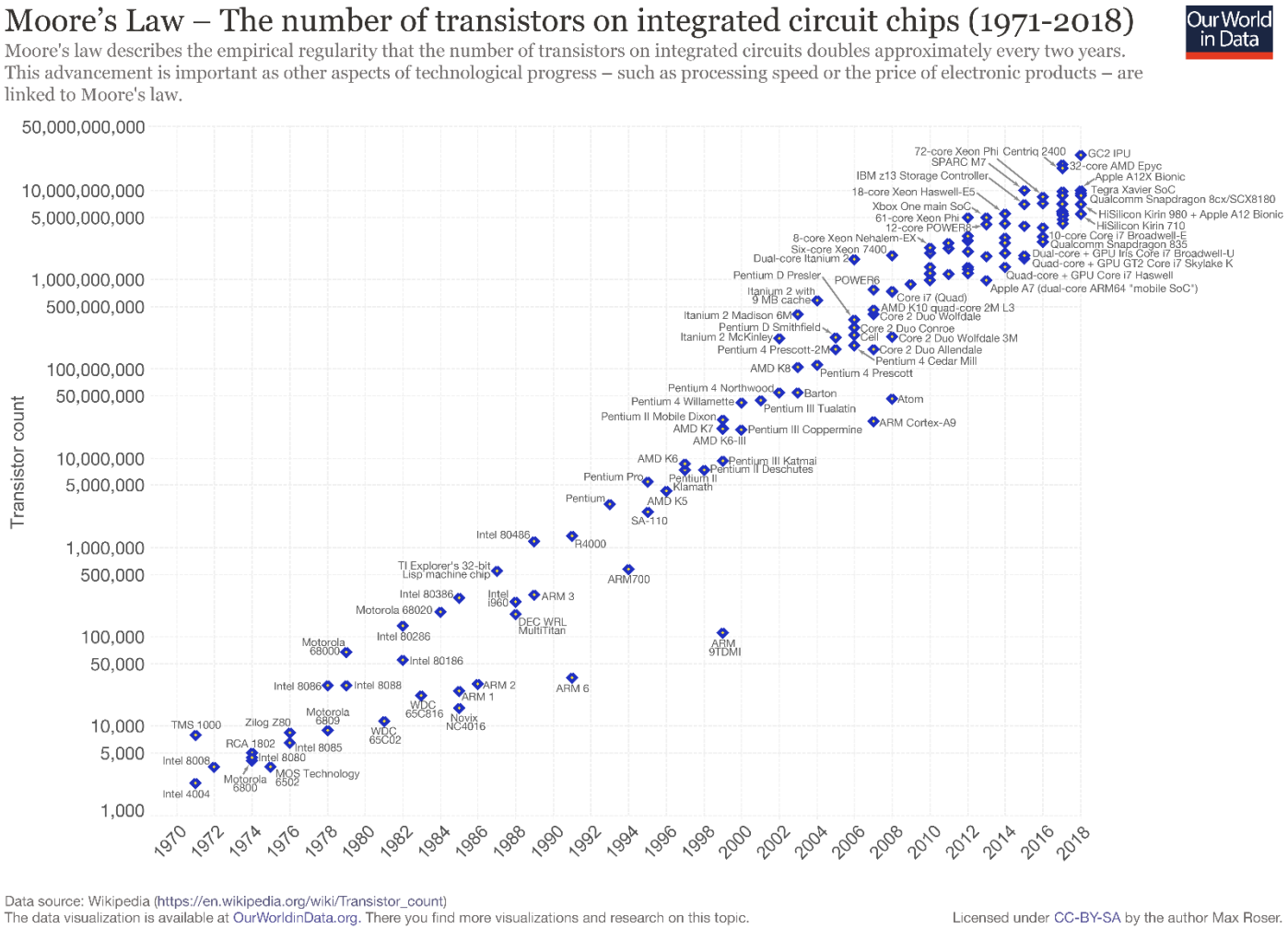




CMOS/HV-CMOS technology

- Why is it so popular?
  - Reliable (industry-standard)
  - Low-power consumption
  - Low-cost
  - Scalable (millions of transistors are integrated into a single chip)
  - Starting material is silicon (sand)

Moore's law (1965) → The number of transistors in a dense integrated circuit (IC) doubles about every two years



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

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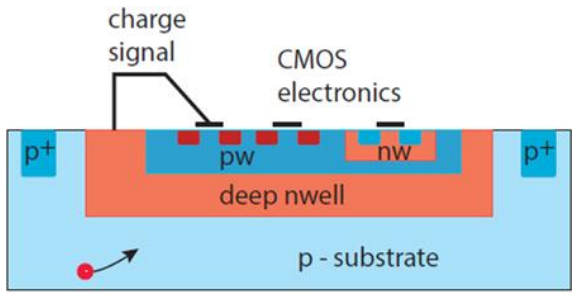
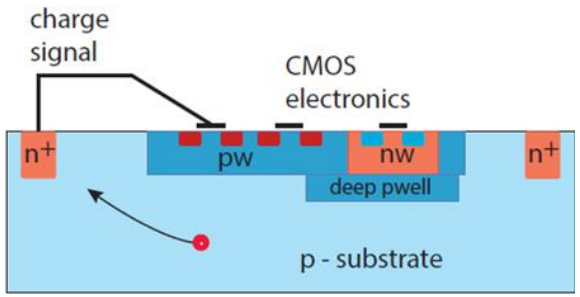
CMOS/HV-CMOS commercial vendors

CMOS/HV-CMOS commercial vendors

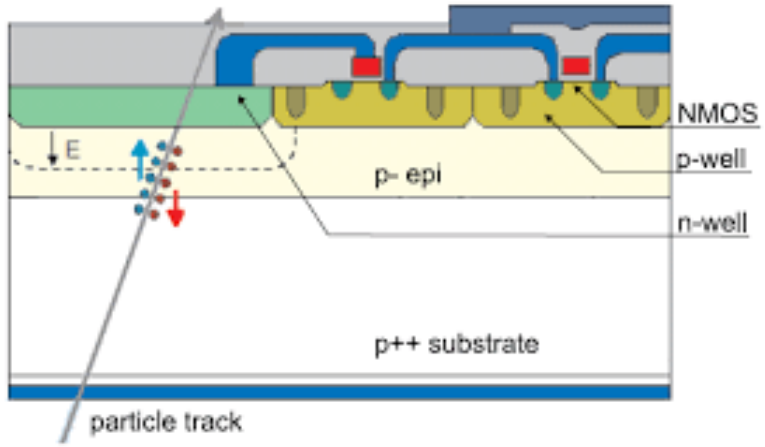
Foundry → / Parameter ↓	LFOUNDRY A SMIC COMPANY	TOWERJAZZ The Global Specialty Foundry Leader	TSI SEMICONDUCTORS
Feature node	150 nm	180 nm	180 nm
HV	Yes	No	Yes
HR	Yes	Yes	Yes
Quadruple well	Yes	Yes	Yes
Metal layers	6	6	6
Backside processing	Yes	Yes	No
Stitching	Yes	Yes	Yes

Monolithic pixel detectors

Sensor cross-section → Parameter ↓		
Name	Large fill-factor (HV/HR-CMOS)	Small fill-factor (HR-CMOS)
1) p/n junction	p-substrate/large deep n-well (RO in charge collection well)	p-substrate/small shallow n-well (RO outside charge collection well)
2) Substrate biasing	High voltage	Low voltage
3) Substrate resistivity	< 2-3 kΩ·cm	< 8 kΩ·cm
1) + 2) + 3)	▪ Large pixel capacity ▪ Higher noise ▪ Higher power consumption ▪ Short drift distances ▪ High radiation tolerance ▪ Good timing resolution	▪ Small pixel capacity ▪ Lower noise ▪ Low power consumption ▪ Long drift distances ▪ Less radiation tolerance ▪ Worse timing resolution
Process	AMS/TSI 180 nm + LFoundry 150 nm	TowerJazz 180 nm

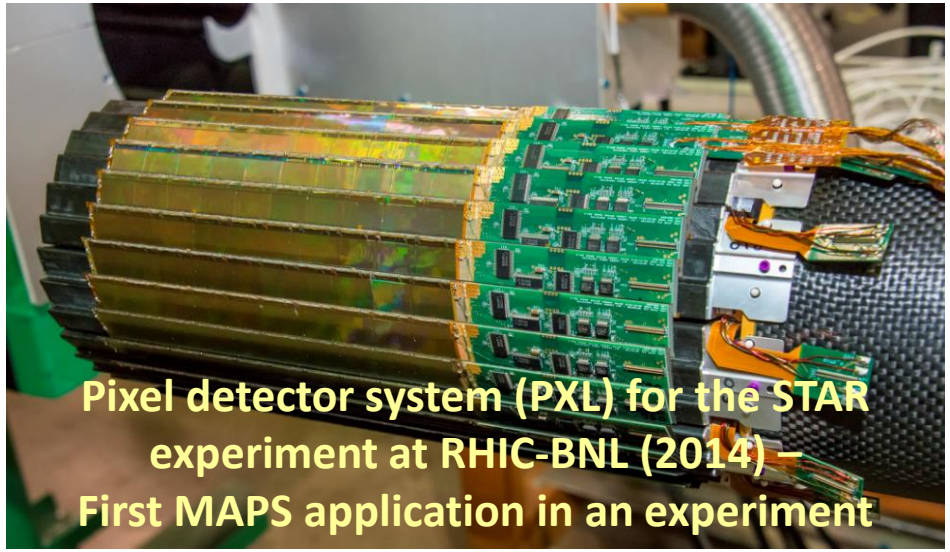
Monolithic pixel detectors: CMOS

- Sensor and readout electronics on single wafer in standard CMOS (low-voltage CMOS)
  - Reduced material thickness (50 µm)
  - Small pixel size (18 µm x 18 µm)
  - In-pixel signal amplification
  - More cost effective (~£100k/m^2)
  - Small bias voltage (V_{bias})
    - Slow charge collection by diffusion (2 µs)
    - Limited radiation tolerance (10^{13} 1MeV n_{eq}/cm^2)
- **State-of-the-art for high precision experiments**

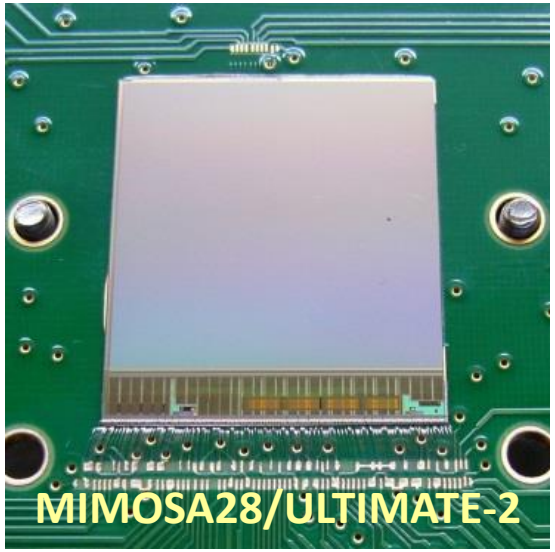


Improved values recently

CMOS detectors in particle physics – STAR experiment



Pixel detector system (PXL) for the STAR experiment at RHIC-BNL (2014) – First MAPS application in an experiment



MIMOSA28/ULTIMATE-2

G. Contin, arXiv:1710.02176v2, 2018

- **MIMOSA-28 / ULTIMATE chip:**
  - Chip size — 20 mm x 22 mm
  - Total detector area — 0.15 m^2
  - Sensor matrix — 928 x 960 pixels (~0.9 Mpixels per chip); 400 pixel chips in total ~360 Mpixels
  - Pixel size — 20.7 µm x 20.7 µm (MAPS chosen to improve hit resolution to enable the reconstruction of hadronic decays of heavy flavour mesons and baryons)
  - Radiation tolerance — 150 krad (TID) + 10^{12} 1 MeV n_{eq}/cm^2 (NIEL)
  - Process — AMS 0.35 µm OPTO

CMOS detectors in everyday life

The best camera phone in 2022

(Image credit: Basil Kronfli / Digital Camera World)

1. Samsung Galaxy S22 Ultra ★★★★★

With a built-in stylus this is the best Android camera phone

SPECIFICATIONS

Release date: February 2022

Rear cameras: 108MP f/1.8, 10MP f/2.4, 10MP f/4.9, 12MP f/2.2 ultrawide

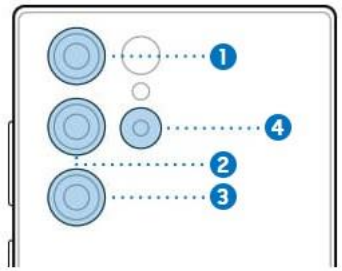
Front camera: 40MP **OIS:** Yes **Weight:** 228 g

Dimensions: 163.3 x 77.9 x 8.9 mm

Storage: 128GB/256GB/1TB

Galaxy S22 Ultra

Quad camera



1 12MP Ultra Wide Camera

- Dual Pixel AF
- Pixel size: 1.4µm
- FOV: 120˚
- F.No (aperture): F2.2
- 1/2.55" image sensor size

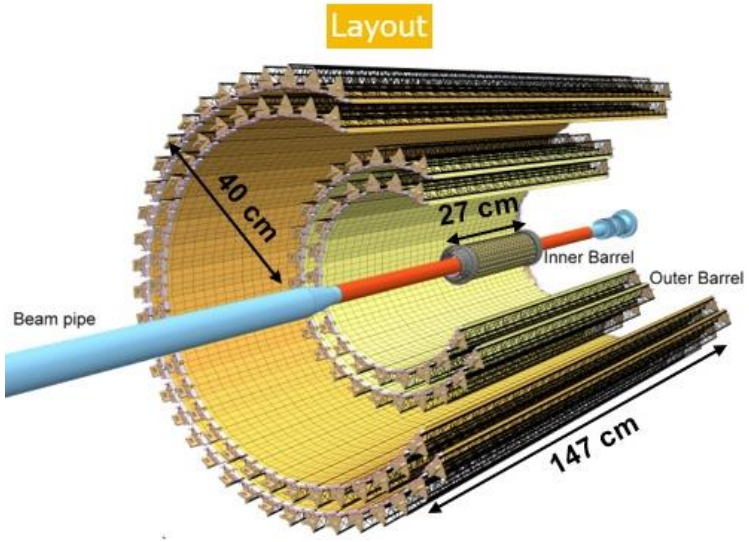
2 108MP Wide-angle Camera

- PDAF, OIS
- Pixel size: 0.8µm (12MP 2.4µm)
- FOV: 85˚
- F.No (aperture): F1.8
- 1/1.33" image sensor size

3 10MP Telephoto Camera

- Dual Pixel AF

CMOS detectors in particle physics – ALICE ITS upgrade



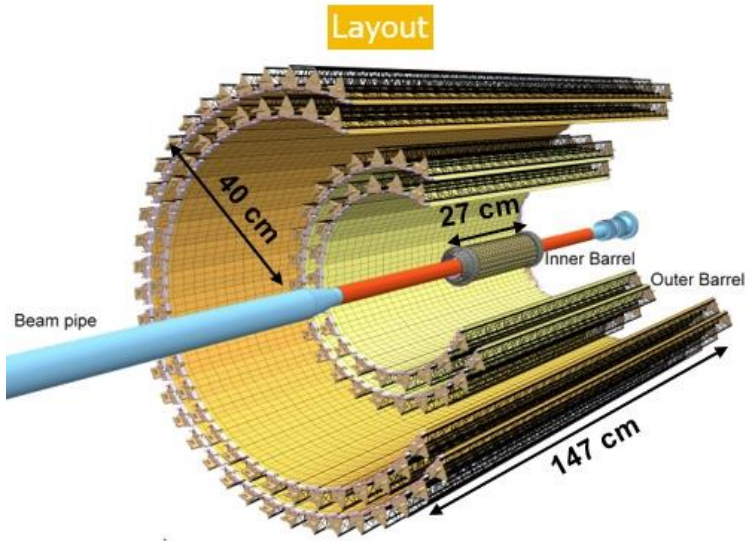
ALICE ITS upgrade ITS2 (2020)

Sensor requirements

Parameter	IB	OB
Sensor thickness (μm)	50	50
Spatial resolution (μm)	5	10
Dimensions (mm^2)	15 × 30	15 × 30
Power density ($mW\ cm^{-2}$)	300	100
Time resolution (μs)	30	30
Detection efficiency (%)	99	99
Fake hit rate[a]	10^{-5}	10^{-5}
TID radiation hardness[b] (krad)	2700	100
NIEL radiation hardness[b] ($1\ MeV\ n_{eq}/cm^2$)	1.7×10^{13}	10^{12}

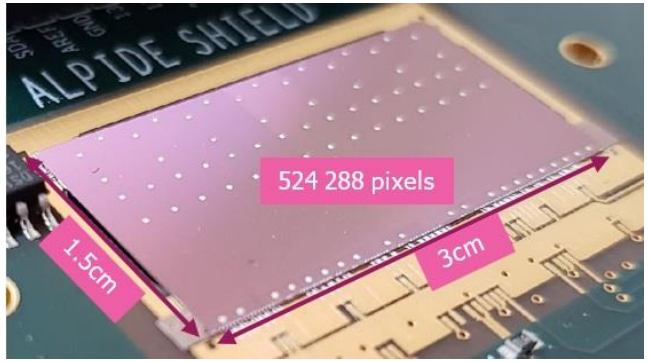
M. Mager, doi.org/10.1016/j.nima.2015.09.057, 2016

CMOS detectors in particle physics – ALICE ITS upgrade

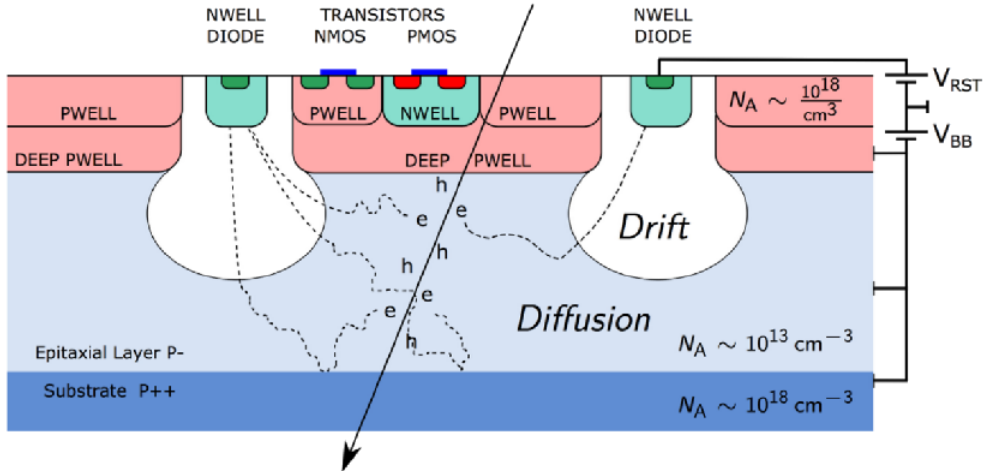


ALICE ITS upgrade ITS2 (2020)

M. Mager, NIM-A: 824 434-438, 2016

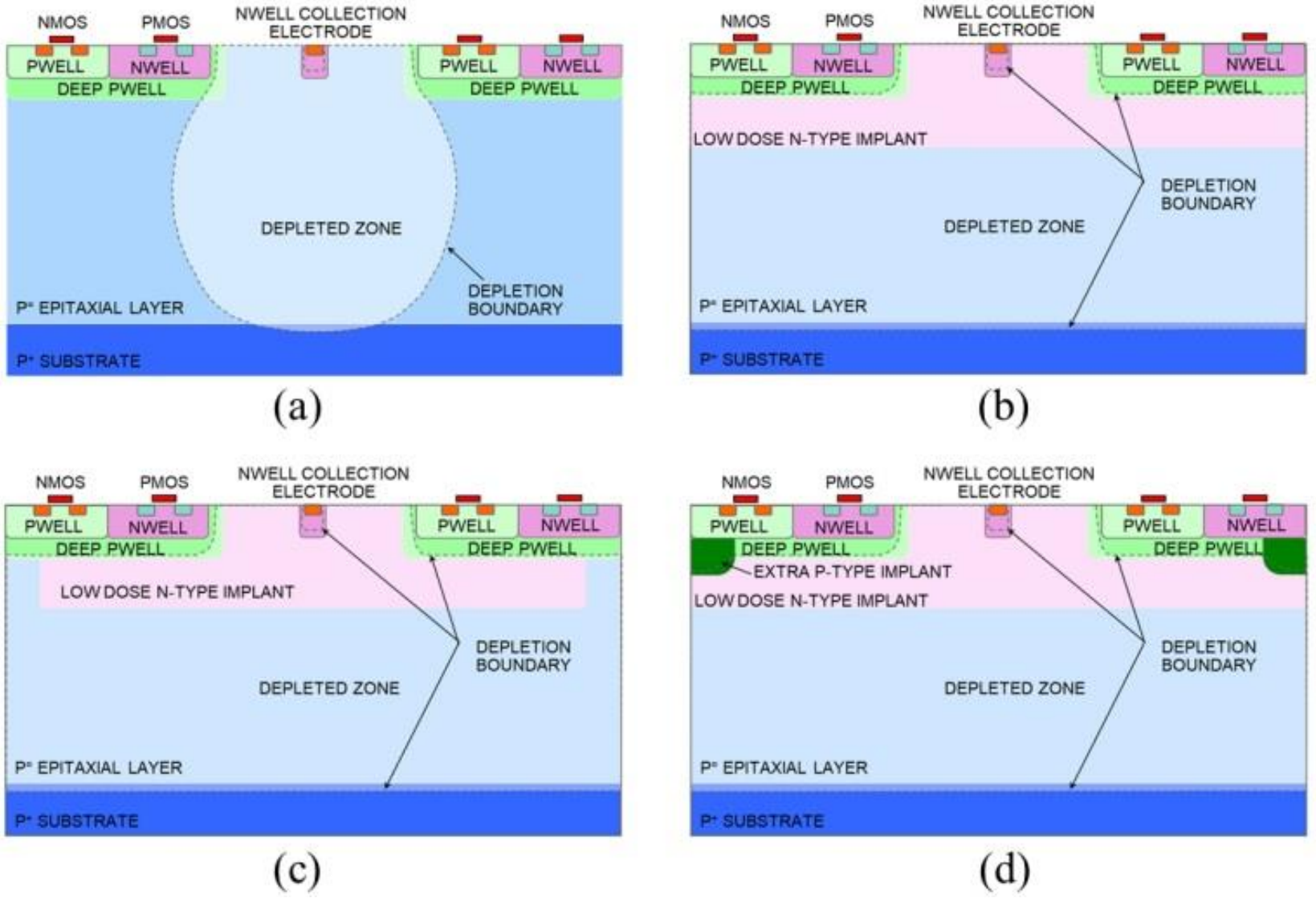


ALPIDE



- **ALPIDE chip:**
  - Chip size — 15 mm x 30 mm
  - Total detector area — 10 m^2
  - Sensor matrix — 1024 x 512 pixels (> 0.5 Mpixels); 24k pixel chips in total ~12.5 Gpixels
  - Pixel size — 26 µm x 29 µm
  - Radiation tolerance — 700 krad (TID)
    10^{13} 1 MeV n_{eq}/cm^2 (NIEL)
  - Process — TowerJazz 180 nm

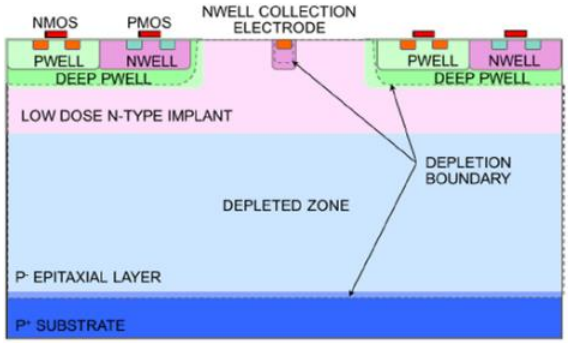
CMOS detectors – Modified and improved TowerJazz



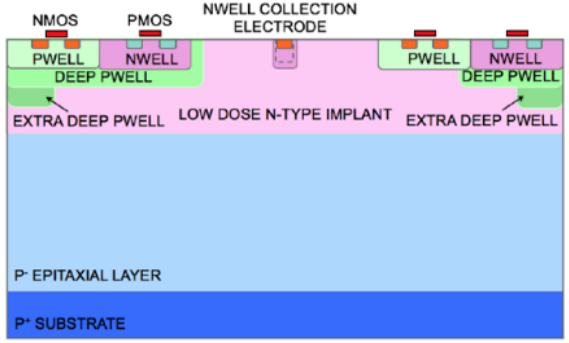
Process modifications to fully deplete the sensor and enhance the lateral electric field in the pixel corners for good tolerance to NIEL (Non-Ionising Energy Loss)

CMOS detectors – Modified and improved TowerJazz

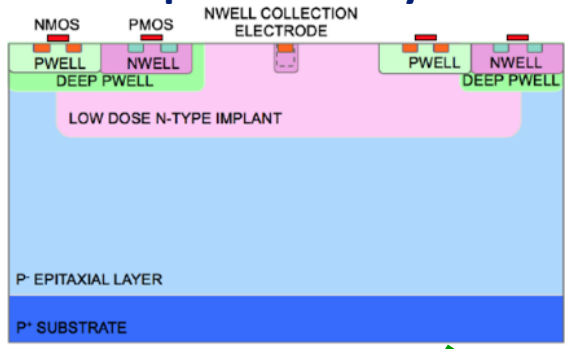
Modified process



Extra deep p-well implant

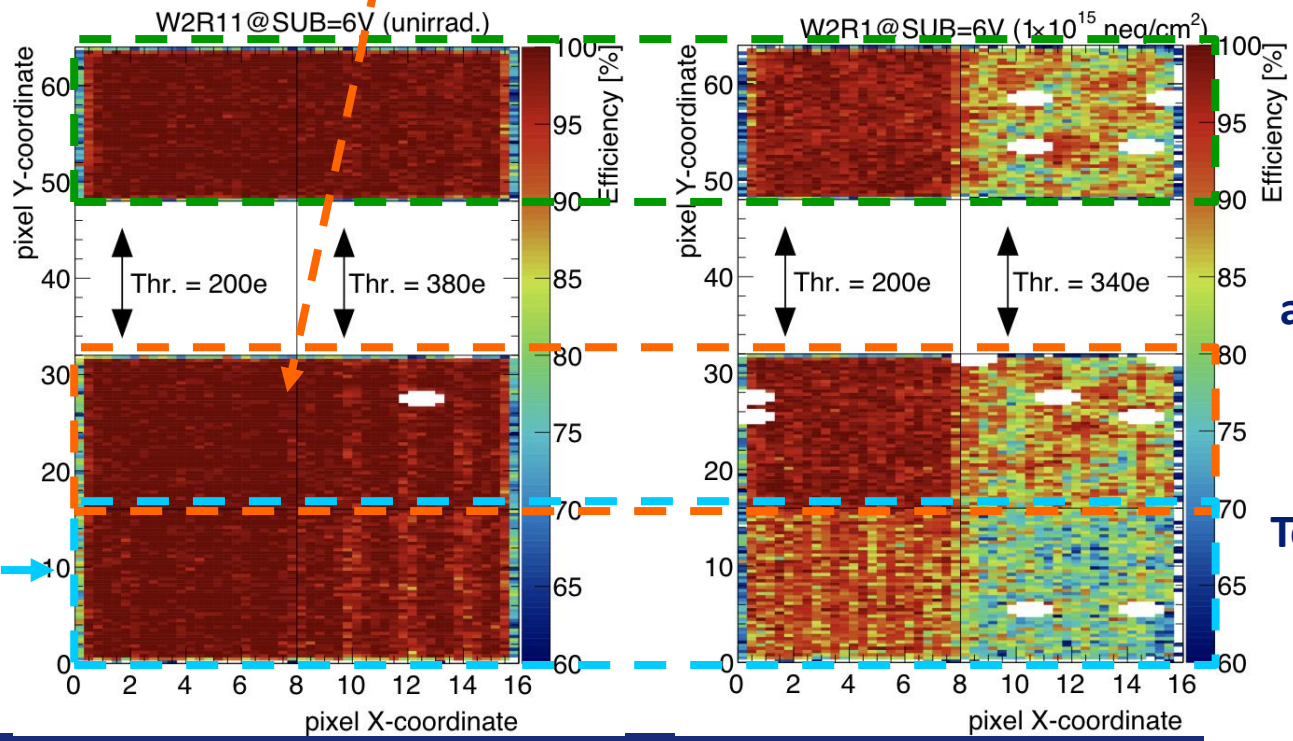


Gap in the n-layer



B. Hiti, 2018

Implemented in MALTA chips



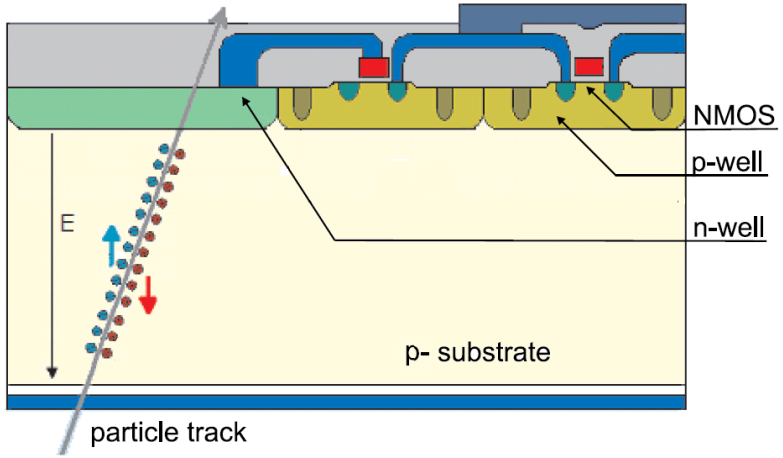
98-99% efficiency after 1x10^{15} n_{eq}/cm^2

Test beam at DESY and ELSA

AIDA innova | UK Research and Innovation | UNIVERSITY OF LIVERPOOL

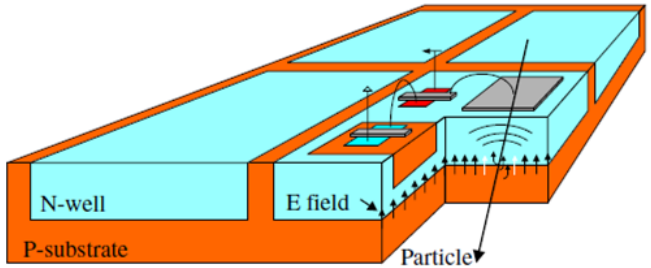
Monolithic pixel detectors: HV-CMOS

- Sensor and readout electronics on single wafer in standard High Resistivity/High Voltage-CMOS (HR/HV-CMOS)
  - Reduced material thickness (50 µm)
  - Small pixel size (50 µm x 50 µm)
  - In-pixel amplification
  - More cost effective (~£100k/m^2)
  - Larger bias voltage (V_{bias})
    - Fast charge collection by drift (~3 ns time resolution)
    - Good radiation tolerance (10^{15} 1MeV n_{eq}/cm^2)
  - One limitation: The chip size is in principle limited to 2 cm x 2 cm, although stitching options are being investigated
- **Next generation**



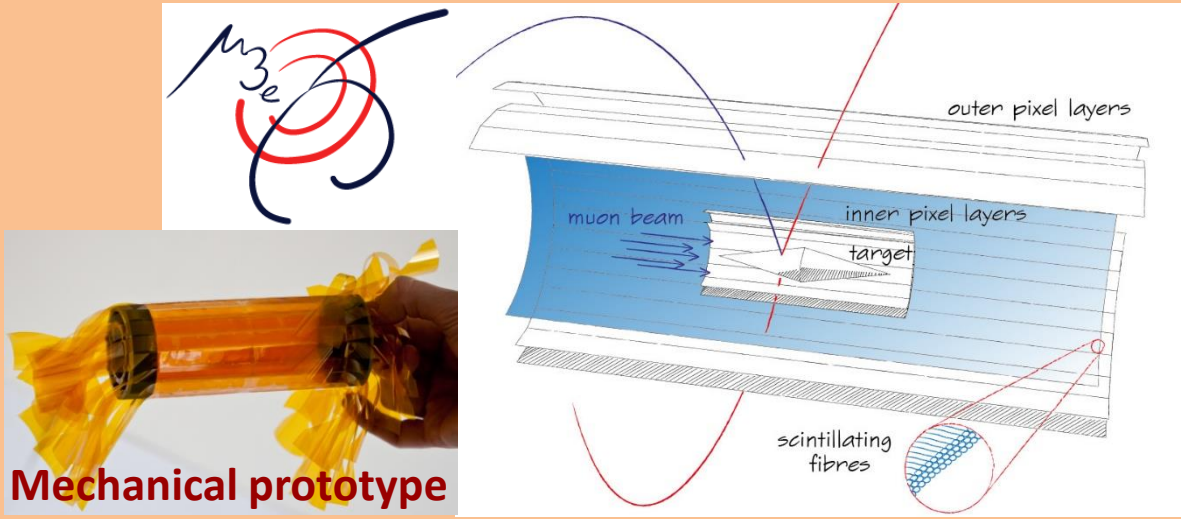
Monolithic pixel detectors: HV-CMOS

- HV-CMOS processes originally used for driving automotive or industrial devices
- 2007 → First publication of a HV-CMOS detector chip (test chip in 0.35 µm HV-CMOS process from AMS)
  - Small pixel matrix
  - Pixels = Sensor + pixel electronics (CSA, discriminator and digital storage)
  - Pixel electronics in the deep n-well
  - Successful measurements with X-ray and beta radioactive sources
  - HV contacts at the top side
- HV-CMOS processes are attractive for particle physics because
  - Silicon bulk biased at high voltage (e.g. -100 V)
  - Multiple nested wells to isolate the low-voltage CMOS readout electronics from the bulk
  - Commercially available (i.e. fabrication is low-cost and reliable, there is availability of multiple vendors and large scale production)



I. Peric, NIM-A: 582 876-885, 2007

HV-CMOS detectors in particle physics



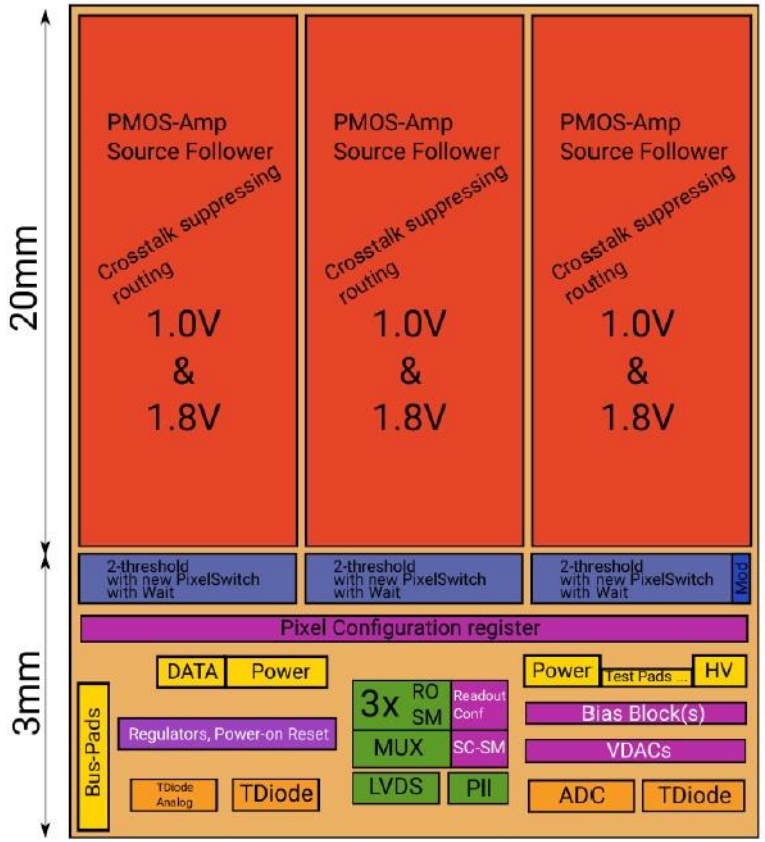
- **First HV-CMOS application in an experiment (202x)**
- Requirements:
  - Low material
    50 µm
  - Good time resolution
    < 20 ns (for pixels)
  - Fine segmentation
    80 µm x 80 µm

HV-CMOS detectors in particle physics – Mu3e

Prototype	Year	Active area (mm^2)	Functionality	Main features
MuPix1	2011	1.77	Sensor + analog RO	First MuPix prototype
MuPix2	2011	1.77	Sensor + analog RO	
MuPix3	2012	9.42	Sensor + analog/digital RO	First digital RO
MuPix4	2013	9.42	Sensor + analog/digital RO	Working digital RO and time-stamping
MuPix6	2013	10.55	Sensor + analog/digital RO	
MuPix7	2014	10.55	SoC (all relevant features for a fully monolithic chip)	First MuPix with SM, clock generation and fast serial RO (1.25 Gbit/s)
MuPix8	2017	160	Large SoC	First large MuPix prototype, with TW correction
MuPix9	2018		SoC	Voltage regulators
MuPix10	2019	400	Full size (reticle) SoC	First full size SoC
MuPix11	2022		Full size (reticle) SoC	Fixes bugs of MuPix10

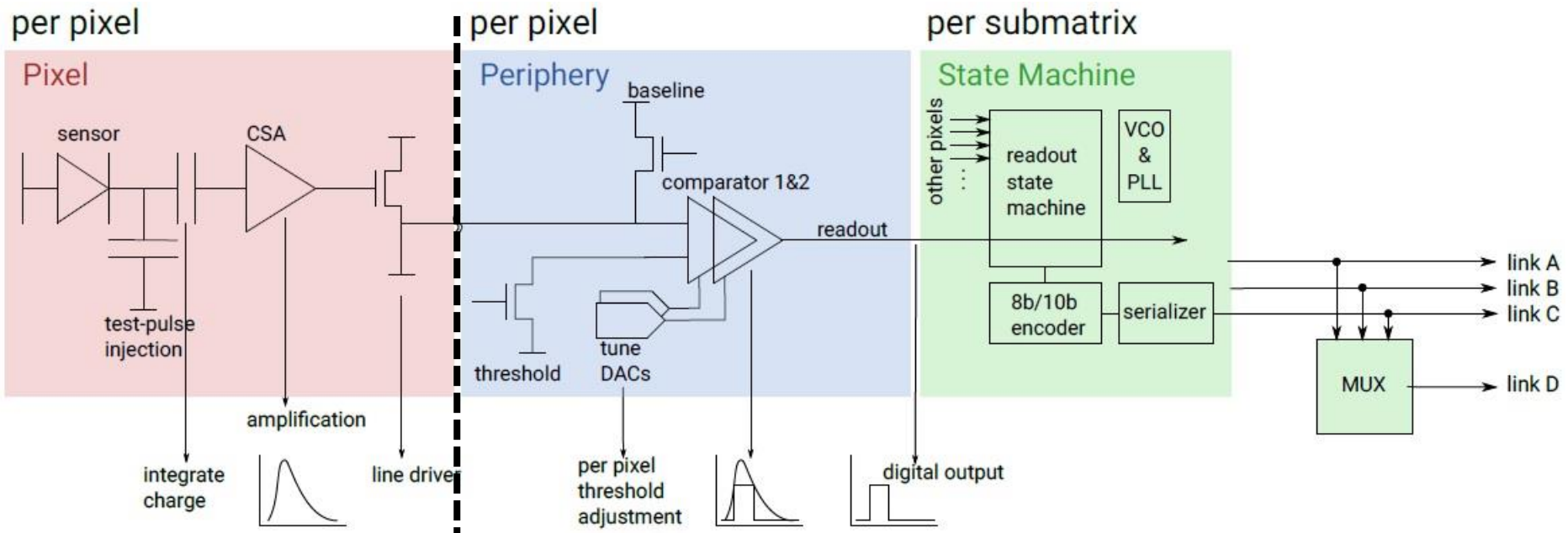
MuPix10 – Main details

- Fully monolithic sensor in the 180 nm HV-CMOS TSI process
- Active pixel matrix size of 20 mm x 20 mm (256 x 250 pixels)
  - Chip split into 3 sub-matrices with 84, 86 and 86 columns
- Pixel size is 80 µm x 80 µm
- Hits are read out using the column-drain architecture
  - Two time-stamps are stored for each hit (rising and falling edges)
- 8b10b encoding
- Hits are sent over up to four serial links with nominal 1.25 Gbit/s
  - One link per sub-matrix + an additional fourth to send combined data
  - Max. hit rate of 90 Mhit/s can be achieved, theoretically
- On-chip biasing to minimise electrical connections
- Measured V_BD = 100 V, 200 Ω·cm substrate resistivity → W_D = 40 µm
  - No inactive bulk for 50 µm thin sensors
- Measured power consumption = 190 mW/cm^2

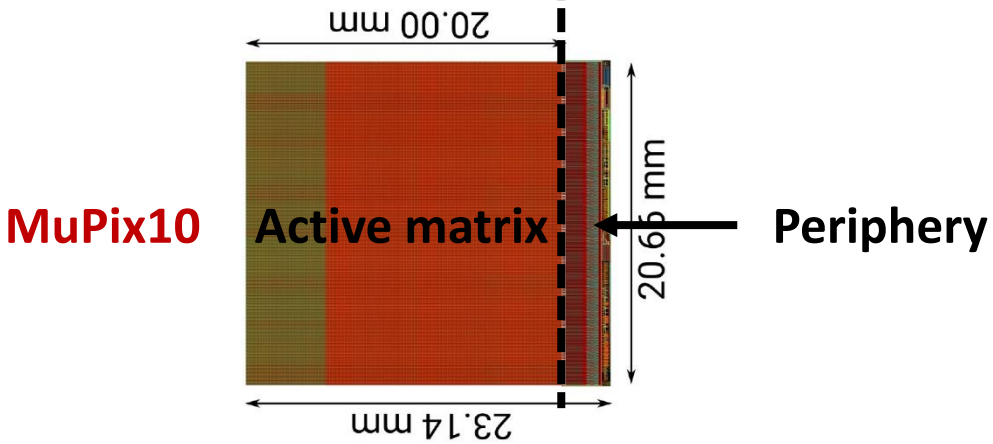


H. Augustin, Tracking Verbund Meeting, 2021

MuPix – Functional diagram



H. Augustin, arXiv:2012.05868v2, 2020



Time-Walk (TW) – What is it & ways to improve it

Time-Walk (TW)

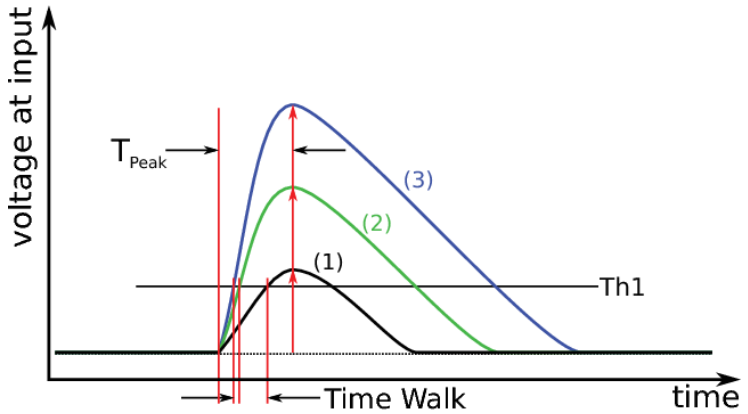
- What is it? Variation of the response time of the readout electronics depending on the number of e^-/h^+ pairs collected by the sensor

TW correction – Two-threshold method

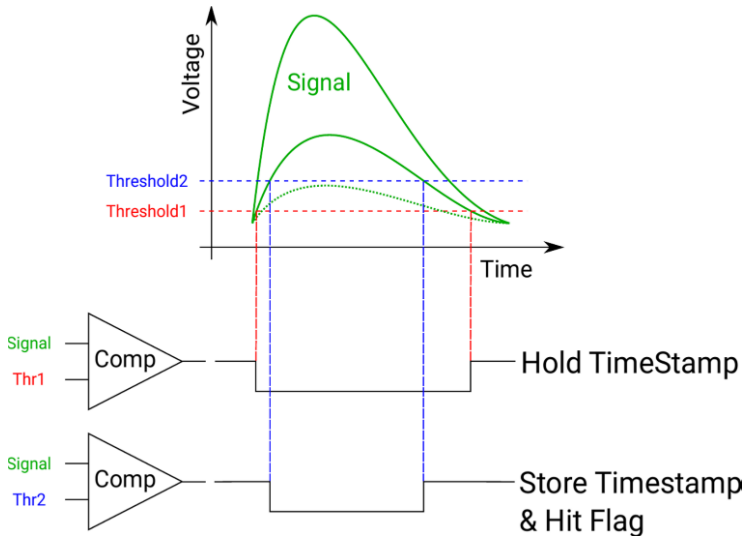
- Two comparators with two threshold voltages:
  - VTH1 is very low (close to the noise level) → it delivers a time-stamp with small TW
  - VTH2 > VHT1 → it confirms that the flagged time-stamp corresponds to a real signal and not to noise
- Measured results show the TW can be reduced to ~3 ns

TW correction – Other methods

- Increasing the response rate of the amplifier (CACTUS, RD50-MPW2)
- Time-walk compensated comparator (HVStripV1, H35DEMO)
- Sampling method (LF-ATLASPix, CERN-RD50)

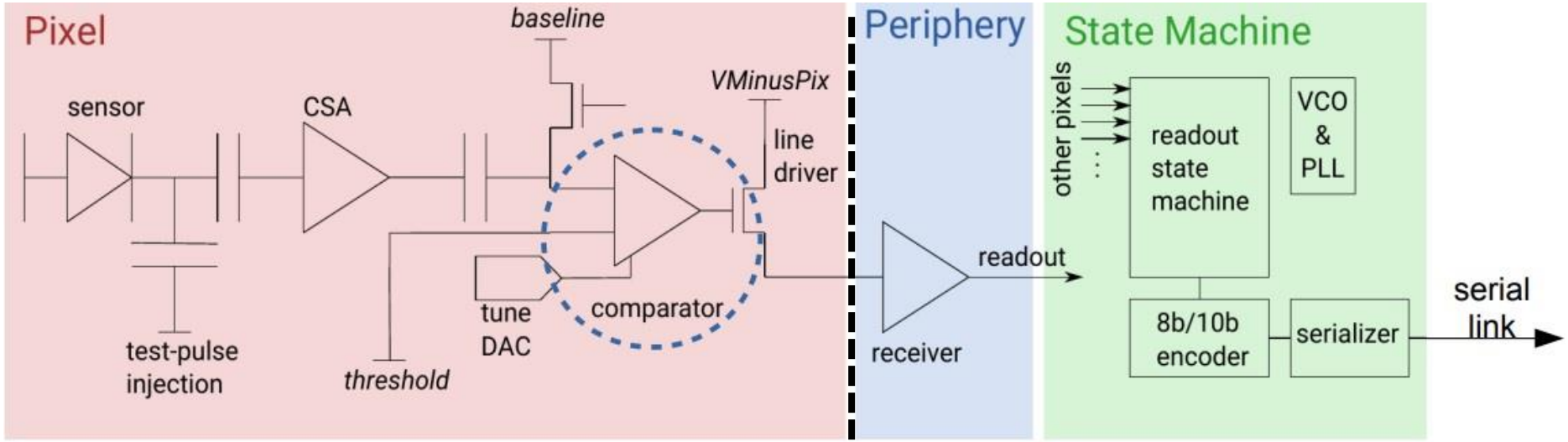


R. Schimassek, IEEE NSS/MIC/RTSD, 2016

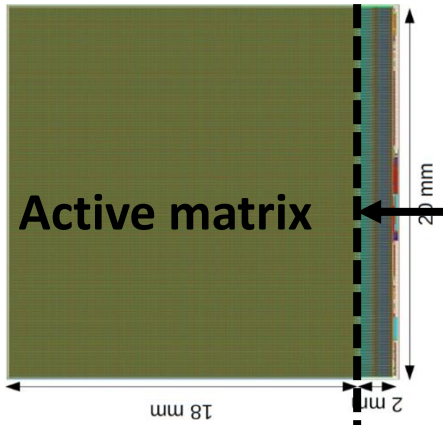


H. Augustin, PoS (VERTEX2017) 057

Other functional diagrams are possible

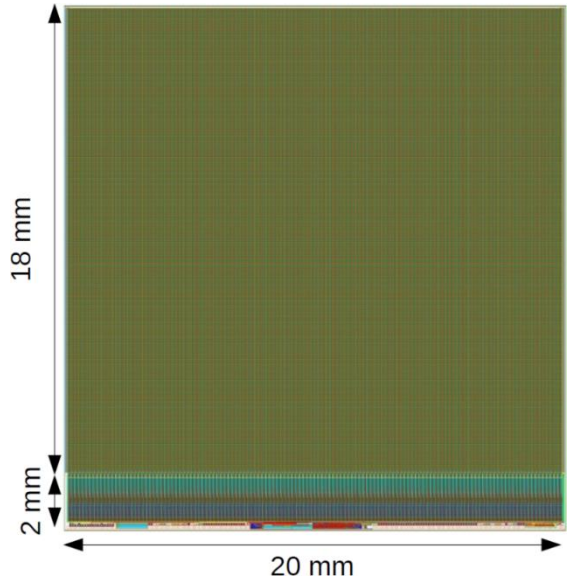


A. Schoening, VERTEX2019

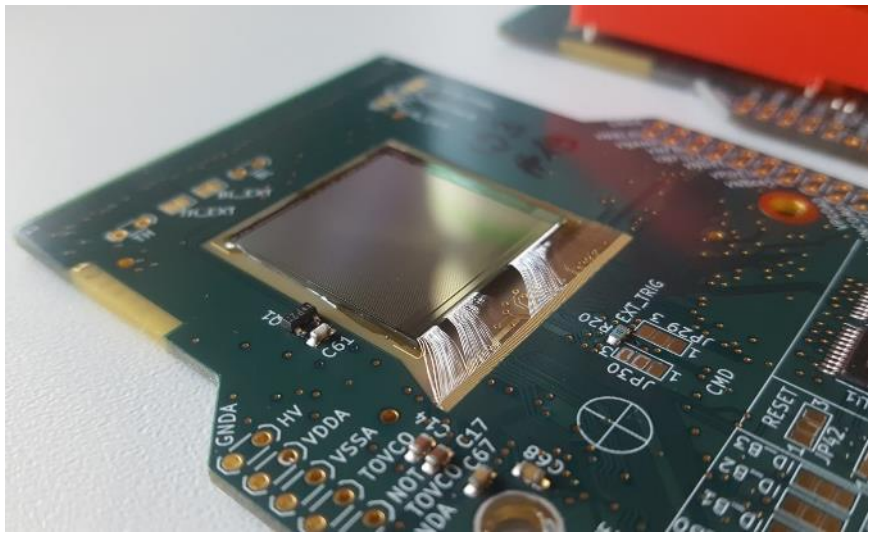


ATLASPix3 **Active matrix** ← **Periphery**

HV-CMOS detectors – ATLASPix3



R. Schimassek, 2019



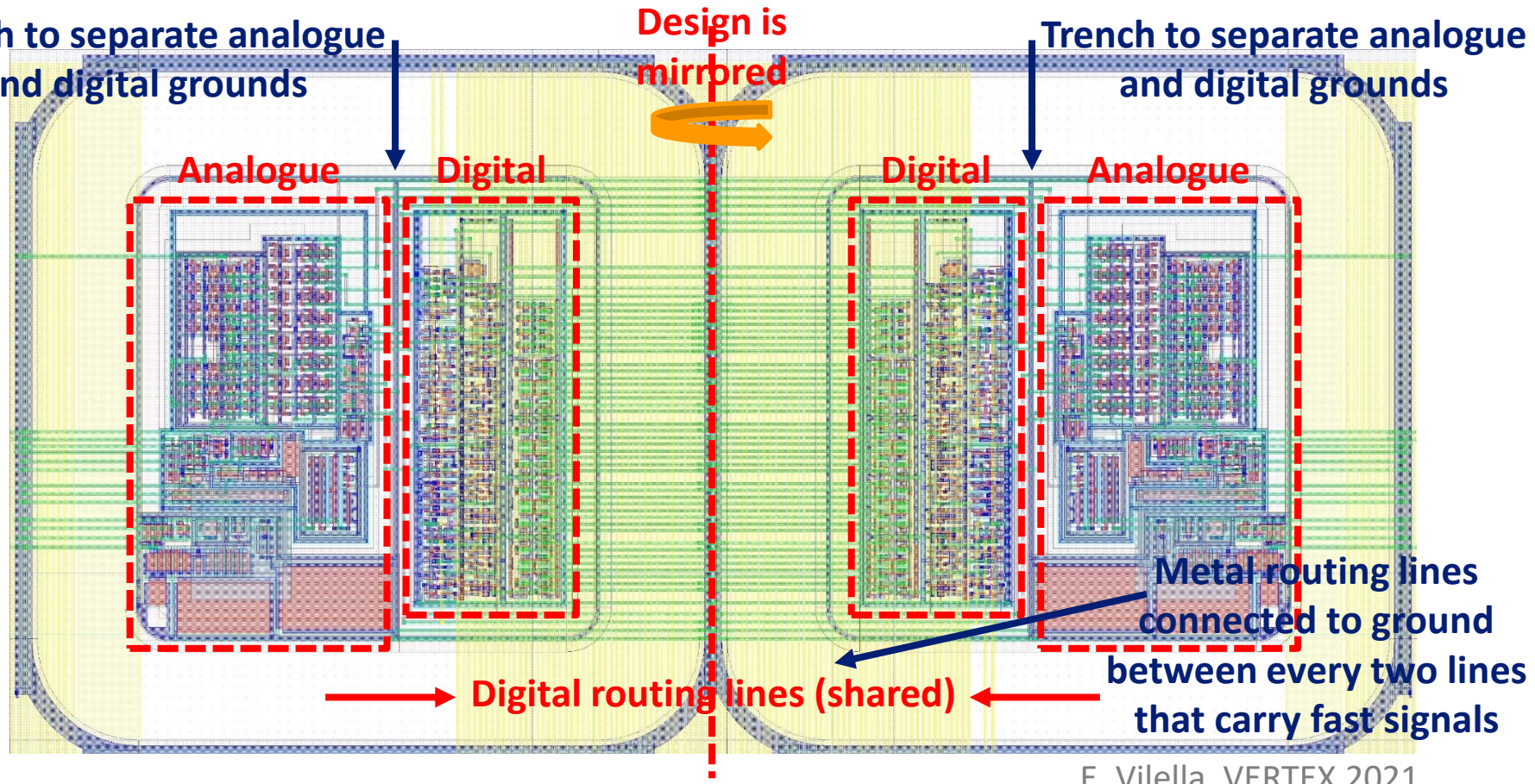
J. Hammerich, 2019

ATLASPix3 – Some chip details

- Matrix with 132 columns x 372 rows
- 150 µm x 50 µm pixel size
- Trigger latency ≤ 25 µs
- Radiation hard design
- Serial powering (only one power supply needed)
- Data interface is very similar to ATLAS RD53 readout chip
- Power consumption is ~200 mW/cm^2 (with 25 ns time resolution)

ATLASPix3 is the first full reticle pixel detector (2 cm x 2 cm) compatible with ATLAS ITk L4 requirements

Other functional diagrams are possible

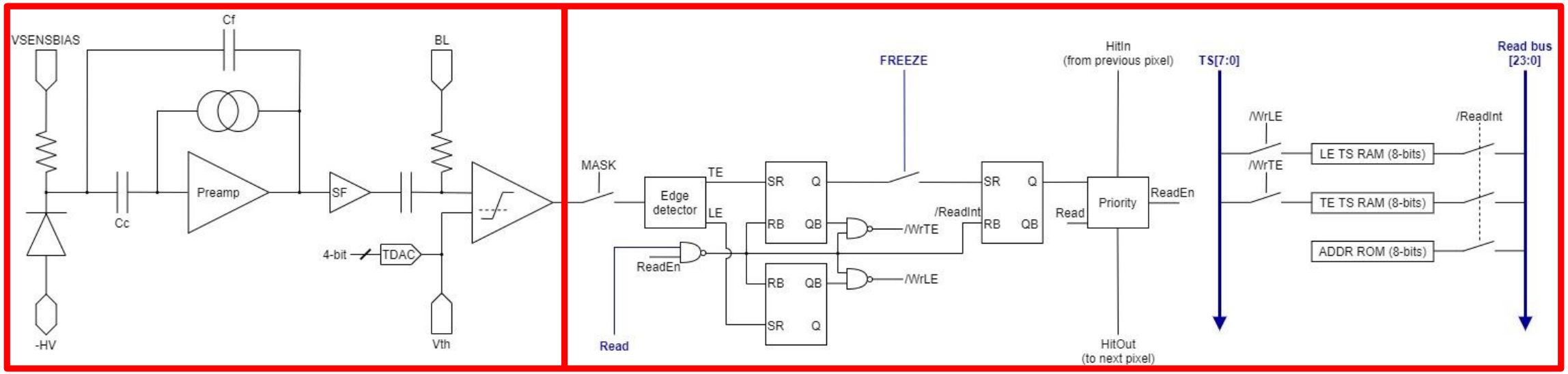


E. Vilella, VERTEX 2021

- **Double column scheme to alleviate routing congestion and minimise crosstalk**
  - Pixels within double column share many signals → ~ x0.5 less routing lines
  - Shared signals are digital input/outputs (TS IN, TS OUT, ADDR), control signals (Read, Freeze, etc.)

RD50-MPW3 – Pixel schematic

Analogue readout (from RD50-MPW2) **Digital readout (from RD50-MPW1, highly improved)**

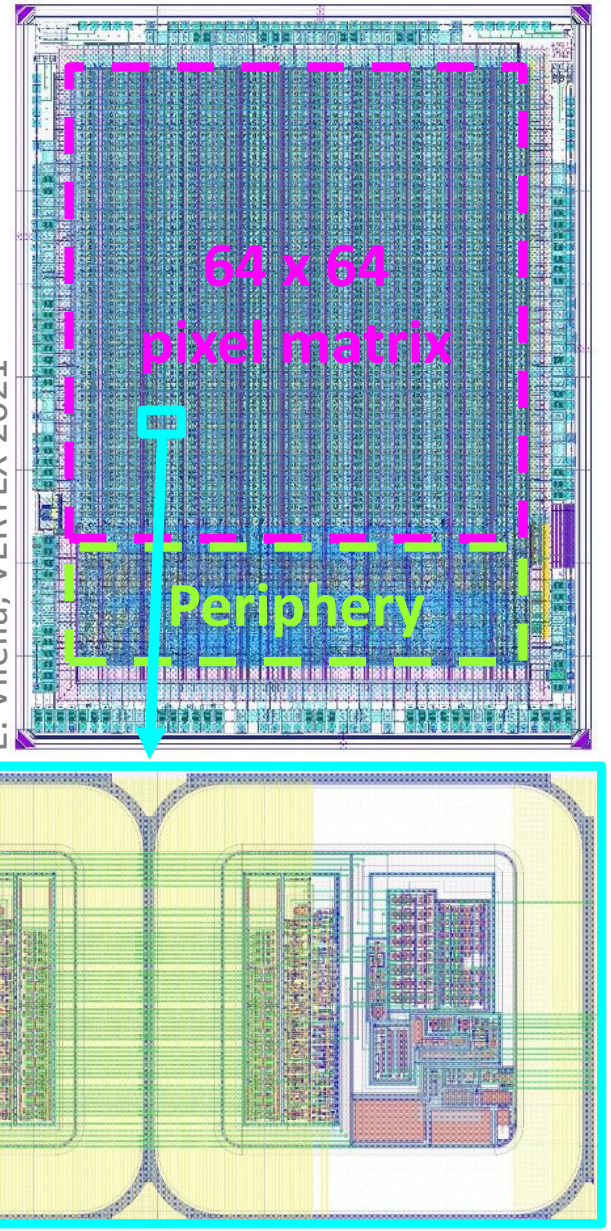


E. Vilella, VERTEX 2021

- Each pixel receives global 8-bit Time-Stamp (TS) and returns
  - 8-bit TS leading edge + 8-bit TS falling edge
  - 8-bit pixel address
- Each pixel integrates 8-bit SRAM shift register for serial configuration (not shown in diagram)
  - Pixel-trimming to compensate for threshold voltage variations (4-bits)
  - Flag to mask noisy pixels (1-bit)
  - Signals to enable/disable calibration circuit (1-bit), SF output (1-bit), COMP output (1-bit)
- Pixels implemented in a double column (DCOL) scheme with shared routing lines to minimise congestion

RD50-MPW3 – Main details

- **RD50-MPW2** very successful chip, but with limitations
  - Pixel matrix with reduced number of rows and columns (8 x 8)
  - No pixel digital readout to identify particle hits
  - Very simple TX readout → some measurements too slow or not possible
- **RD50-MPW3** has larger and more advanced matrix to further study HV-CMOS sensors
  - 64 rows x 64 columns (chip size is 5.1 mm x 6.6 mm)
  - Analogue readout taken from RD50-MPW2
  - In-pixel digital readout (FE-I3 style)
  - Pixel size is 62 µm x 62 µm
  - Optimised peripheral readout for effective pixel configuration and fast data TX
  - Power grid to avoid IR drops
  - With all the lessons learned from RD50-MPW1/2
- RD50-MPW3 submitted in December 2021 through an MPW run
- Delivery expected in late May – early June 2022
- Substrate resistivities: standard, 1.9k and >2k Ω·cm



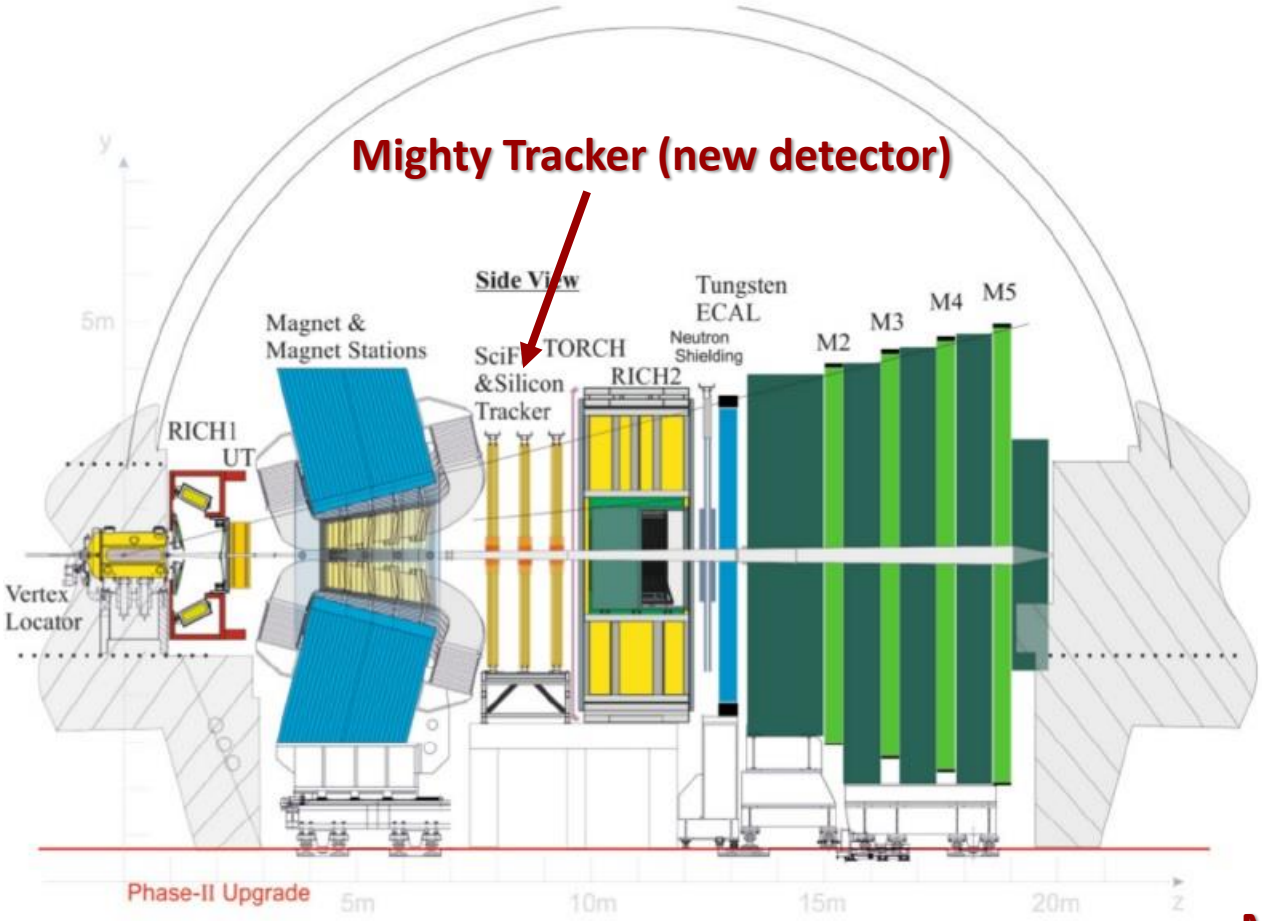
HV-CMOS detectors in particle physics – Mini-quiz

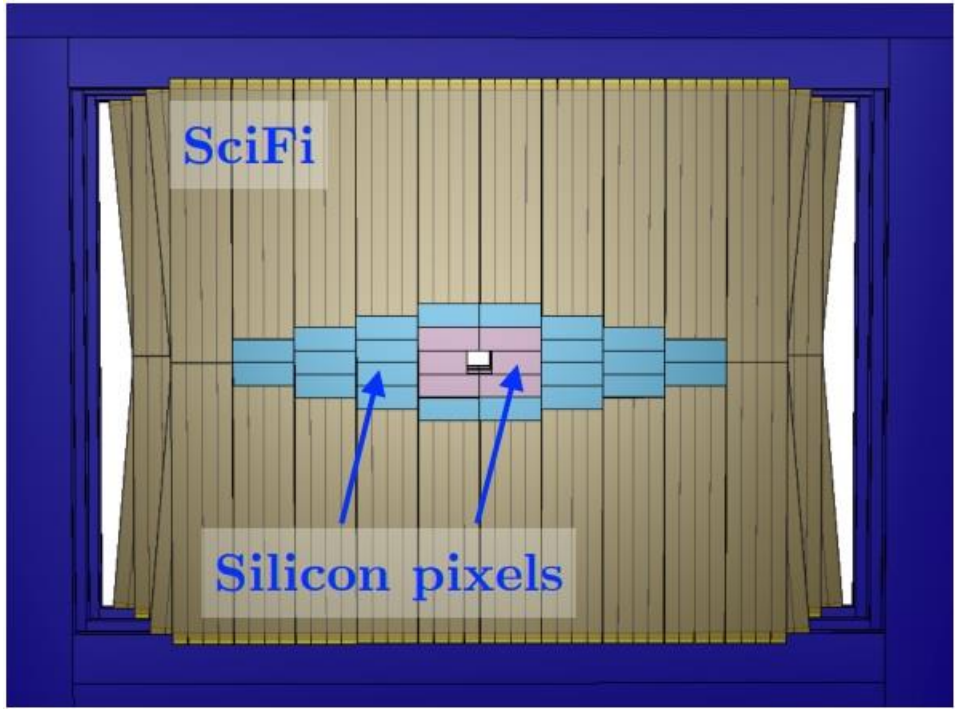
2028/2030+

- **An experiment is proposing a new detector for its next upgrade**
- Requirements:
  - Excellent time resolution 3 ns
  - Pixel size of approximately 50 µm x 150 µm
  - Radiation tolerance $3 \cdot 10^{14}$ 1MeV n_{eq}/cm^2

What detector would you use?
Can you guess the experiment?

HV-CMOS detectors in particle physics – LHCb





MightyPix1 is being submitted, as we speak, to TSI
First HV-CMOS sensor with almost compatible LHCb interface

Thank you for your attention