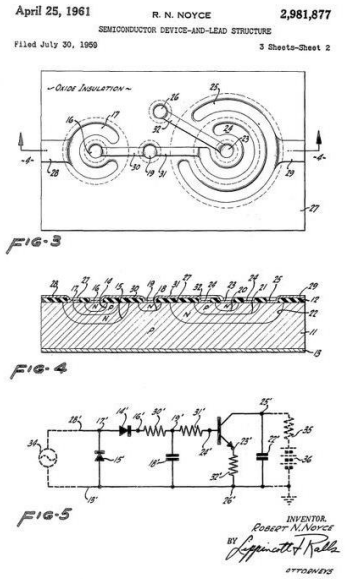
Circuits and Layouts II

Overview

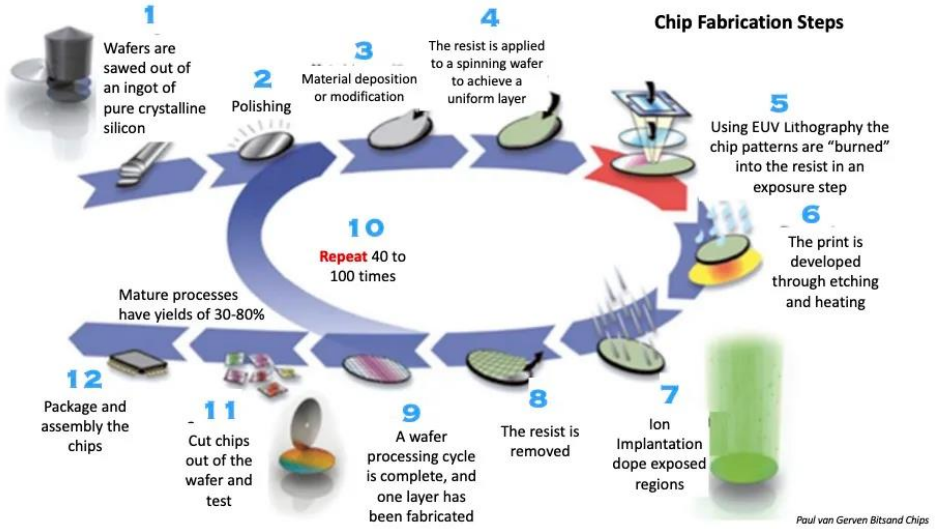
- **Introduction, definitions**
- **Layout and interconnects in IC technology**
- **Transistor MOS layouts**
- **Passive components layouts**

Introduction

- IC (integrated circuits) single silicon chip that includes active and passive interconnected devices to implement complex operations (analogue, digital)
- Planar technology: the processing steps are implemented in a thin layer of the surface of the chip
- Fabrication of chip is an extremely complex process, requiring several steps of atomic precision

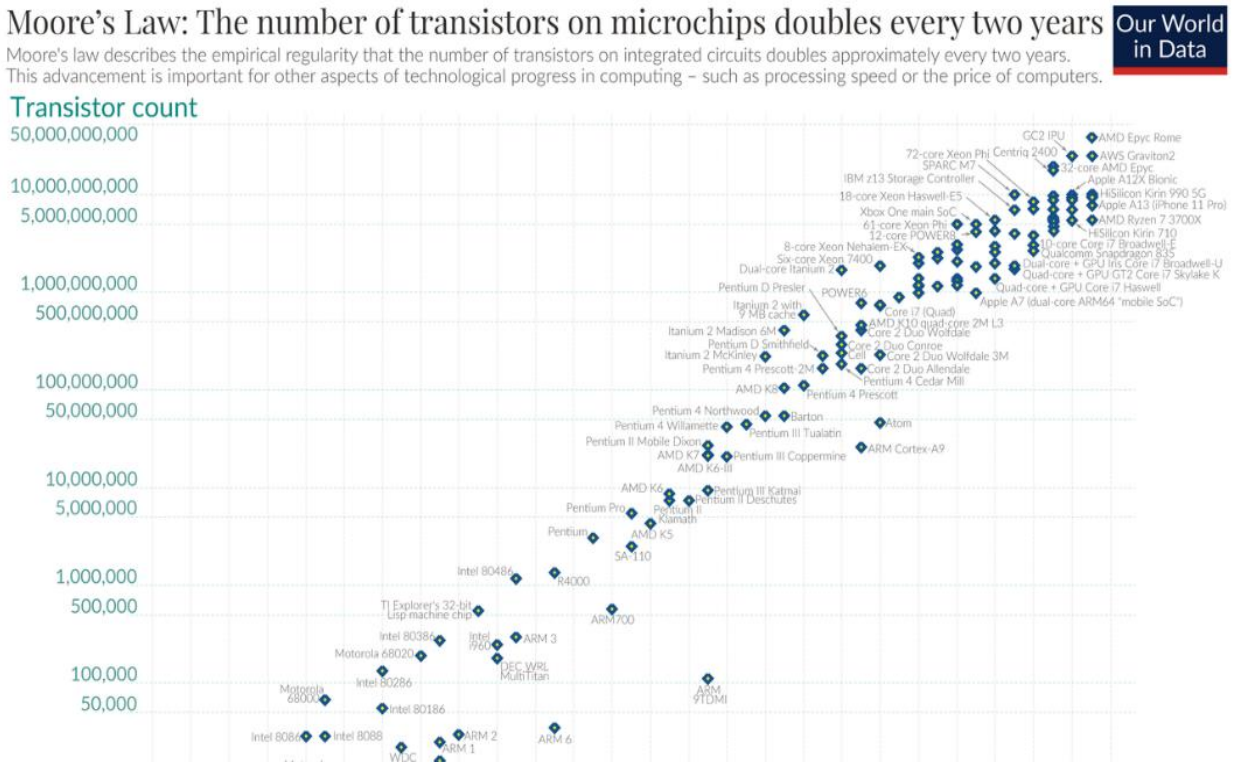


First planar IC patent, 1961



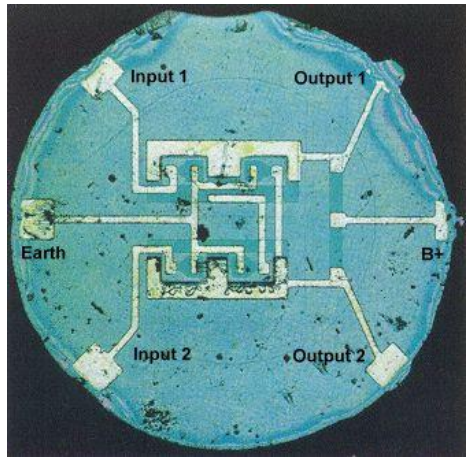
Layout and interconnects

- Device scaling implies cost reduction and increased speed per transistor
- Due to the high number of transistors on chip, layout optimization at chip level has become as important as transistors fabrication
- Interconnecting the devices has become the bottleneck for IC performances



Layouts and interconnects

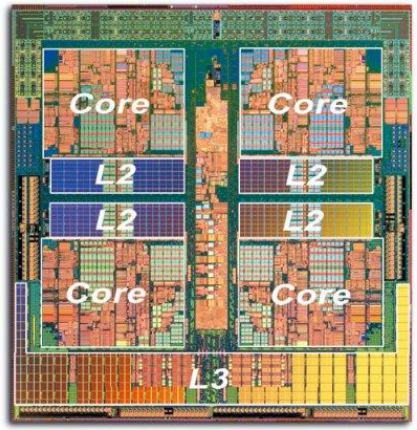
- The processing steps involved in fabricating transistors and their immediate interconnect is called front-end-of-line (FEOL)
- That includes implantation, oxide growth, diffusion and first metal
- Interconnecting all the devices together with higher metals is the back-end-of-line (BEOL)
- As the number of transistors on chips grew, it became impossible to make all connections in a single layer
- Added additional vertical levels of interconnects
- Simpler IC might have a few metal layers, complex ICs can exceed 10 layers

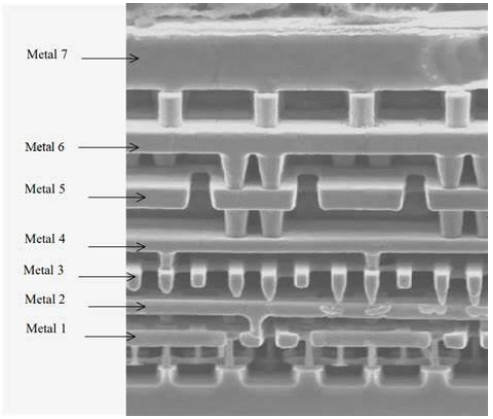


First commercial IC, Fairchild Semiconductor, 1961. Flip-Flop

1. N-Si substrate polishing (80 µm ± 5 µm)
2. Oxidation (wet oxide 8000 Å)
3. MASK 1 (Isolation)
4. Wet etch oxide
5. Boron Deposition and Drive-in
6. MASK 2 (Base and P-Resistor)
7. Boron diffusion (~ 6000 Å oxide, ~ 150 Ω/sq
8. MASK 3 (Emitter and Collector Contacts)
9. Phosphorus Deposition and Drive-in (~ 2 Ω/sq and X_j ~ 1.4–1.6 µm)
10. Resist (front side)
11. Wet etch oxide (back side only)
12. Vacuum Evaporation of Gold on the back side (~ 400 Å)
13. Gold Diffusion (~ 1050°C/~ 15 min with fast cool)
14. MASK 4 (Contacts)
15. Evaporate Aluminum (front side, 0.01 Ω/sq)
16. MASK 5 (Metal)
17. Wet etch metal (25% solution of sodium hydroxide)
18. Metal alloying (~ 600°C/ Argon)

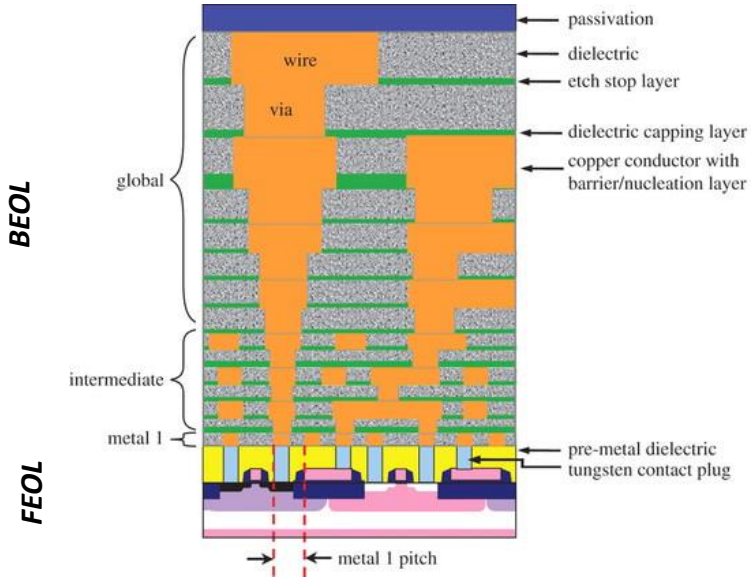
Original Planar process flow (from Fairchild Semiconductor)

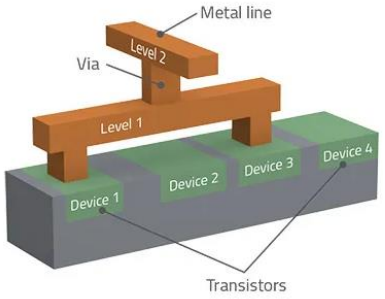




Layout and interconnects

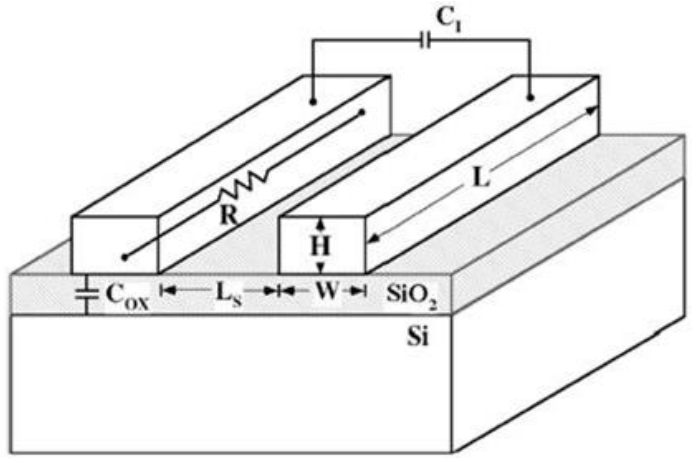
- Various levels of interconnects are present in modern ICs:
  - Metal 1, for short local interconnects
  - Intermediate, to connect devices within blocks
  - Global interconnects, for long, low resistivity connections, including power, grounds
- Various levels are connected by vias and separated by dielectrics





Layout and interconnects

- Interconnects and their layouts are of increasing importance as the feature size of circuit elements become smaller
- Delay times of interconnect transmission line



$$R = \rho \frac{L}{WH}$$

$$C_{ox} = \varepsilon_{ox}\varepsilon_o \frac{WL}{t_{ox}}$$

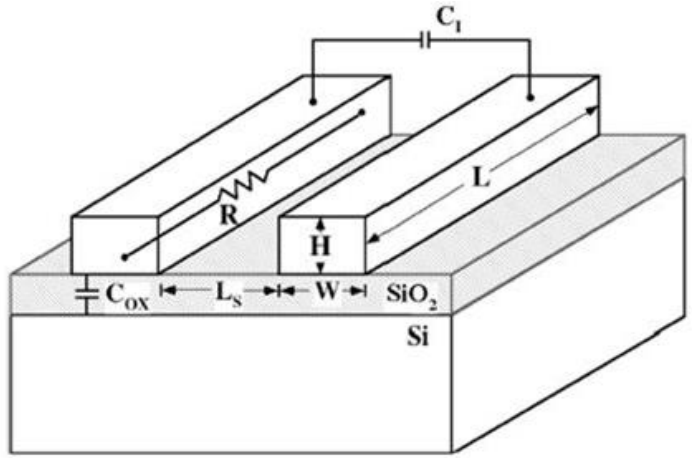
$$C_I = \varepsilon_{ox}\varepsilon_o \frac{HL}{L_s}$$

$$C_{tot} \cong C_I + C_{ox}$$

$$\tau_I \cong \varepsilon_{ox}\varepsilon_o \rho \frac{L^2}{WH}\left(\frac{W}{t_{ox}} + \frac{H}{L_s}\right)$$

Layout and interconnects

- As the technology size decreases:
  - W, L_s and H decrease
  - t_{ox} decrease at ~ the same rate as W and H i.e. scaling factor λ
  - The distance L for local interconnect decreases as the sized of devices gets smaller (~ λ)
  - Time delay for local interconnect remains ~ constant

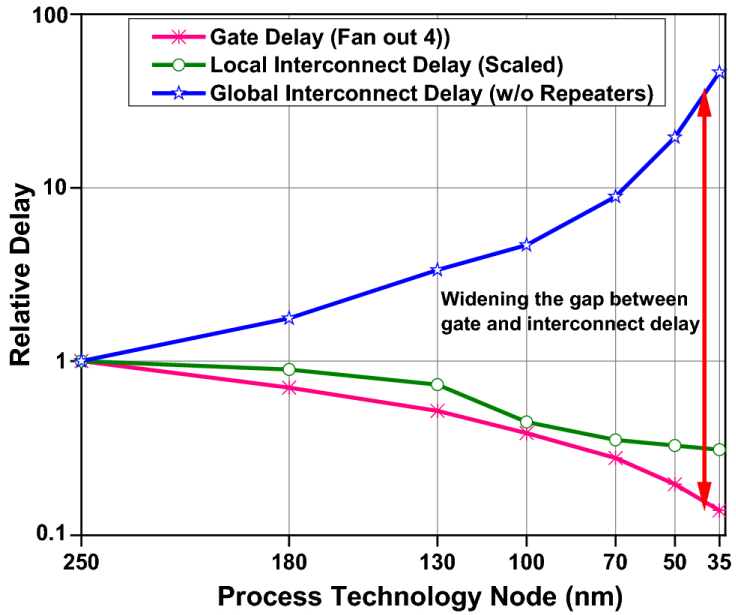


$$\tau_I \cong \varepsilon_{ox}\varepsilon_o\rho\frac{L^2}{WH}\left(\frac{W}{t_{ox}}+\frac{H}{L_s}\right)$$

$$\tau_{Ioc} \cong \varepsilon_{ox}\varepsilon_o\rho\frac{L^2}{\lambda^2}$$

Layout and interconnects

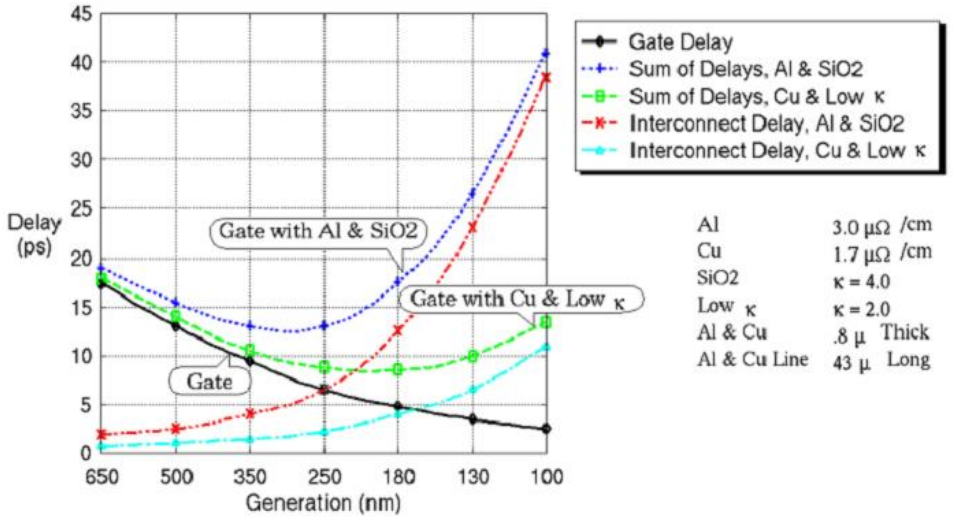
- As the technology size decreases:
  - Area of the die tends to increase
  - Length of global interconnect increases √S
  - Time delay for global interconnect tends to increase



$$\tau_{gIo} \cong \varepsilon_{ox}\varepsilon_{o}\rho\frac{S}{\lambda^2}$$

Layout and interconnects

- Time delay for global interconnect tends to increase as the technology size decreases
- Different materials can be used for the interconnect to reduce ρ and ε

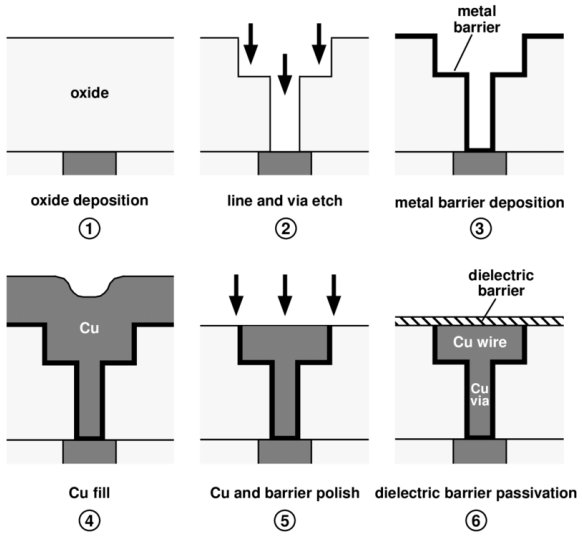


The global interconnect delay vs. technology node for standard and advanced materials

$$\tau_{gIo} \cong \varepsilon_{ox}\varepsilon_o \rho \frac{S}{\lambda^2}$$

Layout and interconnects

- Reducing ρ has been achieved by using Cu instead of Al (Damascene process)
- Reduce ε is more challenging: low-K dielectrics can be obtained using F and other dopants but resulting dielectric show poorer quality
- Air gaps used in some locations in <10 nm nodes



Dual Damascene process. An additional metal barrier (W) is deposited first to avoid Cu contamination of Si. Cu deposited by electroplating. CMP is needed as Cu does not plasma etch.*

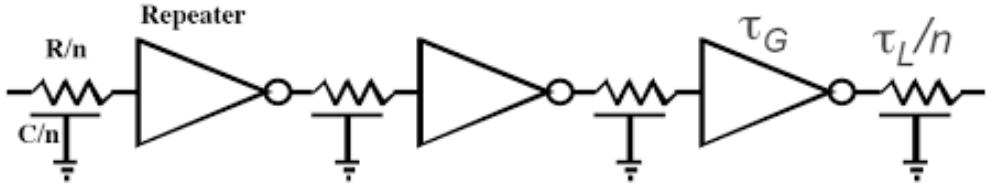
Properties	SiO_2	FSG	Dense low-*k* (OSG)	Porous low-*k*
Density (g/cm^3)	2.2	2.2	1.8~1.2	1.2~1.0
Dielectric constant (k)	4	3.5~3.8	2.8~3.2	1.9~2.7
Modulus (Gpa)	55~70	~50	10~20	3~10
Hardness (GPa)	3.5	3.36	2.5~1.2	0.3~1.0
CTE (ppm/K)	0.6	~0.6	1~5	10~18
Thermal Conductivity (W/mK)	1.0	1.0	~0.8	0.26
Porosity (%)	NA	NA	<10	25~50
Average Pore Size (nm)	NA	NA	<1.0	2.0~10
Breakdown Filed (MV/cm)	>10	>10	8~10	<8

Low- dielectrics have been used for < 100 nm nodes. Reliability issues with very low k-dielectrics

**from ancient sword making technique in Damascus, Syria*

Layout and interconnects

- Another way to reduce interconnect delay is to use pass transistors (or repeaters)
- A long interconnect is broken into n shorter lines, with the delay of each section reduced quadratically
- A small repeaters' delay leads to a reduced global delay but at the expenses of increased occupied area and additional power consumption



A long interconnect line L is broken into n segments

$$\tau_{gIo} \cong \varepsilon_{ox}\varepsilon_o\rho\frac{L^2}{\lambda^2} \qquad \tau_{gIo} \cong \varepsilon_{ox}\varepsilon_o\rho\frac{1}{\lambda^2}\left(\frac{L^2}{n^2}\right)n + (n-1)\tau_g$$

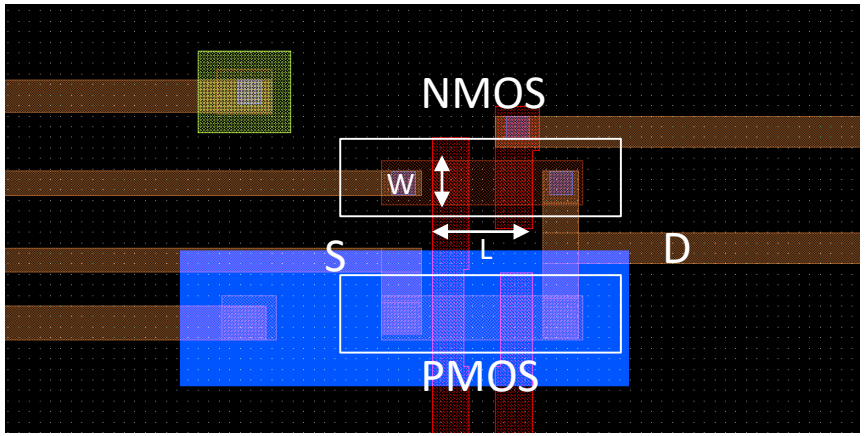
$$n\tau_g < \varepsilon_{ox}\varepsilon_o\rho\frac{1}{\lambda^2}L^2$$

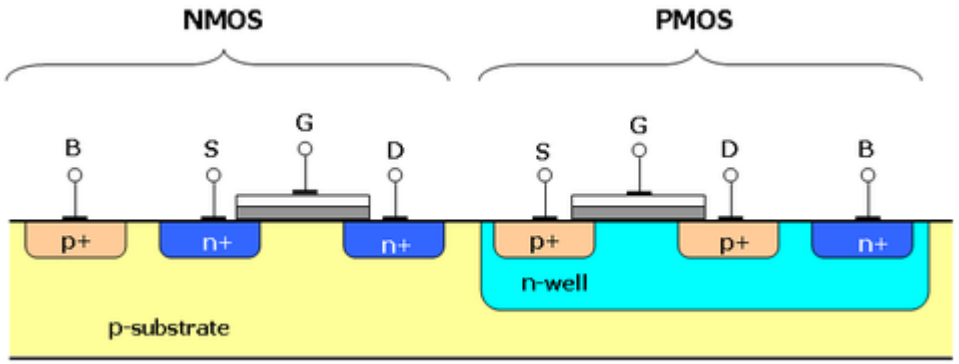
MOS transistor layout

- Very often standard silicon wafers are P type and devices, including MOS transistors, are implemented in them

- This stems from the fact that NMOS are faster than PMOS (e^- mobility higher than h^+)

- Fastest NMOS is obtained from high resistivity (low doping) P substrate rather than lower resistivity (higher doping) P well

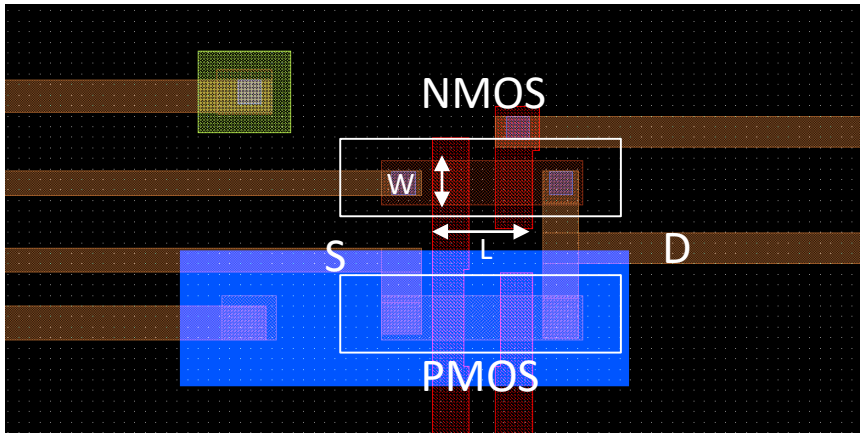




MOS transistor layout

- In digital circuits transistors are normally designed with minimum size, to increase density of functions/storage /area

- In analog circuits a large form factor W/L is required, to increase g_m



$$I_{D,sat} = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

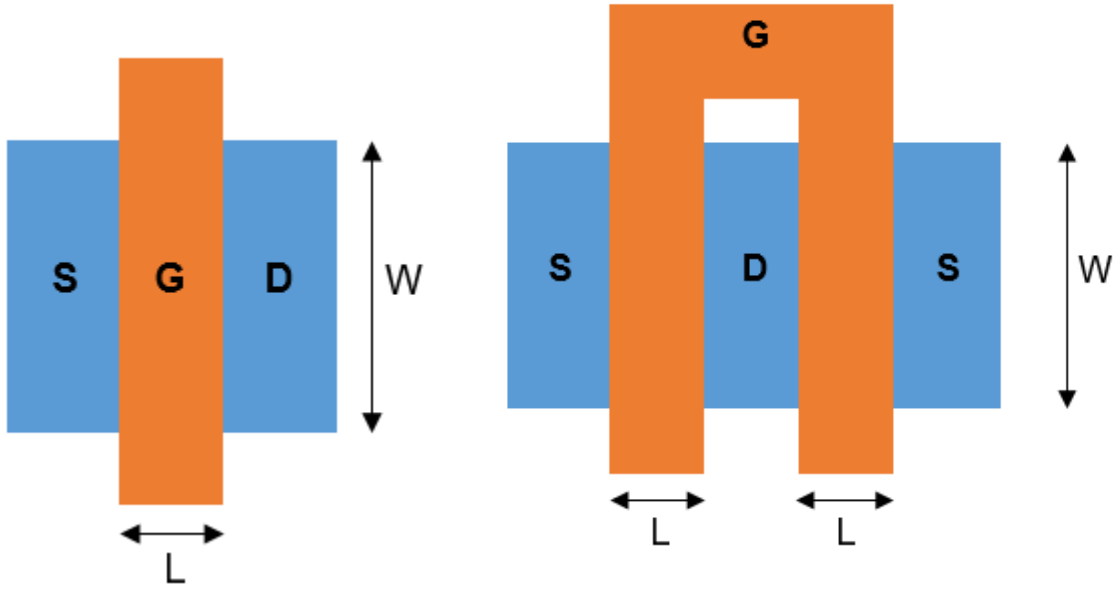
$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu C_o \frac{W}{L}\left(V_{GS} - V_T\right)$$

MOS transistor layout

- In layout of analog transistors the aspect ratio is crucial as it determines g_m (straight structures preferable)

- High W might increase Gate resistance/capacitance

- Special layout issues in analog design:
  - multi-finger structure



$L_{eff}=L$, $W_{eff}=2W$

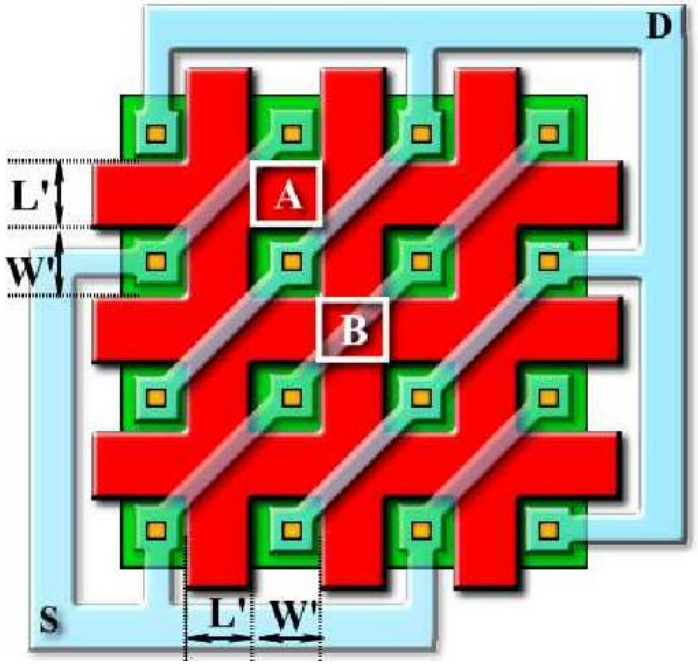
Single finger

Two fingers: W are summed

MOS transistor layout

- Multi finger structures decrease the Gate resistance but increase the parasitic effects (drain-gate coupling, gate to substrate)

- Special structure (Waffle structure) used for RF CMOS applications



$$\left(\frac{W}{L}\right)_{\text{WAFFLE}} = N_{\text{A}}\frac{W'}{L'} + N_{\text{B}}(0.55871)$$

$$N_{\text{A}} = N_{\text{R}} \cdot (N_{\text{C}} + 1) + N_{\text{C}} \cdot (N_{\text{R}} + 1)$$

$$N_{\text{B}} = N_{\text{R}} \cdot N_{\text{C}}$$

P. Vacula 1,2, M. Husák, M. 2013
Waffle MOS channel aspect ratio calculation with Schwarz-Christoffel Transformation

MOS transistor layout

- Typical figures of CMOS process vs. size
- Scaling down does not imply better device characteristics per se

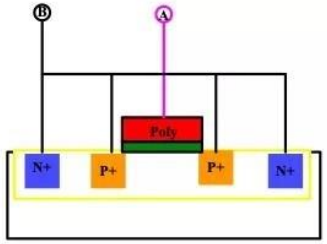
CMOS Tech. min. size L	180 nm	130 nm	90 nm	65 nm	45 nm
V_{DD} (V)	1.8	1.2	1.0	0.9	0.8
g_m (mS/μm)	0.55	0.85	1.01	1.45	1.65
$A_v = g_m/g_{ds}$ (V/V)	19.5	13.1	8.5	7.8	7.1
C_{GS} (fF/μm)	1.37	1.06	0.82	0.55	0.45
C_{GD} (fF/μm)	0.45	0.42	0.39	0.34	0.31
f_T (GHz)	50	90	128	160	226
NF_{min} (dB)*	>0.5	0.5	0.33	0.2	<0.2

*Estimated at 2 GHz for the NMOS devices in [2].

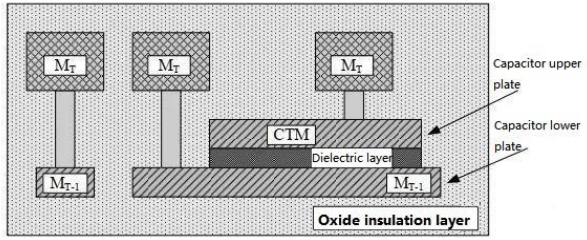
	0.8μm		0..5μm		0..25μm		0.18μm	
PARAMETER	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
$t_{OX}(nm)$	15	15	9	9	6	6	4	4
$C_{OX}(fF/\mu m^2)$	2.3	2.3	3.8	3.8	5.8	5.8	8.6	8.6
$\mu(cm^2/V.S)$	550	250	500	180	460	160	450	100
$\mu C_{OX}(\mu A/V^2)$	127	58	190	68	267	93	387	86
$V_t(V)$	.7	-.7	.7	-.8	.43	-.62	.48	-.45
$V_{DD}(V)$	5	5	3.3	3.3	2.5	2.5	1.8	1.8
$V'_A(V/\mu m)$	25	20	20	10	5	6	5	6
$C_{OV}(fF/\mu m)$	.2	.2	.4	.4	.3	.3	.37	.33

Passive components layout

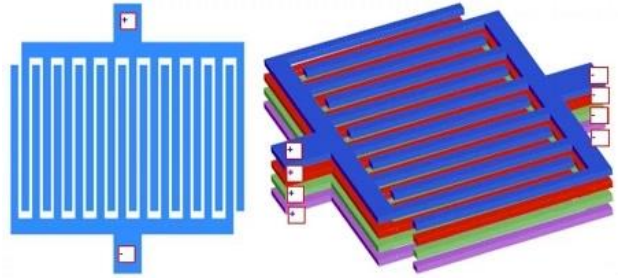
- Integrated Capacitors are normally obtained by structures close to the silicon substrate
- Three type of capacitors:
  - MOS (Poly Oxide Well)
  - MiMs (Metal Insulator Metal)
  - Parasitic (MoM)



MOS capacitor changes with voltage but save area



MIM use different layers of metal and interposed dielectric to form a capacitor. Similar to plate capacitor, good stability but require additional masks



MOM use interdigitated capacitors formed by metal connections, placed in close proximity – preferred choice for advanced CMOS, also no additional mask required

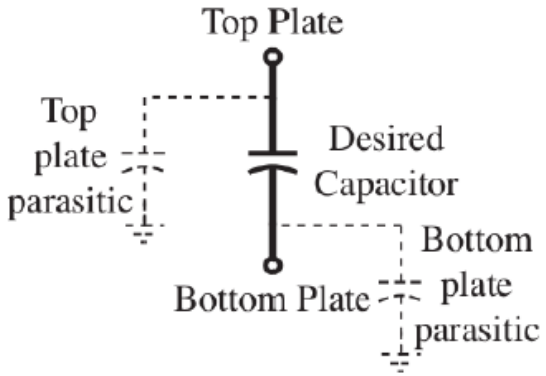
Passive components layout

- Typical values of capacitance
- Typical dielectric layers are SiO_2 or Si_3N_4
- Use of high k materials is common in more advanced CMOS technologies

$$C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL$$

$$t_{ox} = 4\ nm$$

$$C = 8.6\ fF/\mu m^2$$



MIM/MOMs parasitic

$$C_{t,p} = 0.1\ \%\ C$$

$$C_{b,p} = 1\ \%\ C$$

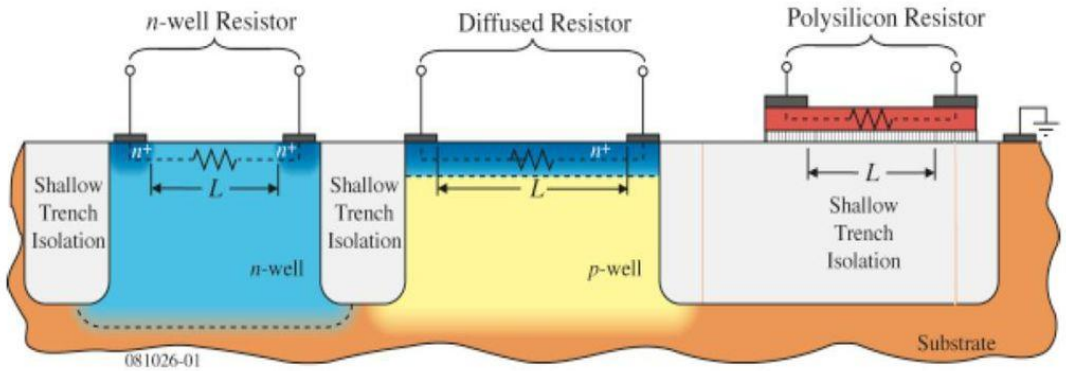
Passive components layout

- Integrated Resistors are normally obtained by thin strips of resistive layers

- Insulation from surrounding achieved by oxide layers or reversed biased junctions

Resistors

- **Diffused and/or implanted resistors.**
- **Well resistors.**
- **Polysilicon resistors.**
- **Metal resistors.**
- **Thin film resistors**



$Nwell$: $\rho_{\blacksquare} \sim 1\ k\Omega/\blacksquare$

$Poly$: $\rho_{\blacksquare} \sim 10\ \Omega/\blacksquare$

$Metallic$: $\rho_{\blacksquare} \sim 0.1\ \Omega/\blacksquare$ $\quad R = \rho_{\blacksquare} \frac{L}{W}$

Thank you

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- Layouts and interconnects in IC
  - FEOL and BEOL different characteristics
  - Interconnect delays and ways to mitigate them
- Transistors layouts intro
- Passive components layouts intro