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Transistors in Instrumentation

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Introduction

Notes on the Content

- Thanks to many people who provided content or useful discussion for these slides (particularly the rest of the CSDG – Seddik Benhammadi, Daniel Brown, Matthew Brown, Nicola Guerrini, Peter Hatfaludi, Herman Larsen, Ben Marsh, Bindu Velagapudi)

- Also Eva Villela (U. Liverpool) who previously delivered this course and generously provided the slides from those courses as the basis for these talks.

- Only an overview is really possible in the available time. Many links are included in the text for further information.

- Time for questions at the end, and very happy to take further questions by e-mail (iain.sedgwick@stfc.ac.uk)

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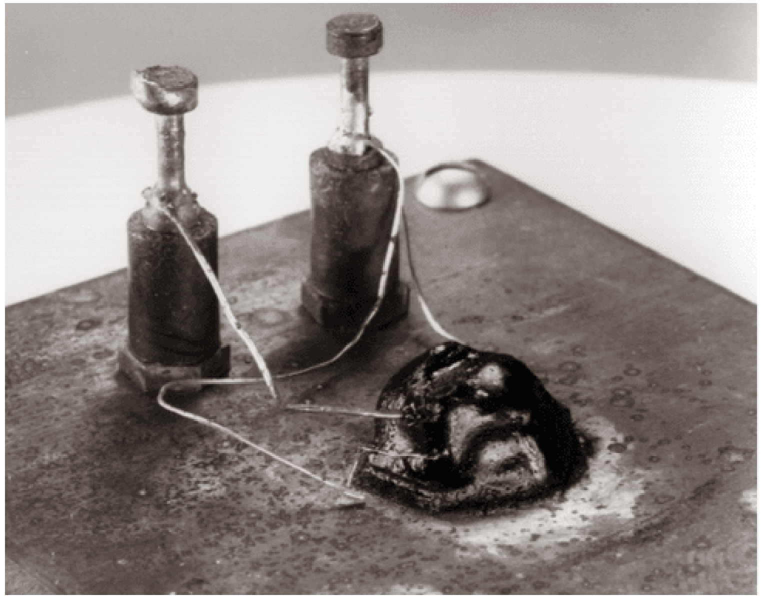
History

History

The First Transistor

- First transistor was invented in 1947 at Bell Labs by John Bardeen and Walter Brattain, in the group of William Shockley – this was the Point Contact Transistor
- Shockley went on to develop the Bipolar Junction Transistor, which Bell announced in 1951
- All three won the Nobel Prize in 1956
- Great summary here and here



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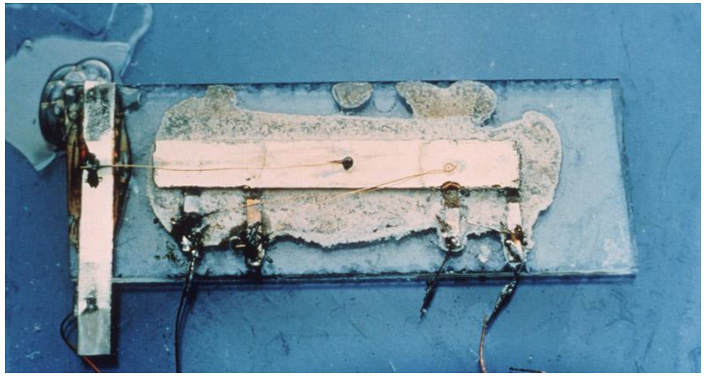
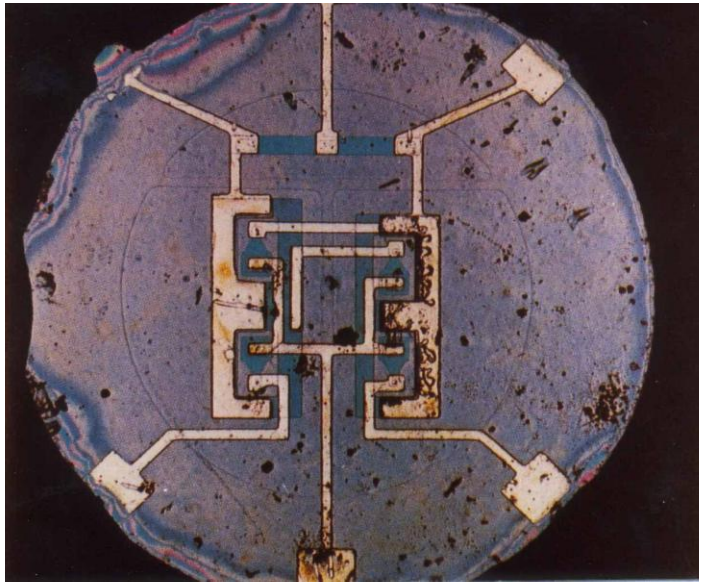
History

The Bipolar Junction Transistor

- However, these were germanium devices. Germanium has a low bandgap, and consequently a high leakage current, which makes for an imperfect transistor.
- In 1954, Texas Instruments produced the first silicon BJT.
- In 1958, they went a step further and produced the first integrated circuits



- J. Kilby, Texas Instruments, 1958
- Circuit with transistors connected by metallic wires (by hand)



- R. N. Noyce, Fairchild Semiconductors, 1959
- First monolithic integrated circuit with devices isolated by PN junctions and interconnected with aluminium lines

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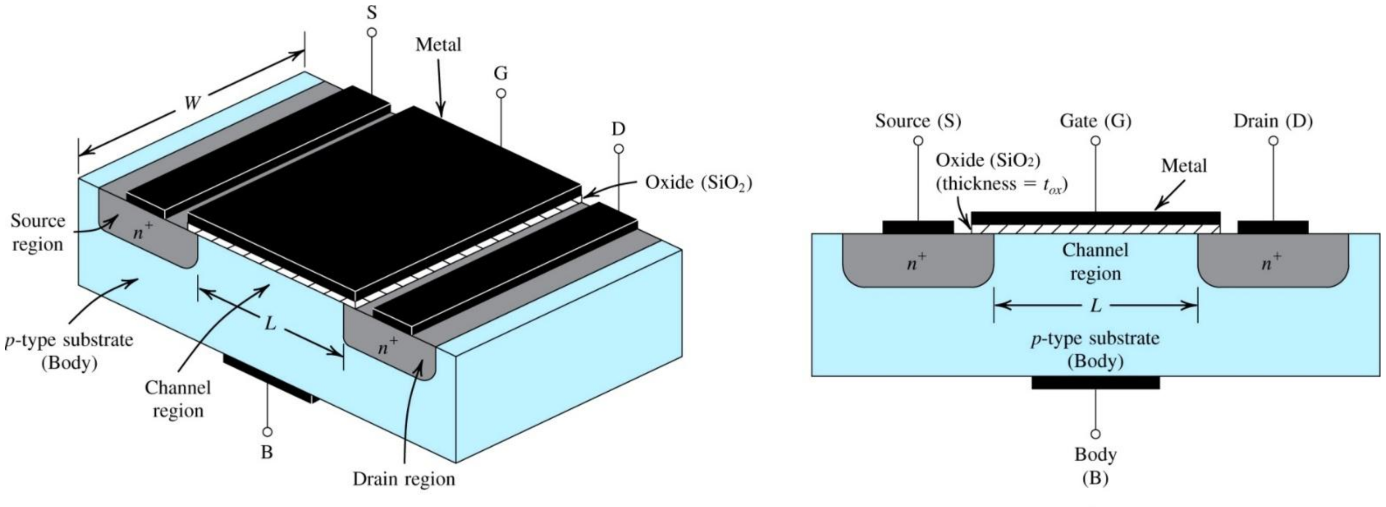
History

Metal Oxide Semiconductor Field Effect Transistor

- First fabricated by Atalla and Kahng, again at Bell Labs, in 1960.
- Controls the conduction between two doped regions using an applied electric field
- MOSFETs advantages make them more suited to digital applications, BJTs to analog
- In practice, advances to support digital have become so ubiquitous that much analog design is carried out in CMOS processes

	BJT	MOSFET
Advantages	• Higher linearity and gain • Better TID resistance	• Higher Input Impedance • Faster switching Speeds • Lower Power • More compact
Disadvantages	• Lower Input Impedance • Slower Switching • Susceptible to bulk damage	• Lower linearity and gain



(a) (b)

Figure 1: Physical structure of an NMOS transistor: **(a)** perspective view, **(b)** cross-section.

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The MOSFET

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The MOSFET

Structure

- Built in a p-type substrate. Two n-type regions form the source and drain
- The gate controls conduction between these nodes
- “Metal” is now a misleading historical term. The gate is polycrystalline silicon (“poly”)
- Note it is a **4 terminal device**. The bulk matters!

N.B. Will focus on NMOS throughout this talk. PMOS is the reverse.

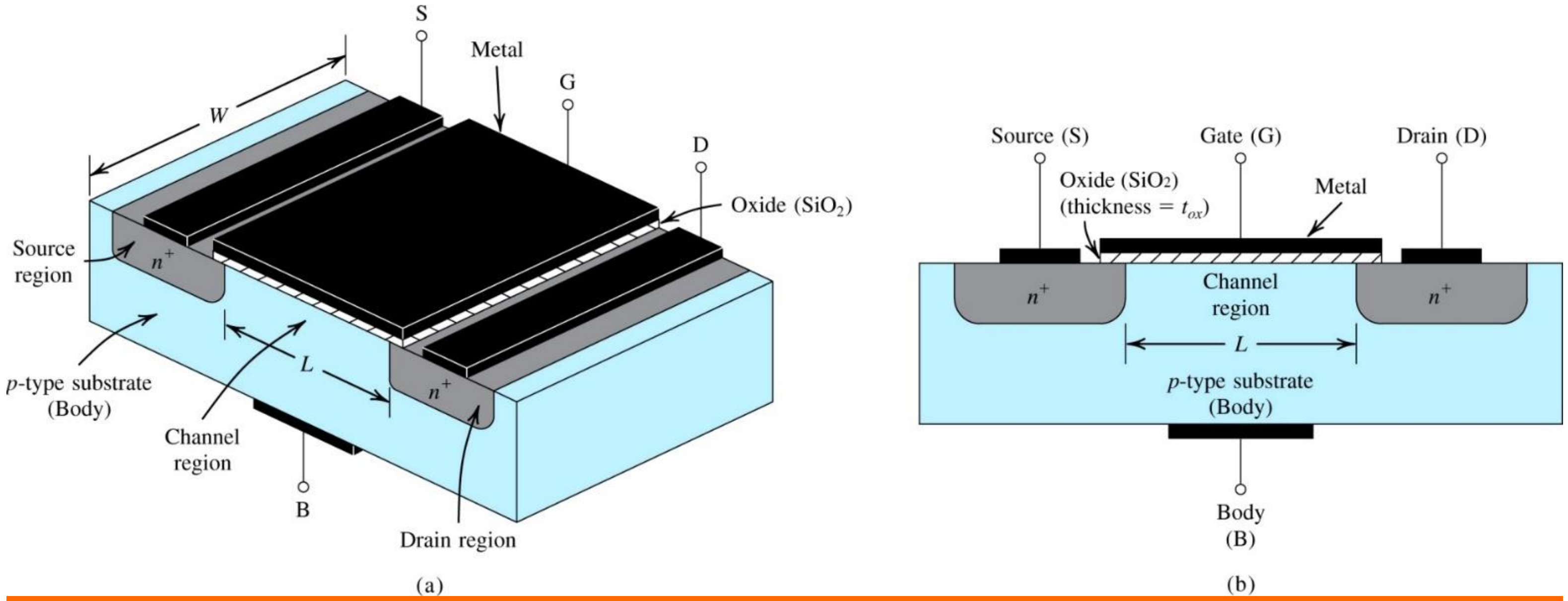

Figure 1: Physical structure of an NMOS transistor: **(a)** perspective view, **(b)** cross-section.

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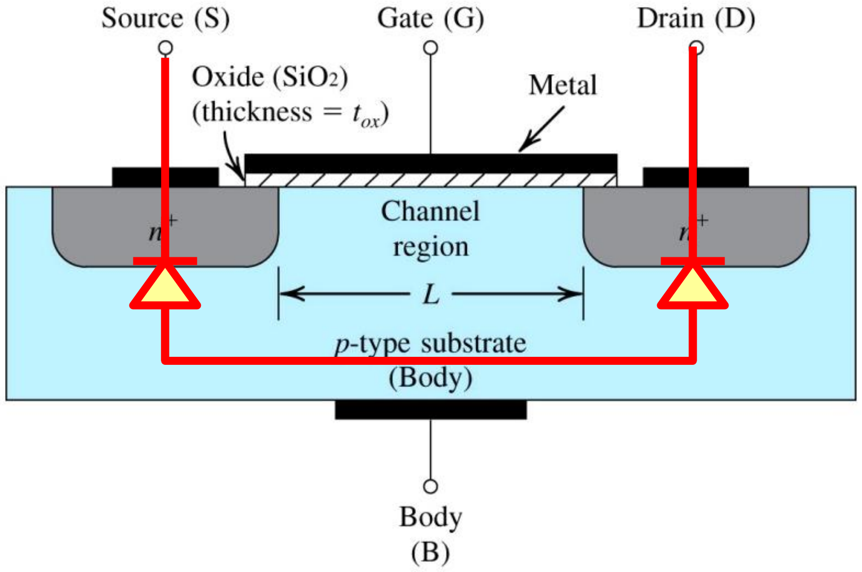
The MOSFET

Mode of Operation

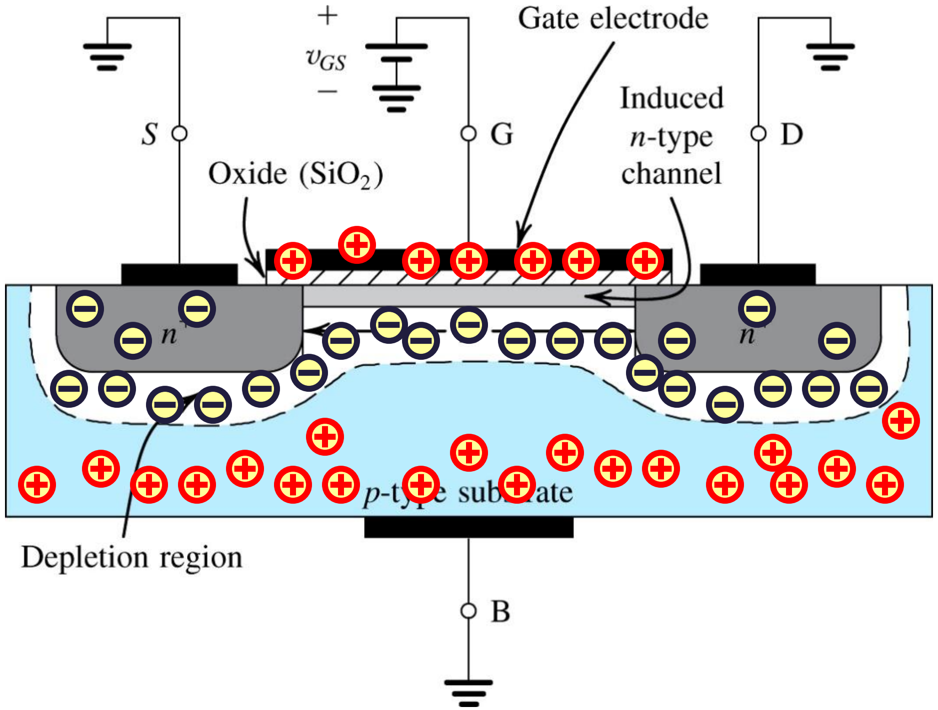
- **Cut-off Region**
  - With zero voltage applied to gate, two back-to-back diodes exist in series between drain and source.
  - “They” prevent current conduction from drain to source when a voltage vDS is applied.
  - Yielding very high resistance (10^{12} ohms)
  - A depletion region exists around the source and drain



The MOSFET

Mode of Operation

- **Sub-threshold and Linear Regions**
  - A positive Vgs is applied to the gate, leading to a build up of positive charge
  - This repels free holes and attracts free electrons under the gate
  - While Vgs is below the MOSFETs threshold voltage Vt, it is said to be in “sub-threshold”
  - Above Vt, sufficient holes have been repelled and electrons attracted that the substrate below the gate is locally n-type.
  - This is called “inversion” and the device is now in the triode region of operation. Increasing Vds will lead to increasing Ids in the ohmic channel

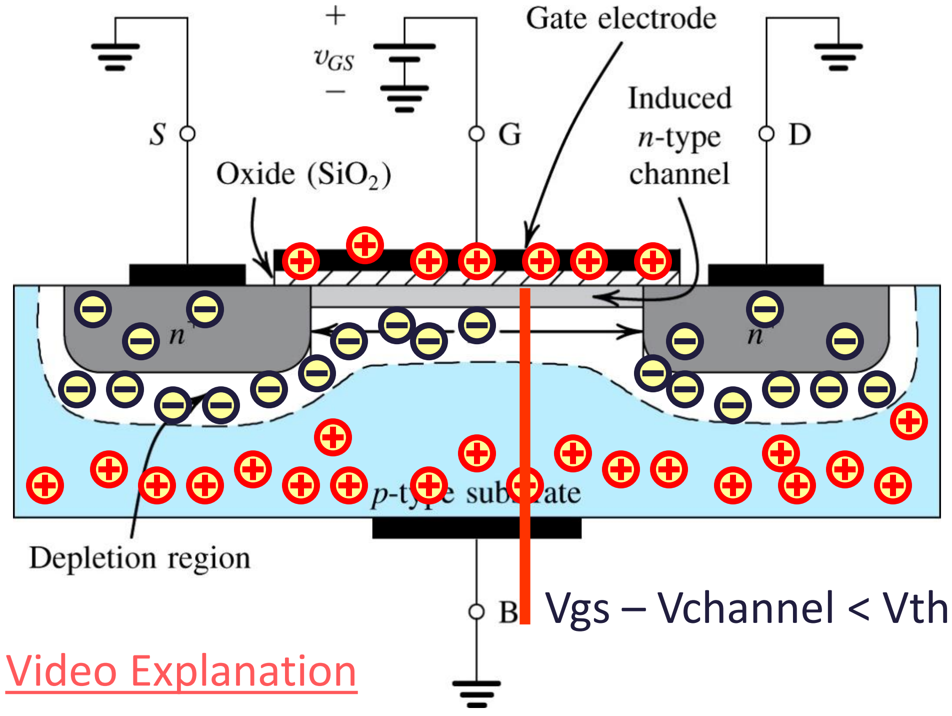


$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2]$$

The MOSFET

Mode of Operation

- **Saturation Region**
  - As Vds increases, the Vds voltage is dropped linearly along the channel.
  - This means that at some point, the gate voltage relative to the channel will be below Vth, and the channel will not exist. This is called "pinch-off"
  - Increasing Vds will not lead to an increase in Ids, because the voltage over the remaining channel is never more than Vgs-Vth
  - Conduction continues without a channel because the electric field in the depletion region sweeps charges into the drain



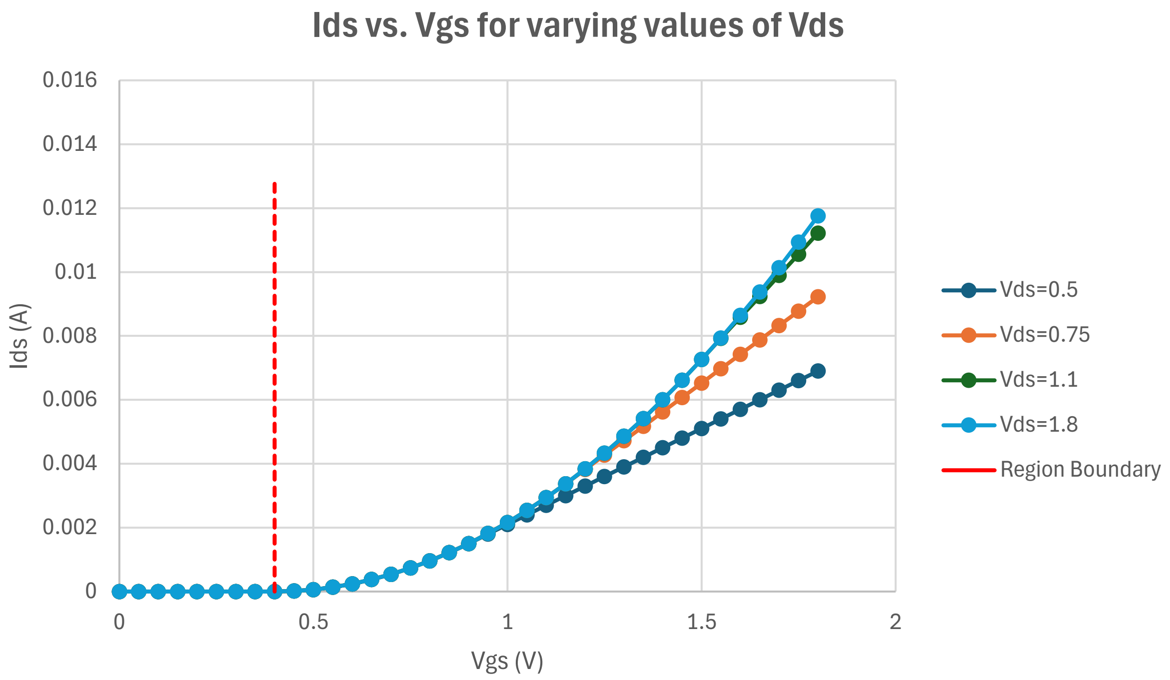
Vgs – Vchannel < Vth

Video Explanation

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{T0})^2$$

So what does that look like when we put it all together?

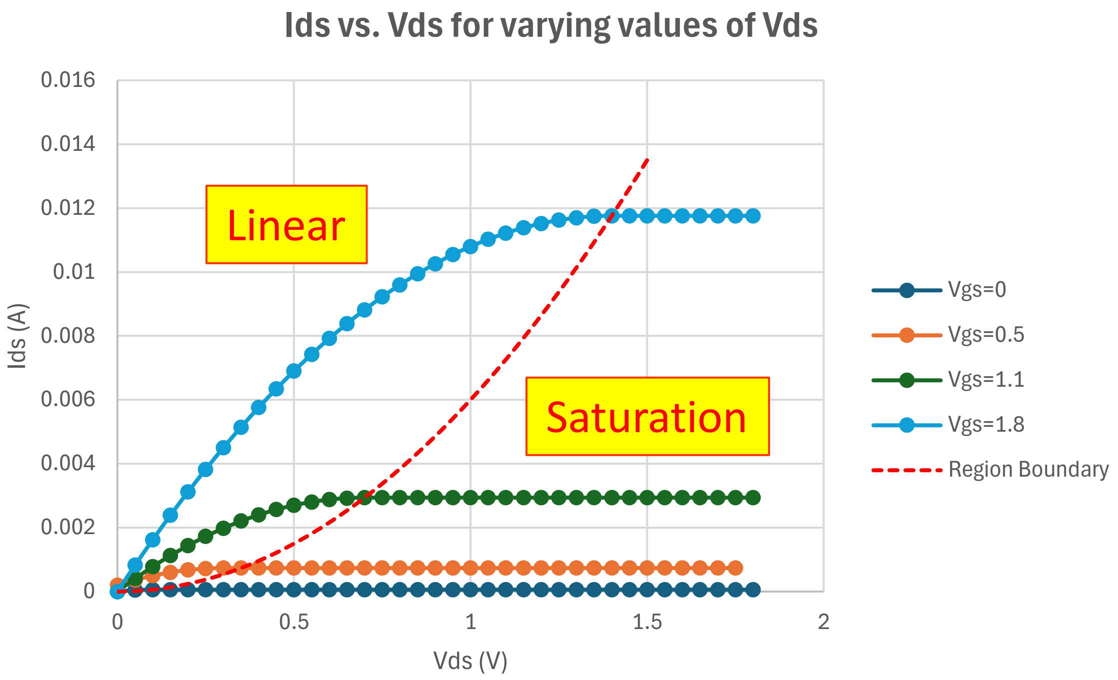
The MOSFET



Cut-off

Linear and Saturation

Sub-threshold



Can this be right?

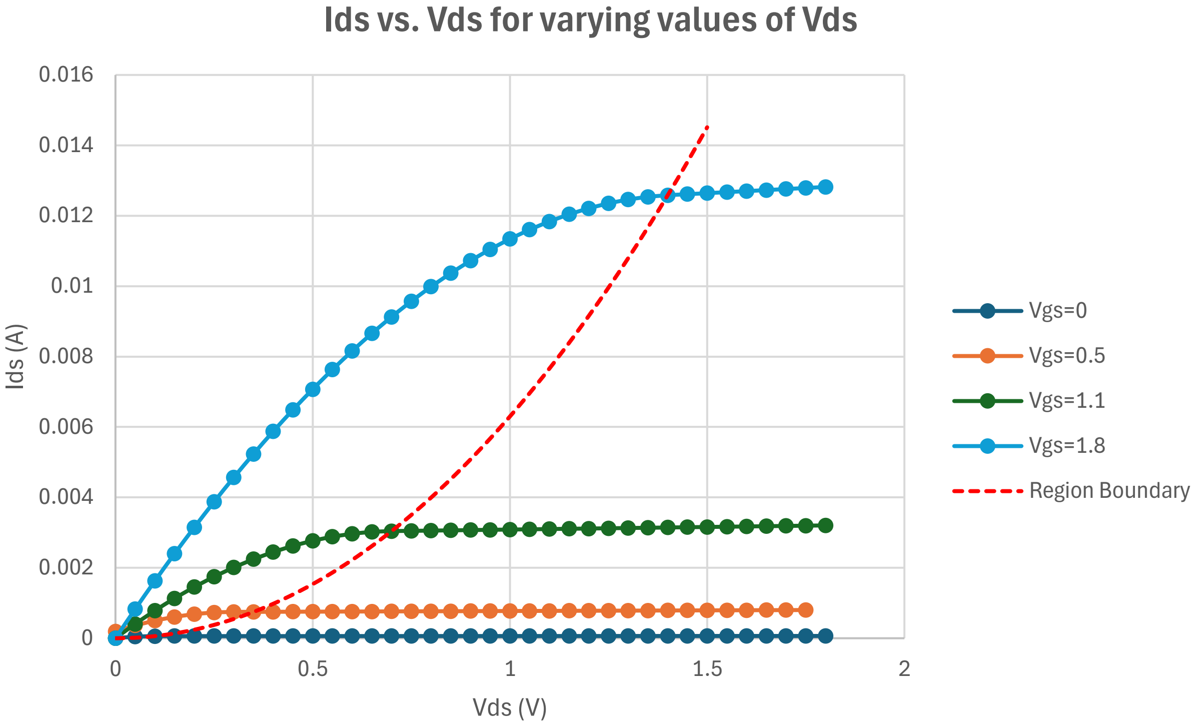
- Curve is completely flat in this region.
- Implies infinite resistance (no variation in current even for an infinite variation in voltage)
- What did we miss?

The MOSFET

Channel Length Modulation

- As Vds is increased, the depletion region around the drain grows larger
- This shortens the channel region
- Since the channel is effectively a resistor, this means the current rises
- Modelled by the parameter λ, which represents the shortening of the channel
- The effect is more pronounced the shorter the channel is

We will stop here, but many other effects exist, especially for short channel devices – DIBL, HCI, leakage, velocity saturation. Then more again for FinFETs, GAA…



$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{T0})^2$$

$$I_D(\text{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{T0})^2(1 + \lambda V_{DS})$$

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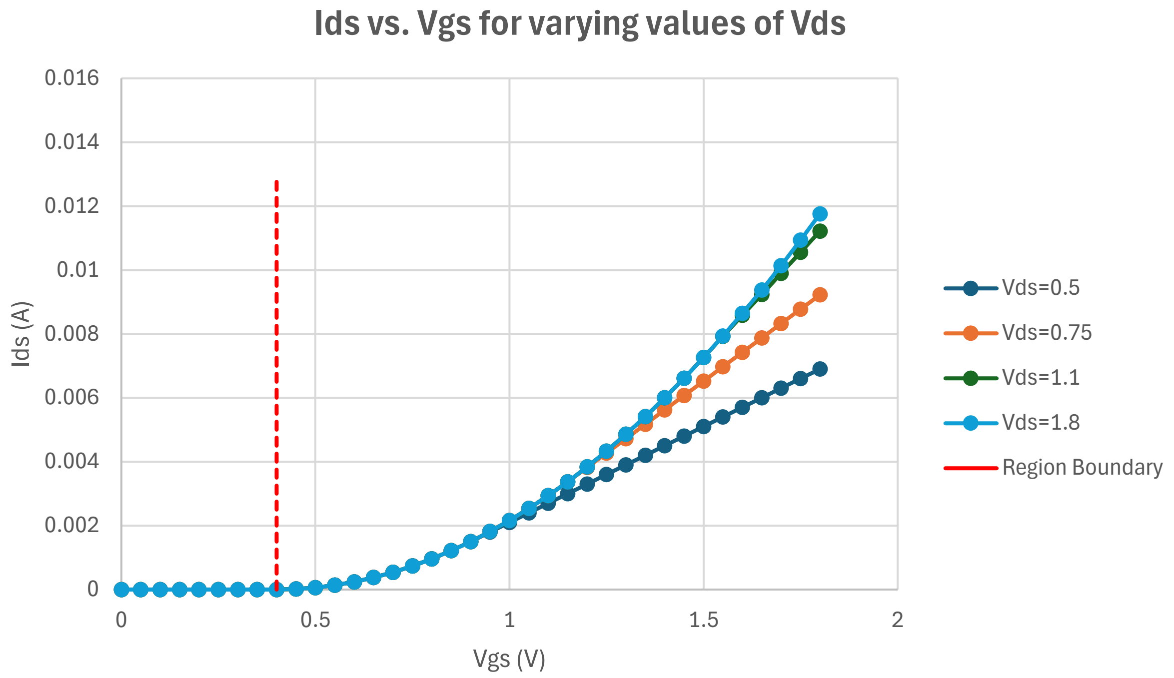
$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2]$$

Linear

$$I_D(\mathrm{sat}) = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS}-V_{T0})^2(1+\lambda V_{DS})$$

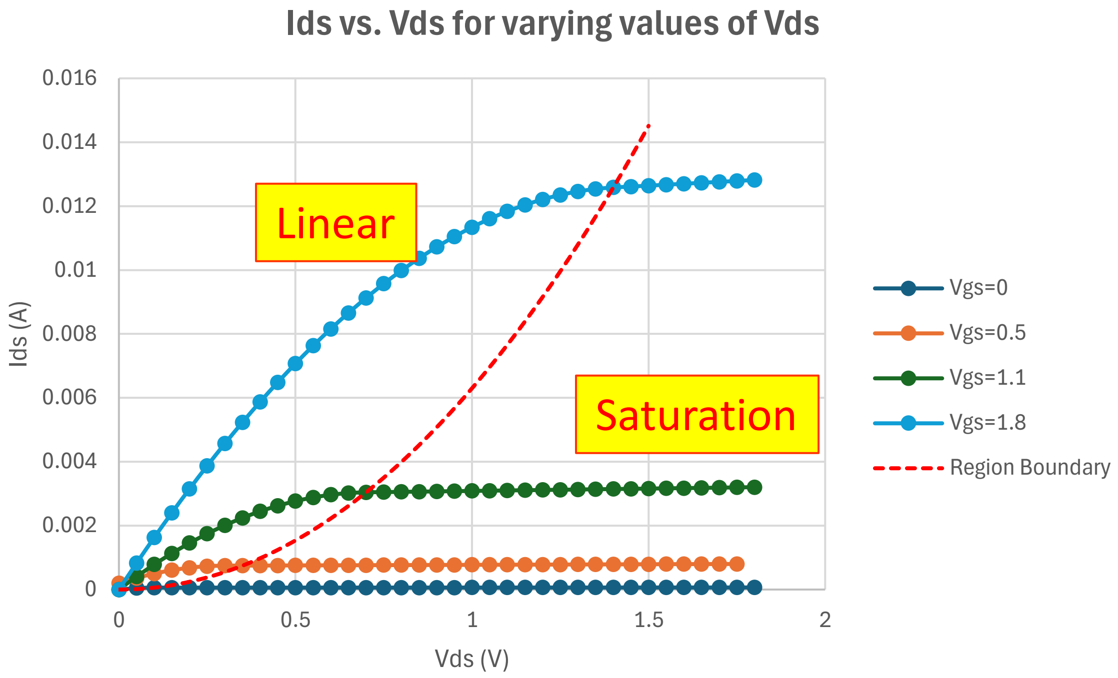
Saturation



Cut-off

Linear and Saturation

Sub-threshold



Linear

Saturation

Summary

- This is called the large signal model
- In SPICE, it is the equivalent of a DC simulation
- It is highly non-linear, so for hand and computer calculation, a linearised small signal model is normally used.

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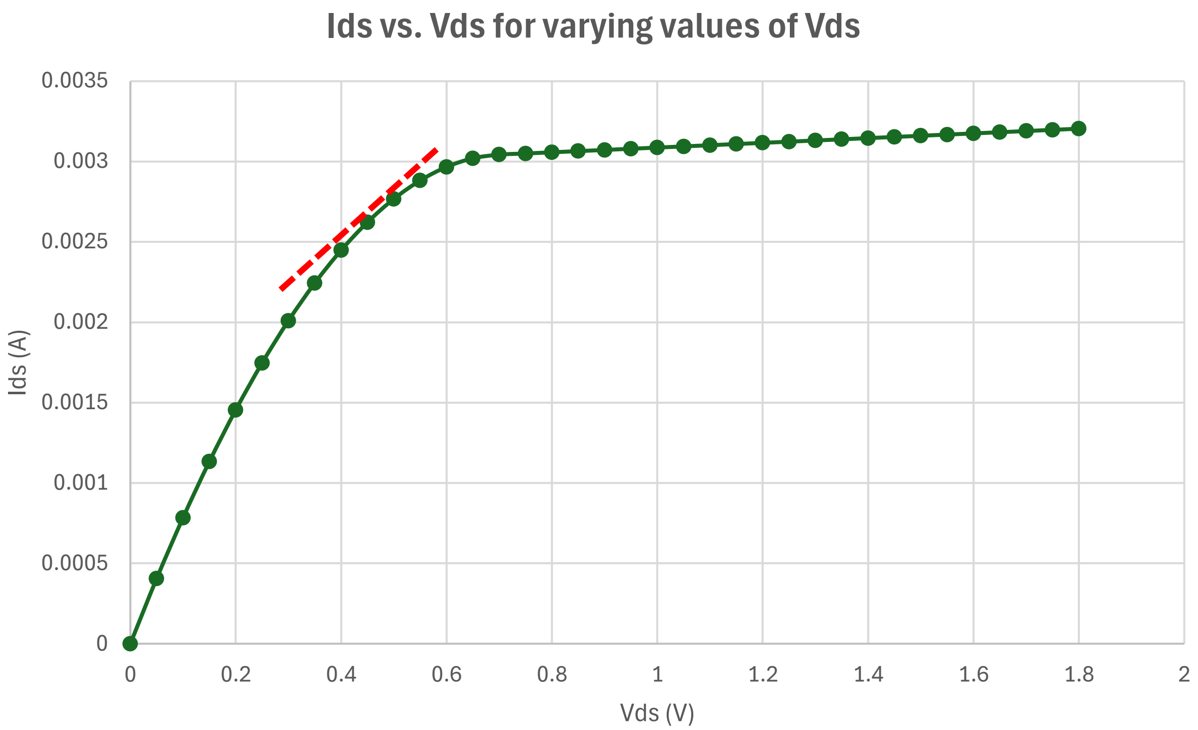
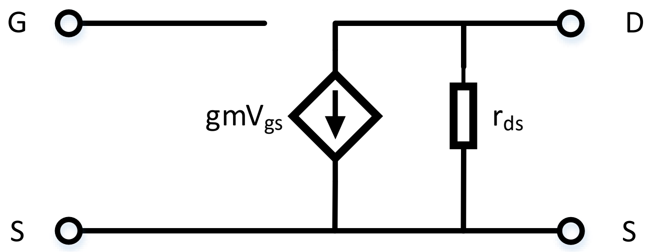
Weida’s Lecture

The MOSFET

The Small Signal Model

- Large signal model covers the whole operating region of the MOSFET, but is highly non-linear
- To simplify calculation, we create a linearised small signal model, which is valid for small regions around a given point of the large signal model
- Graphically, this can be thought of as a small linear region of the curve, mathematically, it involves differentiating the large signal equations
- Simulators work the same way





$$g_{ds} = \frac{dI_{ds}}{dV_{ds}} = \lambda I_{ds}$$

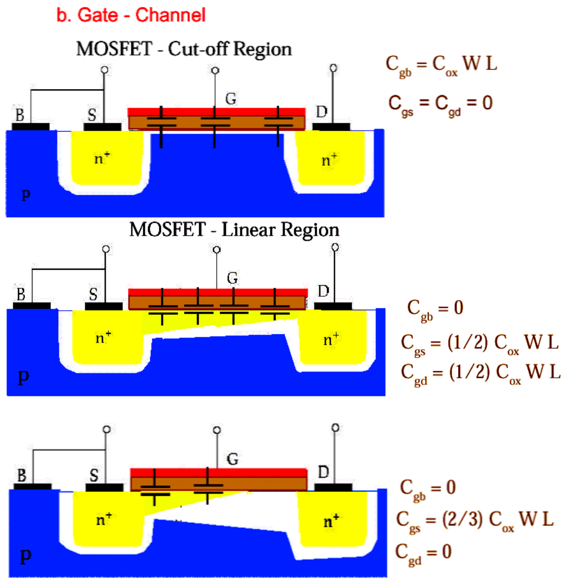
$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\lambda I_{ds}}$$

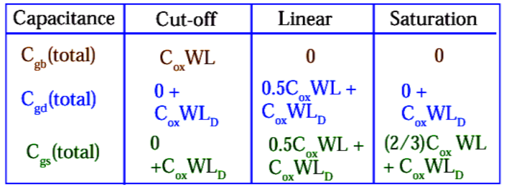
$$gm = \frac{dI_{ds}}{dV_{gs}} = \mu_0 C_{ox} \frac{W}{L} \left(V_{gs} - V_t\right) = \sqrt{2\mu_0 C_{ox} \frac{W}{L} I_{ds}}$$

The MOSFET

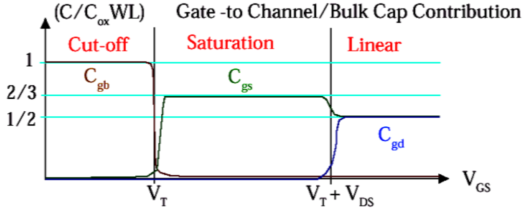
The Small Signal Model

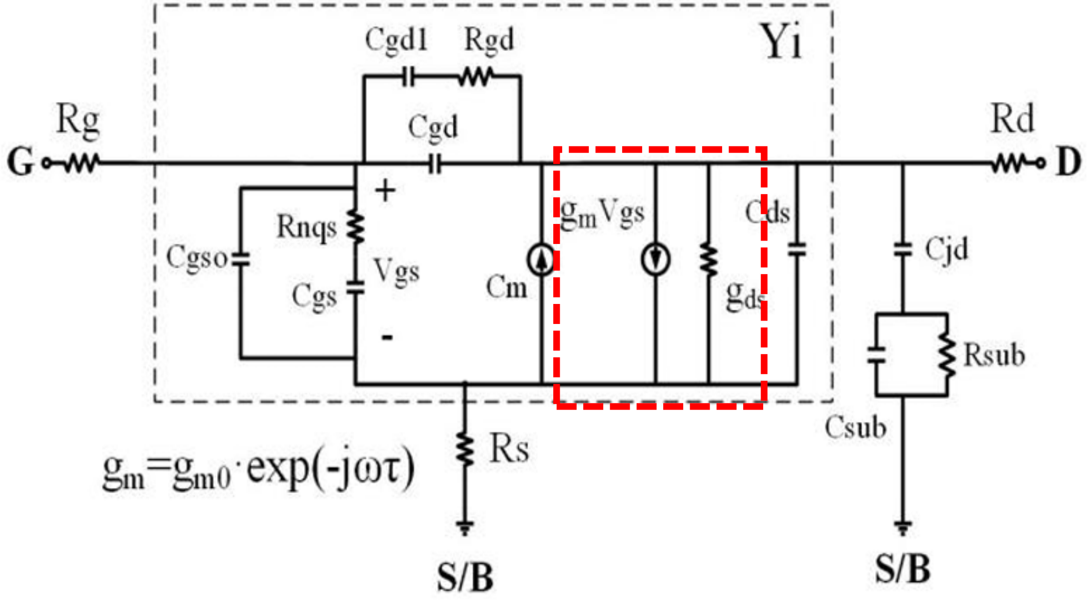
- Note, however, that this is a dramatically simplified version of the small signal model
- Transconductances and conductances exist between all terminals
- Parasitic capacitances exist between all terminals, and their value varies with operating region





Capacitance	Cut-off	Linear	Saturation
C_{gb}(total)	$C_{ox}WL$	0	0
C_{gd}(total)	$0 + C_{ox}WL_D$	$0.5C_{ox}WL + C_{ox}WL_D$	$0 + C_{ox}WL_D$
C_{gs}(total)	$0 + C_{ox}WL_D$	$0.5C_{ox}WL + C_{ox}WL_D$	$(2/3)C_{ox}WL + C_{ox}WL_D$



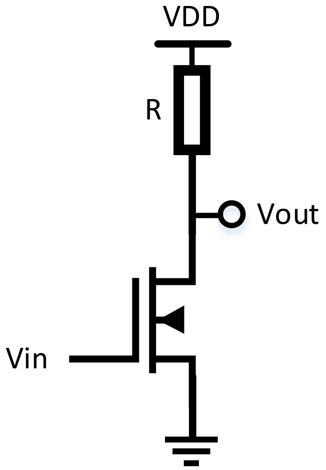


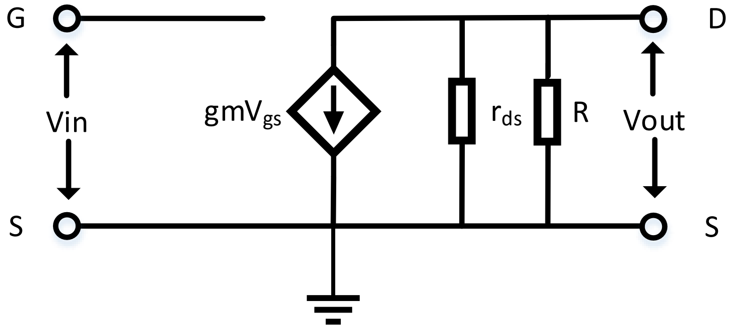
https://doi.org/10.1109/JEDS.2019.2900202

The MOSFET

Designing with MOSFETs

- Use simple common source stage as example
- Small signal model shows how high level specification (gain in this case) depends on parameters the designer can control
- For individual devices, can also use figures of merit for each transistor
- How to go about selecting these?
- Lots of options – will look at two here:
  - Square Law Design
  - Look Up Tables





$$A_v = -g_m\left[\frac{1}{\frac{1}{r_{ds}}+\frac{1}{R}}\right]$$

R

$$r_{ds} = \frac{1}{g_{ds}} = \frac{1}{\lambda I_{ds}}$$

Ids and indirectly, L

$$gm = \sqrt{2\mu_0 C_{ox}\frac{W}{L}\,I_{ds}}$$

Ids, W, L

$\frac{g_m}{I_d}$	Transconductance efficiency
$\frac{f_t}{C_{gg}}$	Transit Frequency
$\frac{g_m}{g_{ds}}$	Intrinsic Gain

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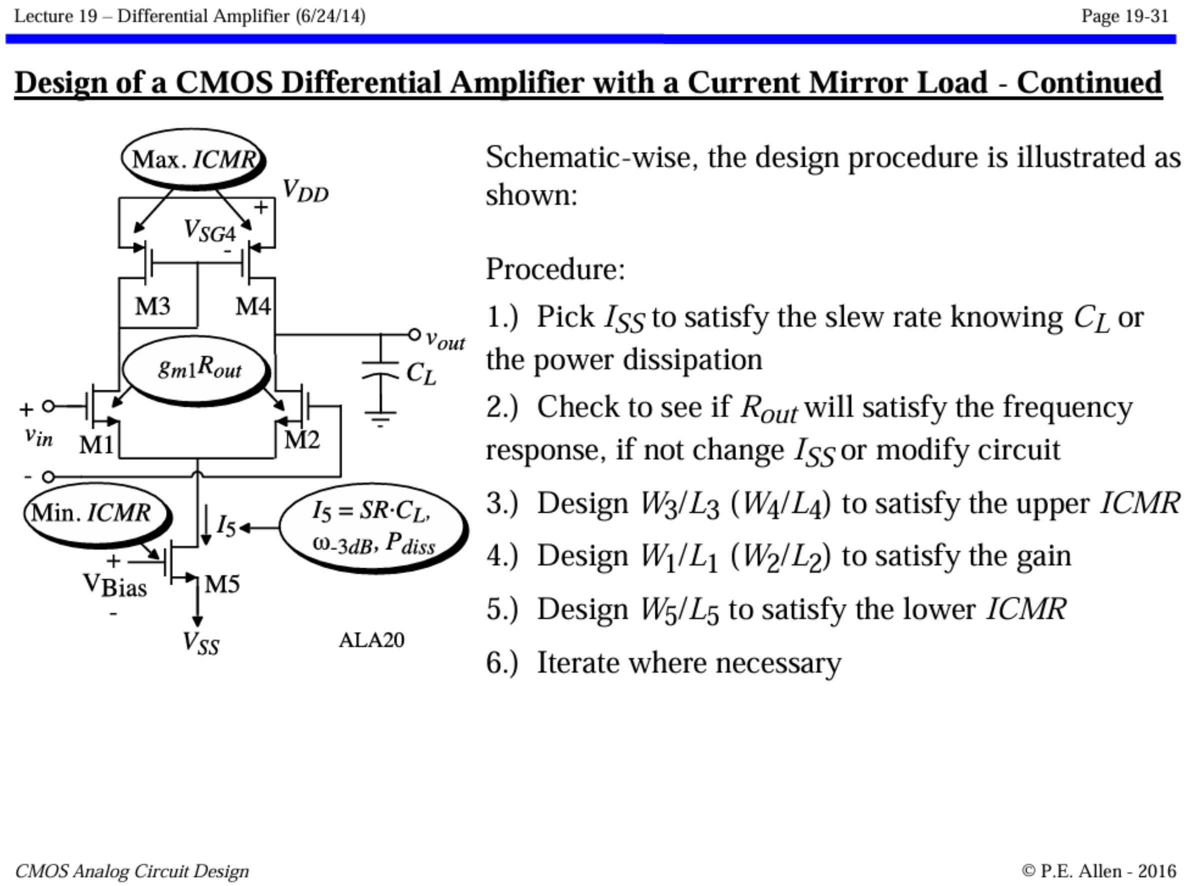
The MOSFET

Square Law vs. Look Up Tables

- Use of the square law equations is the traditional method
- Select an overdrive voltage to bias the FETs well into saturation, then proceed using the equations we have just seen
- Design recipes can be used (good examples here and here), or can optimise figures of merit
- Issues:
    - At smaller nodes, harder to achieve the Vov needed for the square law to be valid
    - Square law is poor in moderate and weak inversion
    - Square law does not apply in sub-threshold



Lecture 19 – Differential Amplifier (6/24/14) Page 19-31

Design of a CMOS Differential Amplifier with a Current Mirror Load - Continued

Schematic-wise, the design procedure is illustrated as shown:

Procedure:

1.) Pick I_{SS} to satisfy the slew rate knowing C_L or the power dissipation

2.) Check to see if R_{out} will satisfy the frequency response, if not change I_{SS} or modify circuit

3.) Design W_3/L_3 (W_4/L_4) to satisfy the upper $ICMR$

4.) Design W_1/L_1 (W_2/L_2) to satisfy the gain

5.) Design W_5/L_5 to satisfy the lower $ICMR$

6.) Iterate where necessary

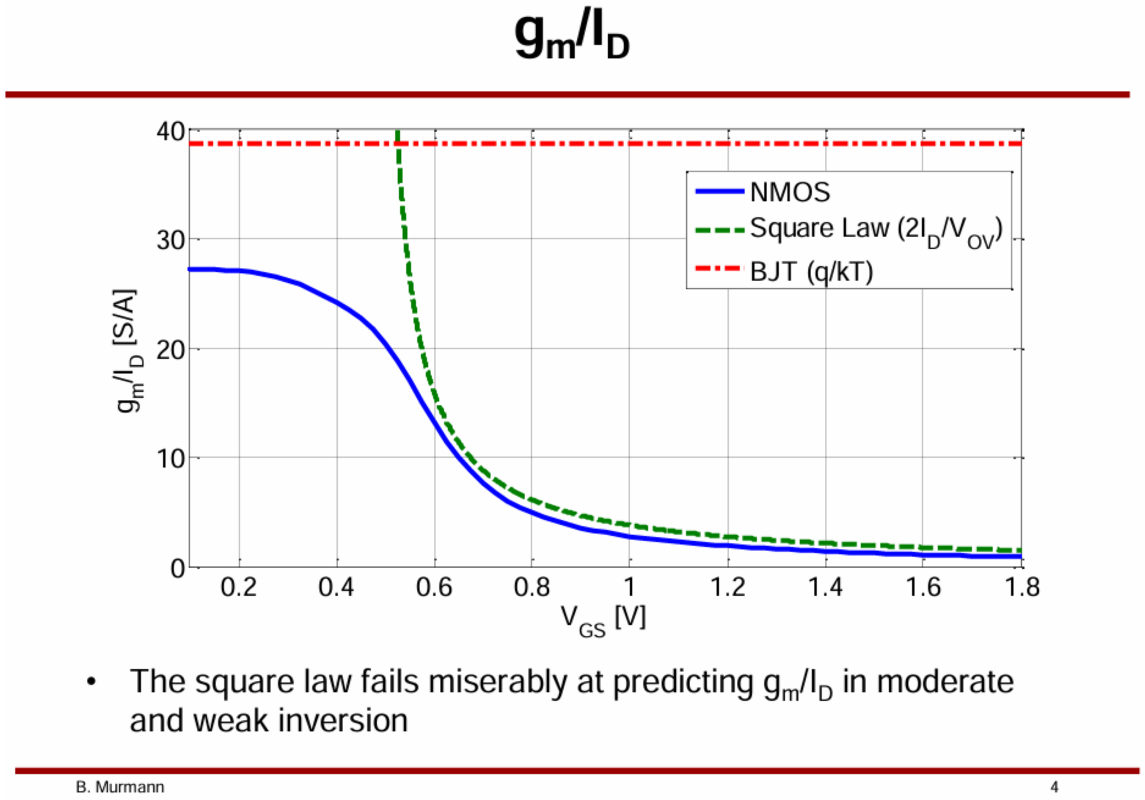
CMOS Analog Circuit Design © P.E. Allen - 2016

https://aicdesign.org/wp-content/uploads/2018/08/lecture19-150211.pdf

The MOSFET

Square Law vs. Look Up Tables

- More advanced models exist which cover all regions (EKV for example) and these can be used for design
- Can be complex to characterise and use. Scripts exist to simplify the starting process
- Another option (pioneered by Paul Jespers and Boris Murmann) is to use Look Up Tables
- These:
    - Allow a perfect match between "hand" calculation and simulation
    - Cover all operating regions
- Ultimately choose most suitable approach for situation



g_m/I_D

- The square law fails miserably at predicting g_m/I_D in moderate and weak inversion

B. Murmann

4

https://www.ieeetoronto.ca/wp-content/uploads/2020/06/20160226toronto_sscs.pdf

https://www.youtube.com/watch?v=oNDmJ2a3tWI

	Square Law	**Lookup Tables**
Accuracy	Poor for advanced nodes and sub-threshold	Perfect match to simulation
Results	Can be poor (always assumes strong inversion)	Highest efficiency
Effort	Low (parameters can be taken from DRM)	High initial effort. Requires testbenches and scripting
Complexity	Low, still a good grounding ☺	High initial effort, but easier than some complex models

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Radiation and MOSFETs

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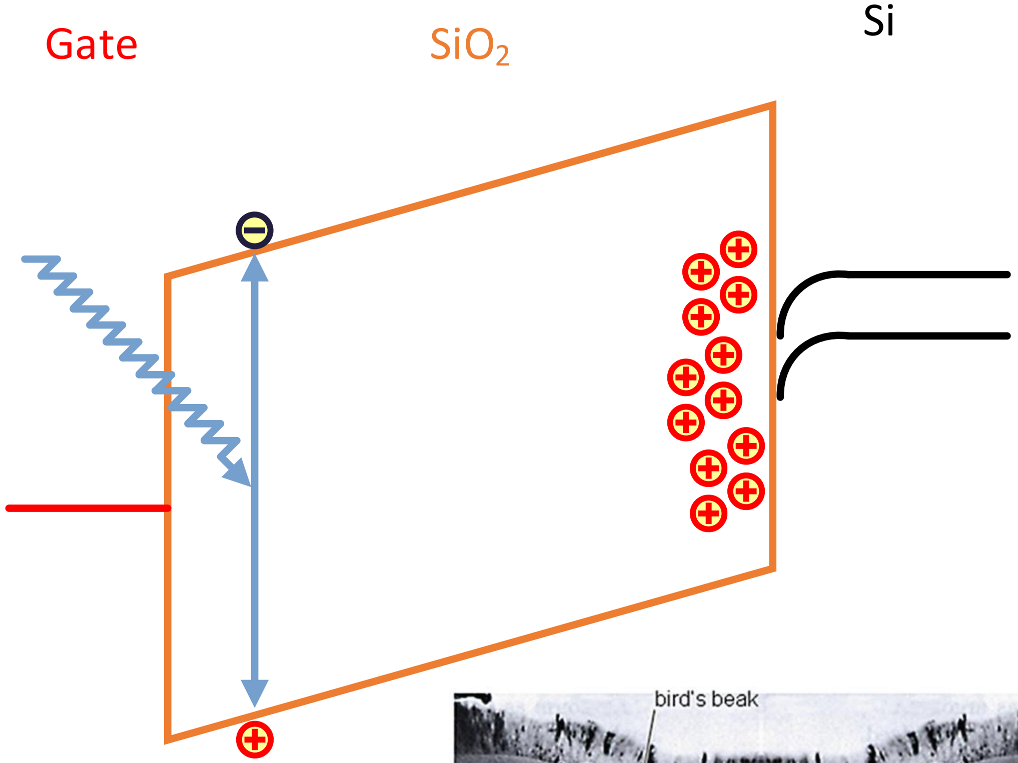
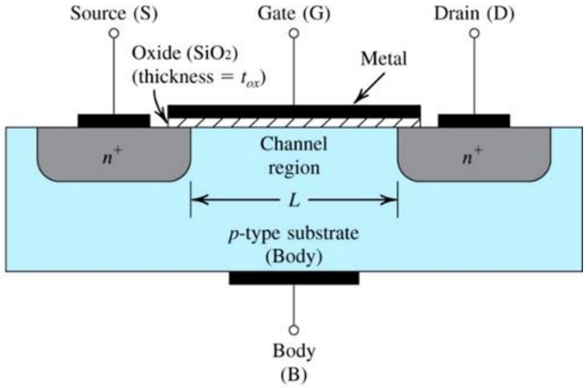
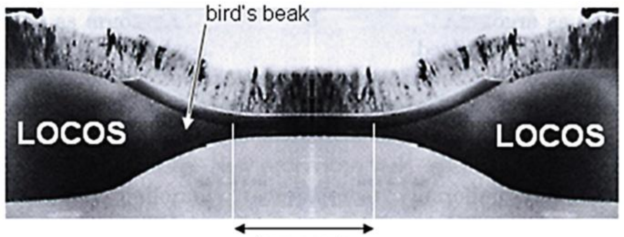
Radiation and MOSFETs

Cause of Degradation

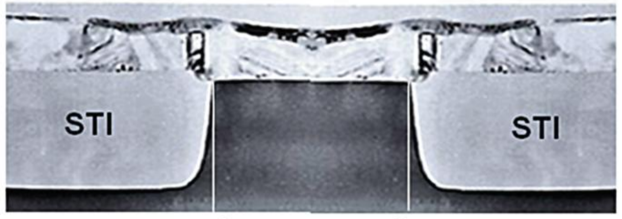
- A topic of interest to instrumentation applications, but fewer commercial/industrial applications is radiation hardness
- Complex topic due to the many structures
- Mostly due to charge generation in the oxide
- Electron mobility is much higher than hole mobility in SiO_2 ($20\ cm^2V^{-1}s^{-1}$ vs $\sim 10^{-4}\ cm^2V^{-1}s^{-1}$ ref)
- Holes therefore get stuck and change the properties of the interface region
- Can also generate further interface traps (not shown)







(a) inaccurate transistor width



(b) accurate transistor width

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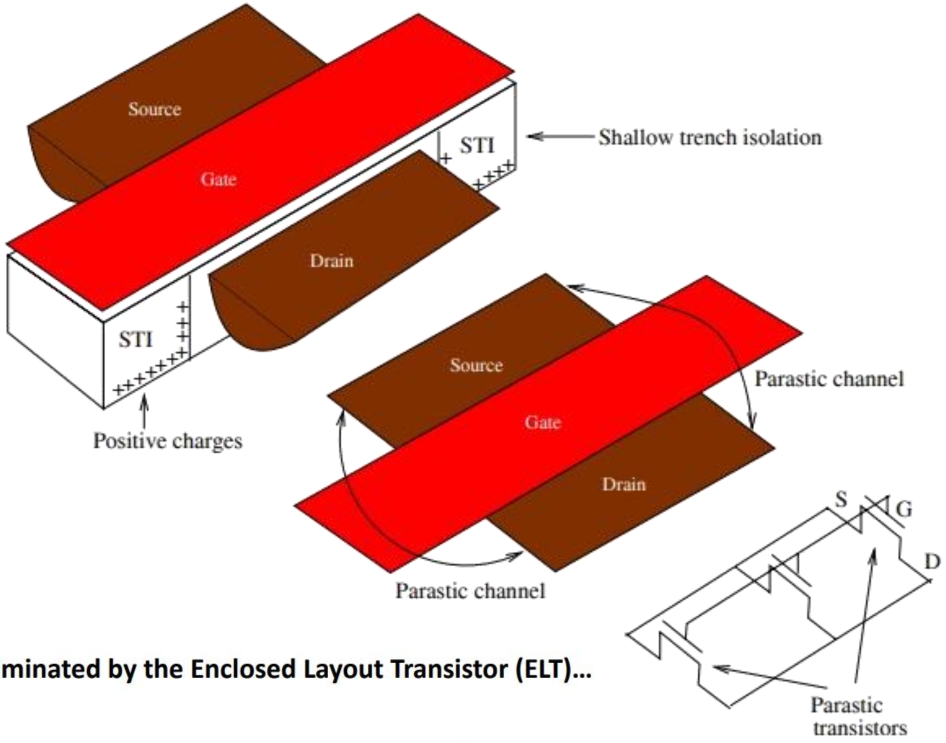
Video

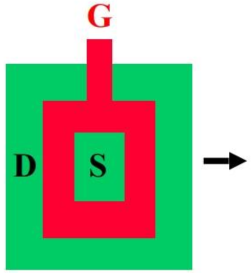
Radiation and MOSFETs

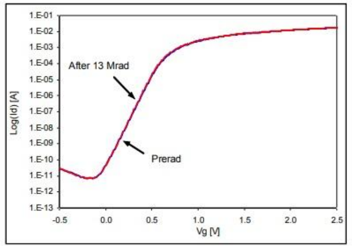
Shallow Trench Isolation Effects

- Positive charge can build-up in the STI
- For PMOS transistors, this makes them harder to turn on, for NMOS, easier
- In the case of NMOS devices, it can even lead to a leakage path around the transistor
- Sometimes called the Radiation Induced Narrow Channel Effect (RINCE)
- This can largely be mitigated by Radiation Hardened By Design (RHBD) techniques
  - Enclosed Layout Transistors – avoid path between source and drain
  - Guard rings – break inter transistor paths

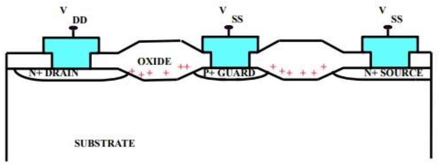


Source-Drain leakage is eliminated by the Enclosed Layout Transistor (ELT)…





Inter-diffusion leakage is eliminated by p+ guard rings…



Radiation Effects in CMOS Technologies for the LHC Upgrades

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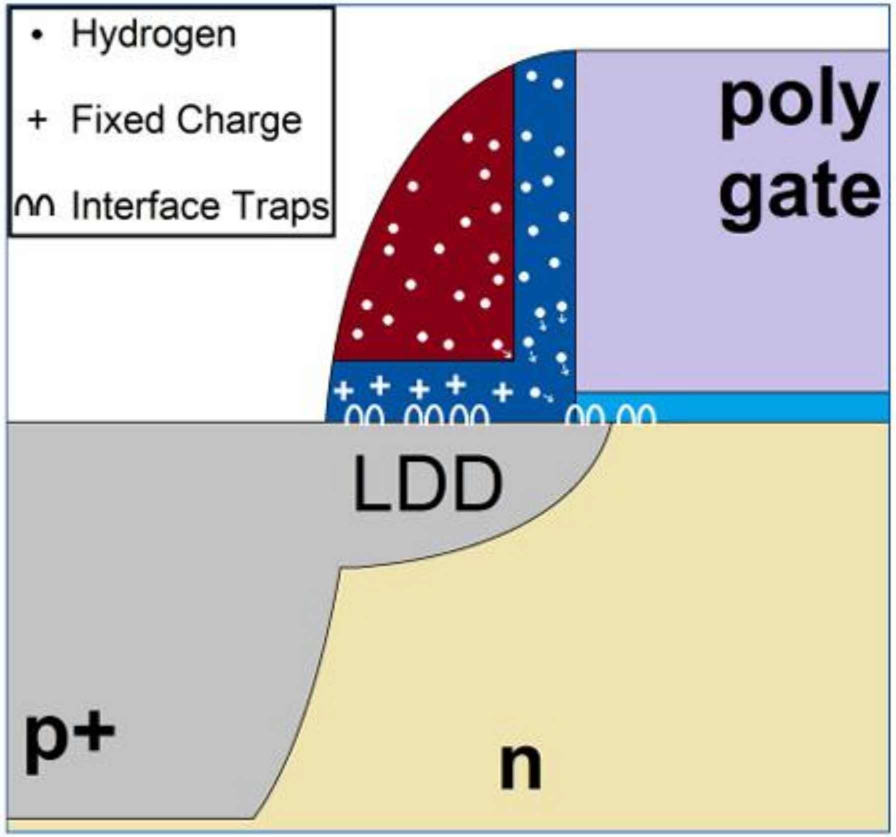
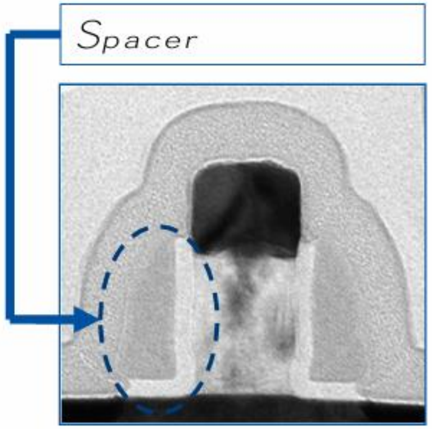
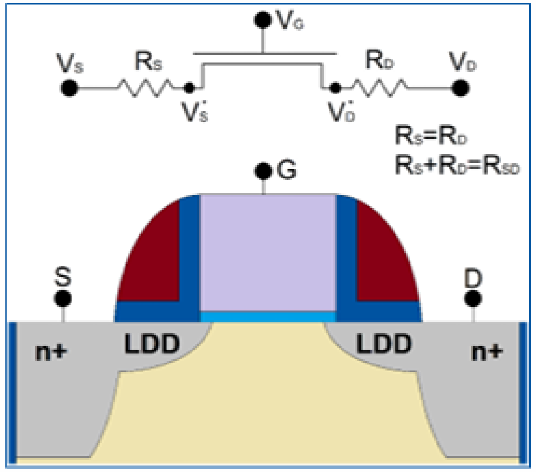
Radiation and MOSFETs

Effects in More Advanced Nodes

- Since oxides get thinner as (planar) technologies shrink, improved rad-hardness might be expected
- In practice, the picture becomes very complex – additional features introduce new vulnerabilities
- 65nm is a good example. Much worse degradation than expected due to additional oxides, effect of spacers
- Little can be done in design. Process, and often individual fab, needs to be characterised
- What about future? 28nm? FinFets?







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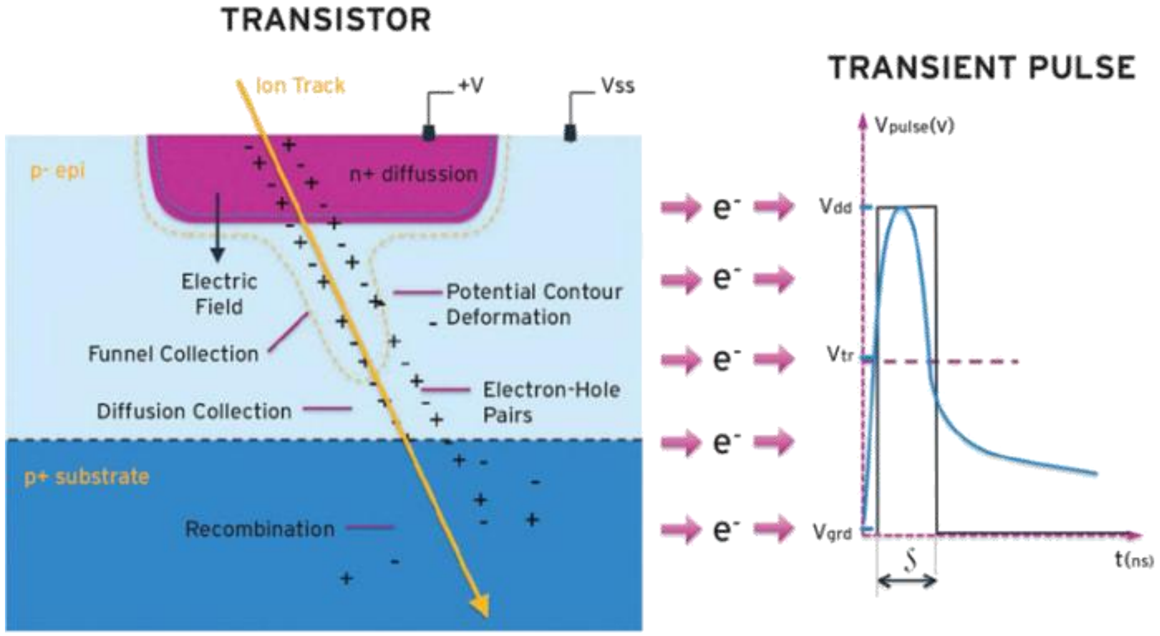
Radiation and MOSFETs

SEE, SET, SEU, Latch-up

- **Single Event Effect**
  - Generation of charge in a semiconductor caused by the interaction of a single ionising particle
- **Single Event Transient**
  - Sub-set of SEE where the effect is short lived
- **Single Event Upset**
  - Sub-set of SEE where the effect results in a permanent effect, like flipping a bit
- **Latch-up**
  - Potentially catastrophic high current condition

SEE, SET



Radiation and MOSFETs

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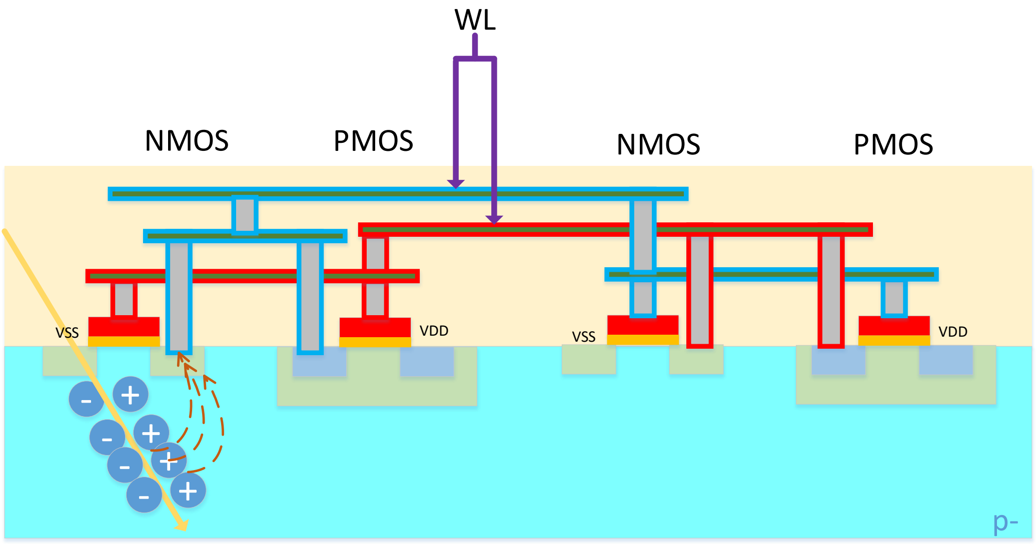

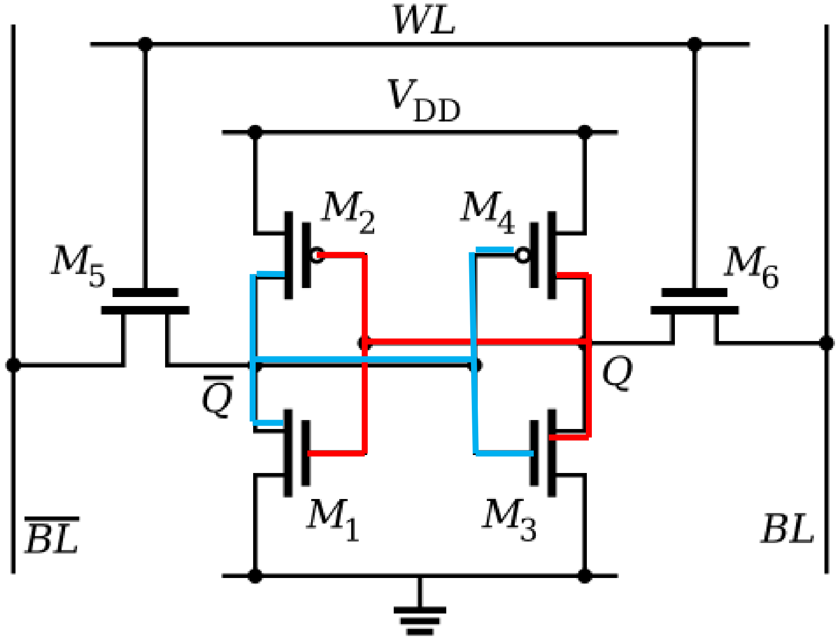

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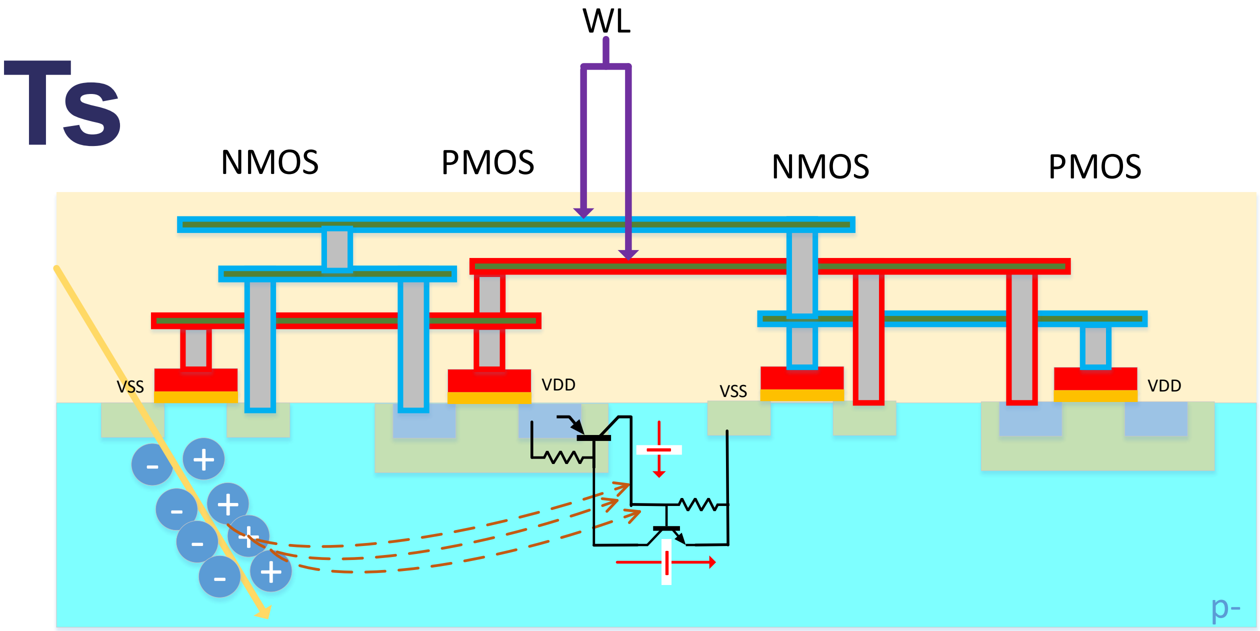
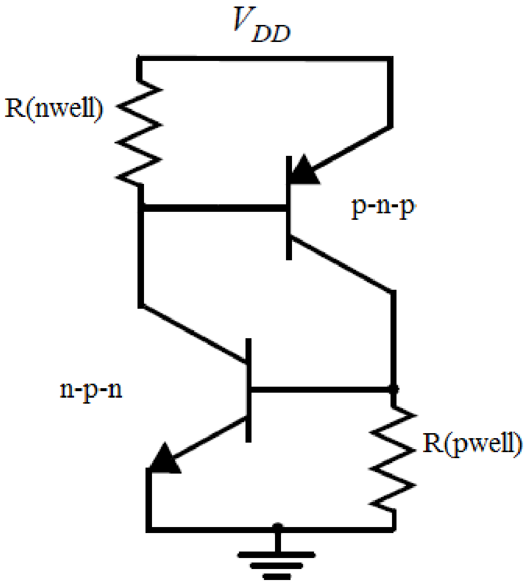
Radiation and MOSFETs

SEE, SET, SEU, Latch-up

- **Single Event Effect**
    - Generation of charge in a semiconductor caused by the interaction of a single ionising particle
- **Single Event Transient**
    - Sub-set of SEE where the effect is short lived
- **Single Event Upset**
    - Sub-set of SEE where the effect results in a permanent effect, like flipping a bit
- **Latch-up**
    - Potentially catastrophic high current condition





https://commons.wikimedia.org/wiki/File:Latchup_ckt.png

Radiation and MOSFETs

Real World and Mitigation

- **Occur in everyday electronics**
  - Aircraft are especially susceptible because cosmics generate the necessary charge
  - But not only!
- **Mitigation**
  - Fairly simple
  - Guard rings and substrate taps
  - Also Silicon-on-Insulator (SOI)

AIRCRAFT

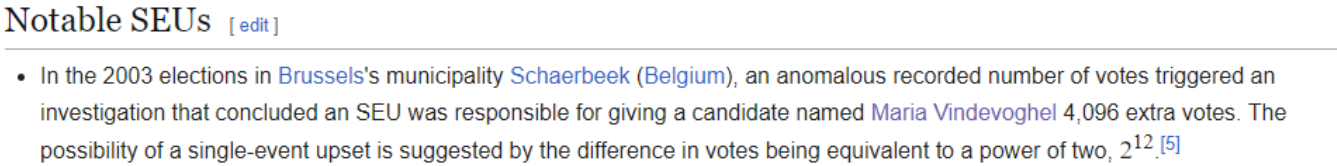
Bit flips: How cosmic rays grounded a fleet of aircraft

(Image credit: Getty Images)

Credits: STCE and FMI

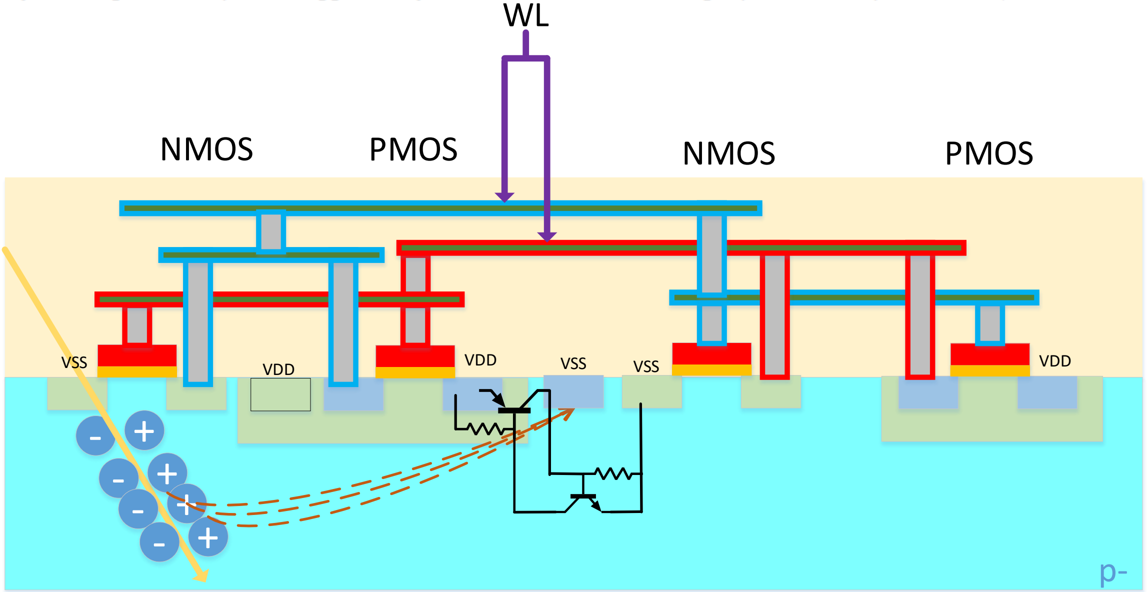
https://www.bbc.co.uk/future/article/20251201-how-cosmic-rays-grounded-thousands-of-aircraft

https://www.stce.be/news/797/welcome.html

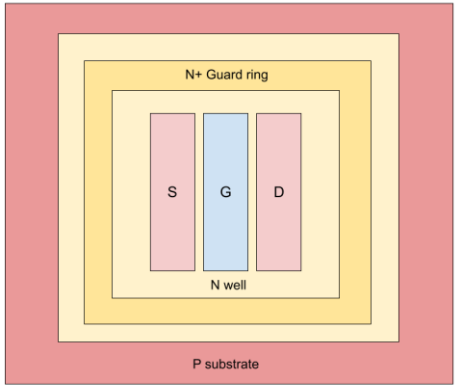


Notable SEUs [edit]

- In the 2003 elections in Brussels's municipality Schaerbeek (Belgium), an anomalous recorded number of votes triggered an investigation that concluded an SEU was responsible for giving a candidate named Maria Vindevoghel 4,096 extra votes. The possibility of a single-event upset is suggested by the difference in votes being equivalent to a power of two, 2^{12}.[5]



https://community.cadence.com/cadence_blogs_8/b/cic/posts/analog-layout-wells-taps-and-guard-rings



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Video

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The Future: Challenges and Opportunities

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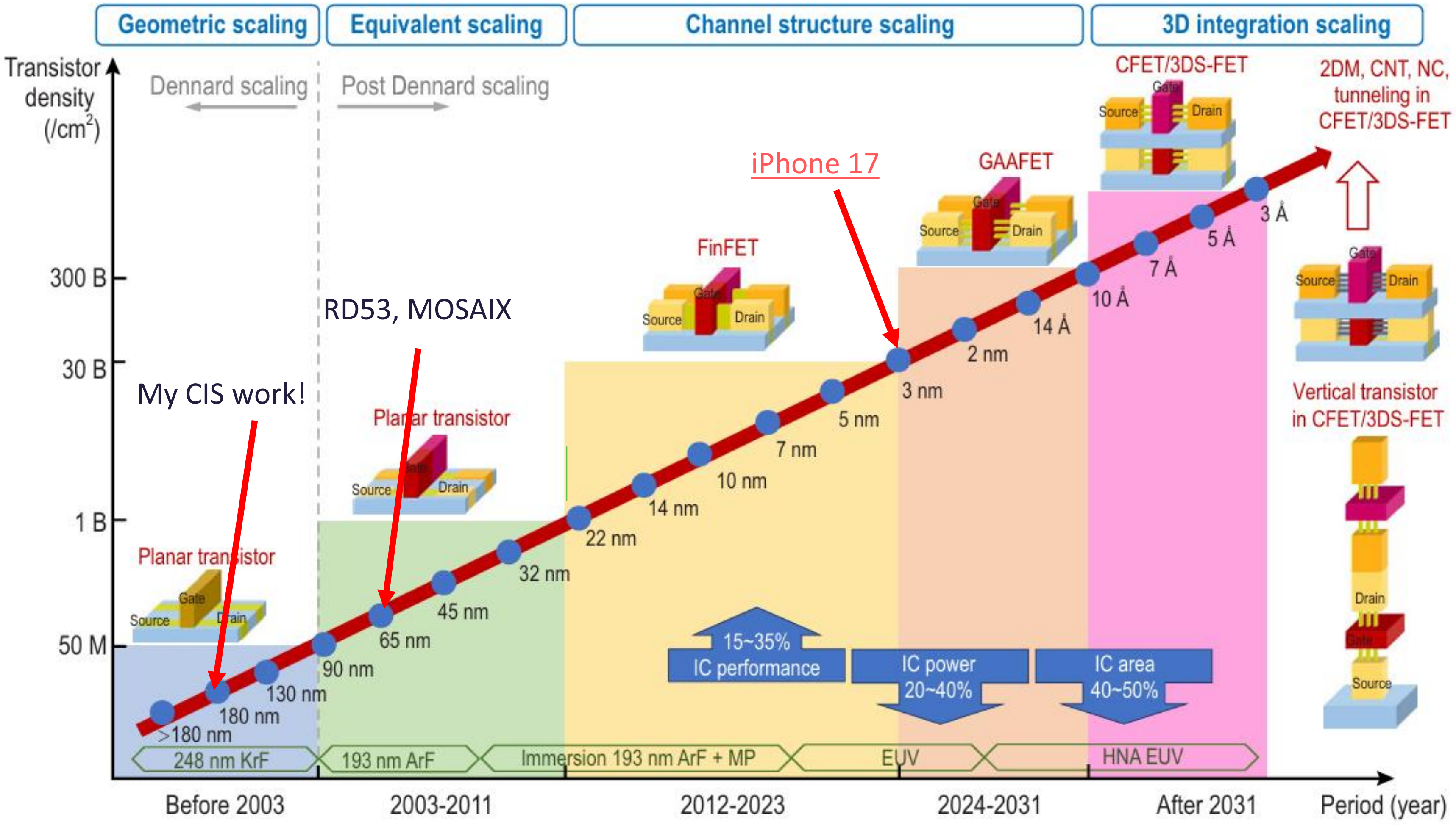
The Future



iPhone 17

RD53, MOSAIX

My CIS work!

https://doi.org/10.1093/nsr/nwae008

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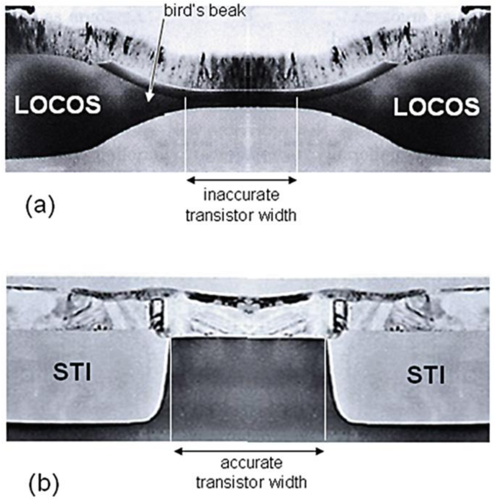
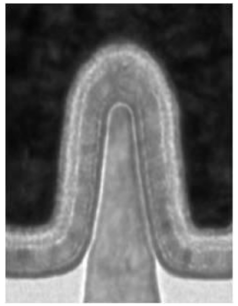
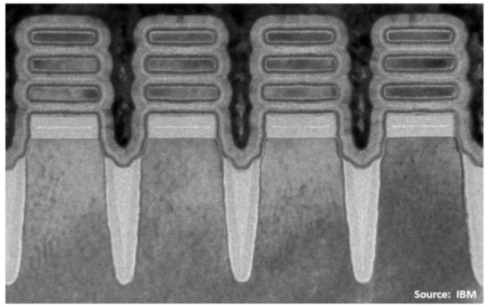


Planar



FinFET

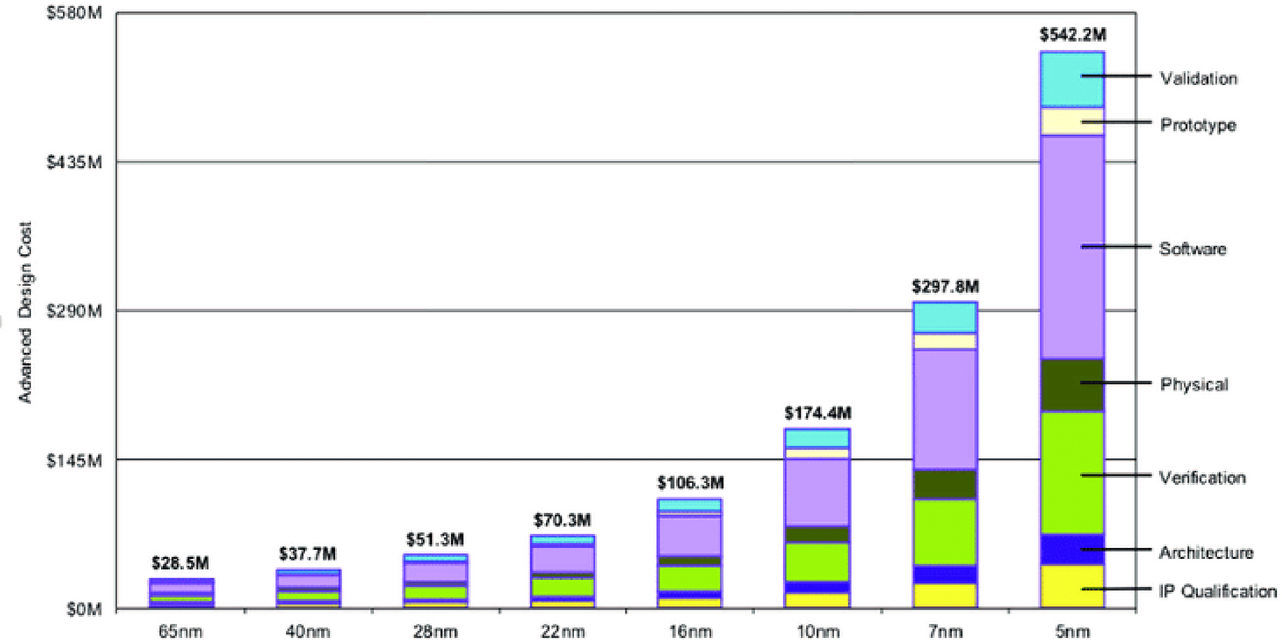


GAA

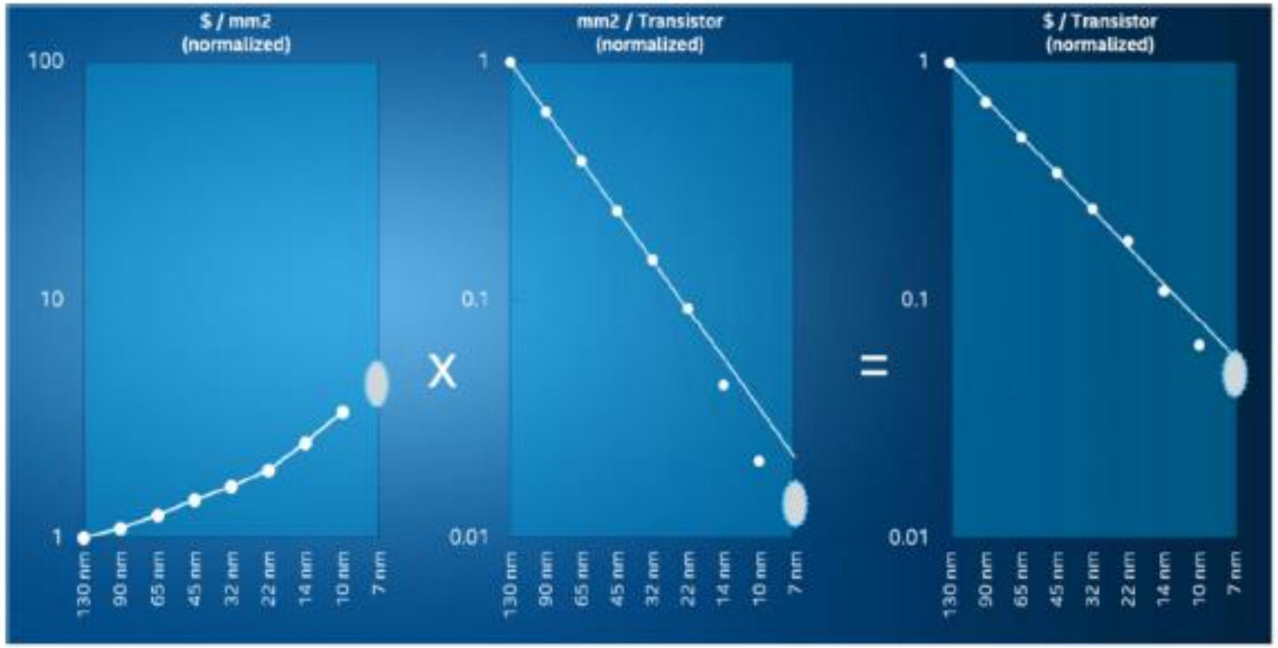
The Future

Challenge: Cost

- Silicon costs increase exponentially with node:
    - Masks, Wafers
    - Design Tools
    - Verification
- Industry is focussed on reduction in cost/transistor. Does that help instrumentation (especially MAPS)?



https://semiengineering.com/what-will-that-chip-cost/



https://www.nber.org/system/files/working_papers/w24553/w24553.pdf

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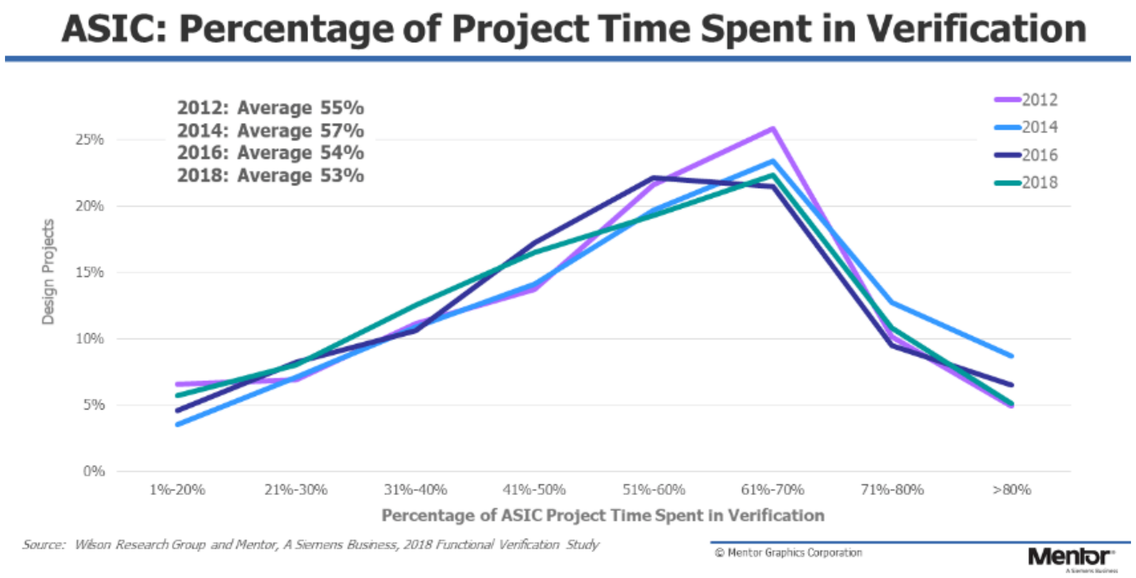
The Future

Challenge: Access and Resources

- Commercial fabs are not focussed on low volume scientific projects…
- IP is strictly protected
- Legal and commercial hurdles are high
- Increasingly a point of global competition – paperwork for customs, end users etc is a significant burden
- Size of available design teams
- Verification requirements

Aspect	CERN HL-LHC ASICs	Big Semi (Qualcomm, Broadcom,…)
Engineers per ASIC	~2–10	50–1000
Total ASIC designers	~150–200	2000–10,000+
Timescale	5–10 years	1.5–2 years
Unique ASIC / cycle	***~50–60 across 4 experiments***	***50+ across product families***

https://indico.cern.ch/event/1502285/contributions/6606418/


ASIC: Percentage of Project Time Spent in Verification

Source: Wilson Research Group and Mentor, A Siemens Business, 2018 Functional Verification Study

© Mentor Graphics Corporation

https://semiengineering.com/the-weather-report-2018-study-on-ic-asic-verification-trends/

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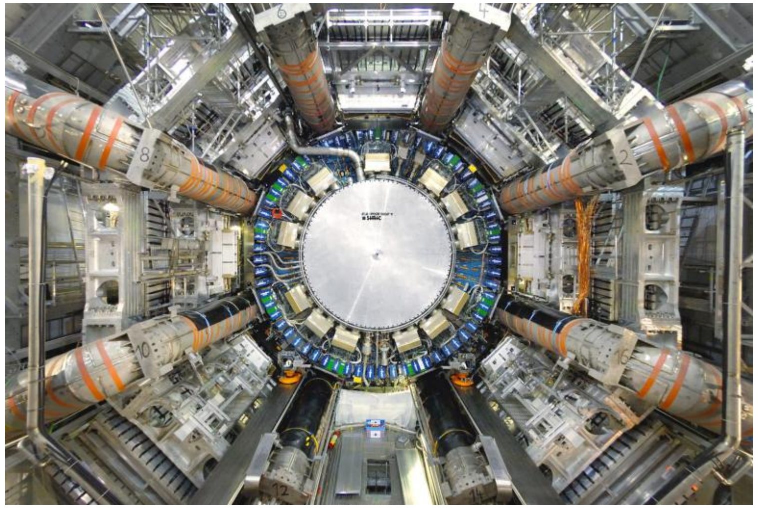
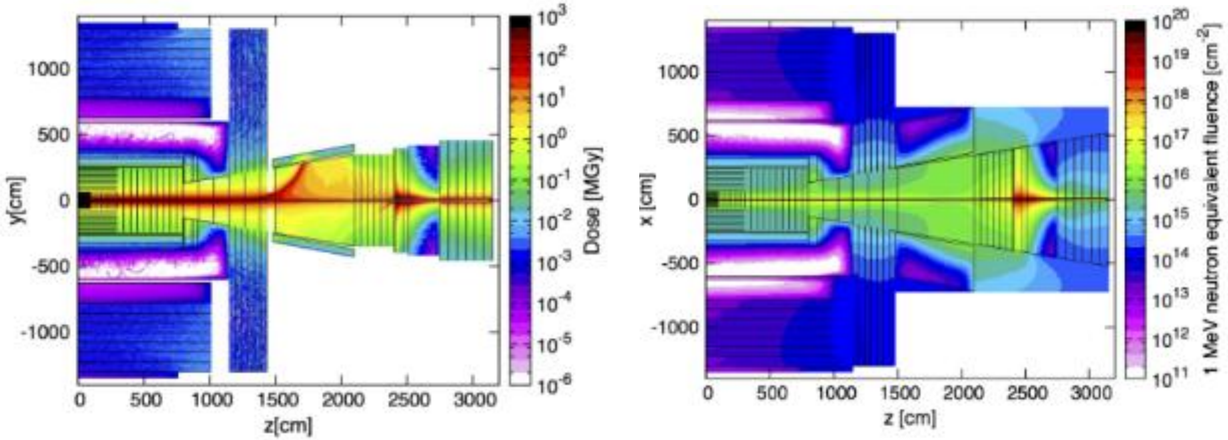
The Future

Challenge: Specifications

- Science does not stand still
- Requirements for detectors increase regardless of the cost and access challenges



Currently, there are no technological solutions which can sustain such values, representing a clear challenge.



M. Besana et al, "Evaluation of the radiation field in the future circular collider detector", PHYSICAL REVIEW ACCELERATORS AND BEAMS19,111004 (2016)

105 Gbits/s!

Specification	Target	
Sensor format	2048 x 2048	
Pixel pitch	50 x 50 µm	
Frame rate	2000 fps	2500 fps
Bit depth	12 bits	10 bits
Operation mode	Rolling shutter	
Readout mode	Continuous	
Readout type	Analogue CML lines	
Sensor size	200 mm wafer-scale sensor	
Manufacturing process	TowerJazz 180 nm CIS process	
Sensitive area	104 cm^2	
Radiation hardness	YES	
Back-thining	NO	
Dark pixels	Only on left and right sides of the pixel array	

From D. Krukauskas, "C100 – CMOS Sensor for 100 keV EM" Rosalind Franklin Institute annual meeting 2019

The Future

Opportunities: Access and Costs

- Europractice
    - Design Tools
    - Fabrication Services

- CERN Foundry Services

- Open Source Design Tools
    - Introduction
    - Docker container
    - Now 3 PDKs, several submission options

- Collaborative working
    - DRD3
    - DRD7

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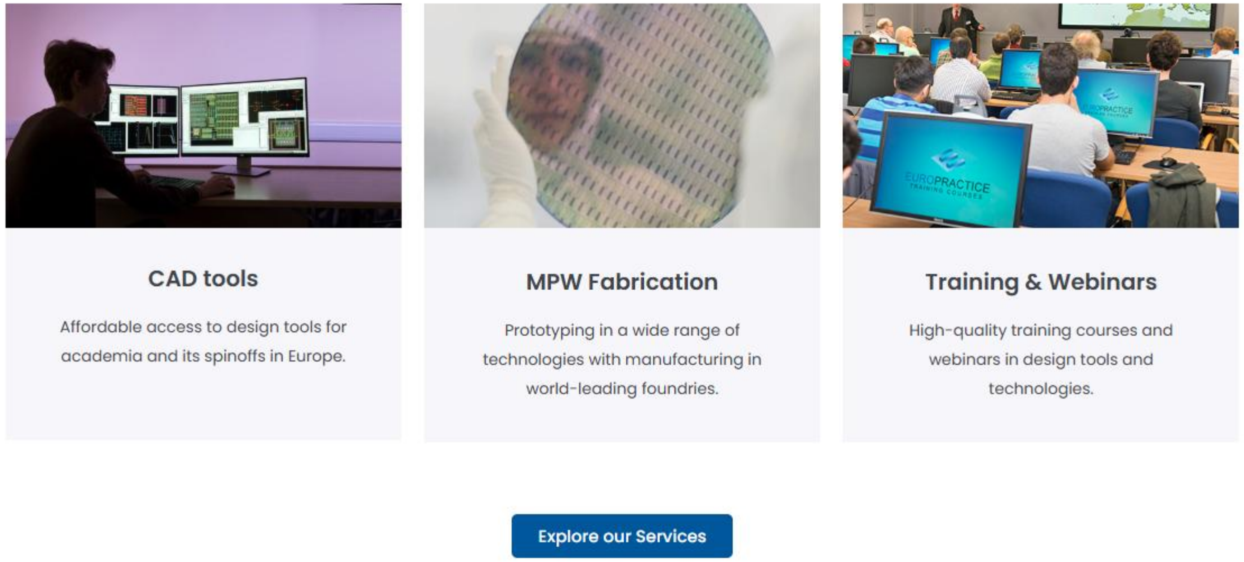


CAD tools

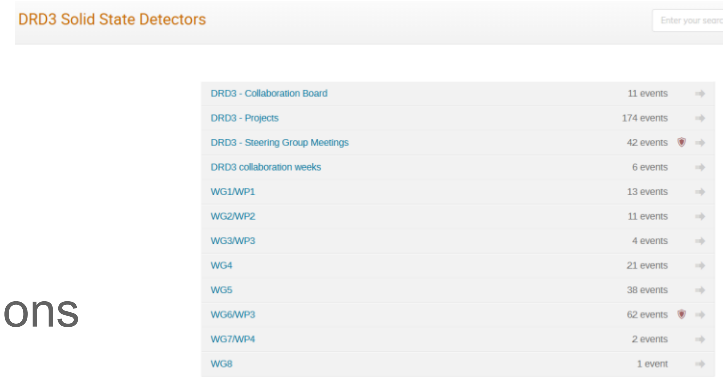
Affordable access to design tools for academia and its spinoffs in Europe.

MPW Fabrication

Prototyping in a wide range of technologies with manufacturing in world-leading foundries.

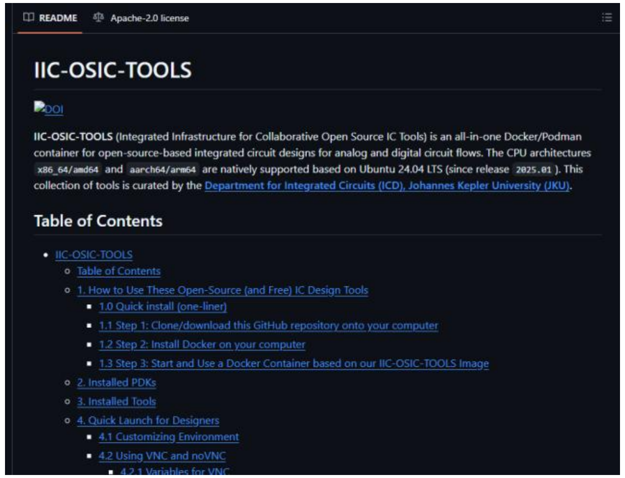
Training & Webinars

High-quality training courses and webinars in design tools and technologies.



DRD3 Solid State Detectors

DRD3 - Collaboration Board	11 events
DRD3 - Projects	174 events
DRD3 - Steering Group Meetings	42 events
DRD3 collaboration weeks	6 events
WG1/WP1	13 events
WG2/WP2	11 events
WG3/WP3	4 events
WG4	21 events
WG5	38 events
WG6/WP3	62 events
WG7/WP4	2 events
WG8	1 event



IIC-OSIC-TOOLS

DOI

IIC-OSIC-TOOLS (Integrated Infrastructure for Collaborative Open Source IC Tools) is an all-in-one Docker/Podman container for open-source-based integrated circuit designs for analog and digital circuit flows. The CPU architectures `x86_64/amd64` and `aarch64/arm64` are natively supported based on Ubuntu 24.04 LTS (since release `2025.01`). This collection of tools is curated by the Department for Integrated Circuits (ICD), Johannes Kepler University (JKU).

Table of Contents

- IIC-OSIC-TOOLS
    - Table of Contents
    - 1. How to Use These Open-Source (and Free) IC Design Tools
        - 1.0 Quick install (one-liner)
        - 1.1 Step 1: Clone/download this GitHub repository onto your computer
        - 1.2 Step 2: Install Docker on your computer
        - 1.3 Step 3: Start and Use a Docker Container based on our IIC-OSIC-TOOLS Image
    - 2. Installed PDKs
    - 3. Installed Tools
    - 4. Quick Launch for Designers
        - 4.1 Customizing Environment
        - 4.2 Using VNC and noVNC
            - 4.2.1 Variables for VNC

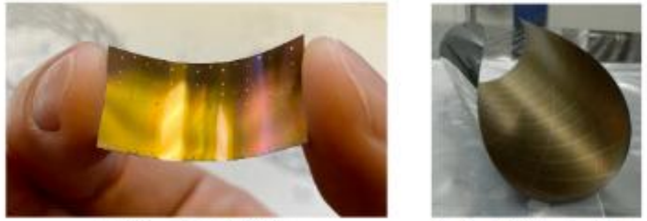
DRD7 Collaboration

Electronics & On-Detector Processing

The Future

Opportunities: Process Improvements

- Vertical Integration (2.5, 3D)
- Thinned Devices
- Depleted Silicon
- Lower process nodes
- New tools
- Stitching

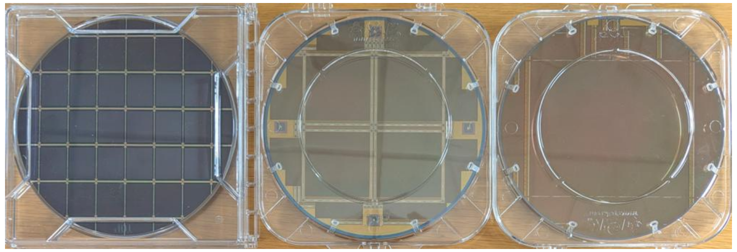


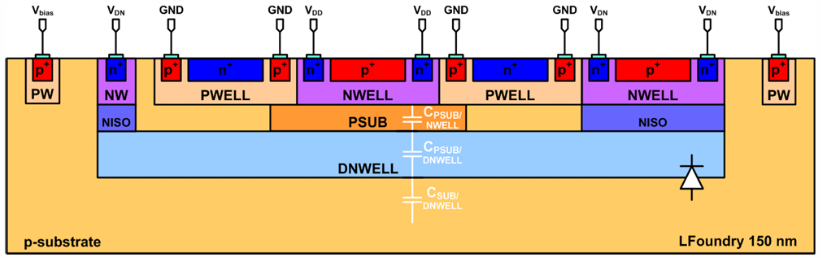
(a) A 50 μm-thick ALPIDE chip

(b) An ALPIDE wafer that detached during the thinning process.

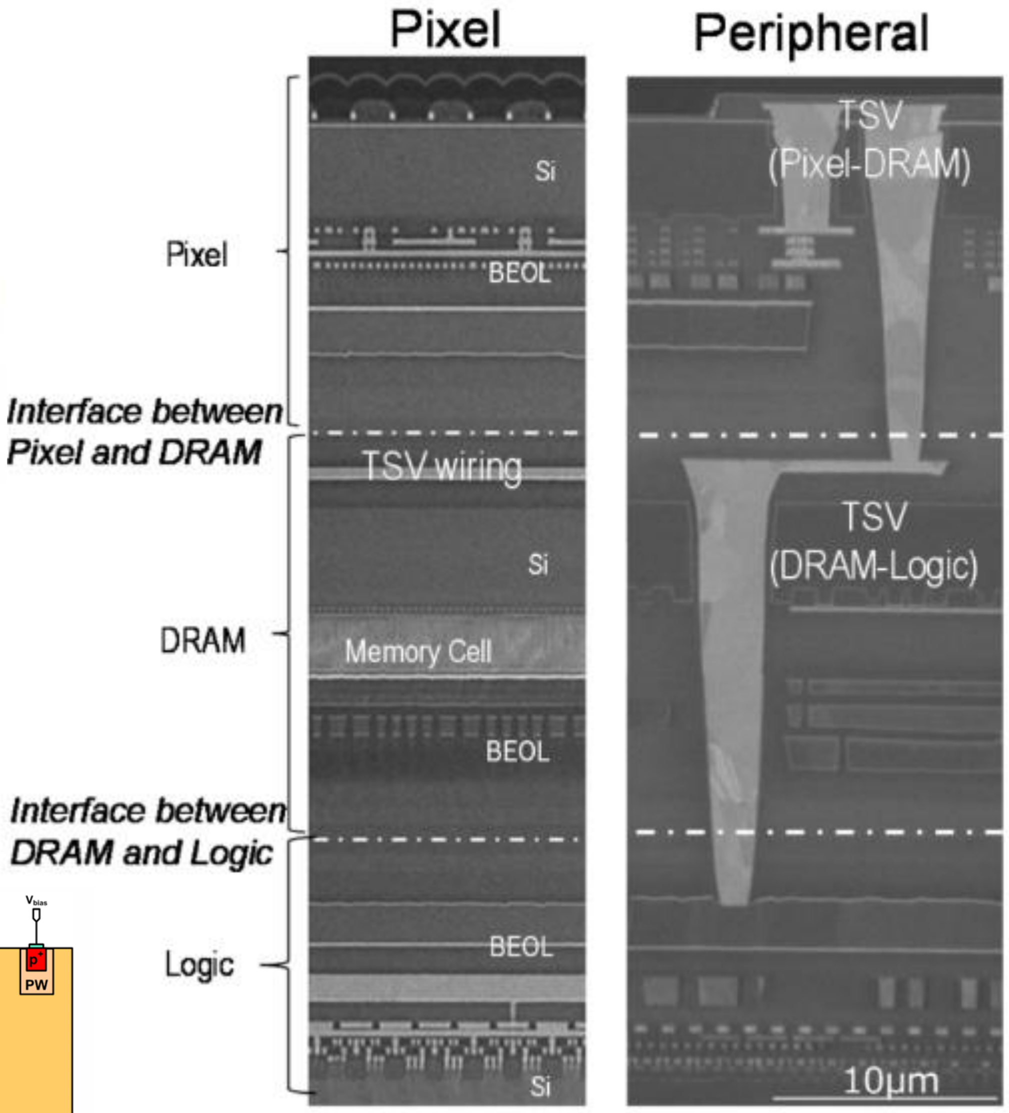
Figure 5: Bent silicon from the ALPIDE production of ITS2.

https://pos.sissa.it/373/040/pdf, M. Mager





https://fuse.wikichip.org/news/763/iedm-2017-sonys-3-layer-stacked-cmos-image-sensor-technology/



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Summary

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Summary

Summary

- CMOS technology has huge application instrumentation
- Currently working at nodes well within state-of-the art
- So plenty of technological scope to meet the challenges of new detectors
- Access and cost have always been issues, but many projects exist to address this
- Lots of interesting work still to do!

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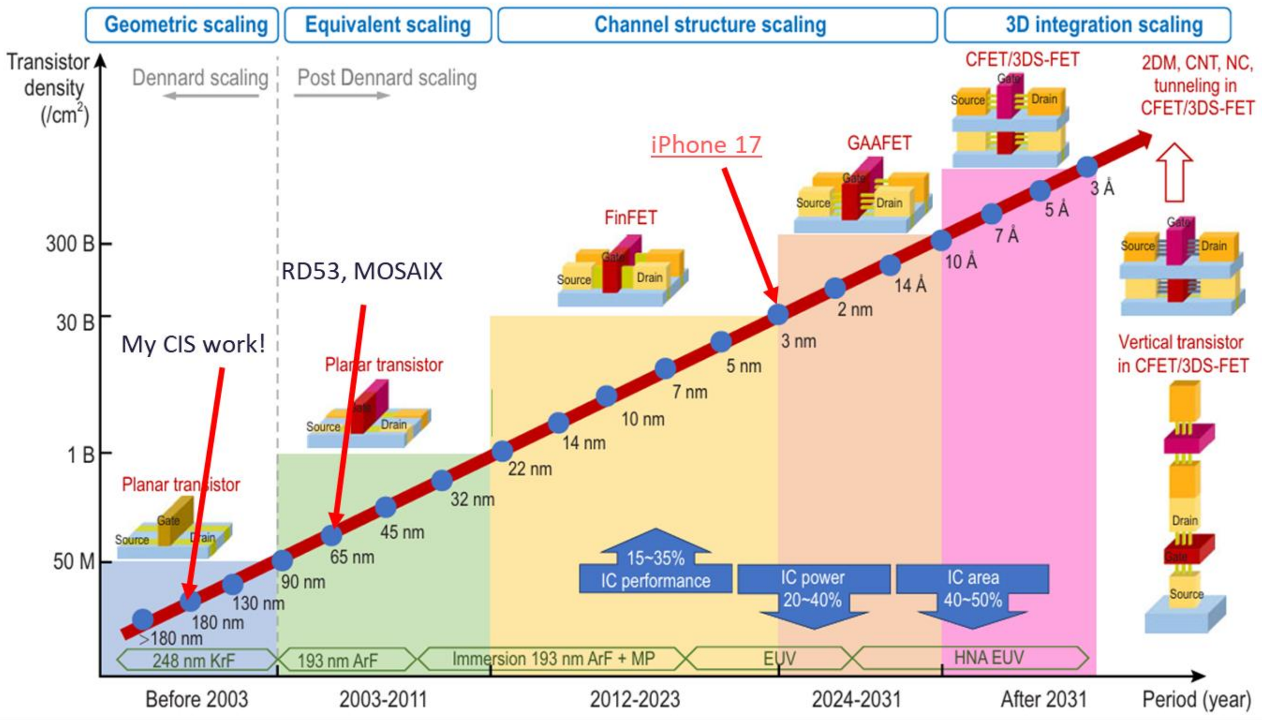
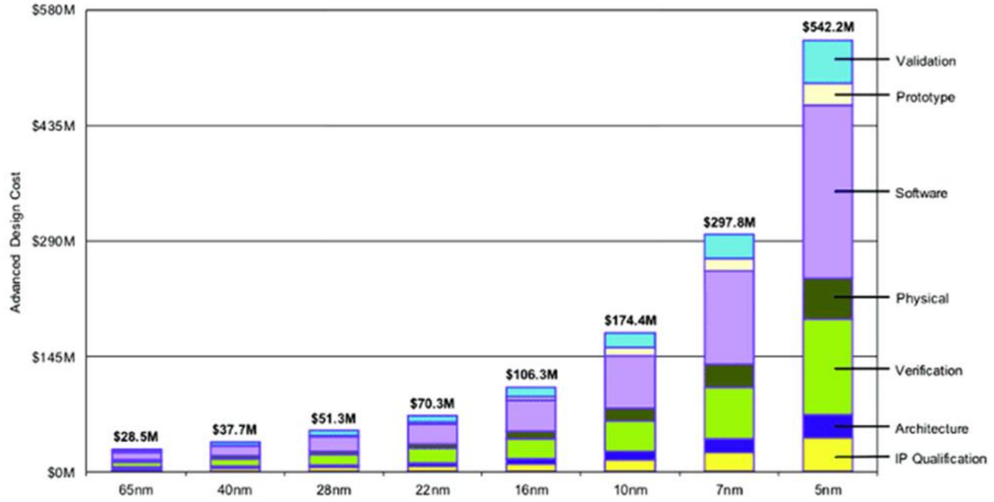


https://doi.org/10.1093/nsr/nwae008



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Questions?

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Thank you