

Circuits and layouts II

E. Giulio Villani

Overview

- **Introduction, definitions**
- **Hybrid and Monolithic Sensors**
- **Common isolation techniques**
- **Example of ATLAS ItK Strips HV biasing**

Introduction

- IC (integrated circuit) single silicon chip that includes active and passive interconnected devices to implement complex operations (analogue, digital)
- Planar technology: the processing steps are implemented in a thin layer of the surface of the chip

April 25, 1961 R. N. NOYCE 2,981,877
SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE
Filed July 30, 1959 3 Sheets-Sheet 2

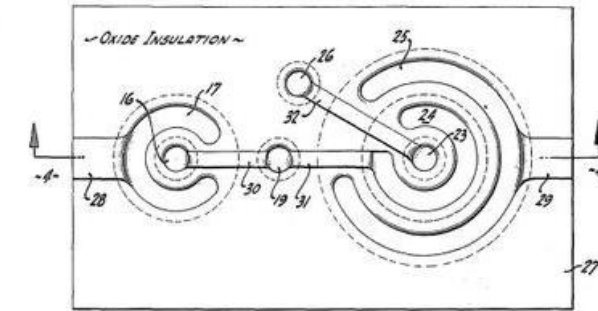


FIG-3

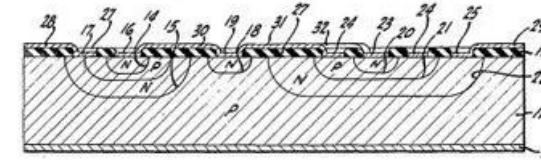


FIG-4

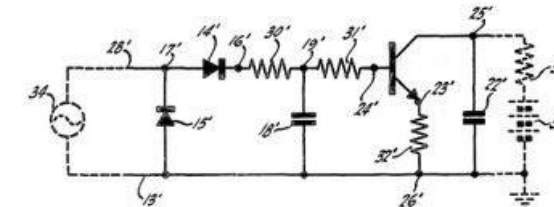


FIG-5

INVENTOR,
ROBERT N. NOYCE
BY *Leppinatt & Kalls*
ATTORNEYS

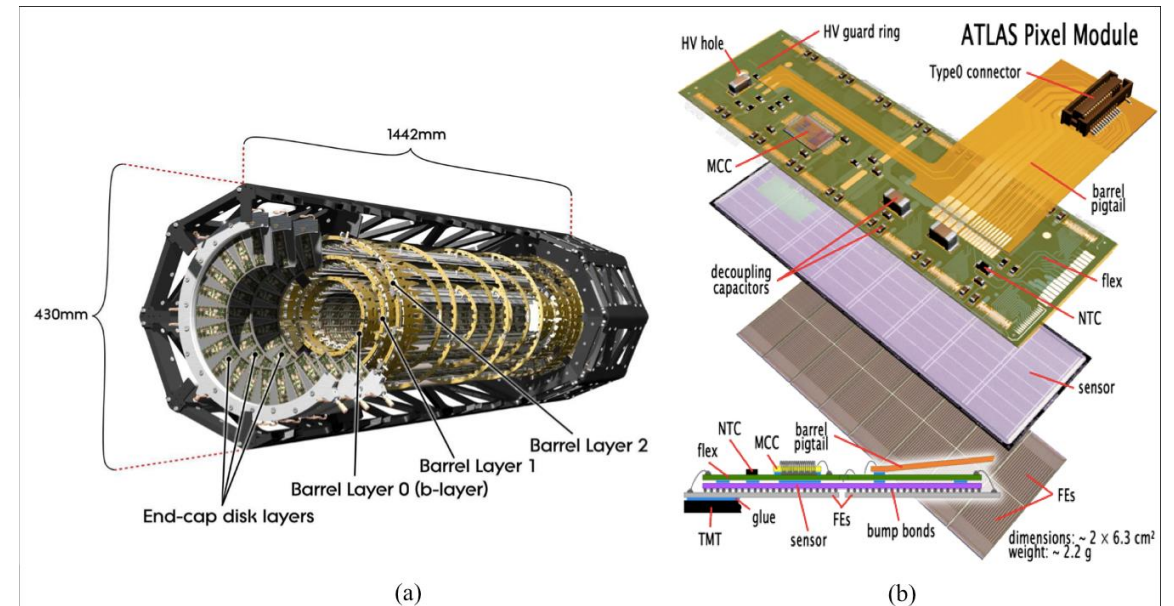
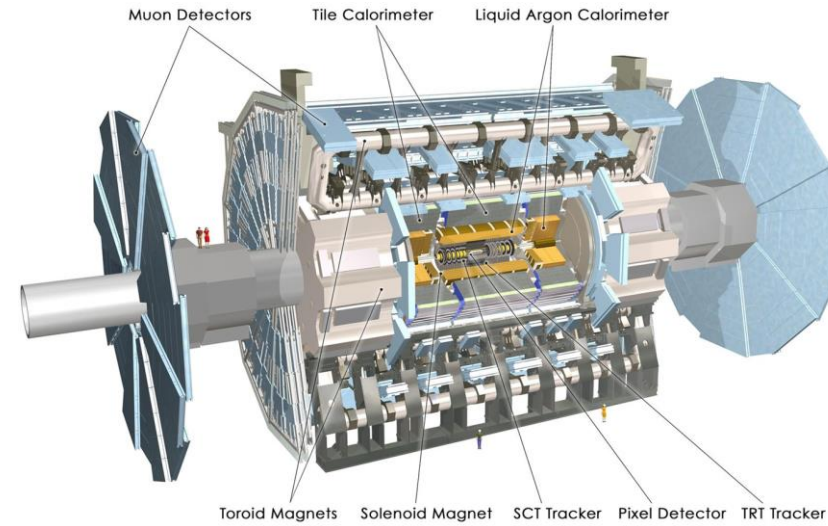
Semiconductor device-and-lead structure

US2981877A

First planar IC patent, 1961

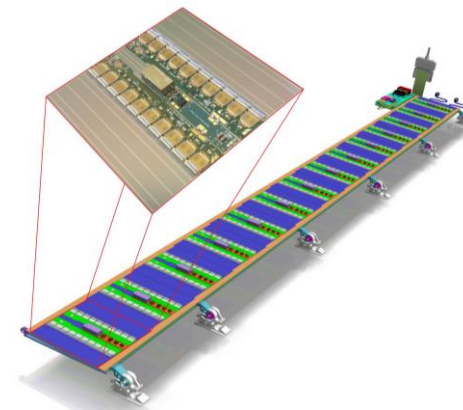
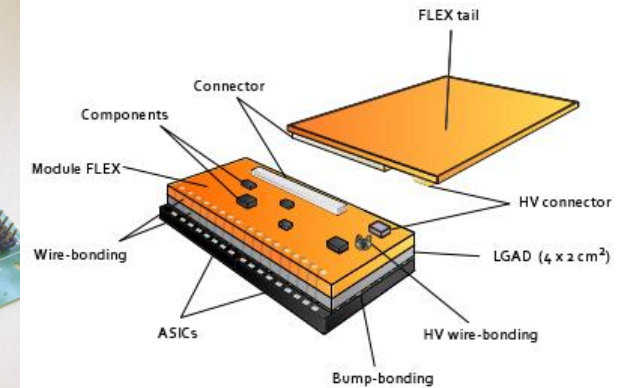
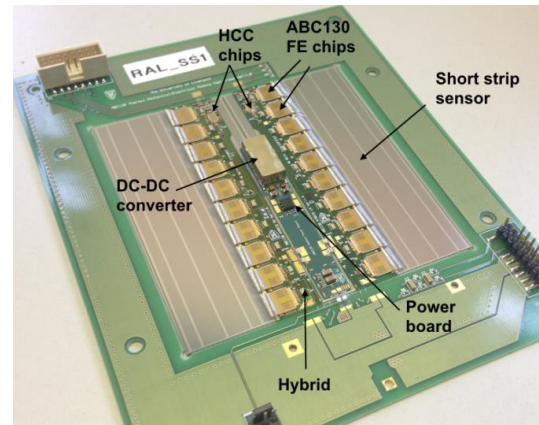
Introduction

- Planar technology used also for HEP detector technology
- Remarkable evolution in planar technologies impacted on detector technology as well
- HEP traditionally used the ‘**hybrid**’ approach

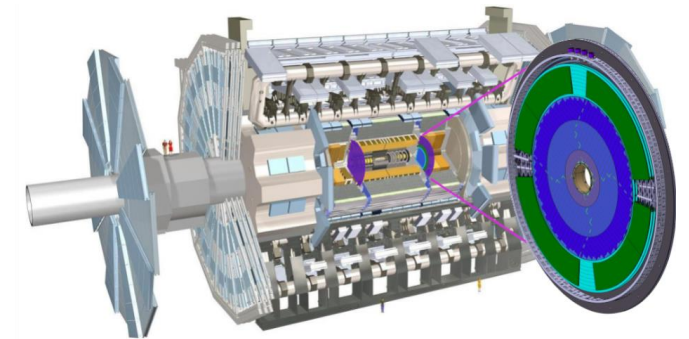


Hybrid solution

- **Hybrid:** different operations are implemented on different silicon chips (like sensing and read out on separate carriers)
 - High quality substrate for the **sensor** to optimize the charge collection efficiency and speed
 - It requires interconnect to the readout, i.e. complex bonding, affecting reliability, costs
 - Extra material due to the various layers



*ATLAS Inner Tracker Upgrade (ITk)
silicon strip module on barrel stave*



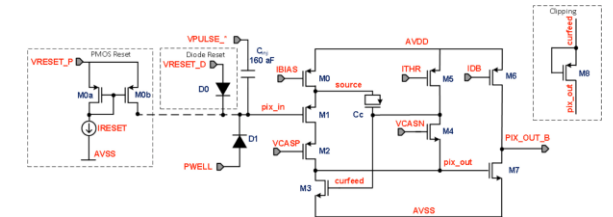
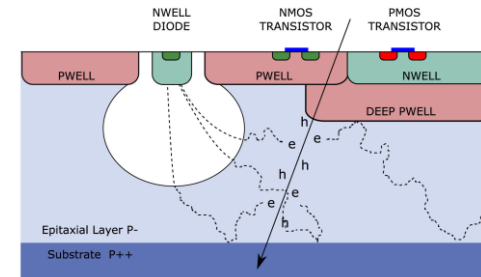
*Hybrid module for the High
Granularity Timing Detector (HGTD)
for the upgraded ATLAS detector*

Monolithic solution

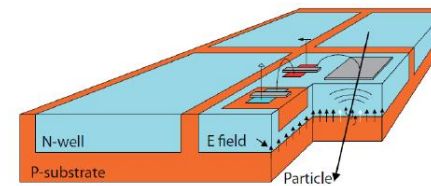
- **Monolithic:** sensor and readout are implemented on the same silicon chip
 - Reliability, no need for wire/bump bonding
 - Reduced mass
 - In-pixel processing possible: amplification and digitization integrated in the same chip
 - Small pixels (10's x 10's um)
 - Low noise, due to small pixel, low leakage, low capacitance, good S/N



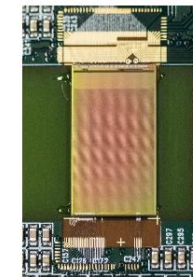
The vertex detector of the STAR experiment, the first to use CMOS MAPS



MAPS used for ALICE ITS upgrade, with in-pixel FE circuitry

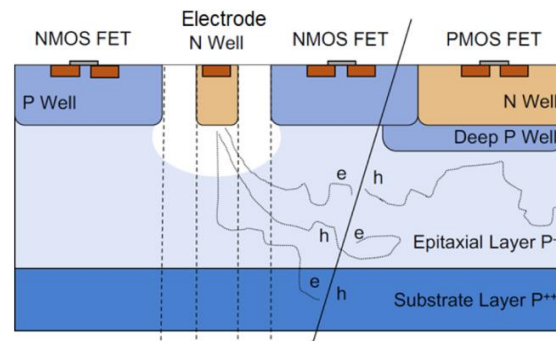


HV MAPS used for Mu3e

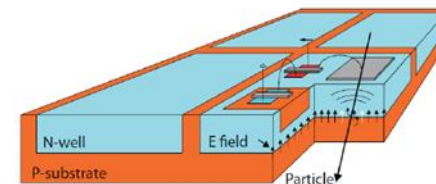


Monolithic solution

- **Monolithic:** sensing and read out are implemented on the same silicon chip
 - It mostly uses commercial CMOS process
 - Redundancies of foundries
 - Potentially low cost, large area cover possible
 - High yield



Deep P Well



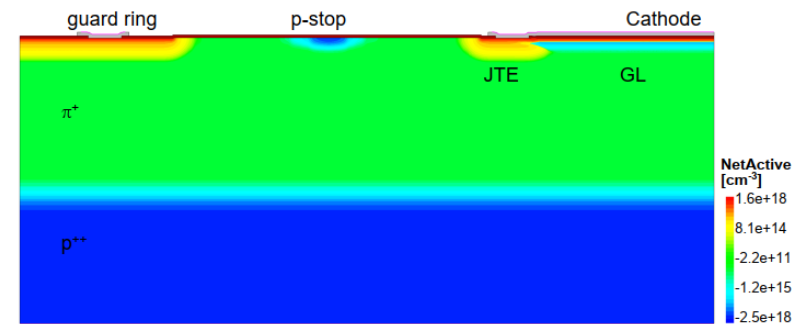
Deep N Well

Monolithic approach is an interesting option for most HEP experiments

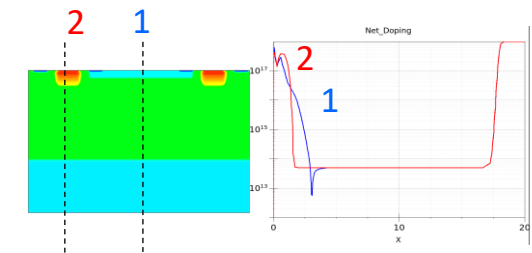
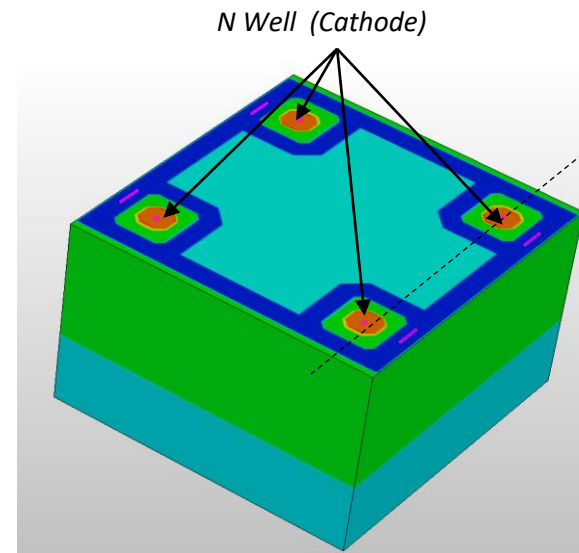
| LHC Tracker Upgrades | Area |
|----------------------|---------------------|
| ALICE ITS | 12 m ² |
| ATLAS Pixel | 8.2 m ² |
| ATLAS Strips | 193 m ² |
| CMS Pixel | 4.6 m ² |
| CMS Strips | 218 m ² |
| LHCb VELO | 0.15 m ² |
| LHCb UT | 5 m ² |
| HGTD | 6.4 m ² |

Layout of Hybrid and Monolithic

- **Hybrid and Monolithic** approach: the sensors share similar 'layouts issues', addressed by various isolation techniques:
 - Channel stops, guard rings, to suppress surface currents and improve breakdown
 - Usually high voltage (100's V) are needed for biasing of sensors in hybrid approach, less for monolithic sensors: HV biasing technique present additional challenges



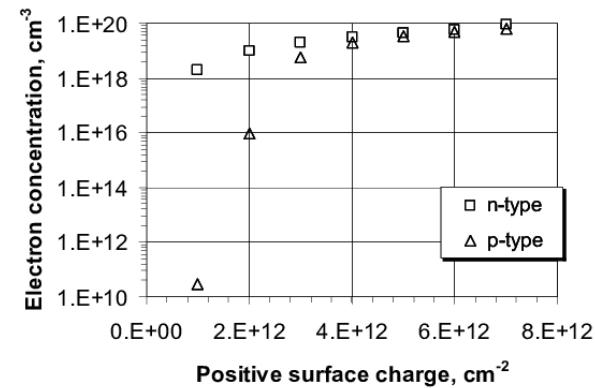
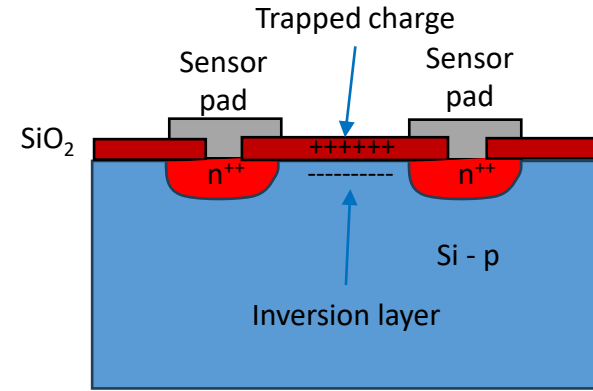
An example of Low Gain Avalanche Detector (LGAD) x-section, with **p-stop** for isolation and Junction Termination Extension (JTE) to increase the breakdown



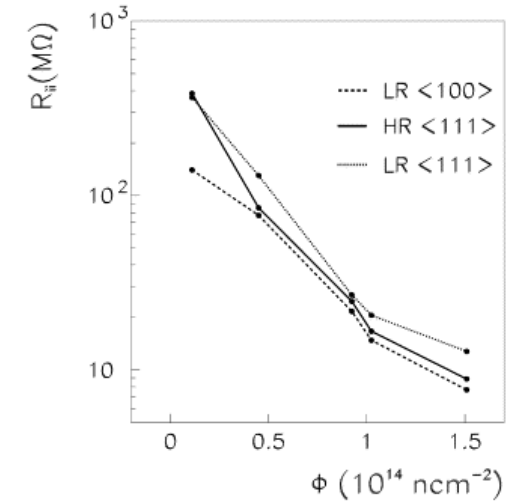
An example of a CMOS sensor on High Resistivity epitaxial x-section, with only p-stop for inter pad isolation

Isolation techniques

- In non-irradiated sensors (depending on the process) the dangling bonds at SiO₂-Si interface usually result in a fixed positive charge around 1e10 (Si <100>) - 1e11 (Si <111>) cm⁻²
- This positive charge creates an accumulation layer of electrons in the substrate between two adjacent pads, decreasing the **interstrip resistance**
- Values up to > 1e12 cm⁻² following ionizing irradiation further decrease the interstrip resistance



Carrier concentration vs. Oxide surface charge

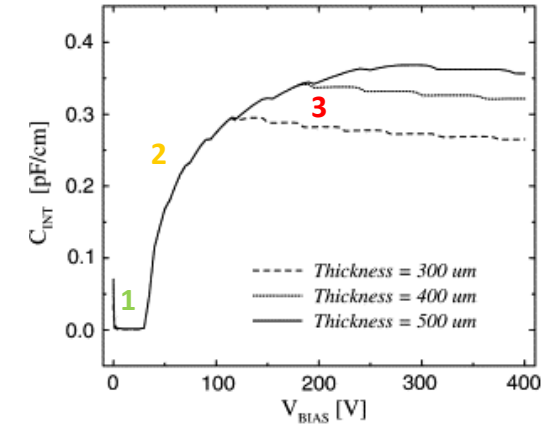
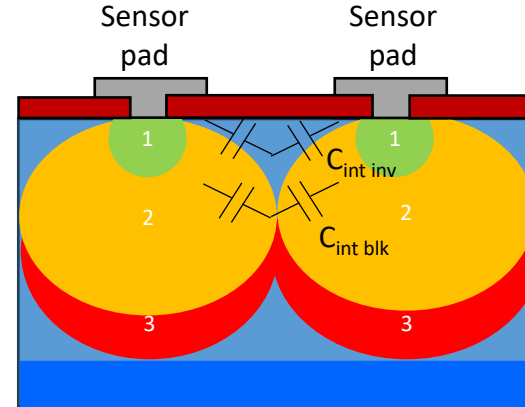


Interstrip resistance vs non-ionising fluence*

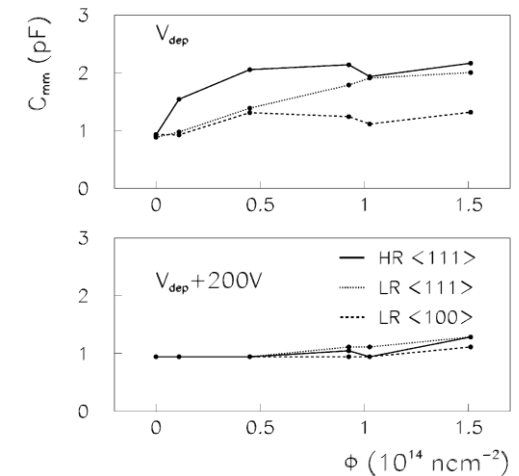
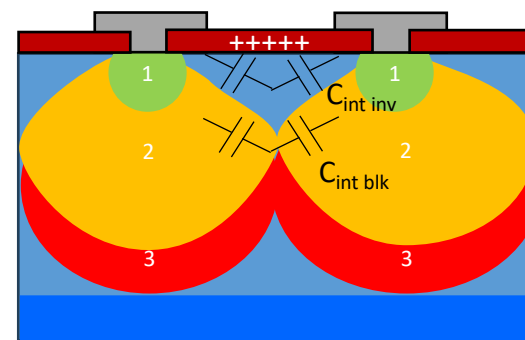
*G. Calefato, et al, s., Comparison on radiation tolerance of <100> and <111> silicon substrates of microstrip detector, [https://doi.org/10.1016/S0168-9002\(01\)01667-9](https://doi.org/10.1016/S0168-9002(01)01667-9).

Isolation techniques

- The inversion layer also affect the **interstrip capacitance**, which affects the noise performances
- An increased in Total Ionising Dose (TID) increases the positive charge at Si-SiO₂ interface
- This might reduce the depletion of the inversion layer and increase the interstrip capacitance



D Passeri, et al. Parasitic capacitances in thick-substrate silicon microstrip detectors, [https://doi.org/10.1016/S0168-9002\(01\)01669-2](https://doi.org/10.1016/S0168-9002(01)01669-2).

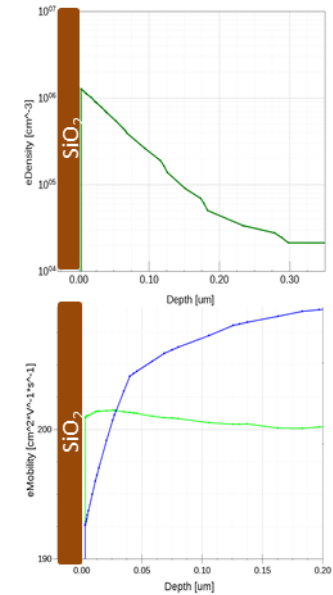
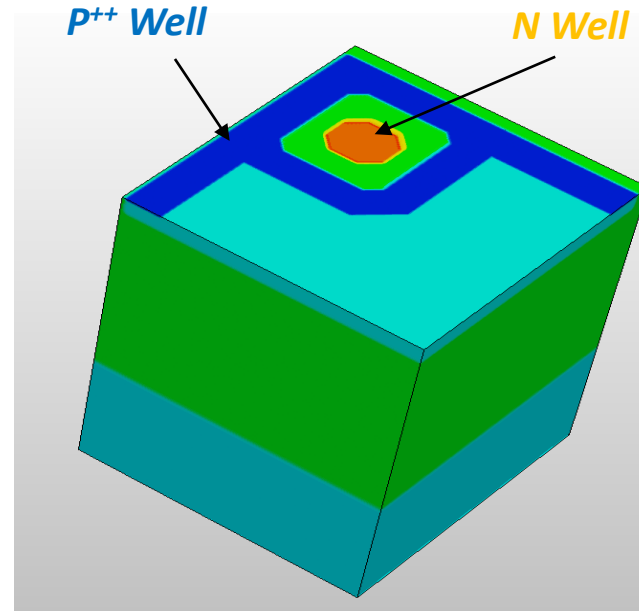


G. Calefato, et al, s., Comparison on radiation tolerance of <100> and <111> silicon substrates of microstrip detector, [https://doi.org/10.1016/S0168-9002\(01\)01667-9](https://doi.org/10.1016/S0168-9002(01)01667-9).

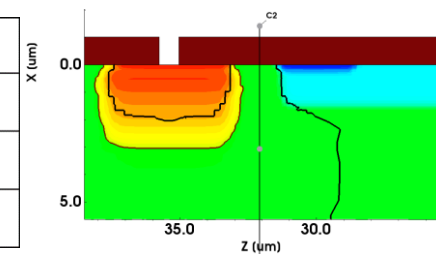
Isolation techniques

- The inversion channel might become even more important in low doped p-substrate, because of the segregation coefficient* S of B in SiO2 is < 1 (it is the opposite in case of n doping, like with P)

* The segregation coefficient S is equal to the ratio of the concentration of boron atoms at the surface of silicon to the concentration in silicon dioxide near the silicon-to-oxide interface.



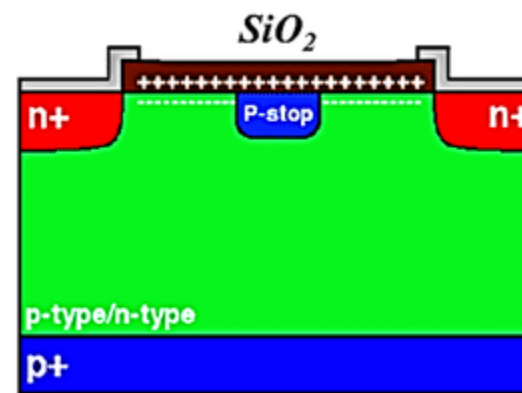
| Interface Defect | Level | Concentration | σ |
|------------------|----------------|--|----------|
| Acceptor | $E_C - 0.4$ eV | 40% of acceptor N_{IT} ($N_{IT} = 0.85 \cdot N_{OX}$) | 0.07 eV |
| Acceptor | $E_C - 0.6$ eV | 60% of acceptor N_{IT} ($N_{IT} = 0.85 \cdot N_{OX}$) | 0.07 eV |
| Donor | $E_V + 0.7$ eV | 100% of donor N_{IT} ($N_{IT} = 0.85 \cdot N_{OX}$) | 0.07 eV |



* Effects of Interface Donor Trap States on Isolation Properties of Detectors Operating at High-Luminosity LHC, DOI: 10.1109/TNS.2017.2709815

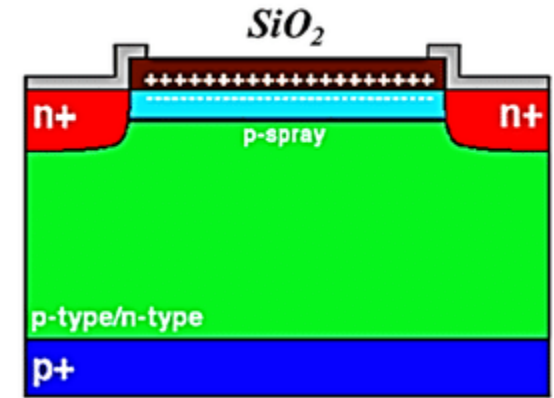
Isolation techniques

- **P-stop** and **p-spray** isolation techniques
- Breaking the inversion channel improves the isolation among cells
- The **p-stop** technique places a p^+ implant between adjacent wells
- The **p-spray** technique implements a uniform p layer between adjacent wells



The *floating p^+ stop* method consists of placing a p^+ implant in between two adjacent n^+ strips

*It requires an additional mask
It might decrease the BV*

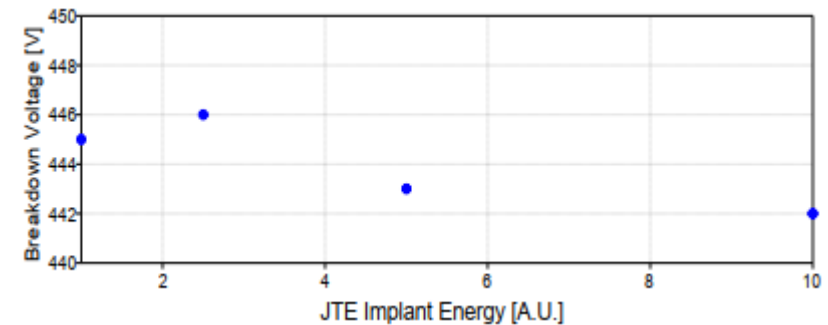
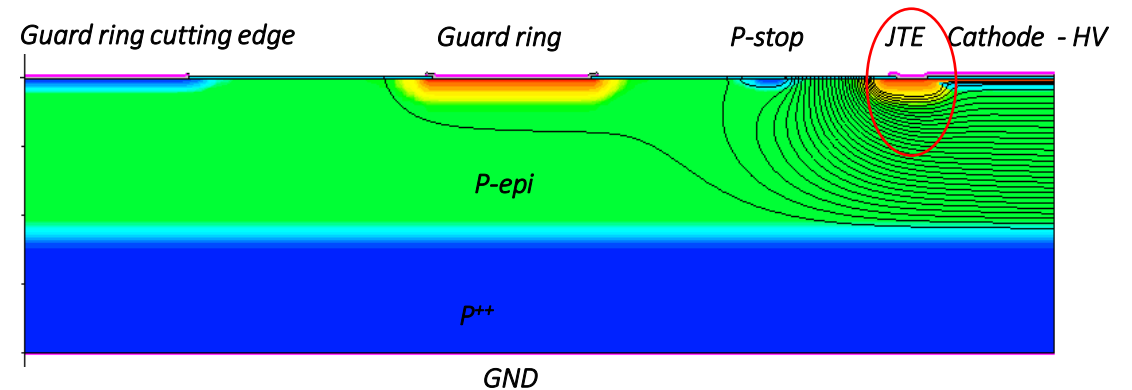


The *p-spray* method consists of having uniform p^+ layer beneath the Si/SiO_2 interface.

*No additional mask required
It requires careful dose of doping
(too low does increase BV but does not isolate, too high isolate but decreases BV)*

Isolation techniques

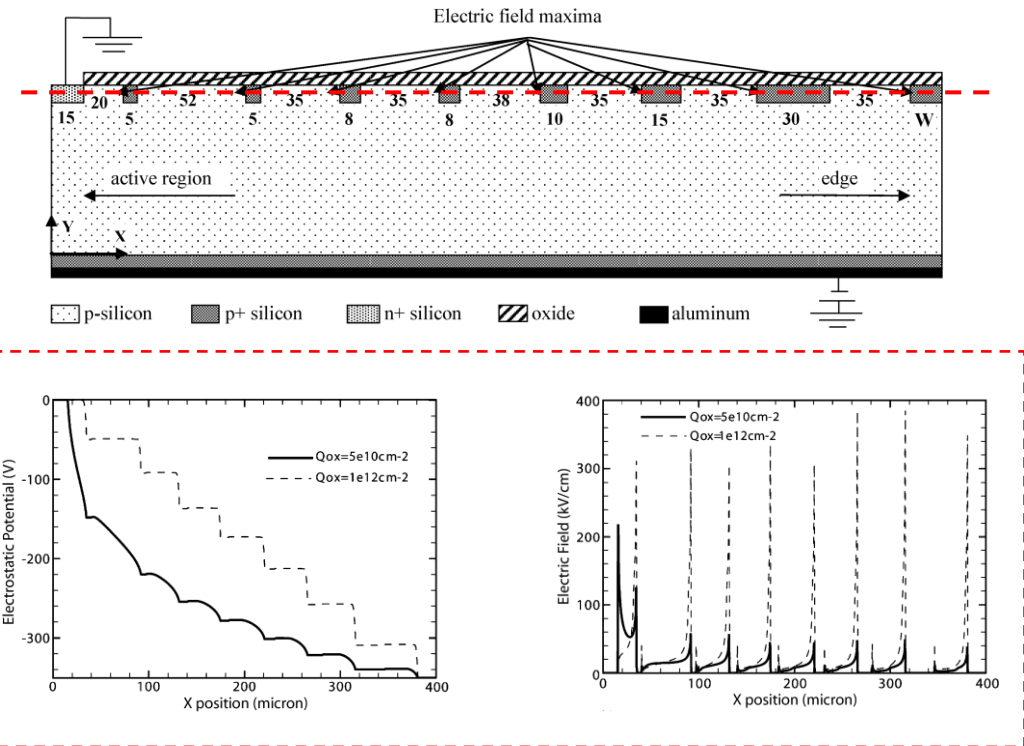
- The biasing of sensors with high voltage is required to guarantee good charge collection efficiency and short collection time
- The bias voltage is usually increased following sensors irradiation, due to loss of charge collection efficiency (reduced depletion, charge trapping –see Rad. Lectures)
- Various techniques to reduce the likelihood of breakdown due to the high voltage operation are used



*The use of **junction termination extension (JTE)** reduces gradually the potential from the edge of the sensor, decreasing the field and increasing the breakdown*

Isolation techniques

- Guard rings are used to ensure a smooth transition from HV to ground towards the edge
- Their design need to include surface charge effects resulting from irradiation
- Multi guard rings are often employed to allow for high voltage operation
- Their use increases the design complexity and the required area

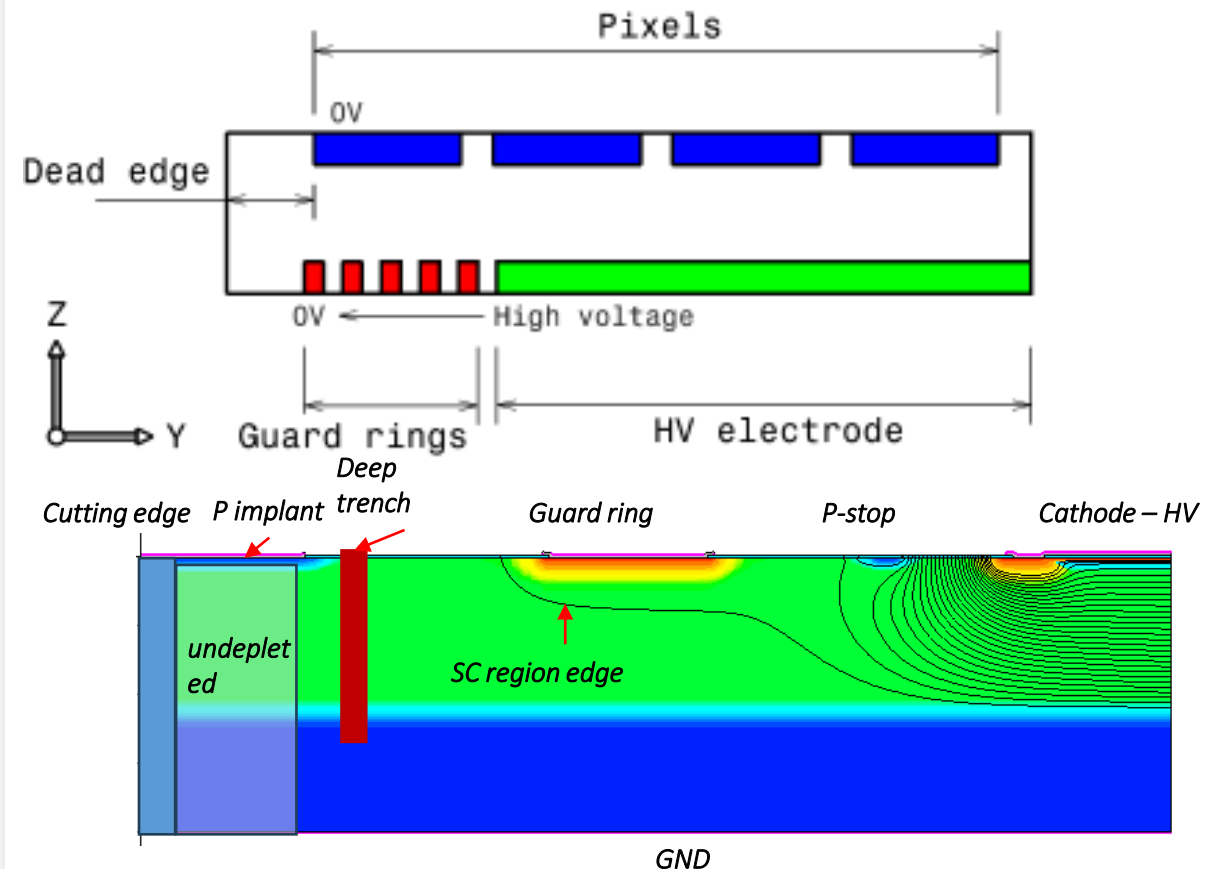


Multi guard rings improve the high voltage operation, by decreasing the electric field at the sensor edge

O. Koybasi, et al. "Guard Ring Simulations for n-on-p Silicon Particle Detectors," in IEEE Transactions on Nuclear Science, doi: 10.1109/TNS.2010.2063439

Isolation techniques

- The cutting edge of the sensor is usually damaged because of the dicing process, resulting in a very effective generation centre
- The SC / depletion region extending laterally may reach this area, leading to high leakage current
- Usually the sensor surface is terminated with a wide p⁺ implant to prevent this by making the region underneath undepleted
- Another approach is isolation via Deep trenches

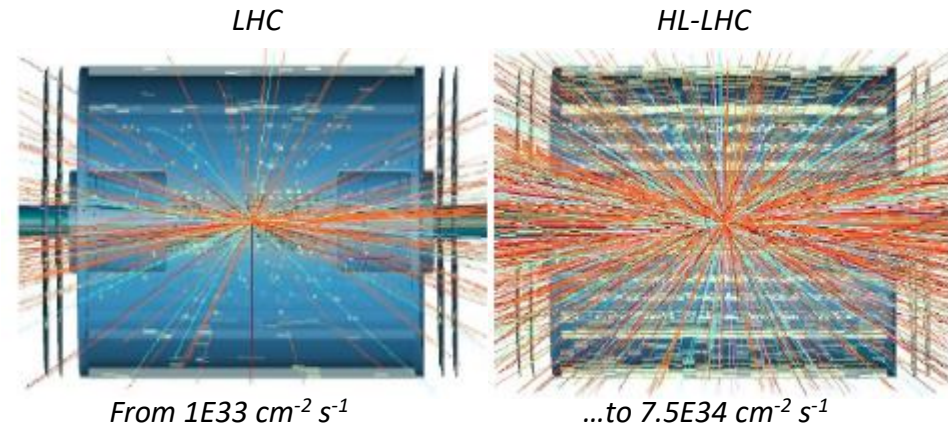


Guard rings are used also to avoid the SC region reaching the cutting edge of the sensor

Simulation of guard ring influence on the performance of ATLAS pixel detectors for inner layer replacement DOI: 10.1088/1748-0221/4/03/P03025

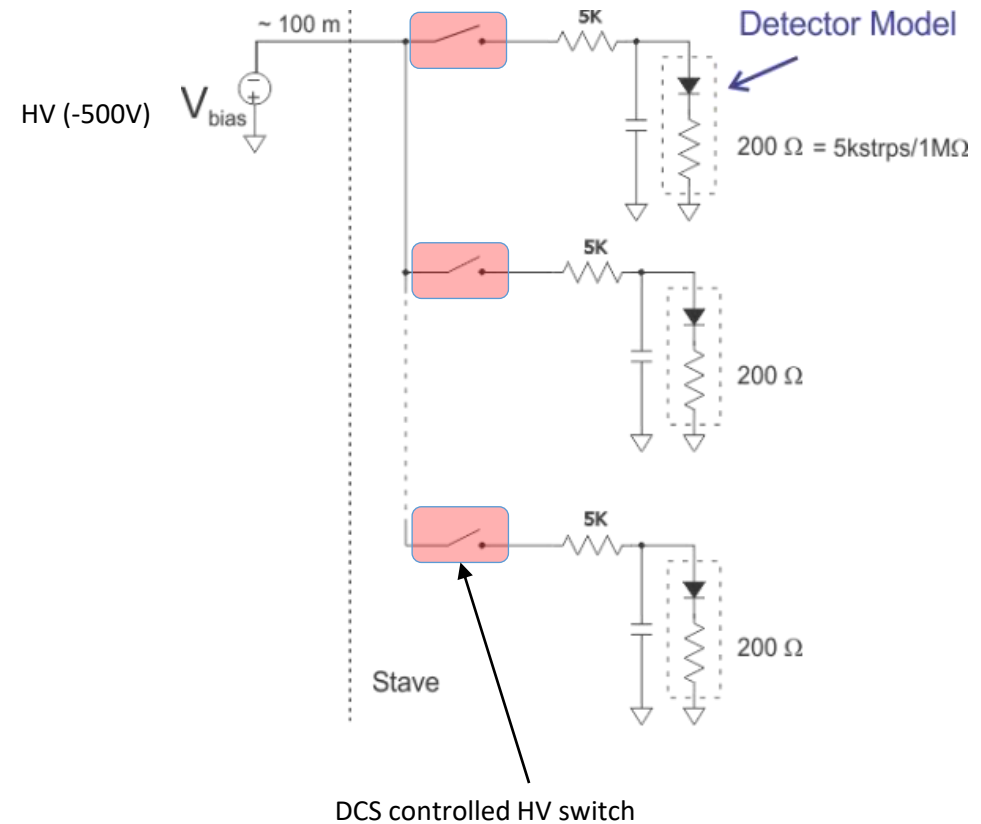
HV biasing

- Current ATLAS SCT uses independent powering for the 4088 detector modules. Each sensor has its own independent HV bias line.
- ‘ideal’ solution:
 - High Redundancy
 - Individual enabling or disabling of sensors and current monitoring
- The increased number of sensors in the Itk (>10 k modules in barrel upgrade vs. ~2 k in present barrel) implies a trade off among material budget, complexity of power distribution and number of HV bias lines.



HV biasing

- Use single (or more) HV bus to bias in parallel all sensors and use one HV switch for each sensor to disable malfunctioning sensors: High Voltage Multiplexing '**HVMUX**'
- The HV switch is DCS controlled, with control signals provided by custom ASIC (Autonomous Monitor And Control, AMAC)



HV biasing

- High Voltage switches strip detector requirements:
Rated to 500V plus a safety margin
- Must be radiation hard, nominal maximum expected $\sim 1 \times 10^{15}$ n_{eq}/cm^2 , ~ 30 Mrad (Si) for strip end cap. Multiply by 1.5 to include safety margin
- On-state impedance $R_{on} \ll 1k\Omega$ // $I_{on} \sim 10mA$ (for irradiated strip sensors)
- Off-state impedance $R_{off} \gg 1G\Omega$ // $I_{lkg} \ll I_{sens}$
- Must be unaffected by magnetic field
- Must maintain satisfactory performance at $-30^\circ C$
- Must be small (mass/area constraint) and cheap (around **1E4** needed)

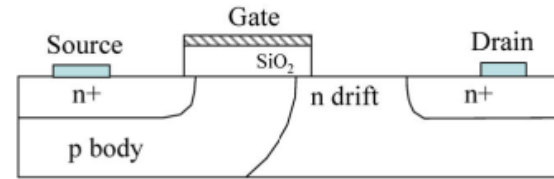
Partial list of investigated HV devices

| | | | |
|-----------------------|----------------|-------------|-------------|
| Crystalonic 2N6449 | Si JFET | 300V | FAILED |
| Interfet 2N6449 | Si JFET | 300V | FAILED |
| IXYS CPC5603 | Si MOSFET | 410V | FAILED |
| ROHM R6006ANX | Si MOSFET | 600V | FAILED |
| Infineon IPA50R950CE | Si MOSFET | 500V | FAILED |
| Semisouth SJEP170 | SiC JFET | 1700V | PASS – N.A. |
| USCi UJN1205 | SiC JFET | 1200V | FAILED |
| CREE CPMF-1200 | SiC MOSFET | 1200V | FAILED |
| ROHM S2403 | SiC MOSFET | 1700V | FAILED |
| GeneSiC GA04JT17 | SiC BJT | 1700V | FAILED |
| TranSiC FSICBH057A120 | SiC BJT | 1200V | FAILED |
| Transphorm TPH2006C | GaN JFET | 600V | FAILED |
| EPC2012 | GaN JFET | 200V | PASS |
| GS66502B | GaN FET | 650V | PASS |
| PGA26E19BV | GaN FET | 600V | PASS |

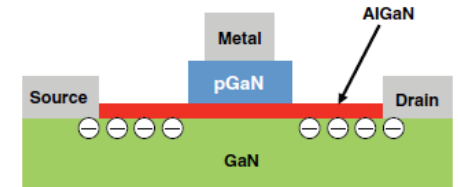
HV biasing

- Typical Si HV MOSFET use regions of low doping to increase high voltage capabilities: this affects their radiation hardness

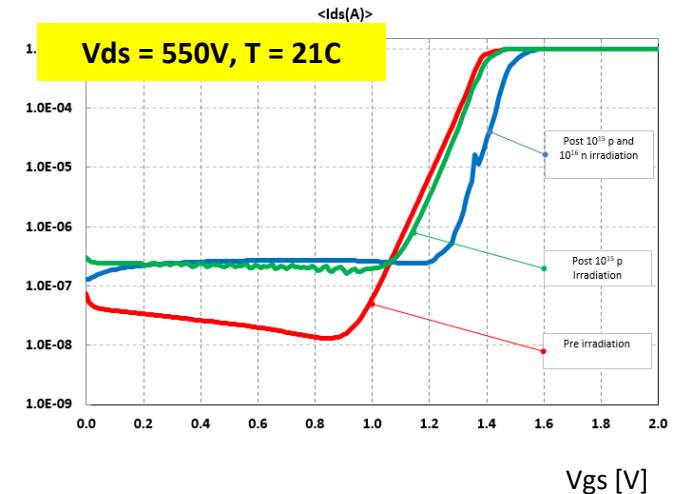
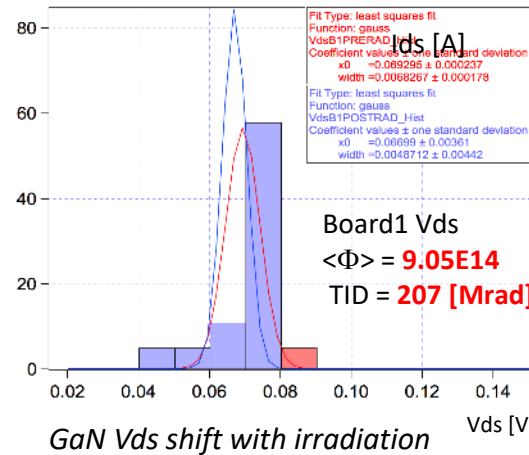
- Non-ionizing and ionizing irradiation test results of GaN FET devices indicate very high radiation hardness



A Lateral Double-Diffused MOS (LDMOS). A long drift region of lower doping reduces the electric field



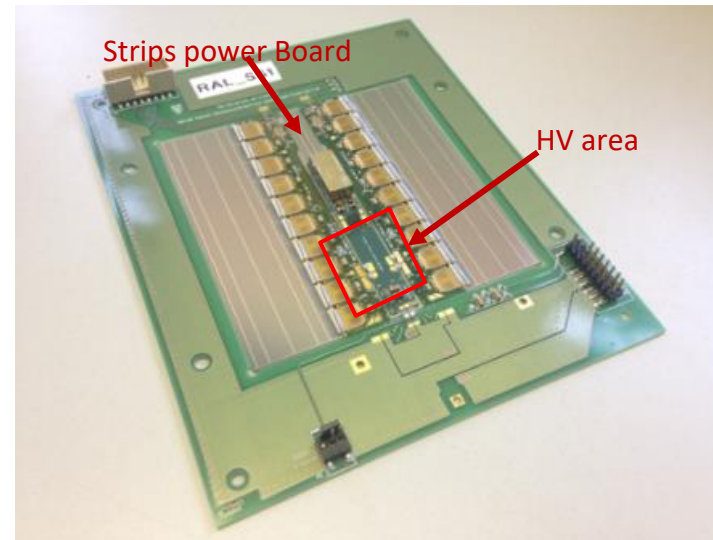
Example Xsection of a HEMT E. GaN FET. Strain-induced polarization at interface forms a 2DEG



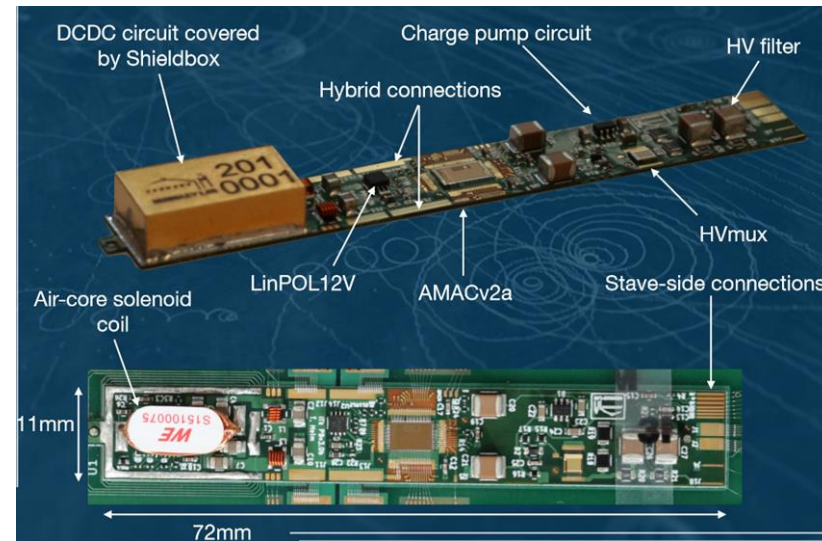
Additional test performed on 18 devices Total p fluence $1.0E15$, \sim TID 200Mrad(GaN)
Total n fluence $1.0E16$

HV biasing

- The HVMUX sits on the lower side of a flexi Power Board (PB)
- The PB final version incorporates power control and HVMUX elements in the AMAC ASIC



A barrel short strip module with two hybrids and one powerboard with HVMUX

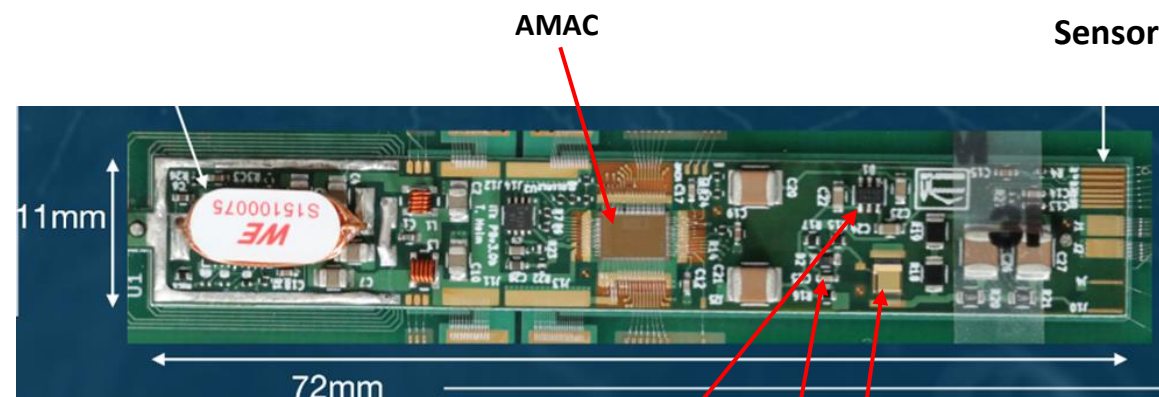


Power board v3.0b

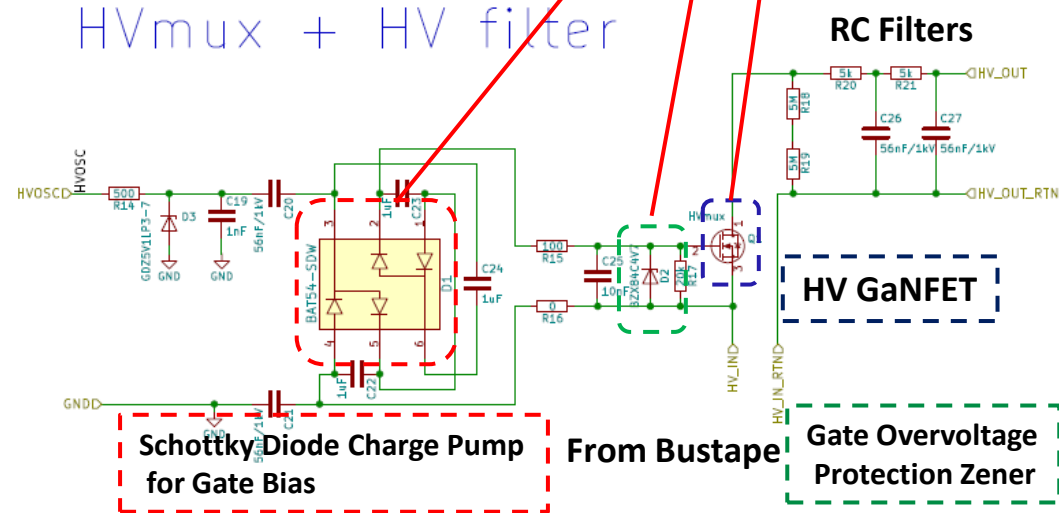
HV biasing

- A charge pump voltage multiplier driven by AC drives the gate of a GaN FET, rated for HV
- Investigated stacked solutions demonstrated switching voltages $> 1\text{kV}$
- Up to 600V with the implemented ItK solution
- Baseline solution for HV bias of ItK strips

LBNL V3 PowerBoard with HV Mux



HVmux + HV filter



Villani, E.G., Technical Design Report for the ATLAS Inner Tracker Strip Detector, CERN-LHCC-2017-005, ATLAS-TDR-025, <https://cds.cern.ch/record/2257755>

Thank you

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Circuits and Layouts II Summary

- Hybrid and Monolithic technology pros and cons
- Common isolation techniques
- Example of ITk Strips HV biasing