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Device Structures: Monolithic

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Overview

Introduction

- CMOS Sensors and ASICs at RAL
- CMOS APS, MAPS, Monolithic???
- Why CMOS – the industrial background

Standard Device Structures

- 3T Pixel
- 4T Pixel
- Improving the dynamic range
- Sensitivity Improvements
- Stitching

Device Structures in Particle Physics

- Challenges
- Typical Pixel Structure
- Efficiency in Complex Pixels
  - Deep P-well
  - Thick Epi
- TID Damage
- Bulk Damage
  - Full Depletion
  - Small Collection Electrode
  - Large Collection Electrode

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Introduction

Introduction

CMOS Sensor Design Group

- Started in 1998
- Part of ~370 staff in the Technology Department
- Over 8 decades combined CMOS experience
- Initially targeting space science, earth observation and particle physics
- Work with both research and industry

- STFC
  - Technology Department
    - Applied Science Division
    - Detectors & Electronics Division
      - Electronic Systems Software Group
      - Electronic Systems Design Group
      - Interconnect Group
      - Detector Development Group
      - ASIC Design Group
      - CMOS Sensor Design Group
    - Microelectronics Support Centre

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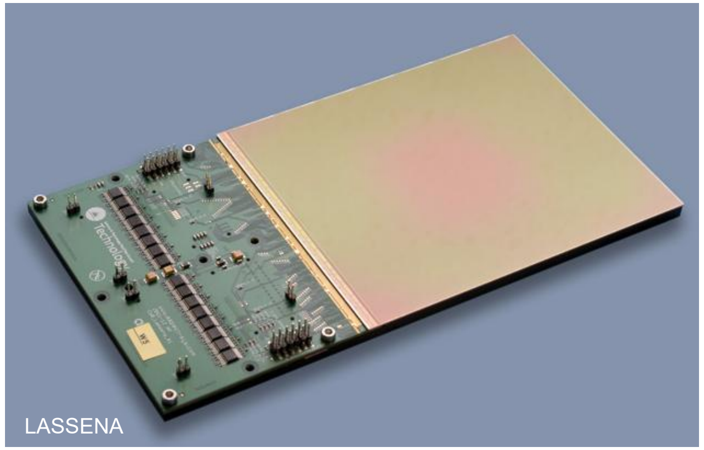
Introduction

CMOS Sensor Design Group

- Sensors for scientific applications
  - Large Area ("stitched") sensors
  - Ultra-High-Speed imagers
  - Bespoke sensor configurations
- Designed to detect
  - Visible, UV, X-Rays and Gamma
  - Charged Particles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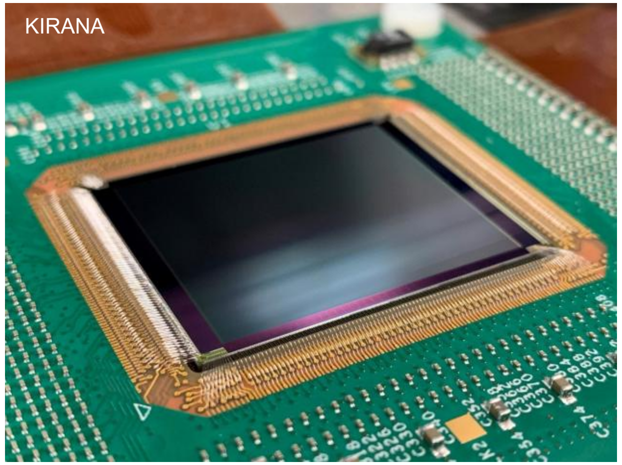
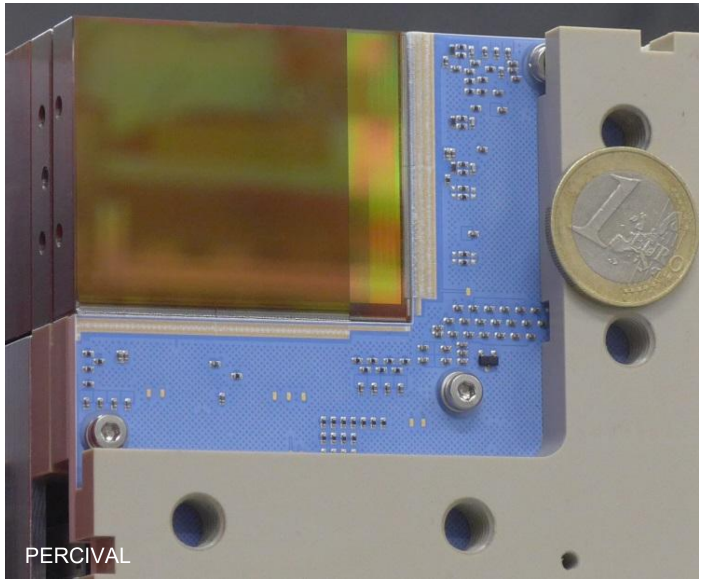
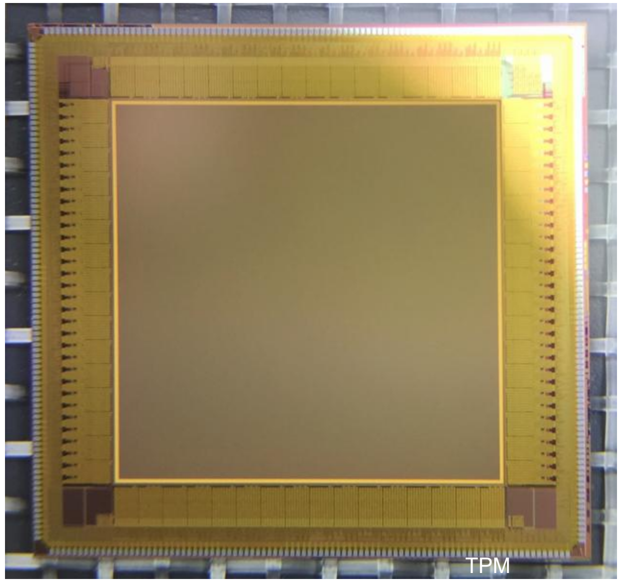

KIRANA


PERCIVAL


TPM

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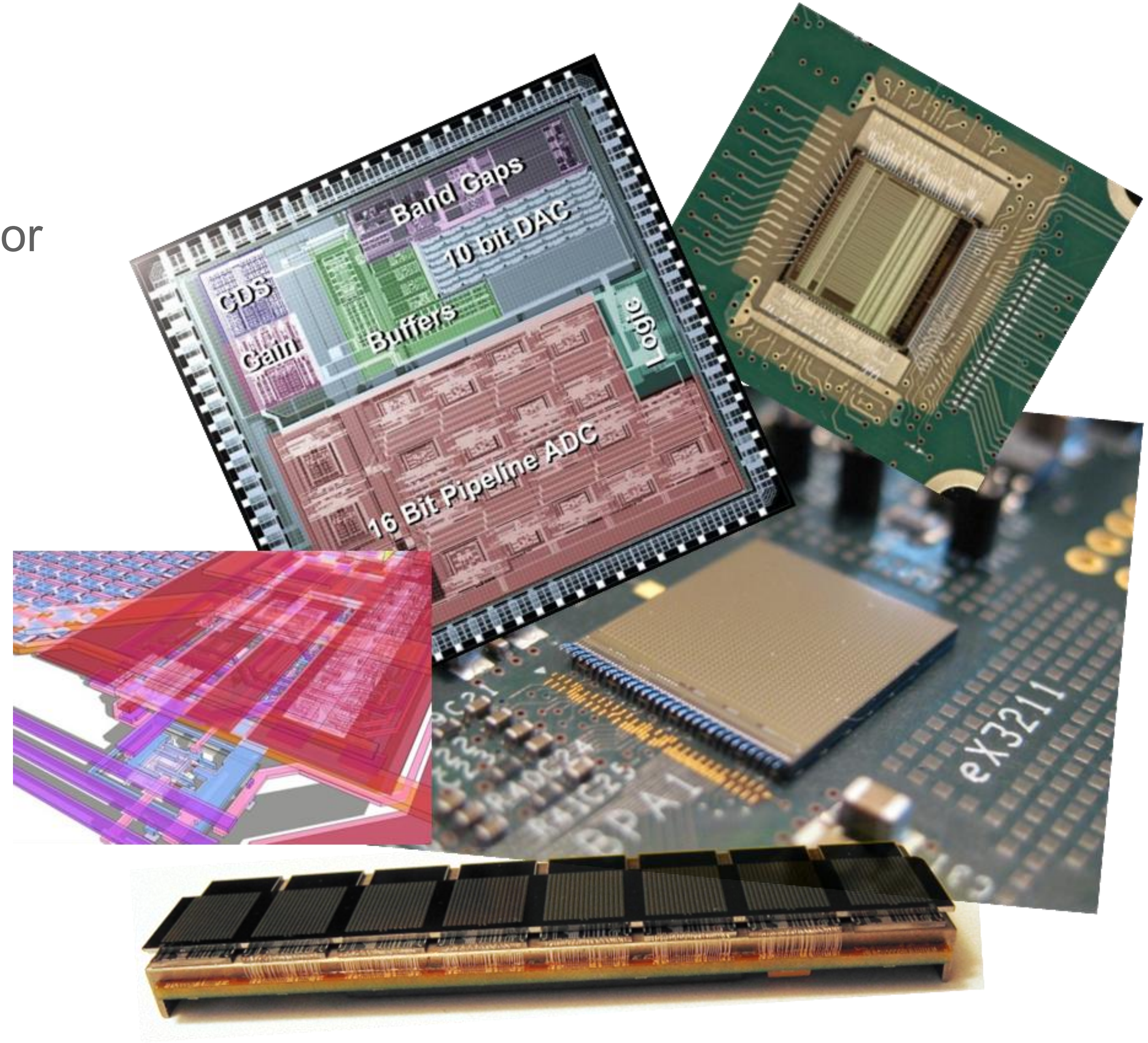
Introduction

ASIC Design Group

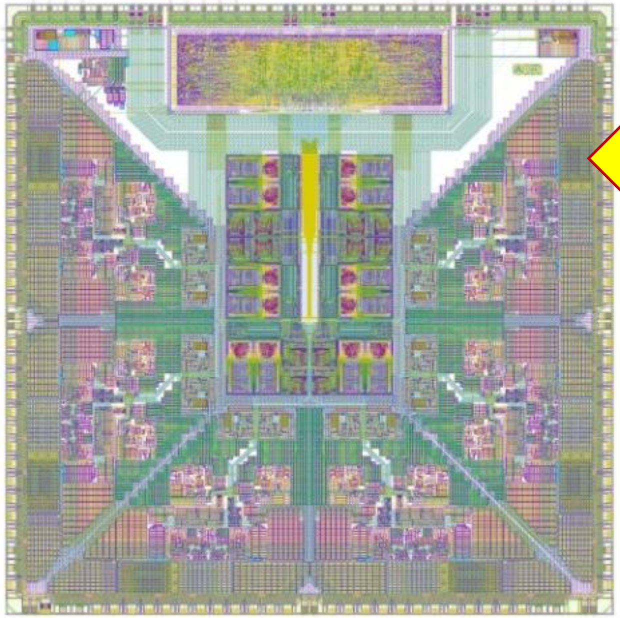
- Complete on-chip solutions to detector readout
- Mixed signal ICs
- High channel density
- Low power, low noise amplifiers
- Design for radiation environments
- High performance ADCs
- Commercial CMOS technologies
- In-house wire and flip-chip bonding



Introduction

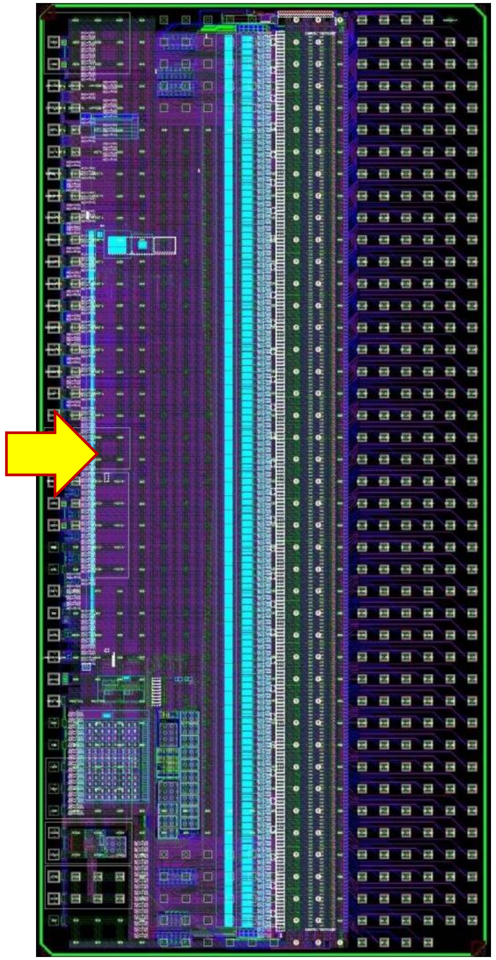
ASIC Design Group

- Space science, particle physics, security, photon science…and many more…



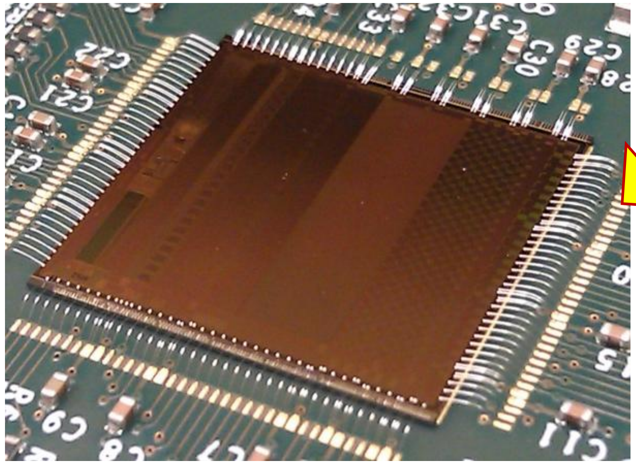
COMET: A Fully Programmable 6 channel CCD Clock driver

- ❖ 350nm HV process



CBC: A 254 Channel Readout ASIC for HL-LHC

- ❖ 130nm process



STAR: A Space Telemetry And Reference chip

- ❖ Multi-channel DAC for low noise reference voltages to science grade CCD’s
- ❖ 350nm HV process

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Notes on the Content

- Thanks to many people who provided content or useful discussion for these slides (particularly the rest of the CSDG – Seddik Benhammadi, Daniel Brown, Matthew Brown, Nicola Guerrini, Peter Hatfaludi, Herman Larsen, Ben Marsh, Bindu Velagapudi)

- Also Eva Villela (U. Liverpool) who previously delivered this course and generously provided the slides from those courses as the basis for these talks.

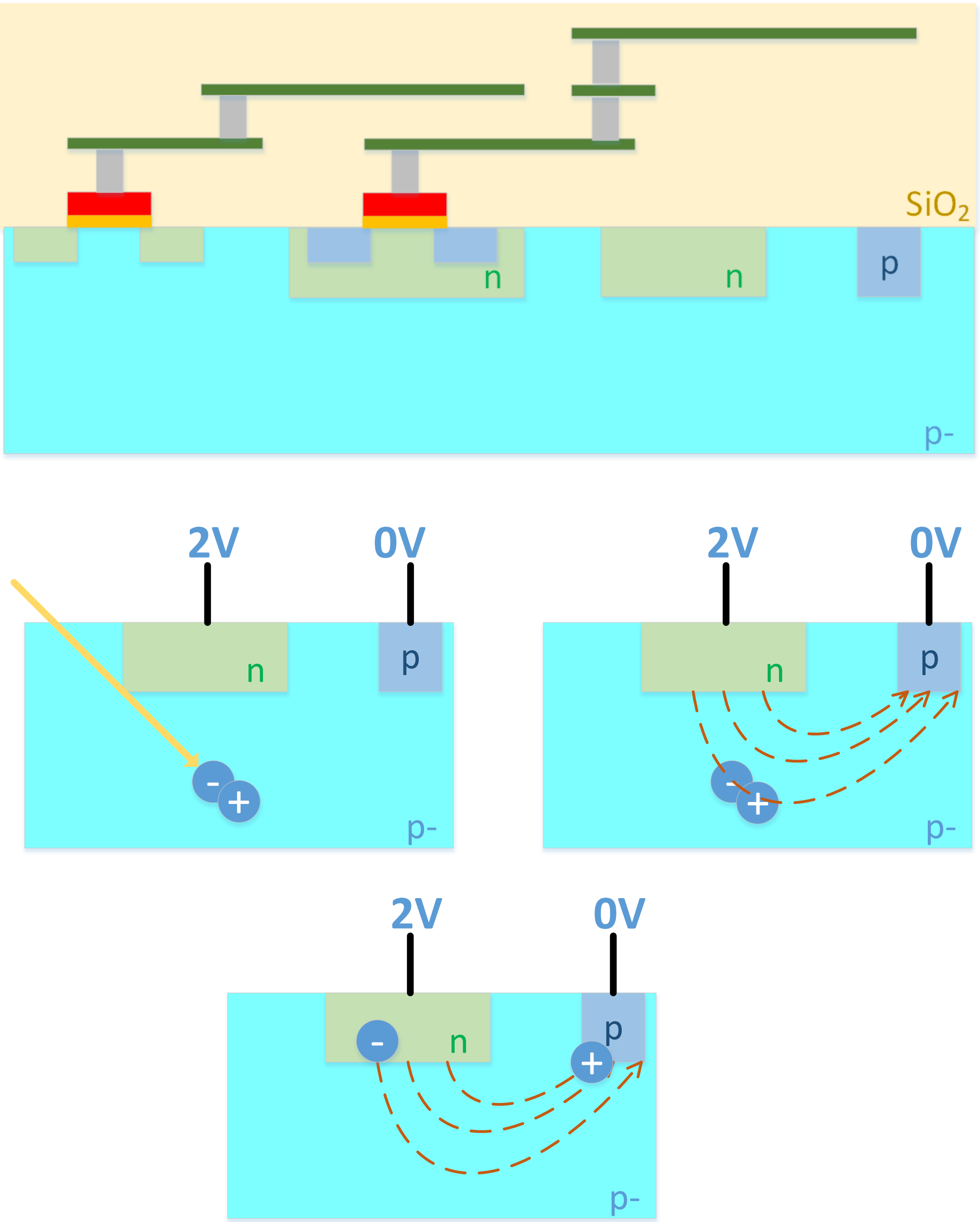
- Only an overview is really possible in the available time. Many links are included in the text for further information.

- Time for questions at the end, and very happy to take further questions by e-mail (iain.sedgwick@stfc.ac.uk)

Introduction

CMOS APS, MAPS, Monolithic, CIS????

- CMOS – Complementary Metal Oxide Semiconductor
- APS – Active Pixel Sensor
- Monolithic:
  - Sensor material and readout electronics are part of the same substrate, as opposed to hybrid detectors, where they are separate
- MAPS – Monolithic Active Pixel Sensor
- CIS – CMOS Image Sensor
- **All refer the to the same technology/effect.**



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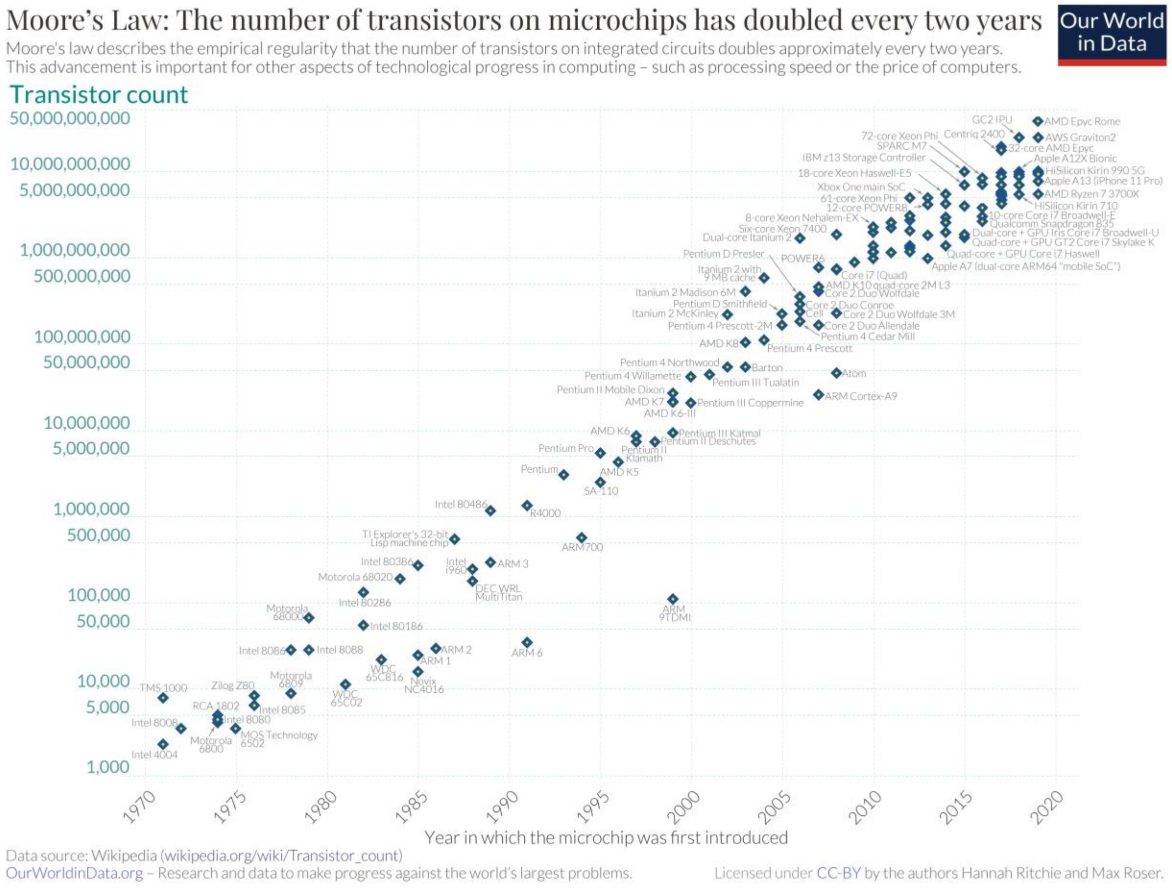
Why CMOS – The Industrial Background

Why CMOS?

- Huge levels of investment have led to dramatic increases in transistor density over the last 60 years (Moore's Law)
- This has led to similar levels of improvement in cost and performance (Dennard Scaling)
- Industry has moved more and more towards the "fabless" model
- End result is the ability to design exceptionally high performance chips for many applications without building a fab



Moore's Law: The number of transistors on microchips has doubled every two years

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important for other aspects of technological progress in computing – such as processing speed or the price of computers.

Data source: Wikipedia (wikipedia.org/wiki/Transistor_count)

OurWorldinData.org – Research and data to make progress against the world's largest problems.

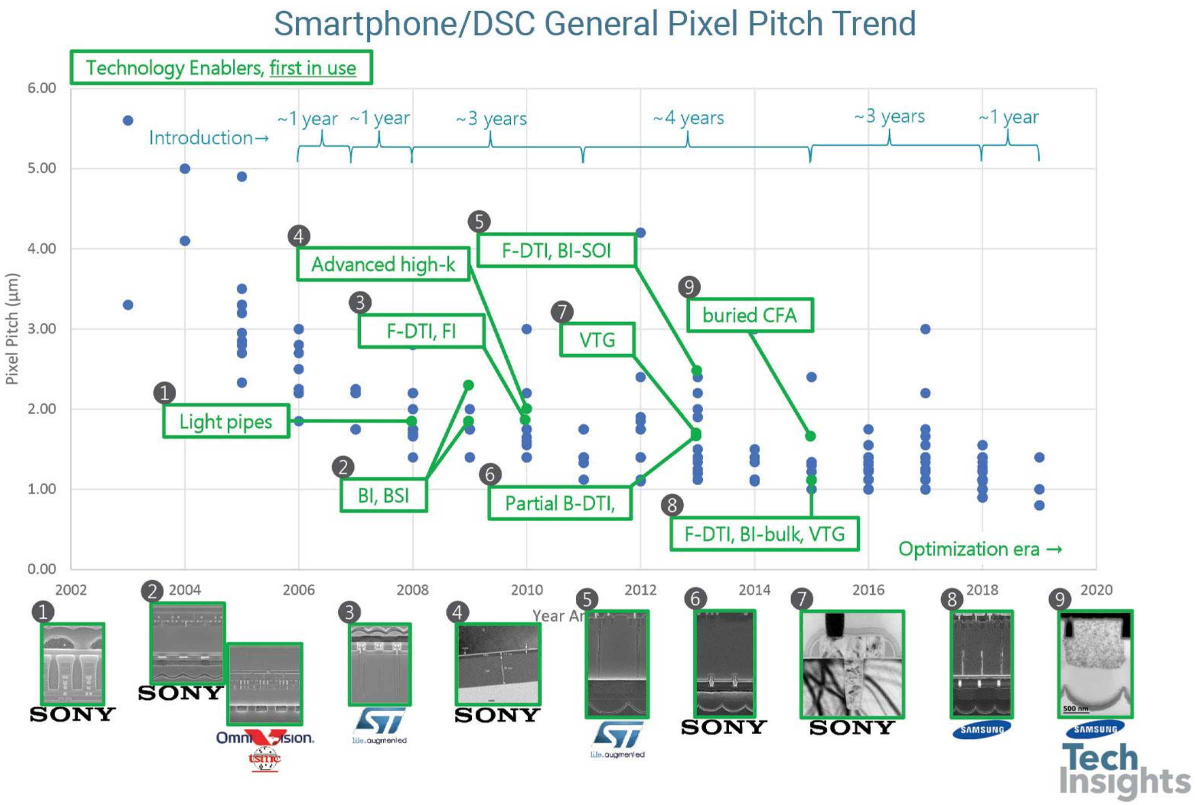
https://ourworldindata.org/moores-law

Why CMOS – The Industrial Background

What about CIS/MAPS/Monolithics?

- Similar trend of improvement
- First image sensors in CMOS were CCDs, later supplanted by CMOS APS (see here and here for the history)
- Initial scientific use, but smartphones provided the key commercial driver
- This has involved the development of many advanced process modifications

Selected Pixel Scaling Enablers



https://www.techinsights.com/blog/part-2-pixel-scaling-and-scaling-enablers

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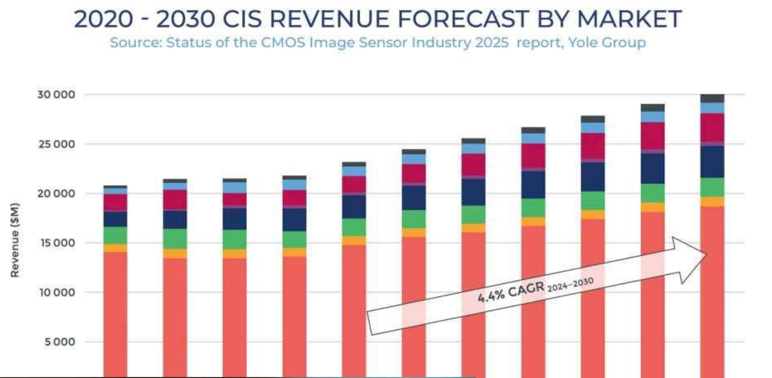
Standard Device Structures

Standard Device Structures

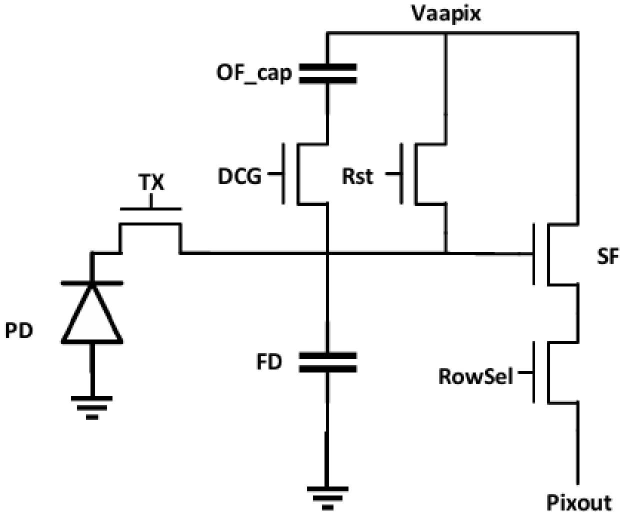
Introduction

- All builds on commercial CMOS Image Sensor structures
- So what are these structures?
  - 3, 4, 5, 6T pixels
  - Dynamic range
  - Large area
  - Microlenses
  - BSI
- Scientific Use – do we need structures beyond this?


2020 - 2030 CIS REVENUE FORECAST BY MARKET

Source: Status of the CMOS Image Sensor Industry 2025 report, Yole Group

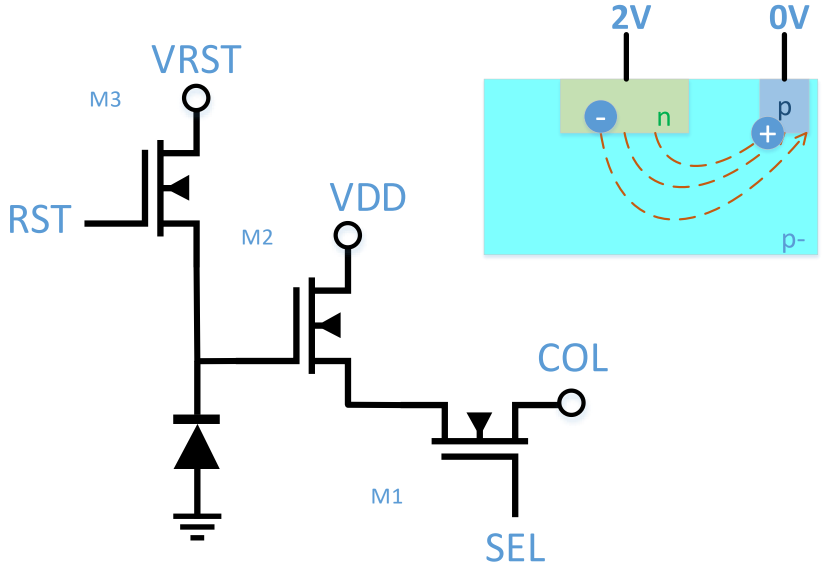
www.yolegroup.com | ©Yole Group 2025

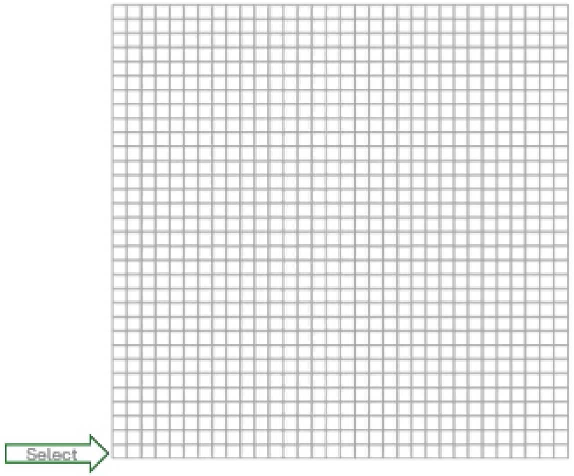


Standard Device Structures

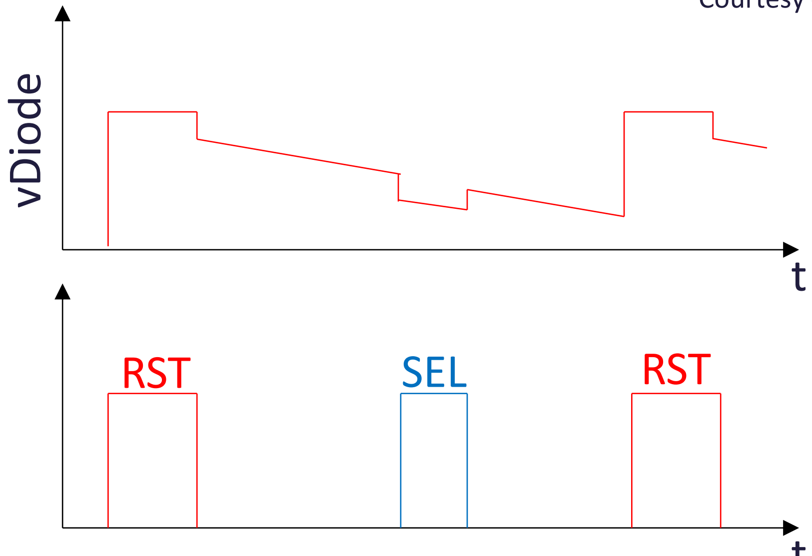
3T Pixel

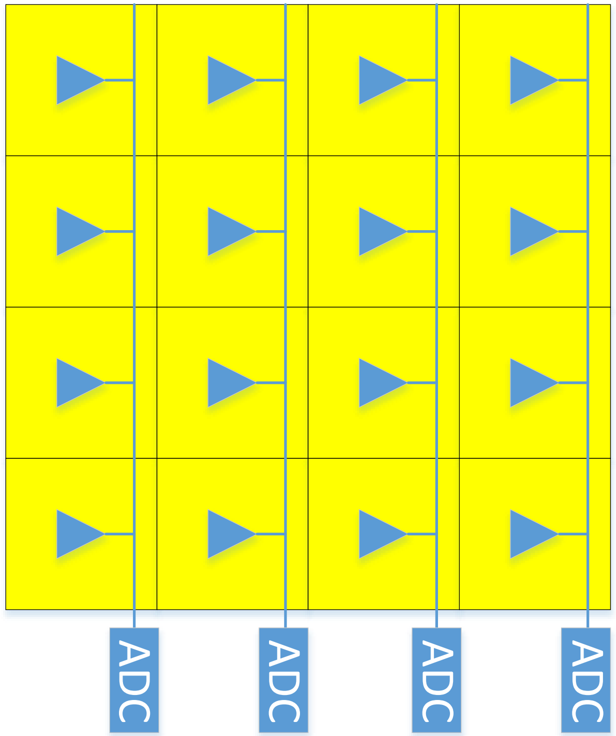
- Simplest CMOS Pixel
  - Diode: charge collection
  - Reset Transistor: resets diode
  - Source Follower: output amp
  - Select Transistor: row based readout





Courtesy of H. Larsen





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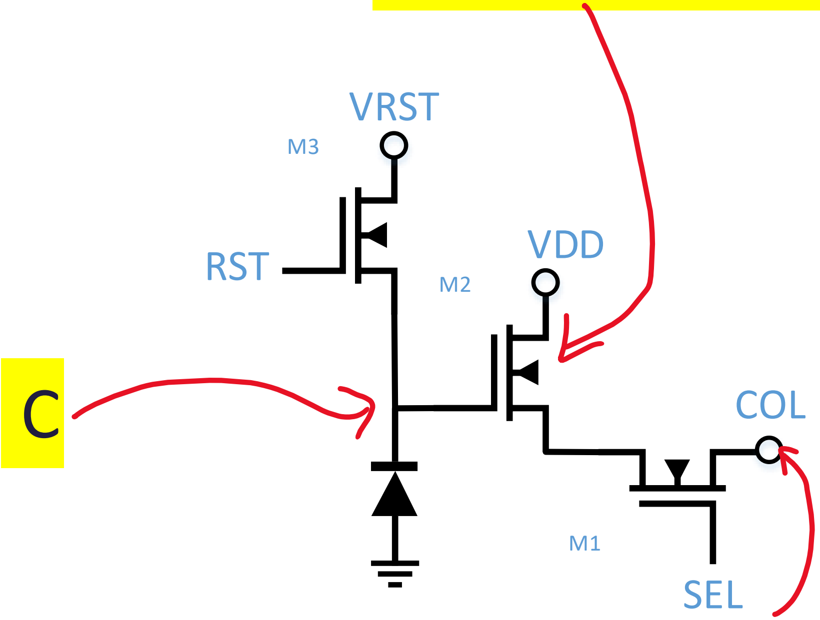
Standard Device Structures

3T Pixel

- All performance parameters depend critically on the capacitance at the diode **node** (C in fF)
  - Full Well (e$^-$) = $6250 * C * MOVS$
  - Gain (µV/e$^-$) = $G_{SF}\left(\frac{160}{C}\right)$
  - kTC Noise (e$^-$) = $12.7\sqrt{C}$
  - Total Noise is quadrature sum of the kTC Noise and the input referred readout noise
- This dependence on the capacitance will remain true for all the subsequent structures we will look at

$$\sigma_{tot}{}^2 = (12.7\sqrt{C})^2 + \left(\frac{C * \sigma_{readout}}{160}\right)^2$$

GSF – Source follower gain. Less than 1 for an NMOS due to body effect



MOVS – Maximum Output Voltage Swing
- Maximum range over which the output node can move
- Affected by:
  - Reset Voltage
  - Vgs of Source Follower
  - Charge injection

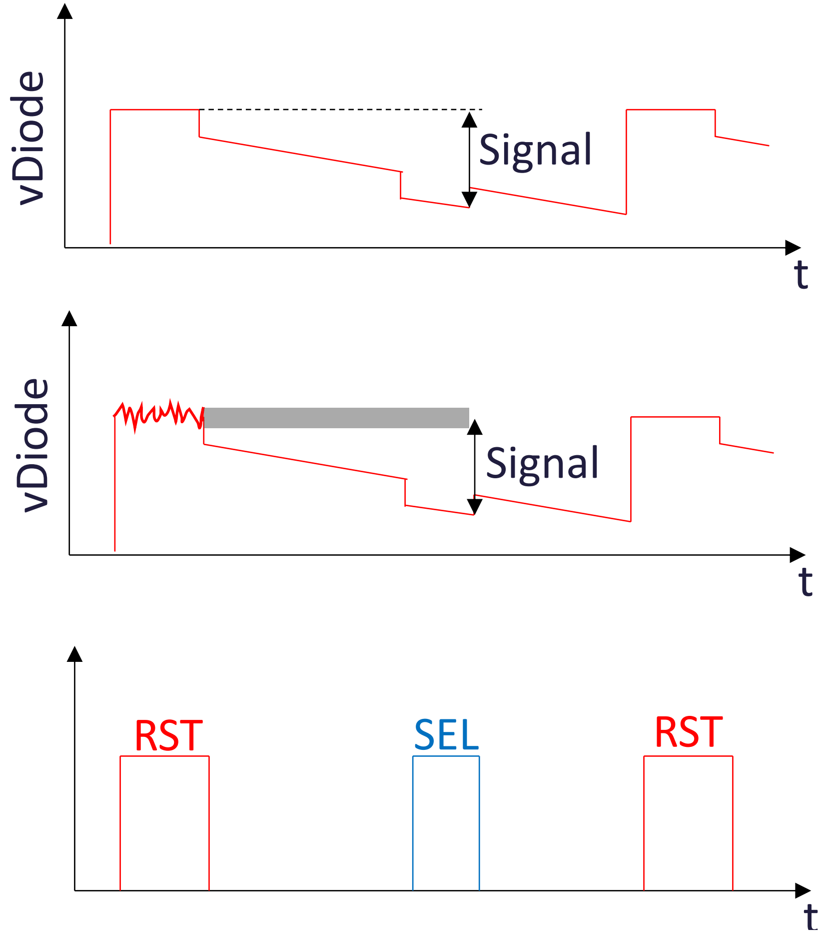
$\sigma_{readout}$
- Total readout noise in µV
- Includes source follower, analog chain, ADC…

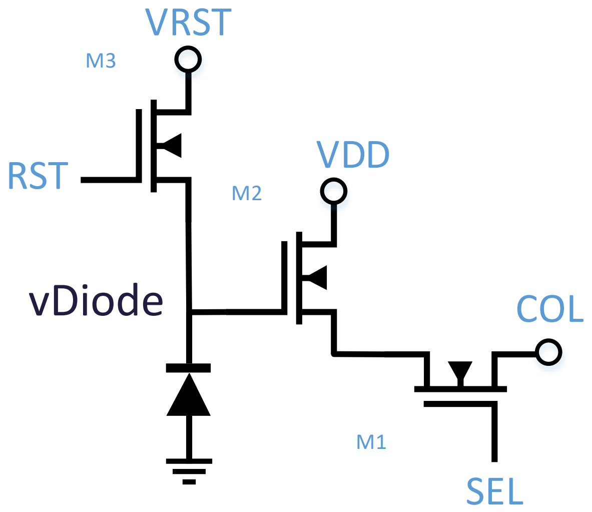
Standard Device Structures

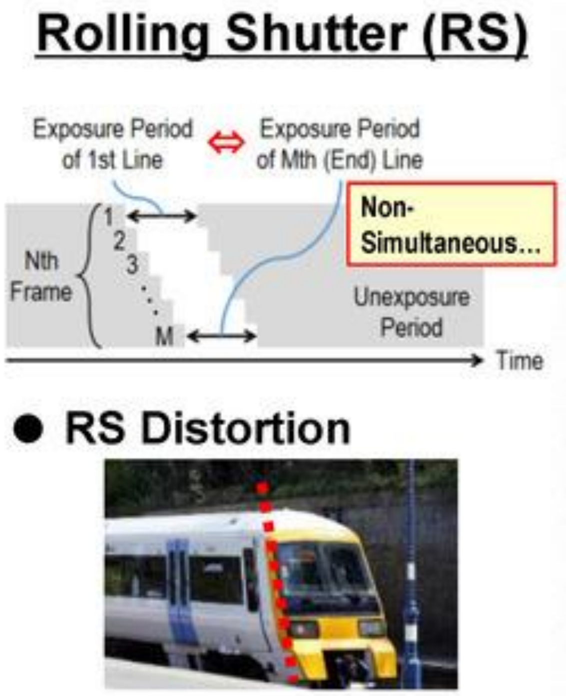
3T Pixel

- Advantages
  - Compact ☺
  - Simple (good yield) ☺
  - Some TID resistance ☺

- Disadvantages
  - Rolling Shutter Artefact ☹
  - High noise (no CDS) ☹
  - Collection by diffusion ☹
  - Limited dynamic range ☹







https://doi.org/10.3390/s17122860

Rolling Shutter

https://www.edge-ai-vision.com/2021/10/what-are-global-shutter-and-rolling-shutter-how-to-choose-the-one-that-fits-the-application/

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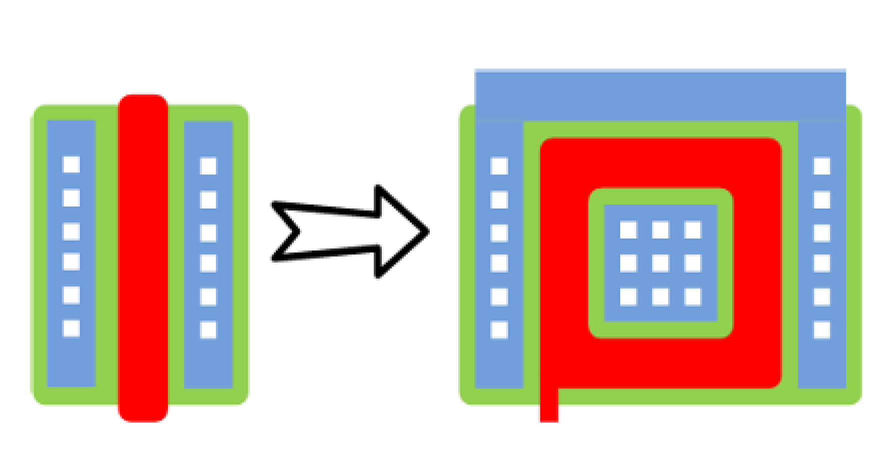
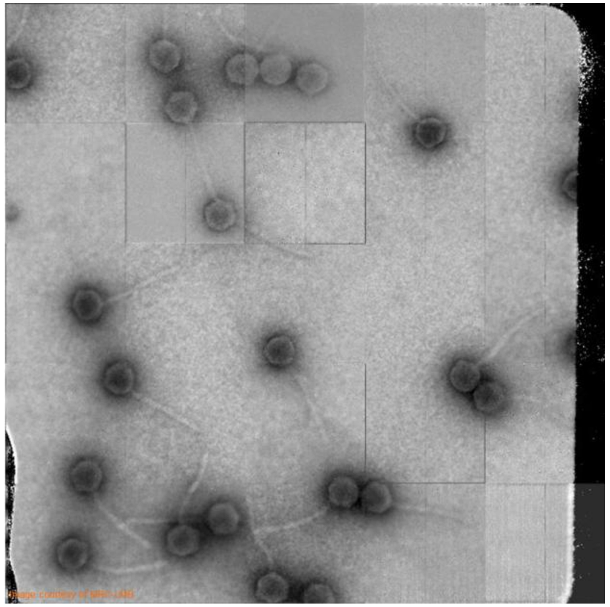
Standard Device Structures

3T Pixel - Example

- Less common in commercial applications (except some low cost applications)
- But easier to radiation harden – use in electron microscopy





https://indico.cern.ch/event/309449/contributions/1680023/attachments/591526/814257/GuerriniCPIX14.pdf

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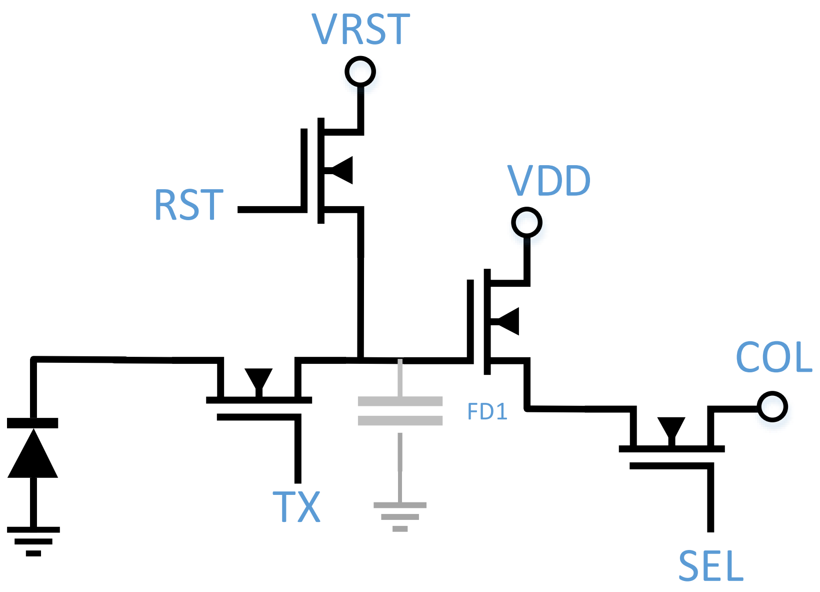
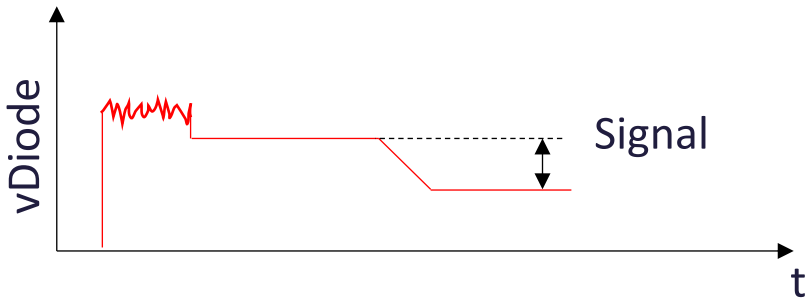
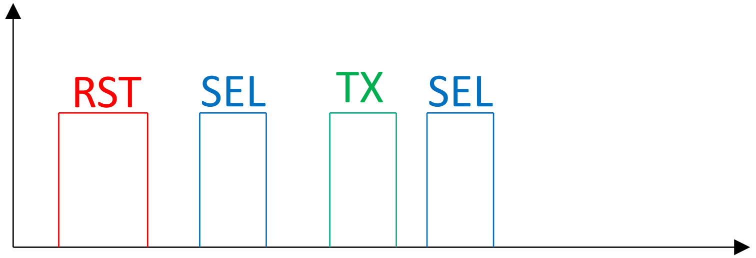
Standard Device Structures

4T Pixel

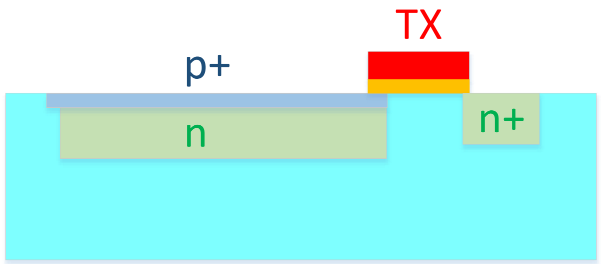
- Adds an extra transistor – the transfer gate
- Uses a pinned photodiode
- Separates the readout node from the charge collecting node
- Allows CDS

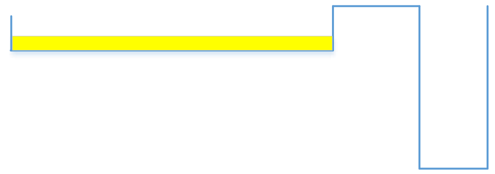






$$\sigma_{tot}{}^2 = 2 * \left(\frac{C * \sigma_{readout}}{160}\right)^2$$





TX Off – Read reset level of Floating Diffusion

TX On – Transfer charge and read signal

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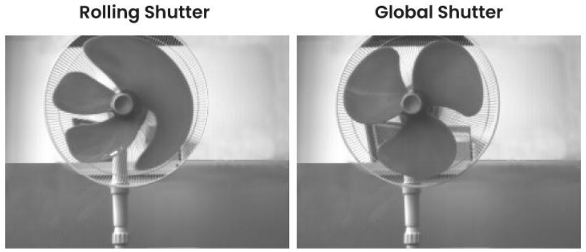
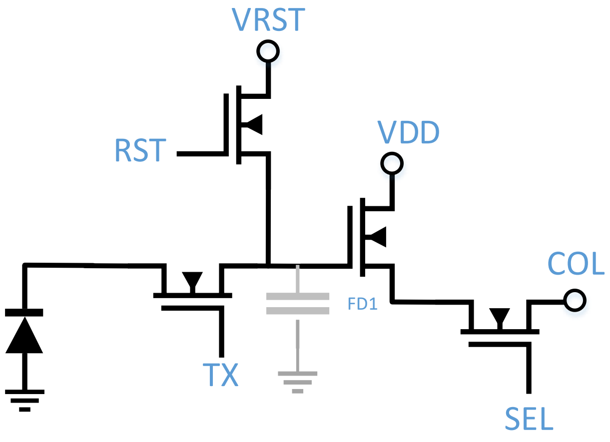
Standard Device Structures

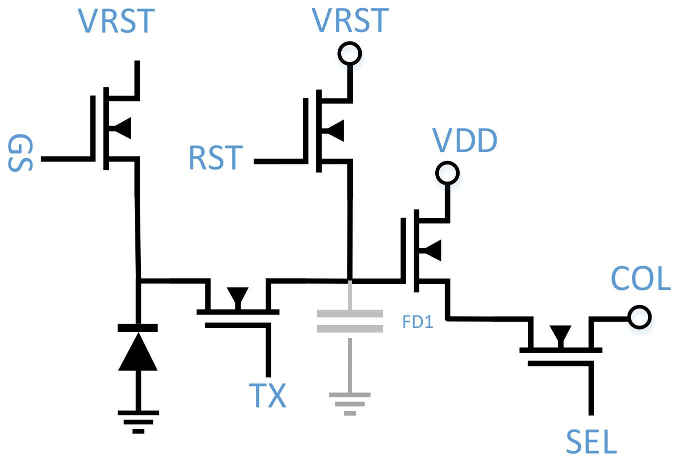


4T, 5T, 6T… Pixel

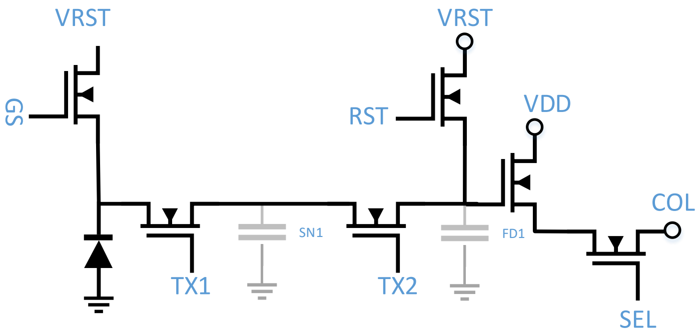
- CDS possible ☺
- Still rolling shutter ☹
    - 5T pixel! ☺
        - But now no CDS… ☹
    - 6T pixel! ☺
- Collection by diffusion ☹
- Limited dynamic range ☹
- Lower TID resistance ☹



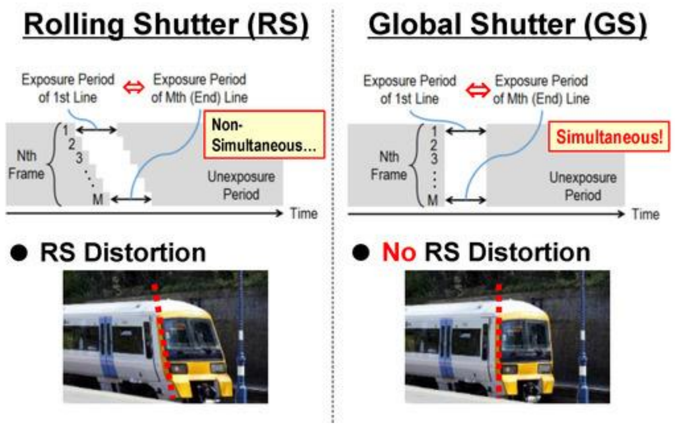
4T



5T



6T



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Further reading 1

Further reading 2

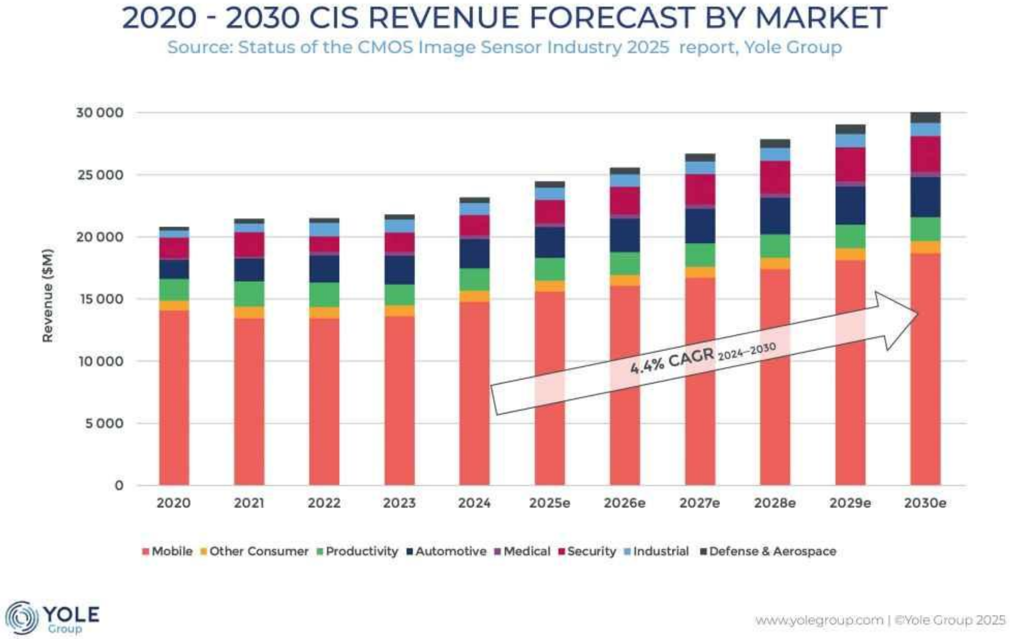
Standard Device Structures

4T, 5T, 6T… Pixel - Example

- Just about everywhere

https://www.pexels.com/photo/mounted-surveillance-camera-on-the-wall-13422379/

https://www.pexels.com/photo/five-smartphones-on-a-gray-background-24181865/



https://www.photonics.com/Articles/CMOS-Image-Sensor-Market-Predicted-to-Reach-30B/a71296

https://www.pexels.com/photo/smartphone-captures-vintage-and-modern-cameras-34808850/

https://www.pexels.com/photo/drone-flying-in-the-sky-19116769/

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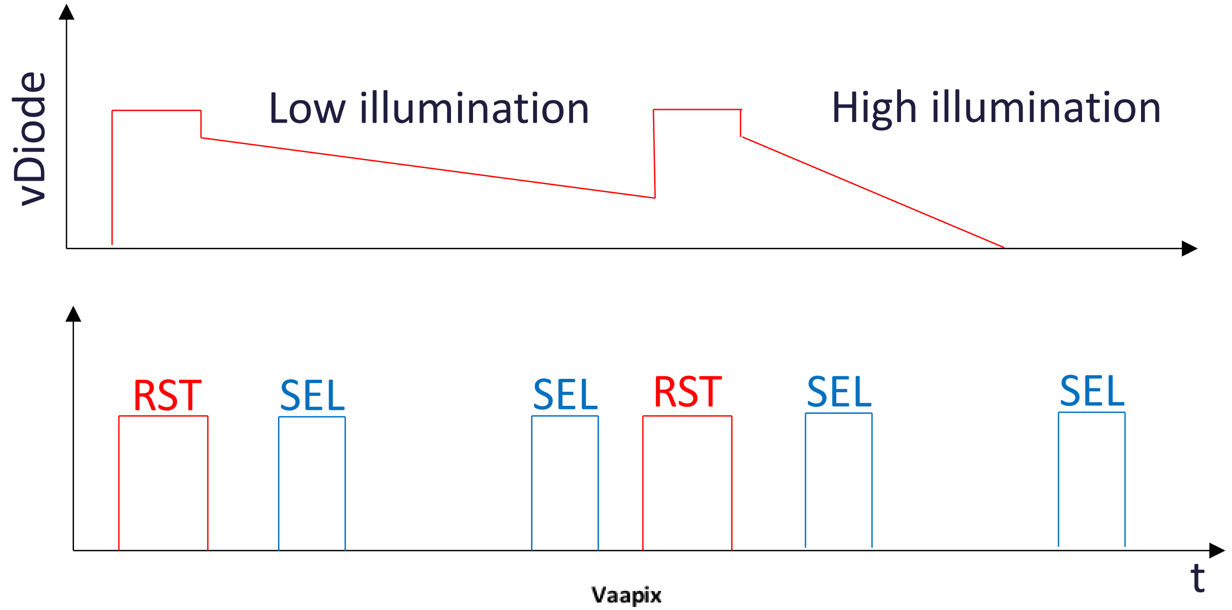
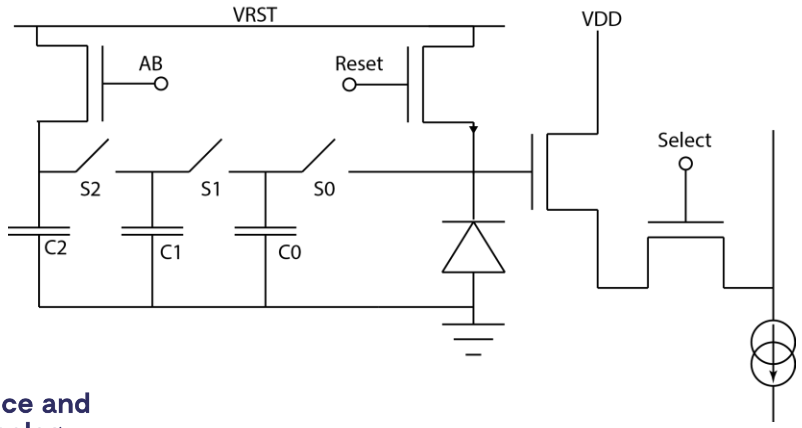
Standard Device Structures

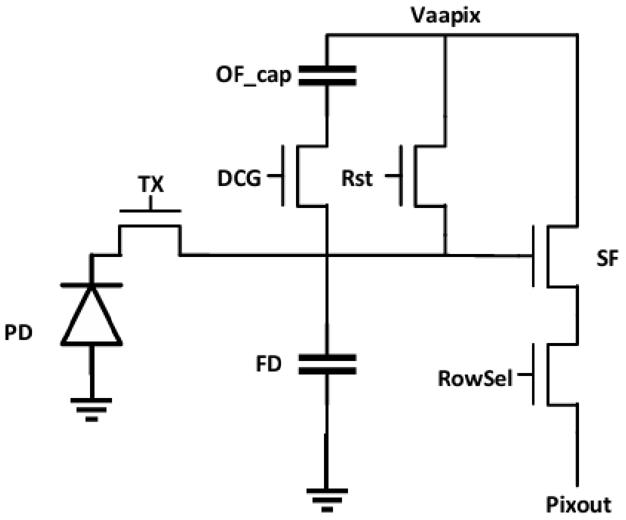
High Dynamic Range

- Several architectures
  - Multi integration time
  - Dual Conversion Gain and Lateral Overflow
  - Logarithmic pixel





3T Lateral Overflow



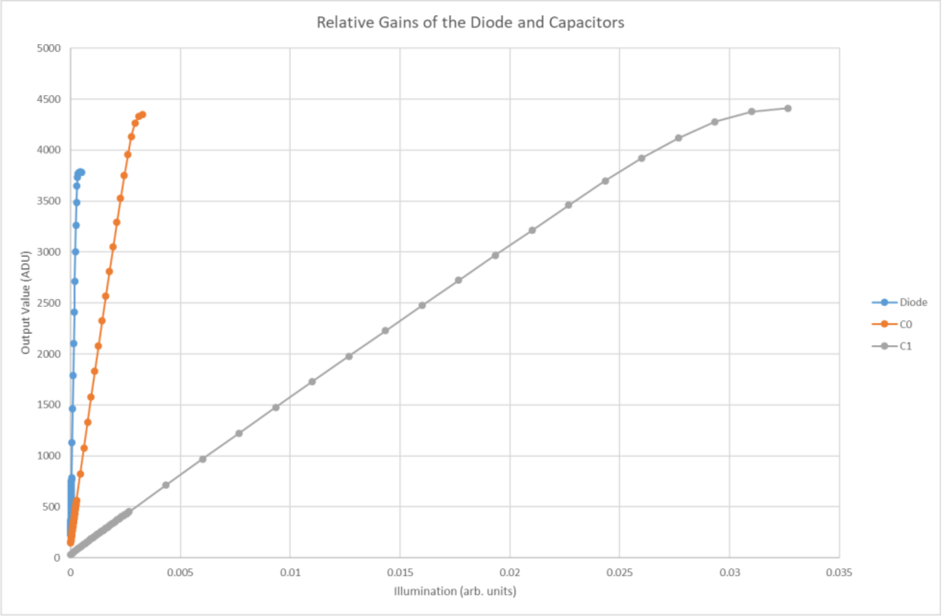
4T Lateral Overflow

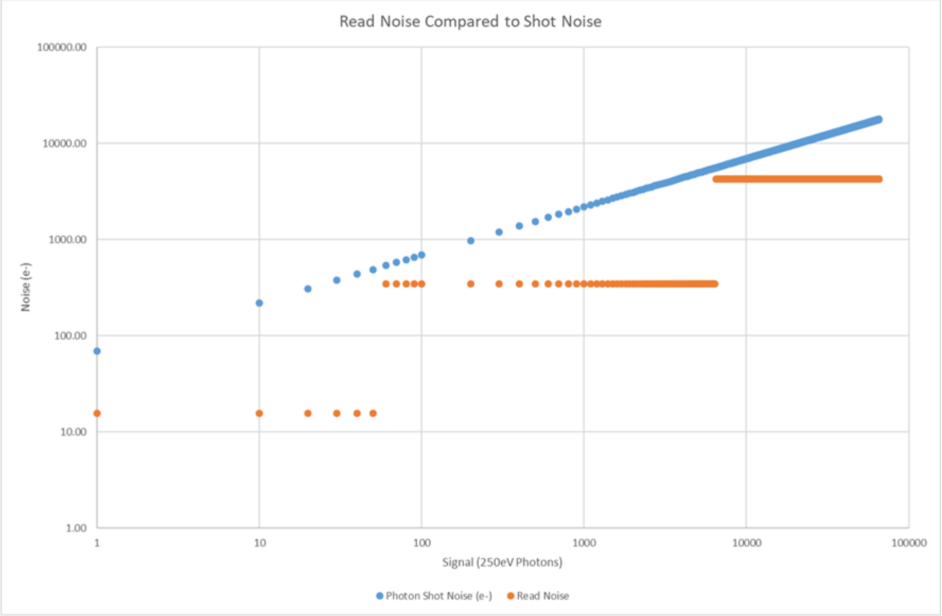
https://www.imagesensors.org/Past%20Workshops/2019%20Workshop/2019%20Papers/R34.pdf

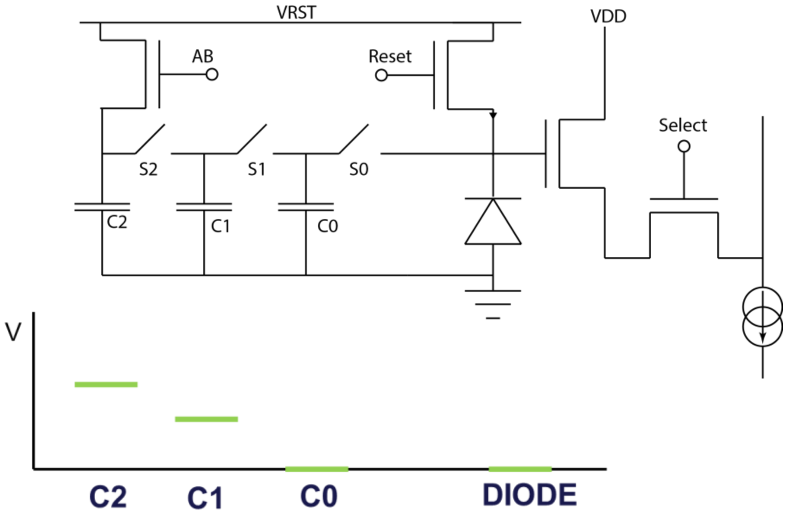
Standard Device Structures

High Dynamic Range - Example

- PERCIVAL
    - High Dynamic Range for Soft X-ray
    - Overflow structure allow noise level suitable for signal level
    - Keeps overall noise below shot noise







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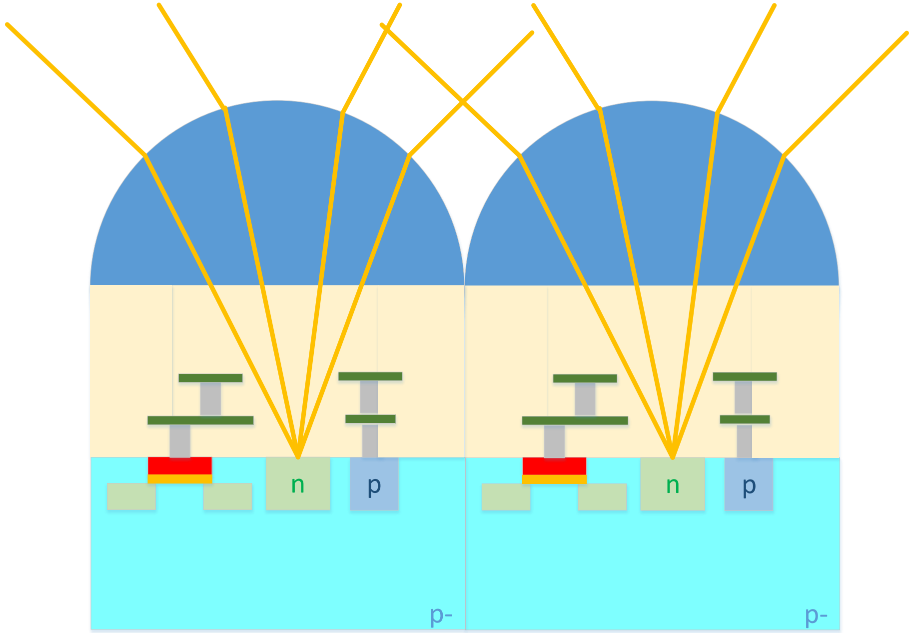
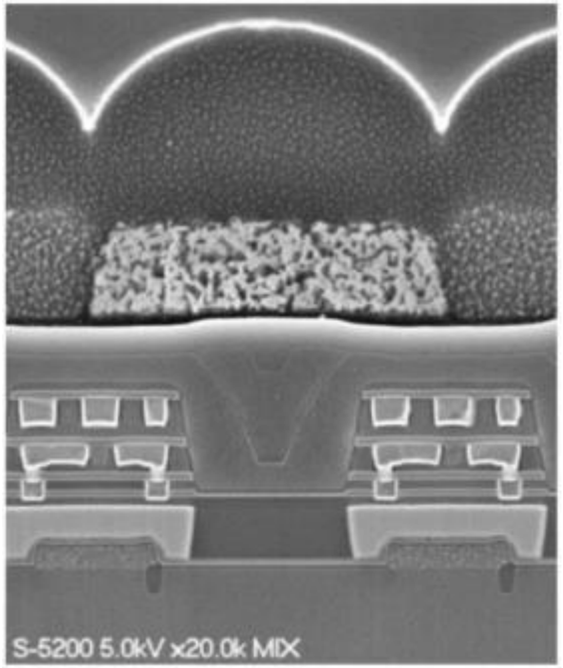
Standard Device Structures

Sensitivity Improvements - Microlenses

- Microlenses



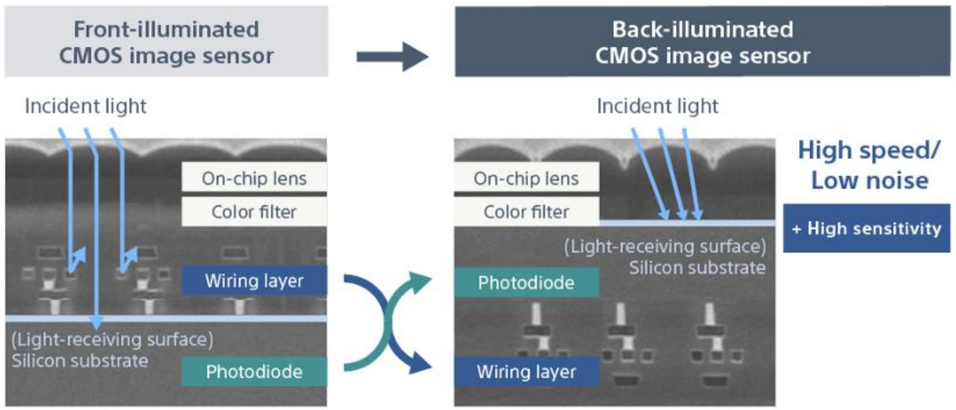


A High-Performance 2.5 µm Charge Domain Global Shutter Pixel and Near Infrared Enhancement with Light Pipe Technology, https://www.mdpi.com/1424-8220/20/1/307/htm

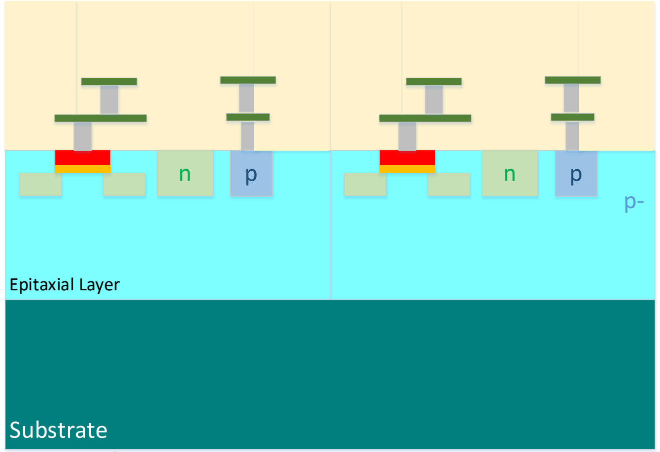
Standard Device Structures

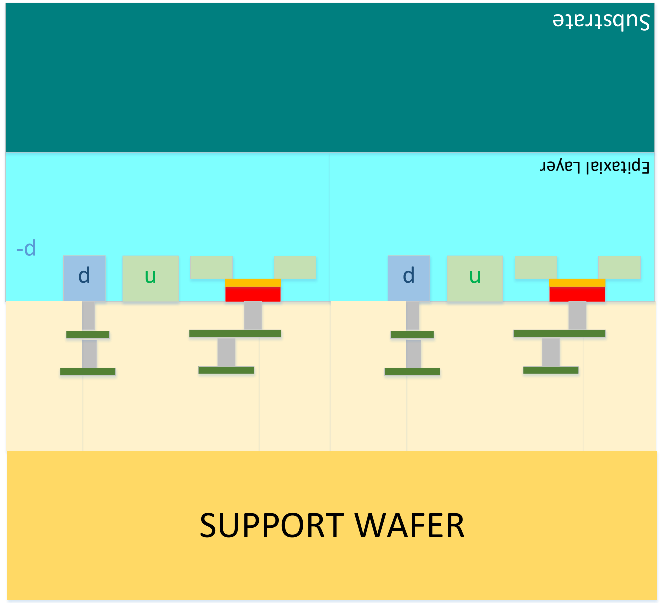
Sensitivity Improvements – Backside Illumination

- Flip Sensor
- Bond to support wafer
- Thin away substrate
- Vastly Improved QE

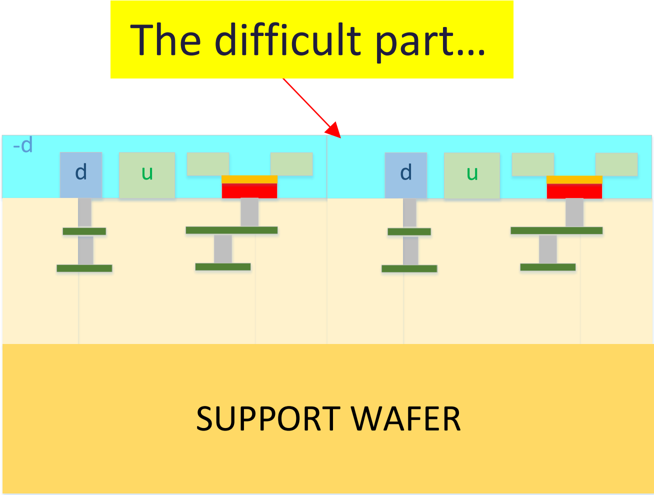


https://www.voltrium.com.sg/en/resources/bsi-vs-fsi-sensors-which-sensor-suits-your-needs/





The difficult part…



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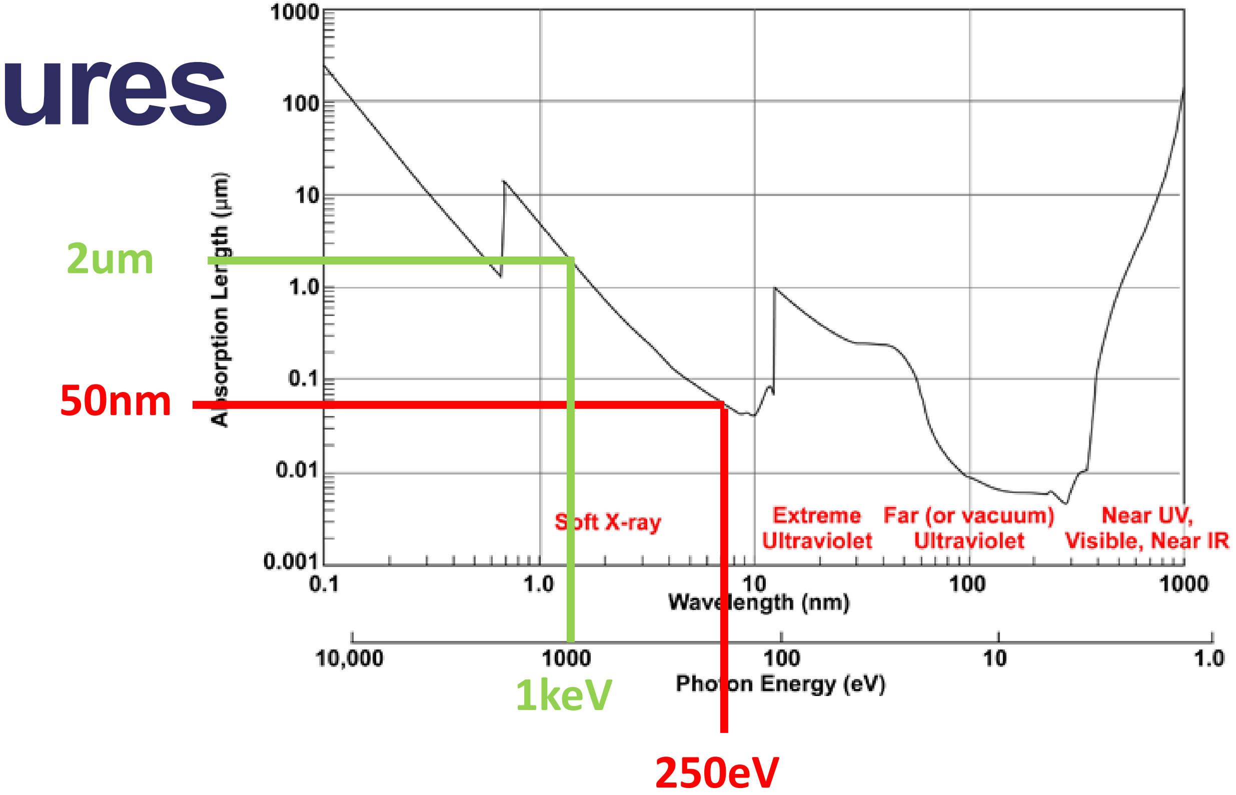
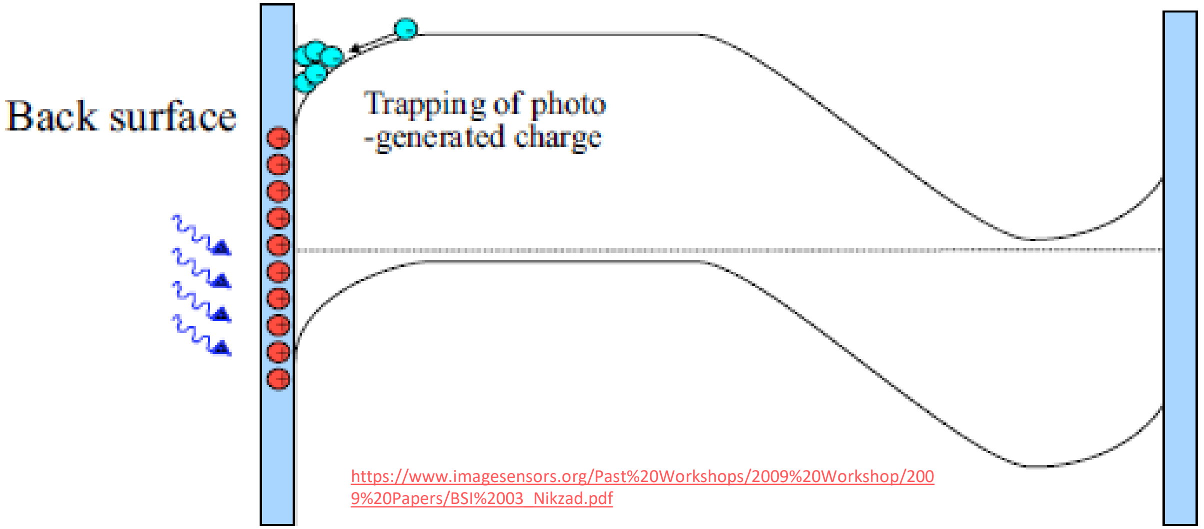
Standard Device Structures

Sensitivity Improvements – Backside Illumination

- Thinning into the epi leaves damage, traps, interface states
- This leads to lost charge, high dark current
- Several options to deal with this. All basically aim to:
    - Neutralise the traps
    - Place a positive charge at the back surface

http://www.ll.mit.edu/mission/electronics/AIT/hisensitivityimage.html





https://www.imagesensors.org/Past%20Workshops/2009%20Workshop/2009%20Papers/BSI%2003_Nikzad.pdf

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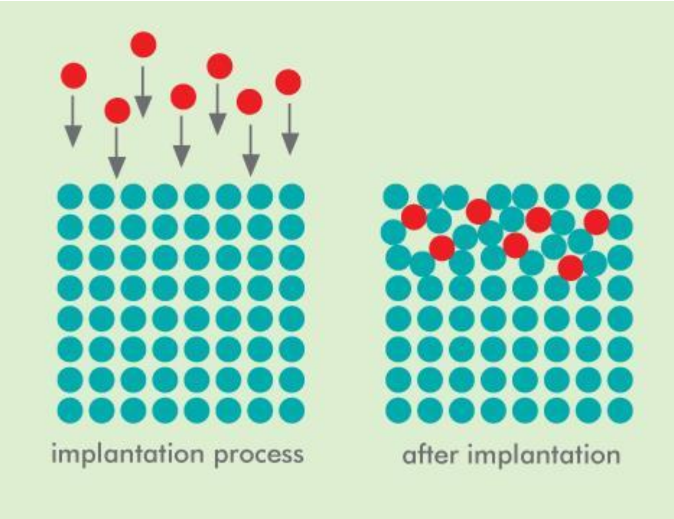
Standard Device Structures

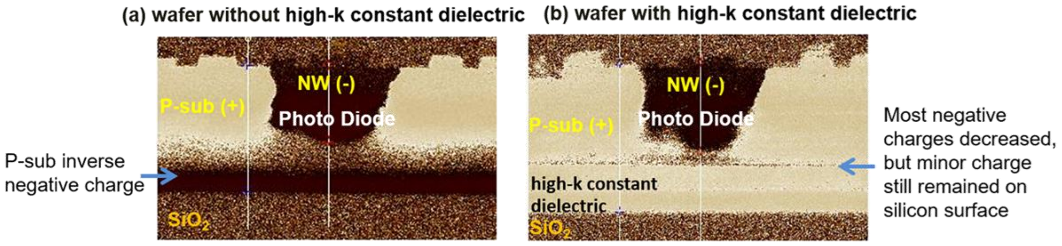
Sensitivity Improvements – Backside Illumination

Ion Implantation and Annealing



https://www.samaterials.com/content/an-overview-of-ion-implantation.html

High-k dielectric



**Remark: Dark for negative charge and Bright for positive charge*

FIG. 2. Charge distribution in the pixel structure (a) without HiK film and (b) with HiK film through SCM.

https://doi.org/10.1063/5.0006700

Hydrogen Annealing

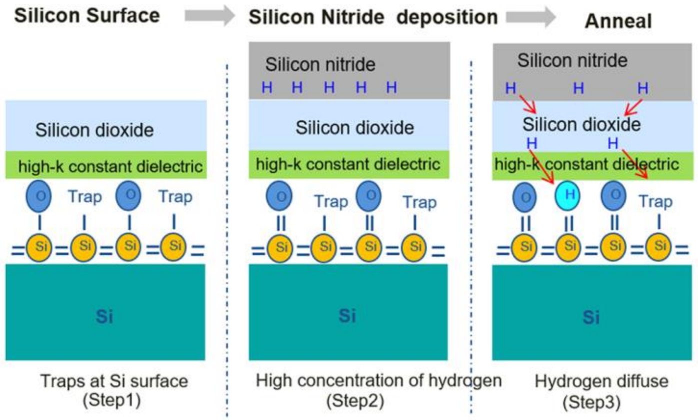
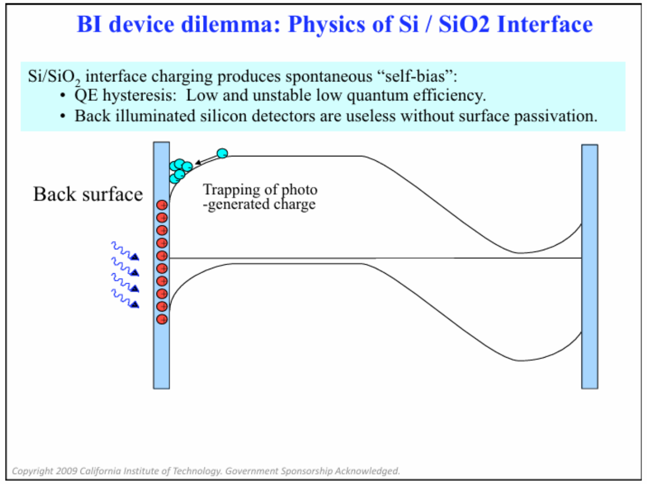


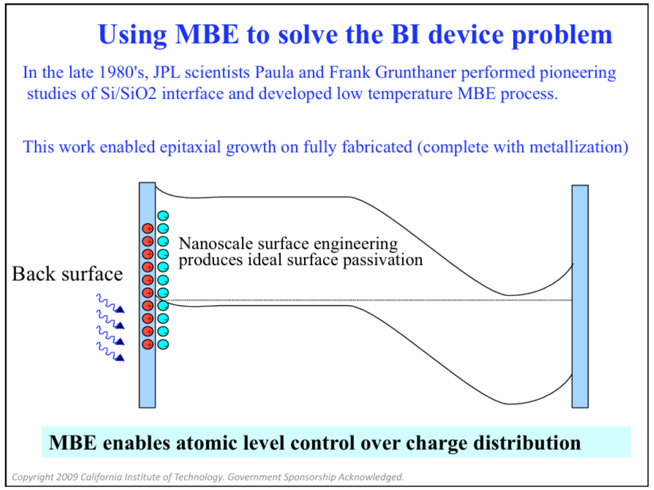
FIG. 6. Illustration of the hydrogen diffusion schemes during annealing.

Molecular Beam Epitaxy



BI device dilemma: Physics of Si / SiO2 Interface

Si/SiO_2 interface charging produces spontaneous "self-bias":
- QE hysteresis: Low and unstable low quantum efficiency.
- Back illuminated silicon detectors are useless without surface passivation.



Using MBE to solve the BI device problem

In the late 1980's, JPL scientists Paula and Frank Grunthaner performed pioneering studies of Si/SiO2 interface and developed low temperature MBE process.

This work enabled epitaxial growth on fully fabricated (complete with metallization)

MBE enables atomic level control over charge distribution

https://www.imagesensors.org/Past%20Workshops/2009%20Workshop/2009%20Papers/BSI%2003_Nikzad.pdf

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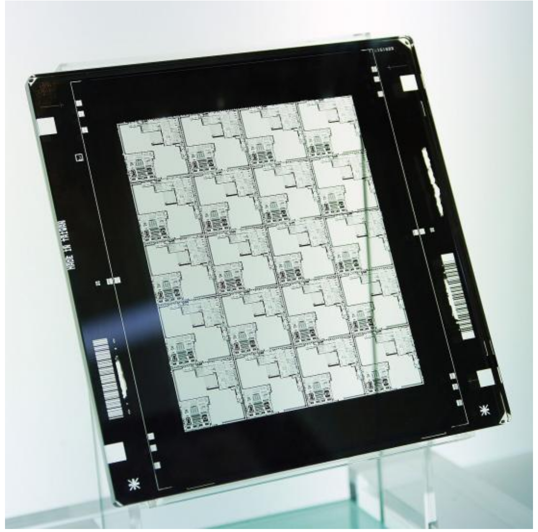
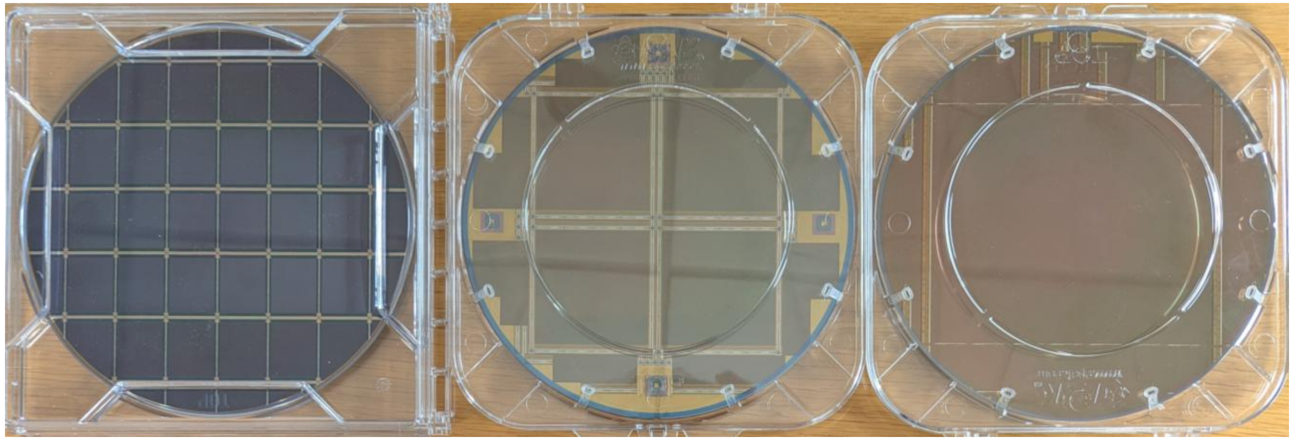
Standard Device Structures

Stitching

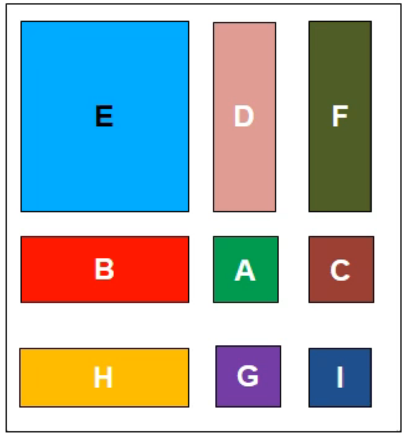
- Large area
- Works by sub-dividing mask and exposing repetitively



https://en.wikipedia.org/wiki/Photomask



Reticule sized (KIRANA) 4DPW (TEMAPS) 1DPW (C100)



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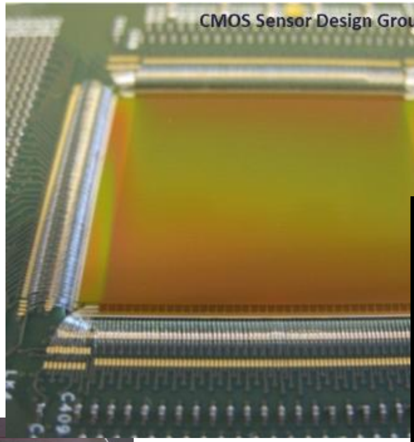
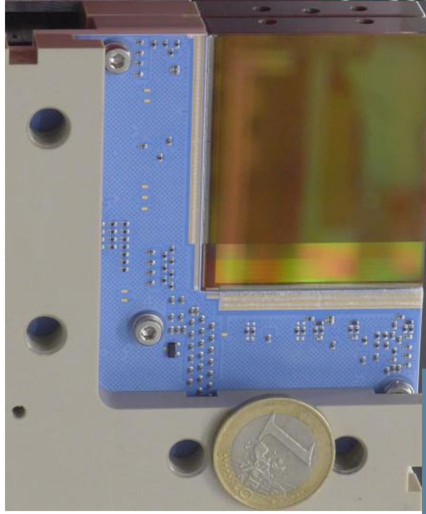
Standard Device Structures

Scientific Use

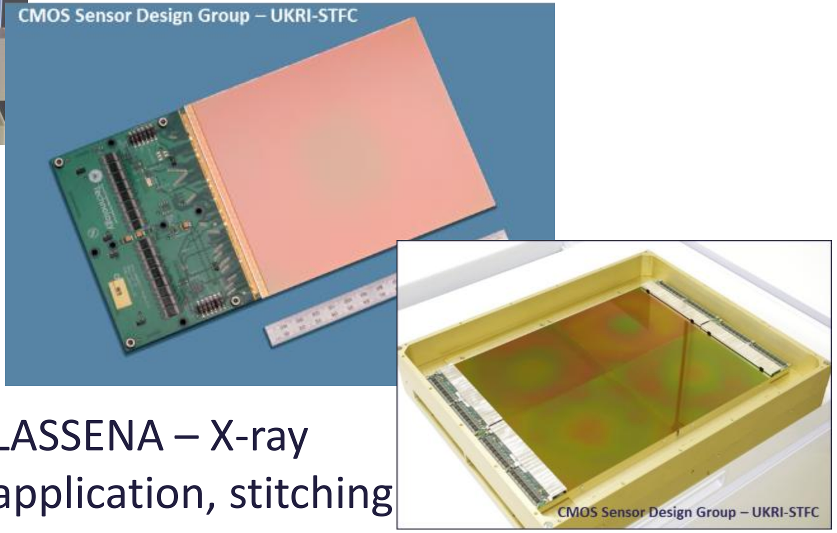
- Drivers for all these developments are high volume or high margin consumer, industrial and medical applications
- Are also useful in scientific applications, especially those using visible light
- However, more specialist advances are needed for some fields…



KIRANA – High speed imaging, microlenses



PERCIVAL – Low Energy X-ray, stitching, BSI



LASSENA – X-ray application, stitching

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Device Structures for Particle Physics

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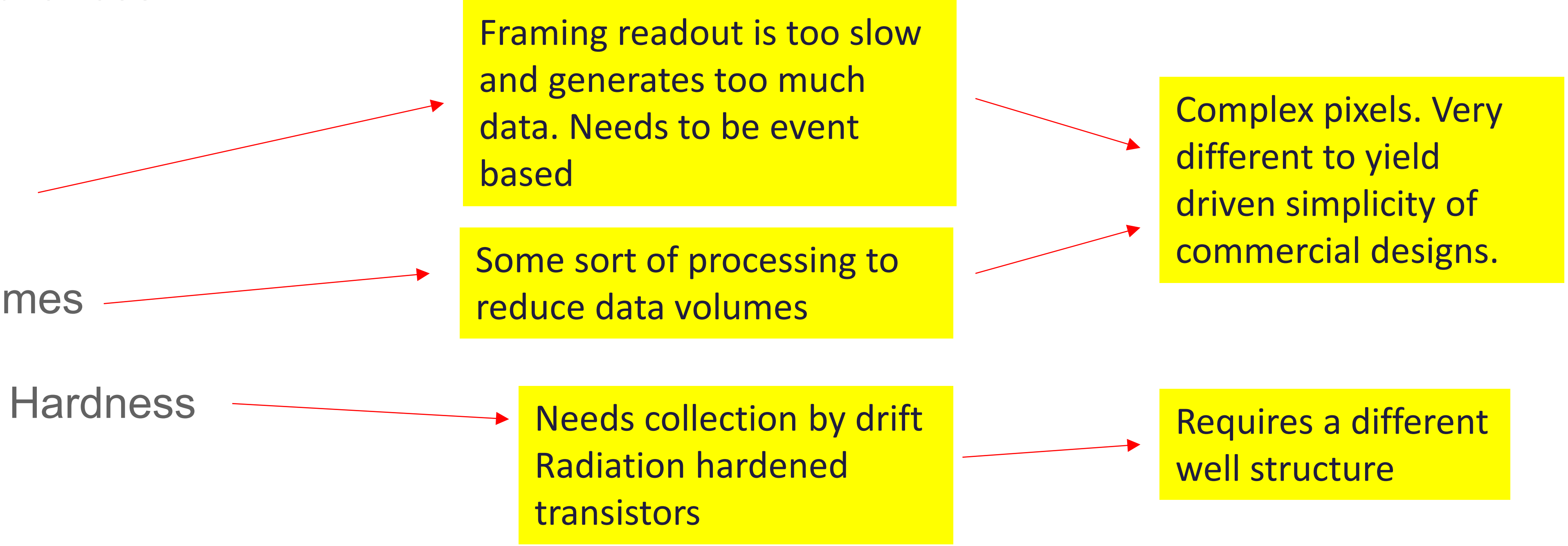
Device Structures in Particle Physics

Challenges

- Particle (and nuclear) physics have unique challenges not necessarily addressed by commercial advances
- Particularly:
  - Timing
  - Data Volumes
  - Radiation Hardness



Framing readout is too slow and generates too much data. Needs to be event based

Some sort of processing to reduce data volumes

Complex pixels. Very different to yield driven simplicity of commercial designs.

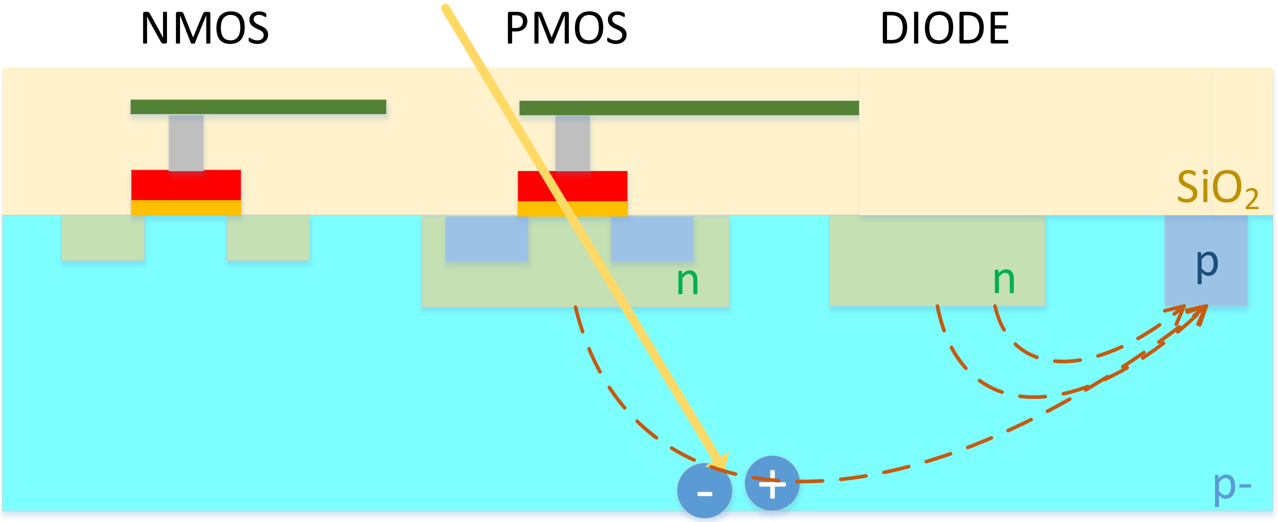
Needs collection by drift Radiation hardened transistors

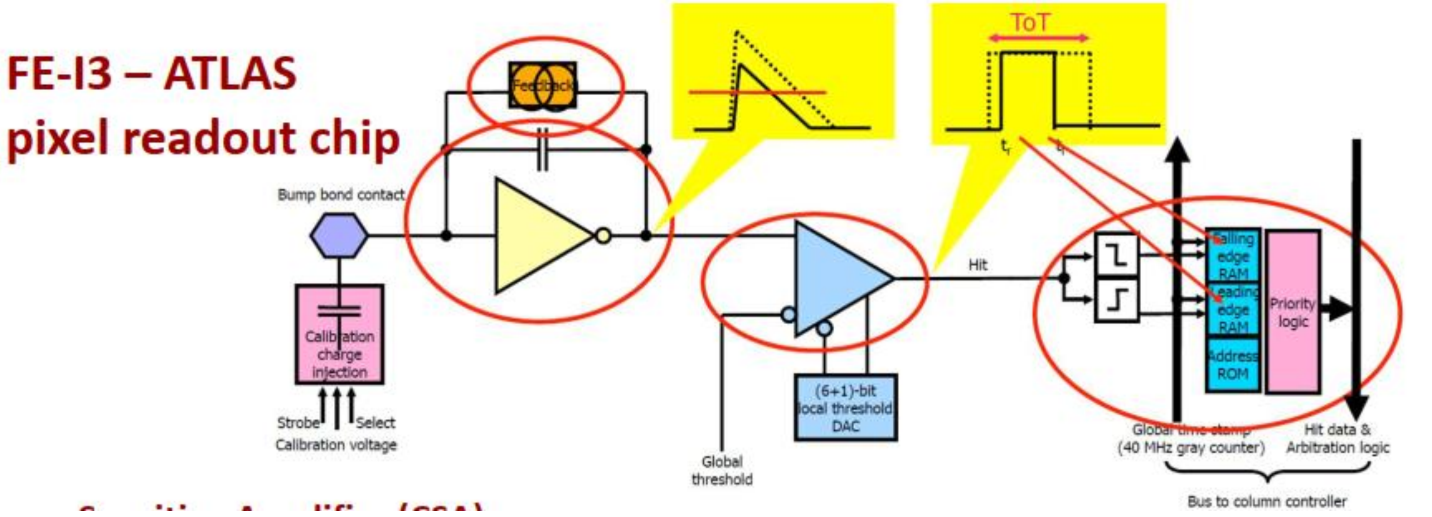
Requires a different well structure

Device Structures in Particle Physics

Typical Pixel Structure

- Normally includes:
  - Charge Sensitive Amplifier
  - Pulse Shaping
  - Comparator
  - Digital Logic
- Note challenges compared to previous structures:
  - Many (>20) transistors/pixel
  - PMOS Transistors





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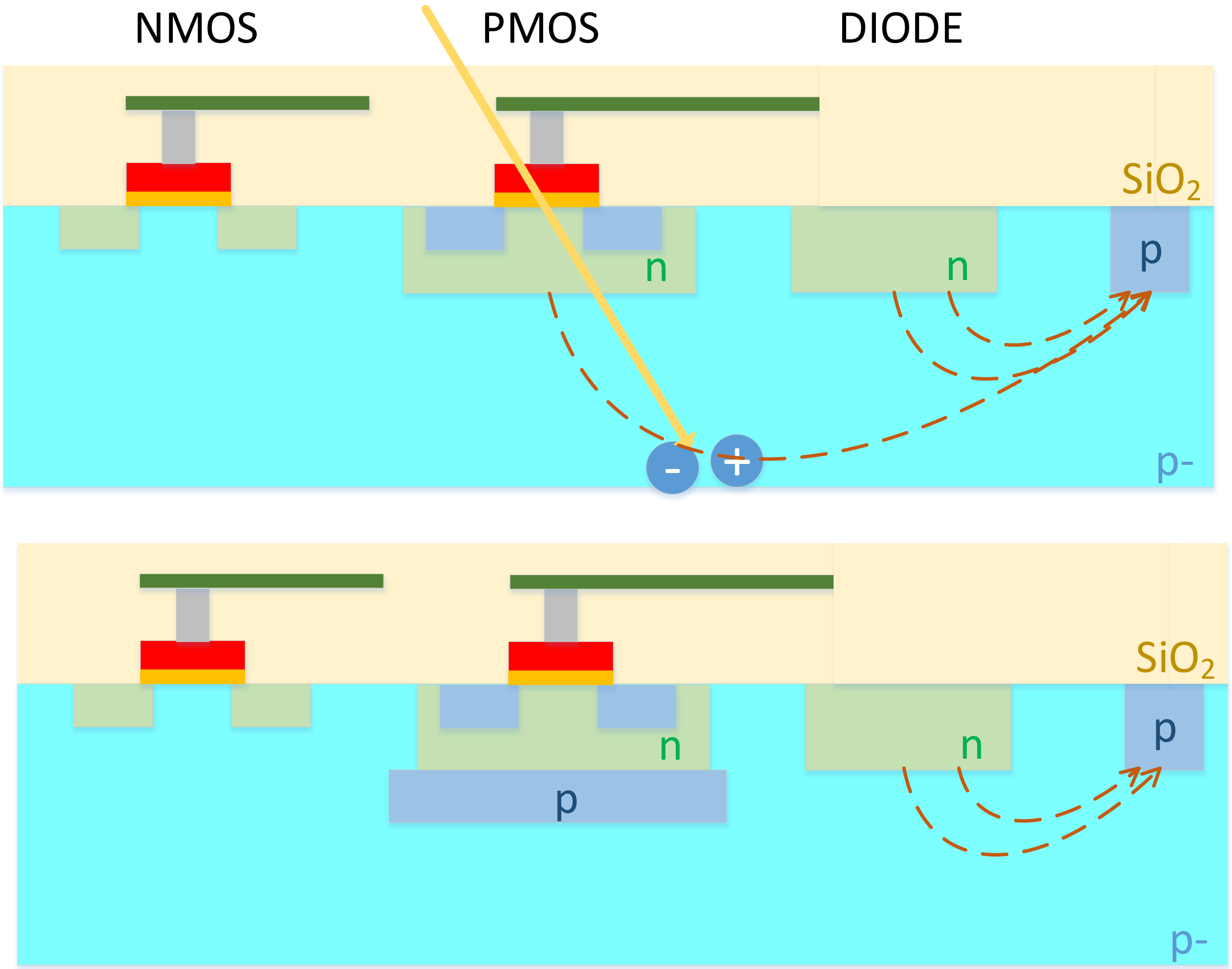
Device Structures in Particle Physics

Efficiency in Complex Pixels

- N-well under PMOS transistors acts as a parasitic collector
- Can shield this with a deeper P layer
- Often exists in foundry processes for other reasons
- Has been commonplace in MAPS design for some years (ref)



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Karol’s Lecture

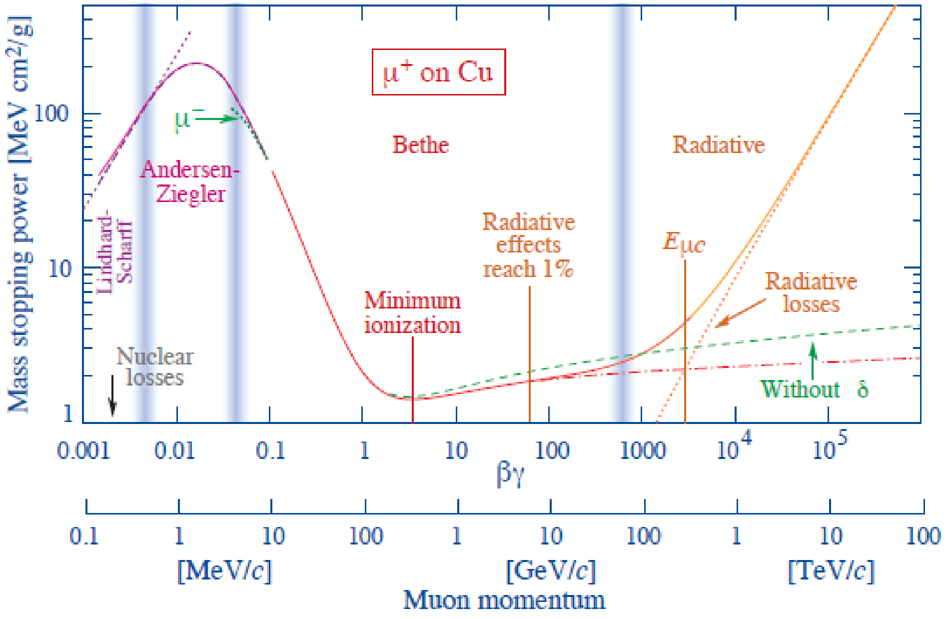
Device Structures in Particle Physics

Thick Epitaxial Layer

- CIS processes are typically epitaxial, with a thin sensitive region
- However, MIPS deposit charge per interaction length
- X-Ray mean free path increases rapidly with energy
- Detectors then typically have epi thicknesses up to 25 or even several hundred um

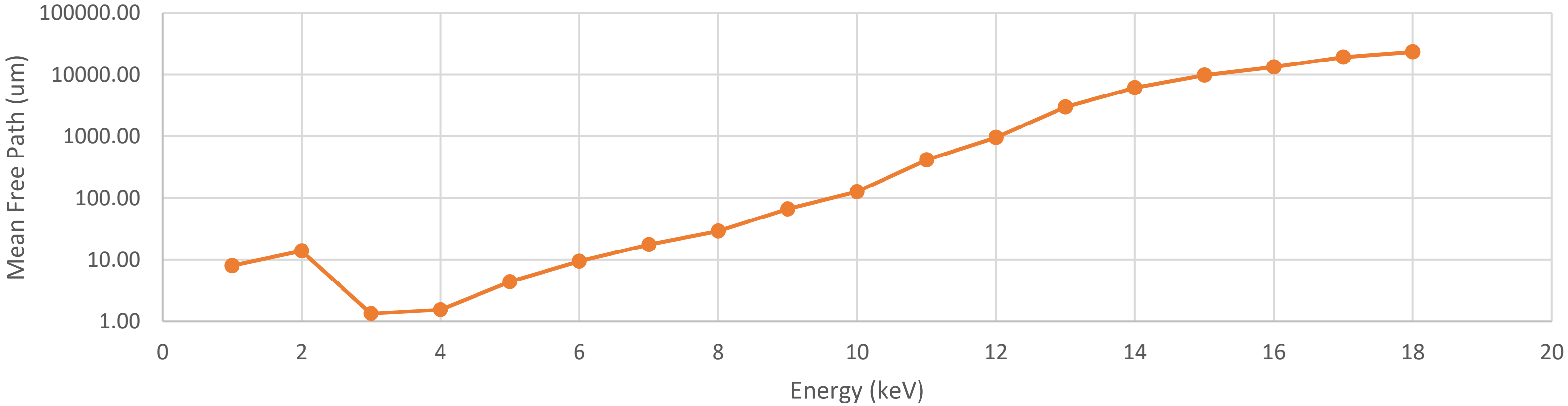
- Generates ~80e-h pairs/um (~2MeV cm2*g /2.32g/cm3)
- 5um epi = 400e-
- 18um epi = 1440e-

Particle Data Group PDG, Passage of particles through matter, Nuclear and Particle Physics, vol. 33, no. 27, pp. 258-270, July 2006.



https://www.physics.nist.gov/PhysRefData/Xcom/html/xcom1.html

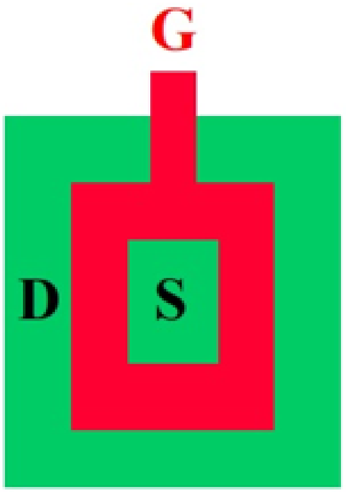
Mean

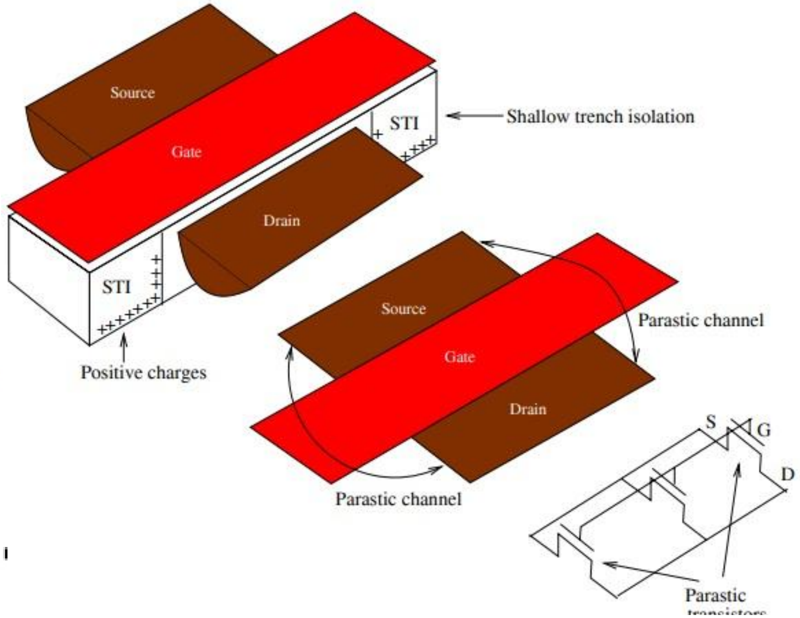


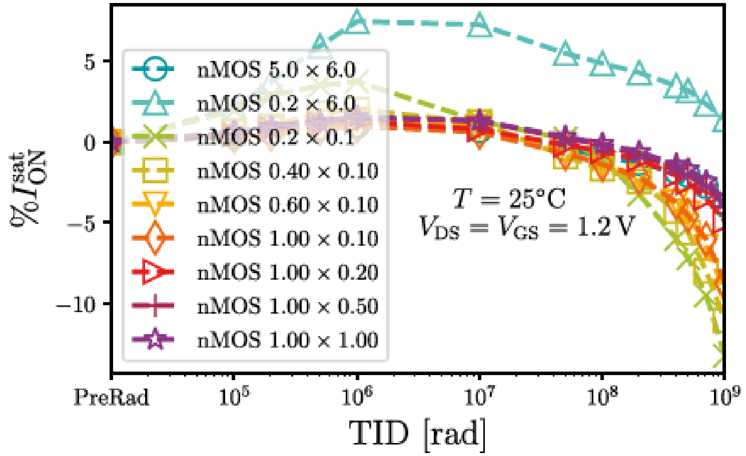
Device Structures in Particle Physics

Total Ionising Dose (TID) Damage

- Radiation interaction leads to a build up of positive charge in the oxide
- Can effectively create a parasitic transistor, leading to increased leakage current and eventually failure
- ***Broadly*** speaking, lower nodes with thinner oxides show this effect less
- Can also be mitigated with Enclosed Layout Transistors and larger devices
- End result is that this can largely be mitigated by design and process choice. Results up to 1Grad have been shown in CIS processes





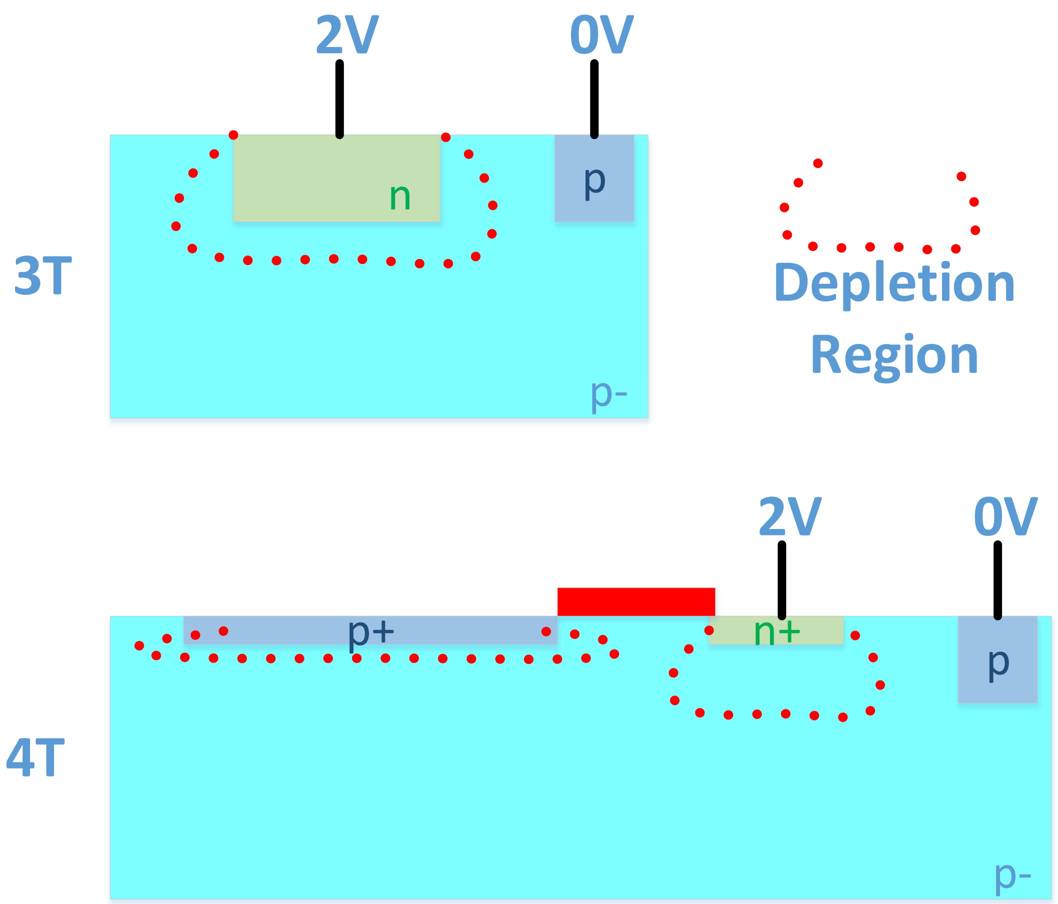


http://doi.org/10.1088/1748-0221/18/02/C02036

Device Structures in Particle Physics

Bulk Damage

- More complex to solve than TID
- Collection in a commercial CIS is mostly by diffusion, thanks to the low electric fields and small depletion regions involved
- However, bulk damage from NIEL can cause traps in the epi
- Charge generated by MIPS will be absorbed in these traps unless it is collected quickly
- Collection needs to be by drift for high resistance to NIEL damage.
- How?



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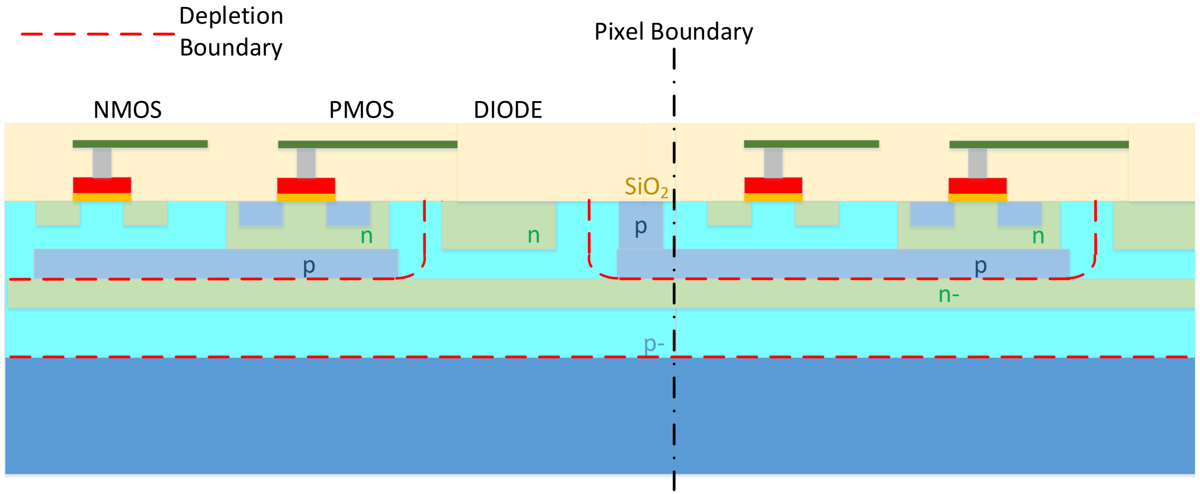
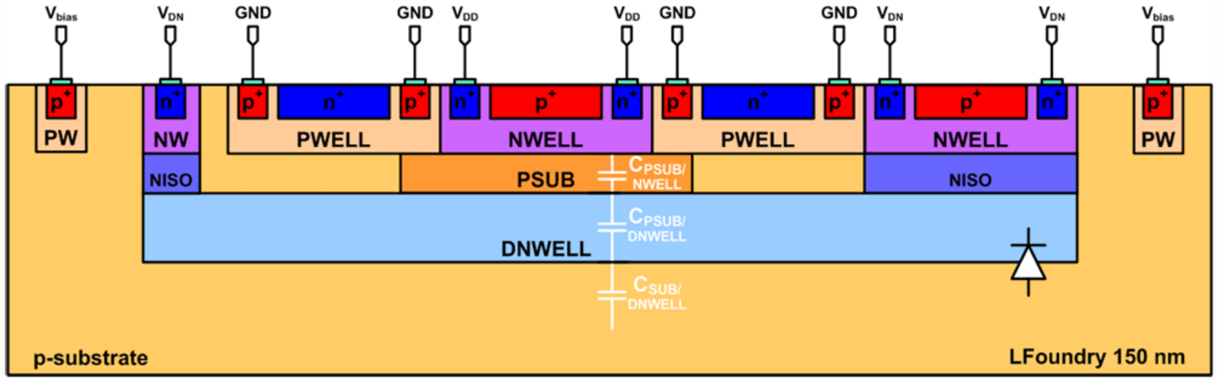
Device Structures in Particle Physics

Bulk Damage - Full Depletion

- Two options exist, both of which work by using a fully depleted epi layer:
  - Small collection electrode
    - Low dose deep n-implant used to achieve full depletion at low voltage
  - Large collection electrode
    - Electronics sits inside large collection electrode. High voltages used to deplete.



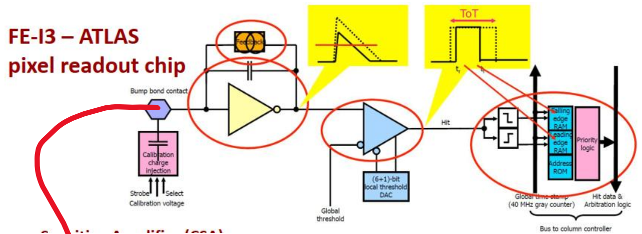


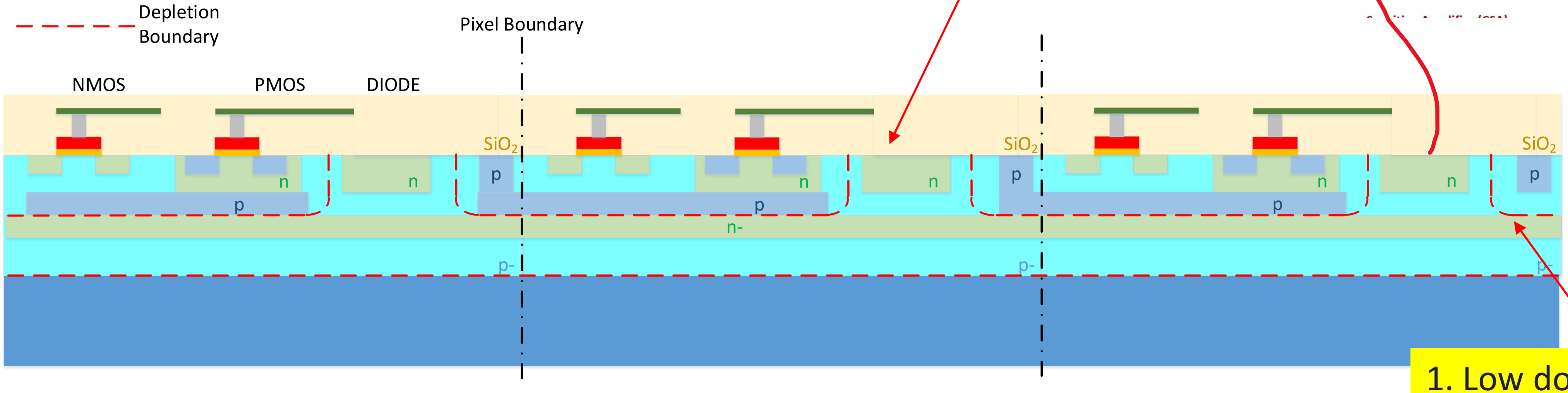
Device Structures in Particle Physics

Bulk Damage - Small Collection Electrode

- Developed by CERN in the TJ 180nm process (ref)
- Since ported to the TPSCo 65nm process (ref)

2. Low voltage on collection electrode needed to deplete





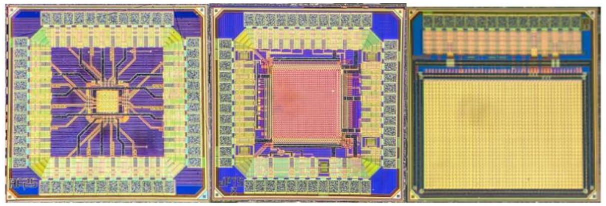
1. Low dose N-implant added to process

- Small collection electrode, hence low detector capacitance
- Higher input referred noise can therefore be tolerated
- Implies lower gm, hence lower bias current, hence lower power of the front end
- Since collection node is small, drift paths can be long unless pixel is small -> worse radiation tolerance
- Implies smaller pixels to compensate, which can mitigate to some extent the power advantage

Device Structures in Particle Physics

Bulk Damage - Small Collection Electrode

- Development from the non-fully depleted process used for ALPIDE
- Started in the TJ 180nm process and now in TPSco 65nm
- Currently finding application in the MOSAIX chip for the ALICE ITS3 upgrade (which is also stitched!)



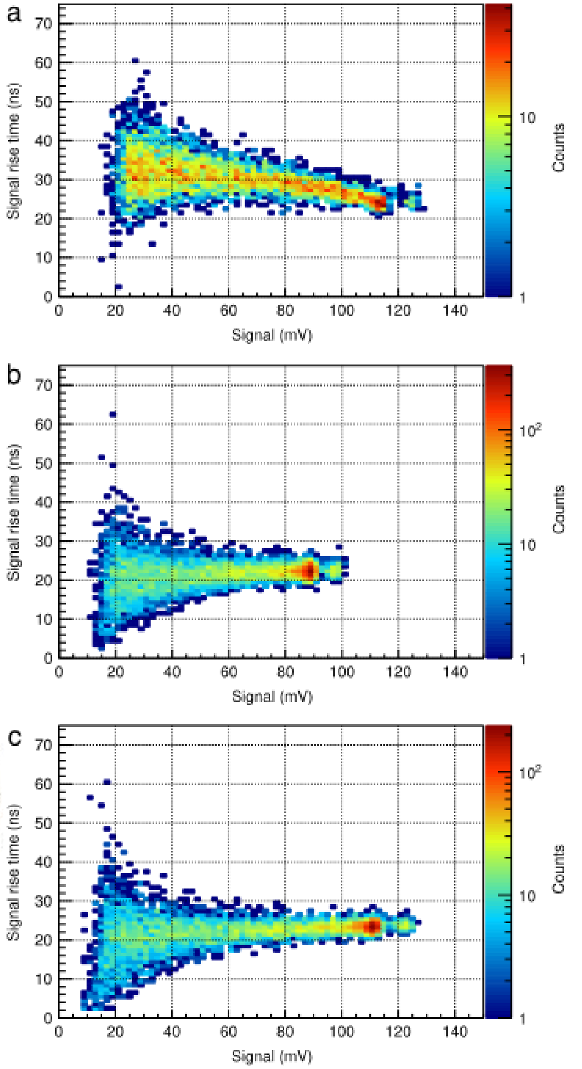


Fig. 8. (color online). Measured charge collection time at room temperature versus signal from a ^{55}Fe radioactive source for standard (a) and modified process with higher (b) and lower (c) dose for the low dose implant [19,20].

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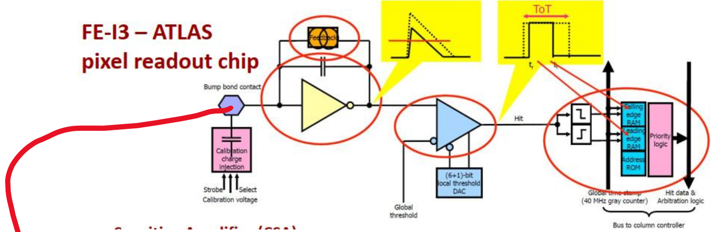
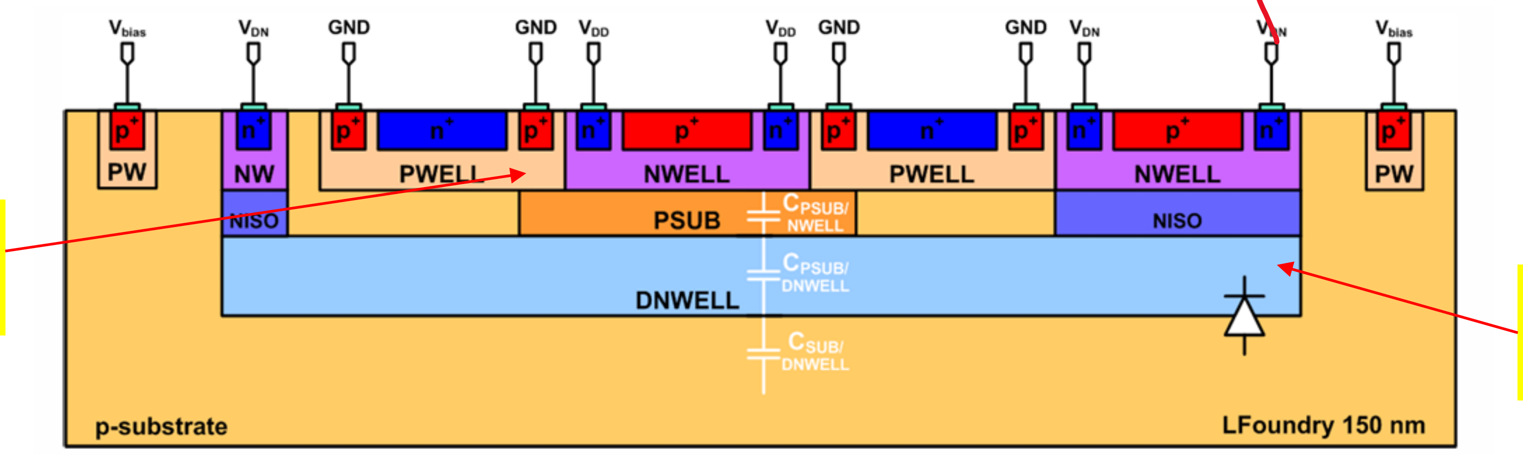
http://doi.org/10.1016/j.nima.2017.07.046
http://doi.org/10.22323/1.420.0083
https://doi.org/10.1016/j.nima.2026.171297

Device Structures in Particle Physics

Bulk Damage - Large Collection Electrode

- Several examples – AMS (TSI) and LFoundry 150nm


FE-I3 – ATLAS pixel readout chip



1. Electronics contained in well

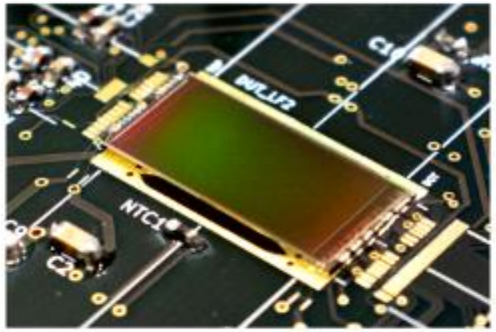
1. Large deep N-well used as collecting node

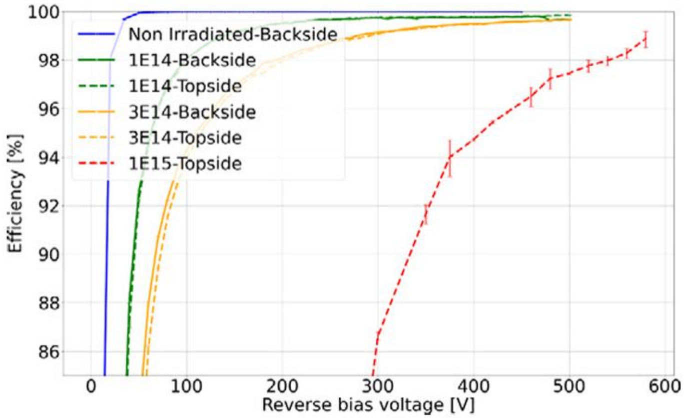
- Large collection electrode, hence high detector capacitance
- Need low input referred noise
- Implies higher gm, hence higher bias current, hence higher power of the front end
- Since collection node is large, drift paths are short even for large pixels -> better radiation tolerance

Device Structures in Particle Physics

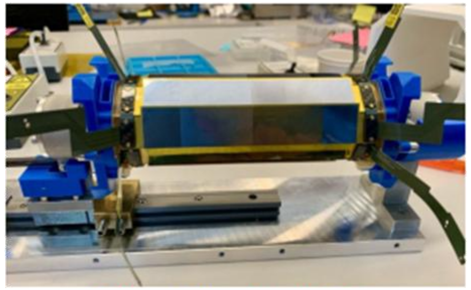
Bulk Damage - Large Collection Electrode

- Several examples – Mu3e, ATLASPix, RD50, LFMonopix
- AMS/TSI, LFoundry

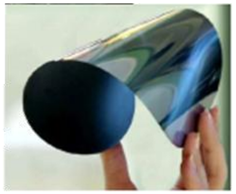


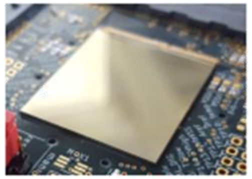


https://doi.org/10.1016/j.nima.2025.170752

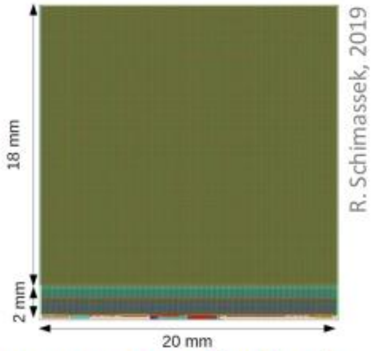


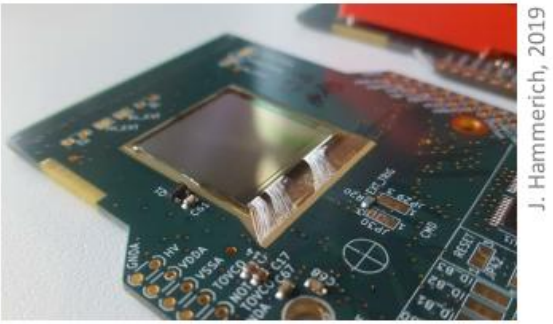
Mu3e pixel tracking detector





MuPix11



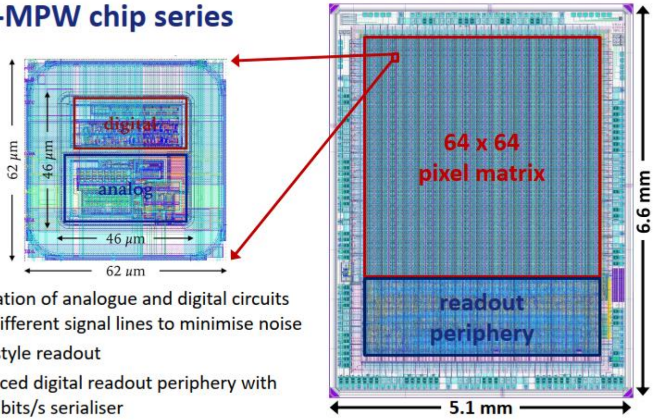


ATLASPix3 – Some chip details

- Matrix with 132 columns x 372 rows
- 150 µm x 50 µm pixel size
- Trigger latency ≤ 25 µs
- Radiation hard design
- Serial powering (only one power supply needed)
- Data interface is very similar to ATLAS RD53 readout chip
- Power consumption is ~200 mW/cm² (with 25 ns time resolution)

ATLASPix3 is the first full reticle pixel detector (2 cm x 2 cm) compatible with ATLAS ITk L4 requirements

RD50-MPW chip series



- Separation of analogue and digital circuits with different signal lines to minimise noise
- FE-I3 style readout
- Advanced digital readout periphery with 640 Mbits/s serialiser

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Summary

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Summary

Summary

- Huge investment in CMOS in general and CIS in particular has provided a vast amount of technology for scientific imaging
- Further niche developments have expanded this to other fields beyond commercial applications
- New and exciting developments all the time!

This X-ray video is taken using the Lassena Wafer Scale CMOS sensor developed by STFC. Four sensors were used here and combined into a single detector. The sensors are 12 cm x 14 cm, 6.7 MPixels and can operate at 30 frames per second. This results in the whole detector having 26.8 MPixels and an area of 24 cm x 28 cm. The detector can generate 1.5 GB of images per second. The image sensors are inefficient at detecting X-rays, therefore a Scintillator is used as the X-ray detection medium. The X-rays are converted into 550 nm light by the scintillator that is then detected by the image sensor. The scintillator used in this detector is Caesium Iodide doped with Thallium.

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Questions?

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Thank you

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