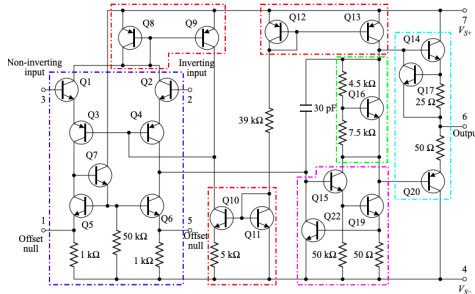
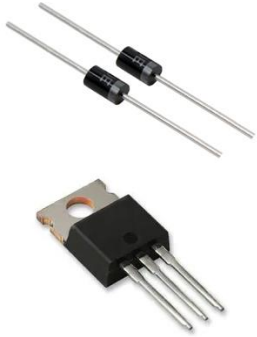


# Introduction into Electronics

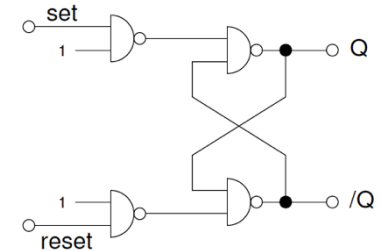
- (1) Reminder: Electrical circuits
- (2) Analog electronics
- (3) Digital electronics
- (4) Circuit analysis, circuit topologies



## Literature:

Paul Horowitz, Winfield Hill  
The Art of Electronics  
Cambridge University Press (2015)

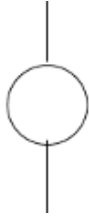
D. Sundararajan  
Introductory Circuit Theory  
Springer (2019)



## (1) Reminder: Electrical circuits

# Basic elements

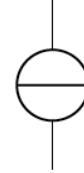
**Power source:**



DC voltage  
source:



DC current  
source:



AC source:

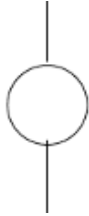
$$U(t) = U_0 \sin(\omega t)$$

$$\hat{U} = U_{\text{eff}} = U_0 / \sqrt{2}$$

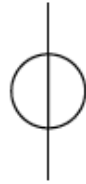


# Basic elements

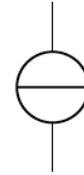
Power source:



DC voltage source:



DC current source:



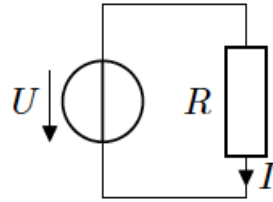
AC source:

$$U(t) = U_0 \sin(\omega t)$$

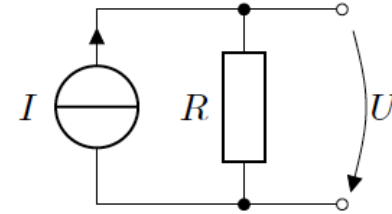
$$\hat{U} = U_{\text{eff}} = U_0 / \sqrt{2}$$



Resistance:

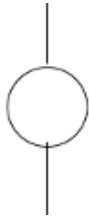


$$U = R \cdot I.$$

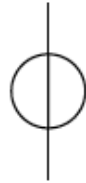


# Basic elements

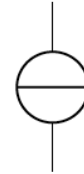
Power source:



DC voltage source:



DC current source:



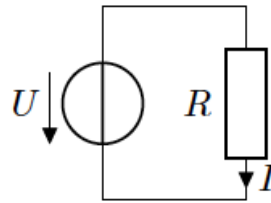
AC source:

$$U(t) = U_0 \sin(\omega t)$$

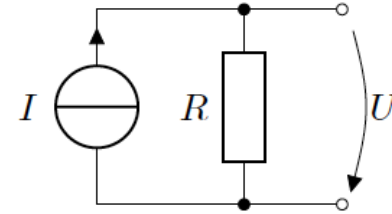
$$\hat{U} = U_{\text{eff}} = U_0 / \sqrt{2}$$



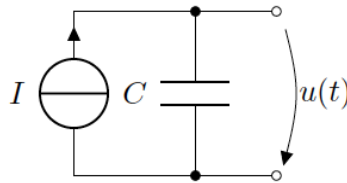
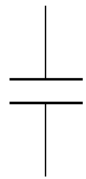
Resistance:



$$U = R \cdot I.$$



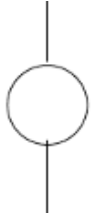
Capacitance:



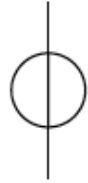
$$Q = C \cdot U \quad i(t) = \frac{dq}{dt} = C \cdot \frac{du}{dt}$$

# Basic elements

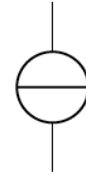
Power source:



DC voltage source:



DC current source:



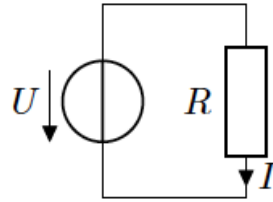
AC source:

$$U(t) = U_0 \sin(\omega t)$$

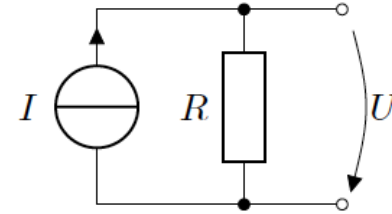
$$\hat{U} = U_{\text{eff}} = U_0 / \sqrt{2}$$



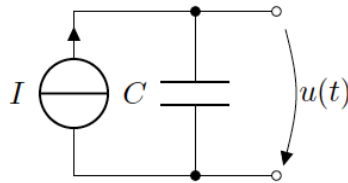
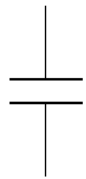
Resistance:



$$U = R \cdot I$$

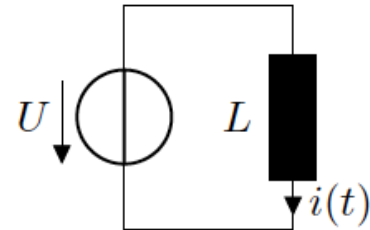
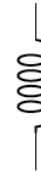


Capacitance:



$$Q = C \cdot U \quad i(t) = \frac{dq}{dt} = C \cdot \frac{du}{dt}$$

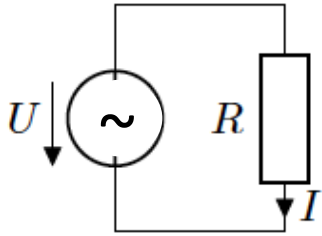
Inductance:



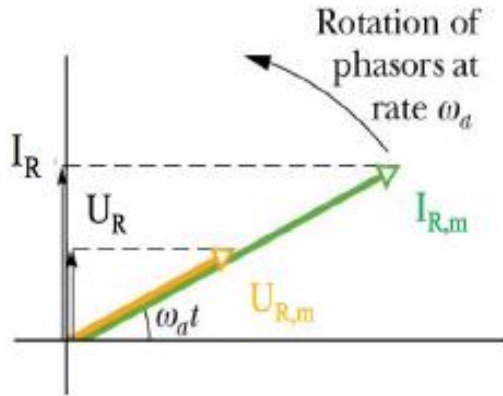
$$u(t) = L \frac{di}{dt}$$

# AC resistance (reactance)

Resistance:

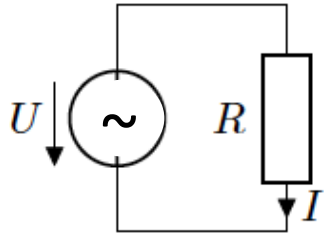


$$I_R = \frac{U_R}{R}$$

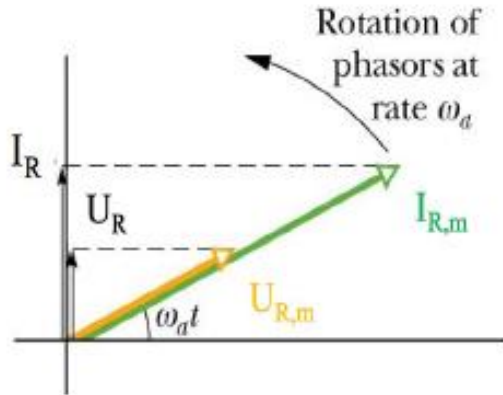


# AC resistance (reactance)

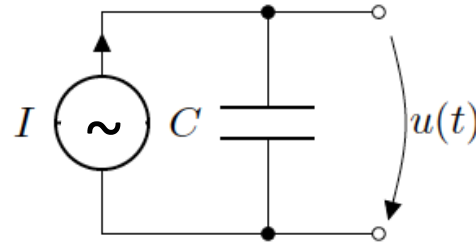
## Resistance:



$$I_R = \frac{U_R}{R}$$

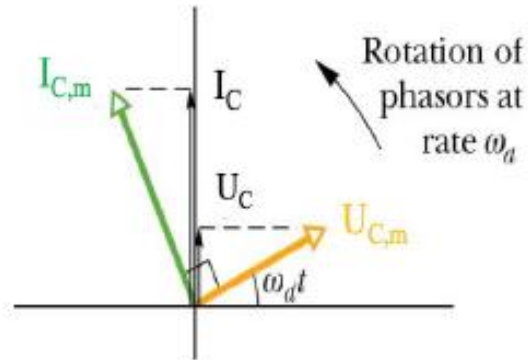


## Capacitance:



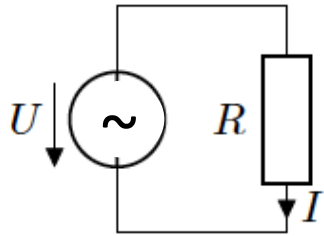
$$\hat{U}_C = \hat{I}_C X_C$$

$$X_C = -\frac{1}{i\omega C}$$

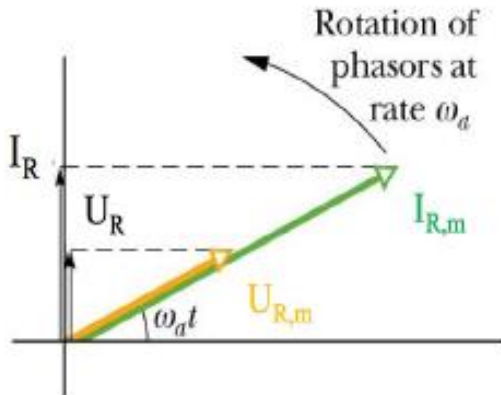


# AC resistance (reactance)

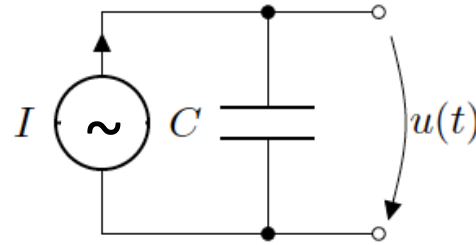
## Resistance:



$$I_R = \frac{U_R}{R}$$

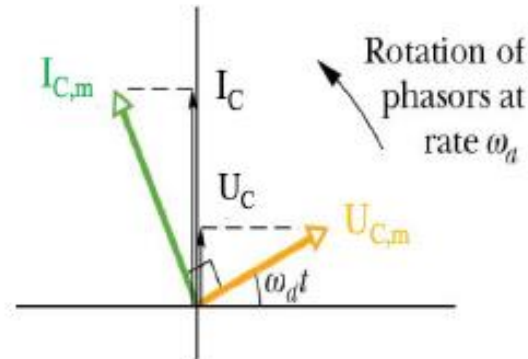


## Capacitance:

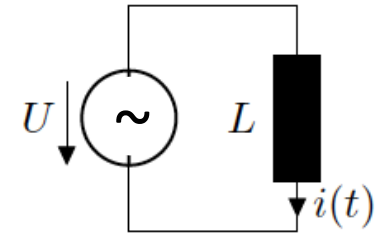


$$\hat{U}_C = \hat{I}_C X_C$$

$$X_C = -\frac{1}{i\omega C}$$

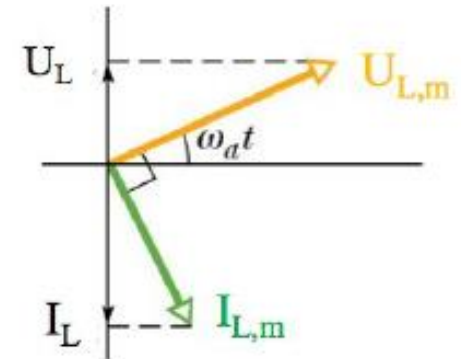


## Inductance:



$$\hat{U}_L = \hat{I}_L X_L$$

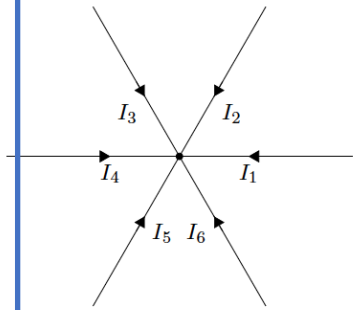
$$X_L = i\omega L$$



# Networks (more later)

**Junction rule:**

$$\sum_{k=1}^n I_k = 0$$

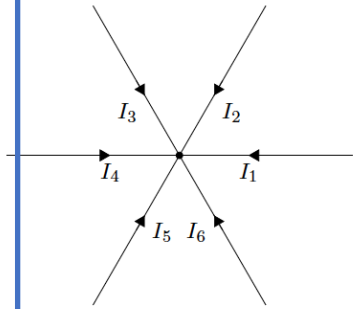


$$X_C = \frac{1}{i\omega C}$$

# Networks (more later)

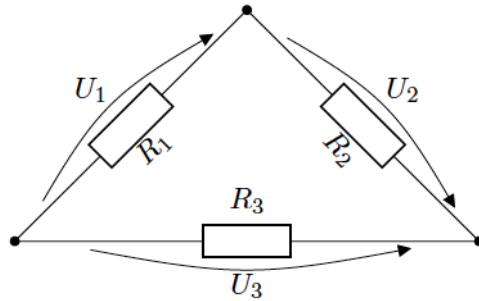
**Junction rule:**

$$\sum_{k=1}^n I_k = 0$$



**Loop rule**

$$\sum_{k=1}^n U_k = 0$$

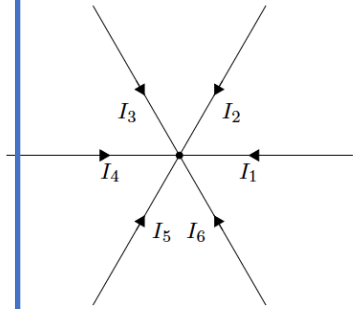


$$X_C = \frac{1}{i\omega C}$$

# Networks (more later)

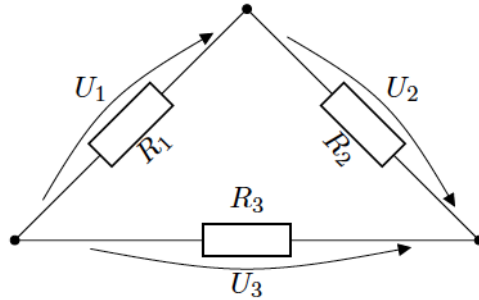
## Junction rule:

$$\sum_{k=1}^n I_k = 0$$

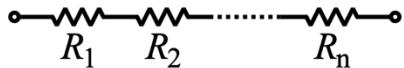


## Loop rule

$$\sum_{k=1}^n U_k = 0$$



## Resistance in series:

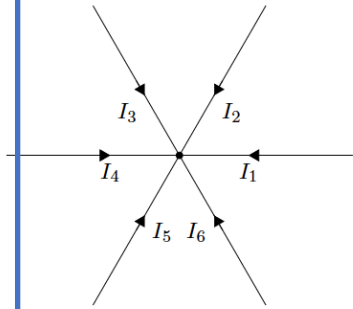


$$R_{\text{total}} = R_s = R_1 + R_2 + \dots + R_n$$

# Networks (more later)

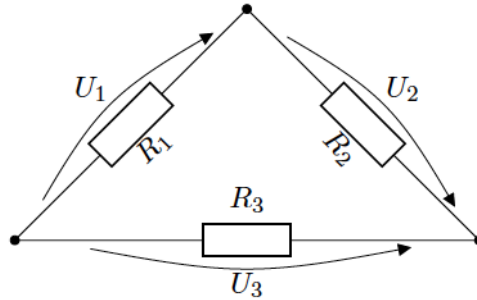
## Junction rule:

$$\sum_{k=1}^n I_k = 0$$

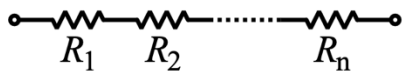


## Loop rule

$$\sum_{k=1}^n U_k = 0$$

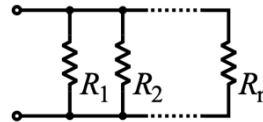


## Resistance in series:



$$R_{\text{total}} = R_s = R_1 + R_2 + \dots + R_n$$

## Resistance in parallel:

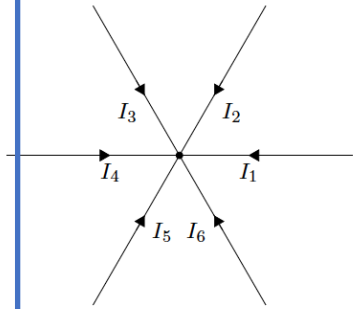


$$\frac{1}{R_{\text{total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}$$

# Networks (more later)

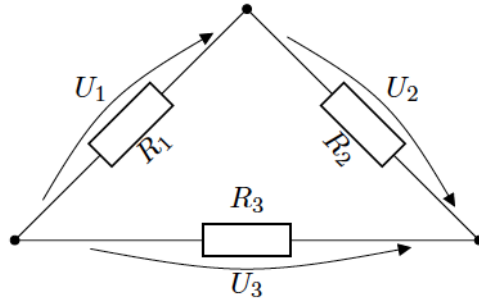
## Junction rule:

$$\sum_{k=1}^n I_k = 0$$

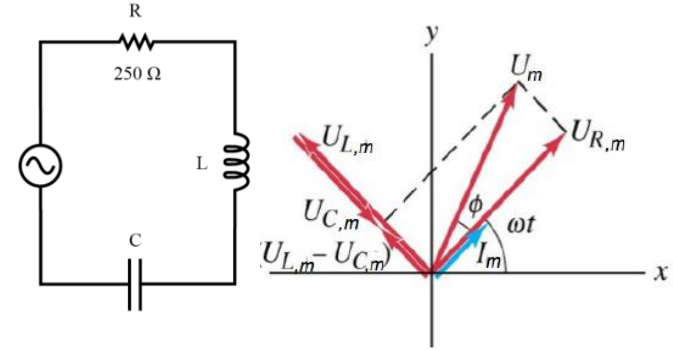


## Loop rule

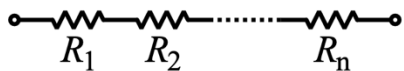
$$\sum_{k=1}^n U_k = 0$$



## Impedance in AC circuits

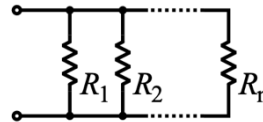


## Resistance in series:



$$R_{\text{total}} = R_s = R_1 + R_2 + \dots + R_n$$

## Resistance in parallel:

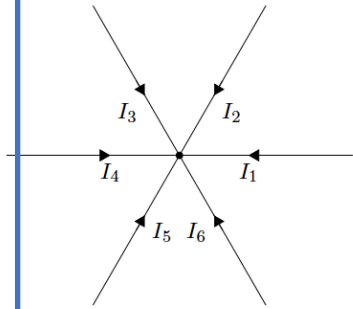


$$\frac{1}{R_{\text{total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}$$

# Networks (more later)

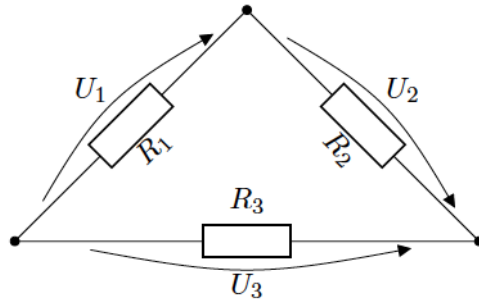
## Junction rule:

$$\sum_{k=1}^n I_k = 0$$

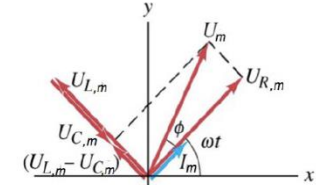
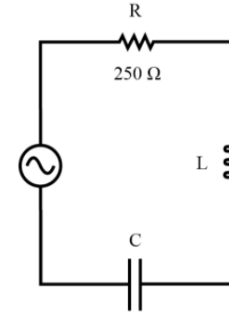


## Loop rule

$$\sum_{k=1}^n U_k = 0$$



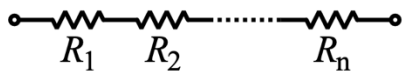
## Impedance in AC circuits



Impedance Z:

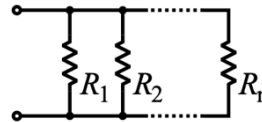
$$Z = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \quad \hat{I} = \frac{\hat{U}}{Z}$$

## Resistance in series:



$$R_{\text{total}} = R_s = R_1 + R_2 + \dots + R_n$$

## Resistance in parallel:

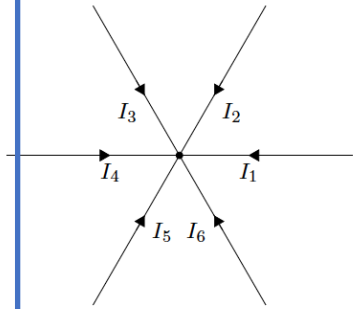


$$\frac{1}{R_{\text{total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}$$

# Networks (more later)

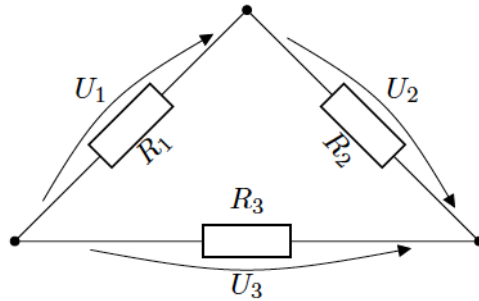
## Junction rule:

$$\sum_{k=1}^n I_k = 0$$

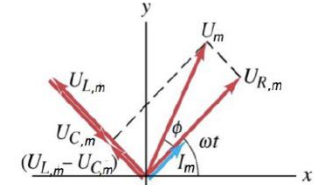
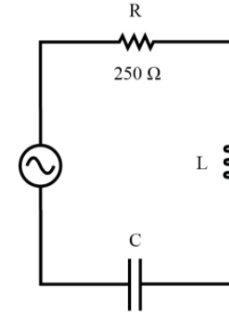


## Loop rule

$$\sum_{k=1}^n U_k = 0$$



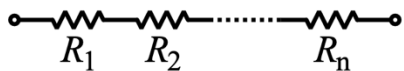
## Impedance in AC circuits



Impedance Z:

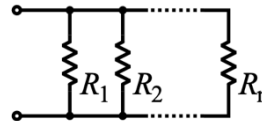
$$Z = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \quad \hat{I} = \frac{\hat{U}}{Z}$$

## Resistance in series:



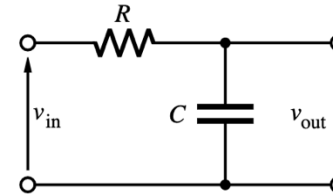
$$R_{\text{total}} = R_s = R_1 + R_2 + \dots + R_n$$

## Resistance in parallel:



$$\frac{1}{R_{\text{total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}$$

## Low-pass filter

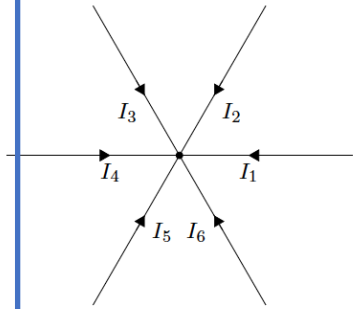


$$X_C = \frac{1}{i\omega C} \text{ decreases with } \omega$$

# Networks (more later)

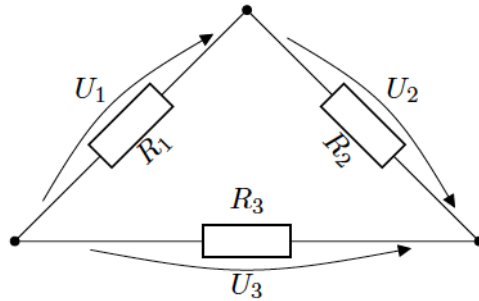
## Junction rule:

$$\sum_{k=1}^n I_k = 0$$

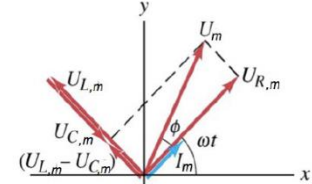
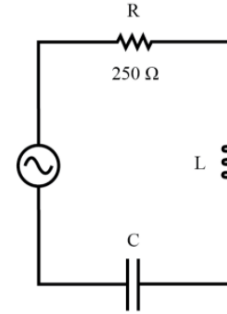


## Loop rule

$$\sum_{k=1}^n U_k = 0$$



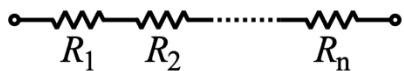
## Impedance in AC circuits



Impedance Z:

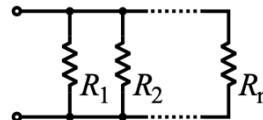
$$Z = \sqrt{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \quad \hat{I} = \frac{\hat{U}}{Z}$$

## Resistance in series:



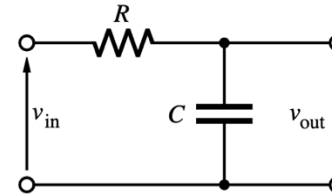
$$R_{\text{total}} = R_s = R_1 + R_2 + \dots + R_n$$

## Resistance in parallel:

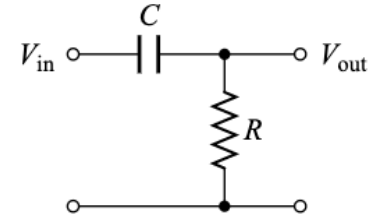


$$\frac{1}{R_{\text{total}}} = \frac{1}{R_1} + \frac{1}{R_2} + \dots + \frac{1}{R_n}$$

## Low-pass filter



## high-pass filter



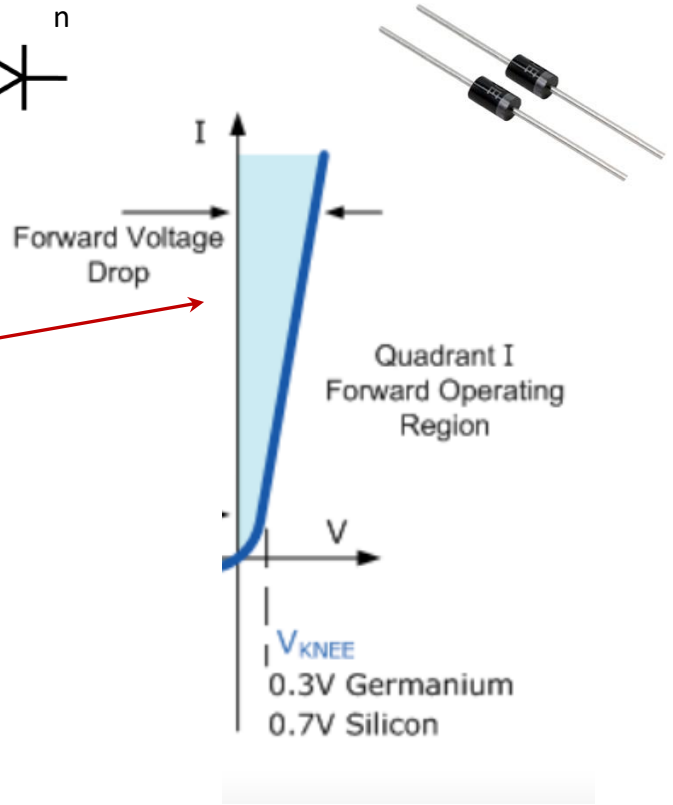
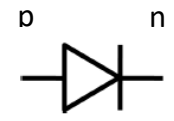
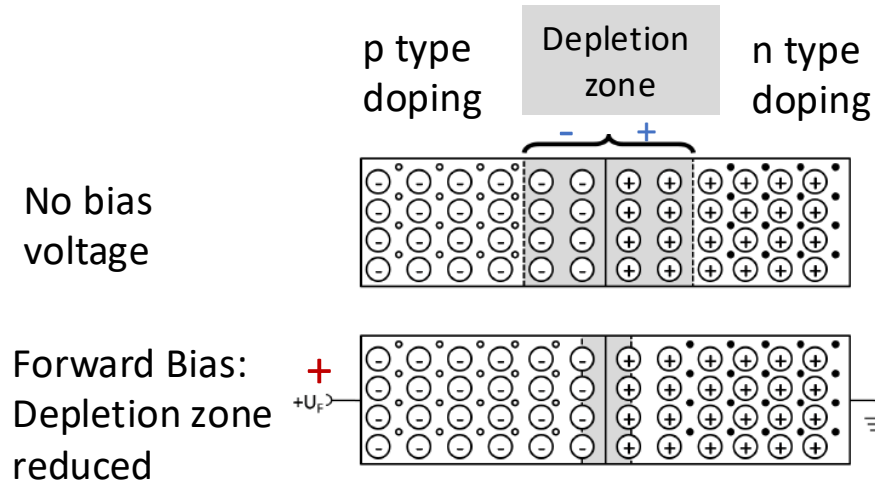
$$X_C = \frac{1}{i\omega C} \text{ decreases with } \omega$$



## (2) Analog electronics

### 2.1.: Building blocks

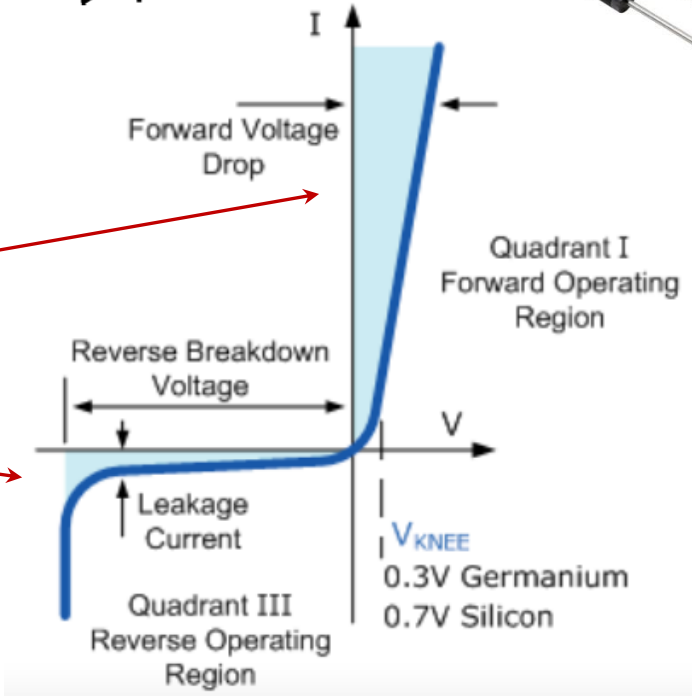
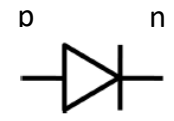
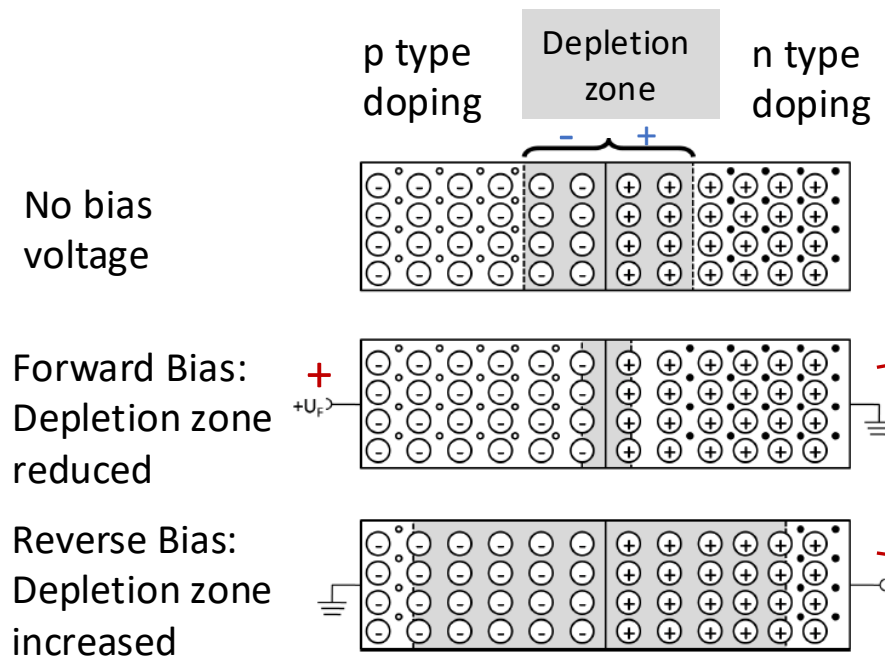
# Diode: pn junction and biasing



Electrons cross the junction from n to p type → depletion zone, barrier voltage

Current-voltage characteristic

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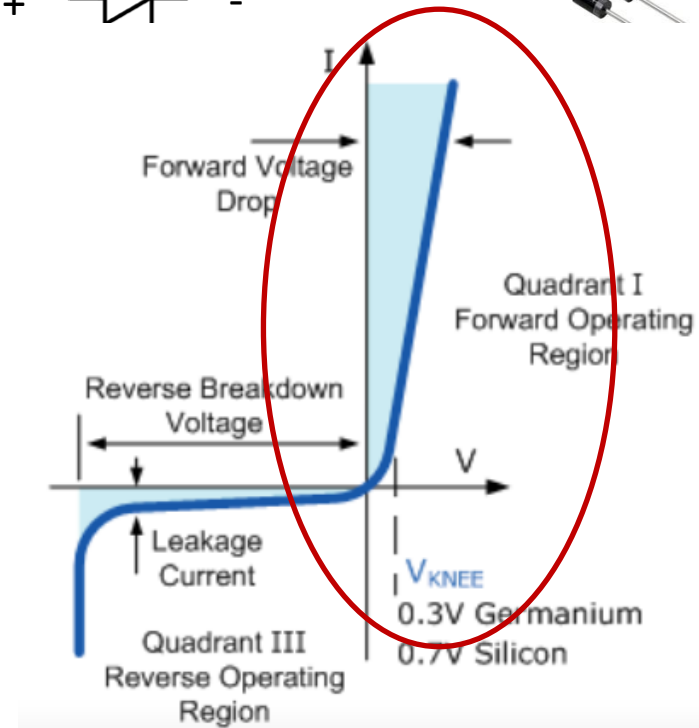
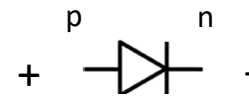
# Diode: forward biasing

**Ideal diode** (forward bias):

$$I(U) = I_S \cdot \left( e^{\frac{U}{U_T}} - 1 \right)$$

$I_S$ : leakage current  $\approx 1\text{-}100 \mu\text{A}$

$U_T = kT/e \approx 40 \text{ mV}$



Current-voltage characteristic

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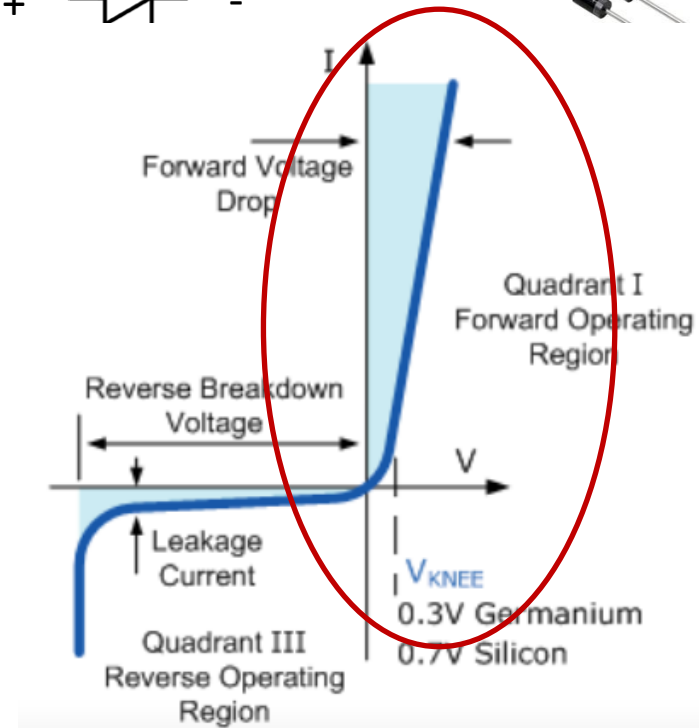
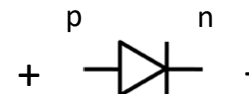
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**Real diode** (forward bias):

$I(U)$  only  $> 0$

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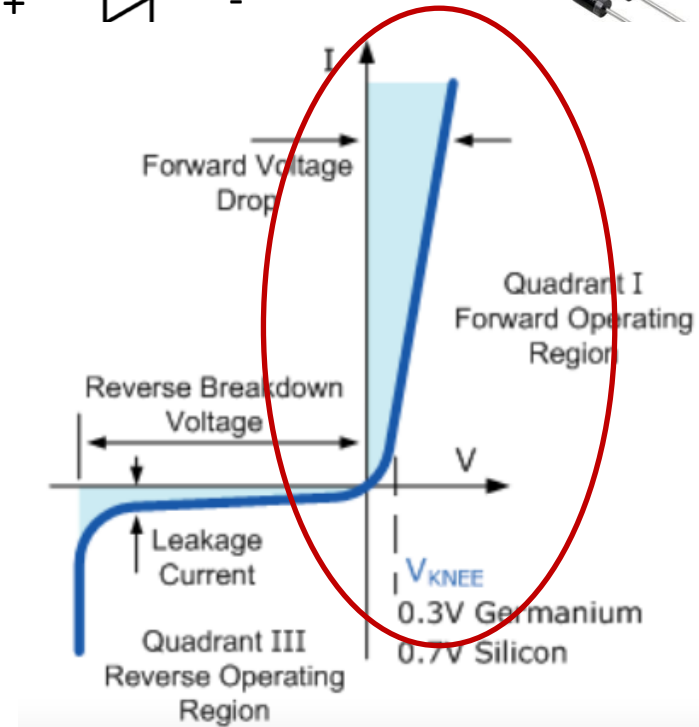
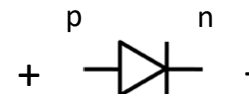
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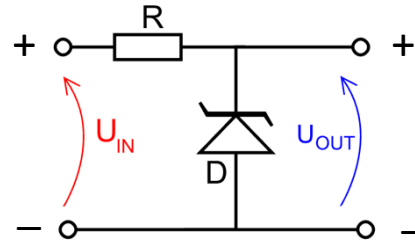
**Differential resistance:**

$$r = \frac{dI}{dU}$$



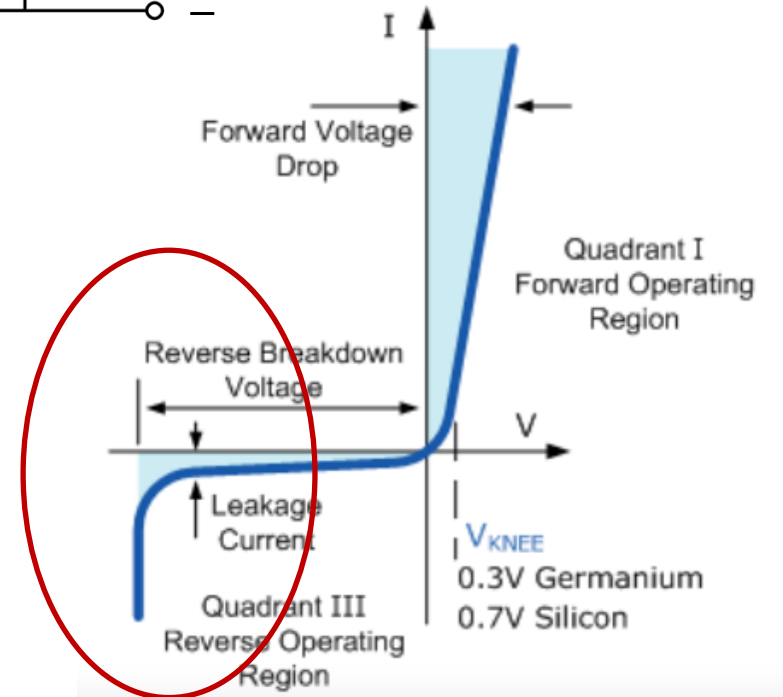
Current-voltage characteristic

# Zener diodes: reverse biasing

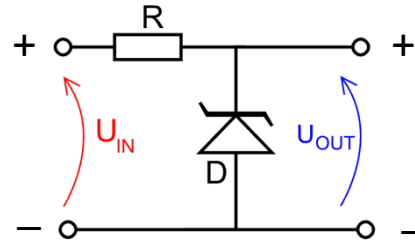


Conventional diodes destroyed by large reverse-bias voltages.

Zener diode: operated with reverse bias.  
Typically, heavily doped: small depletion zone.



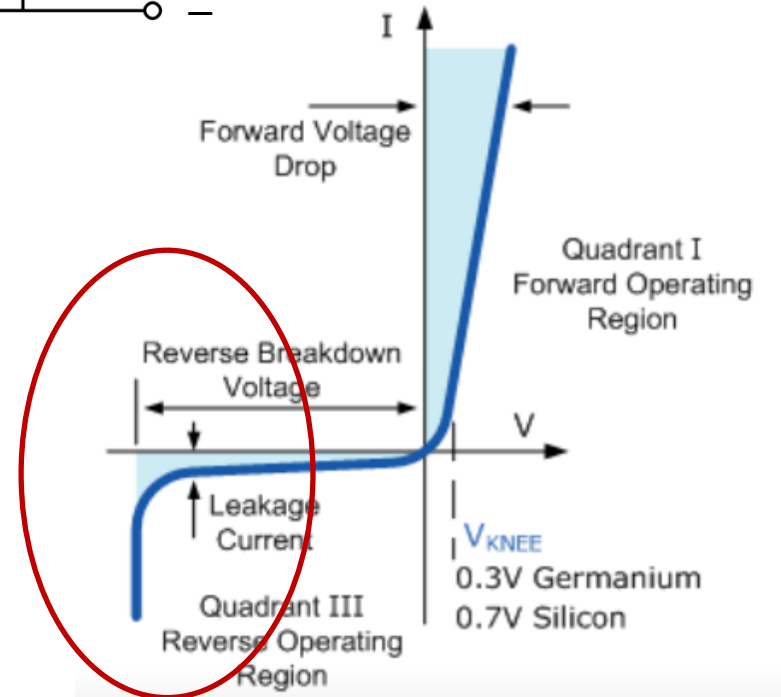
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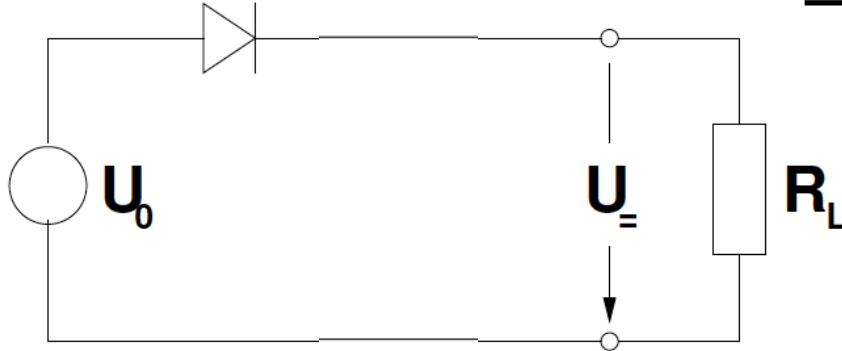
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Typically, heavily doped: small depletion zone.

Resistance breaks down at the Zener voltage: tunneling of electrons from p-type valence into n-type conduction band  
→ Voltage stabilizer, reference voltage

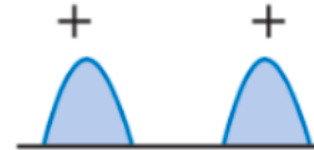


# Circuits with diodes (1)

## Half-wave rectifier

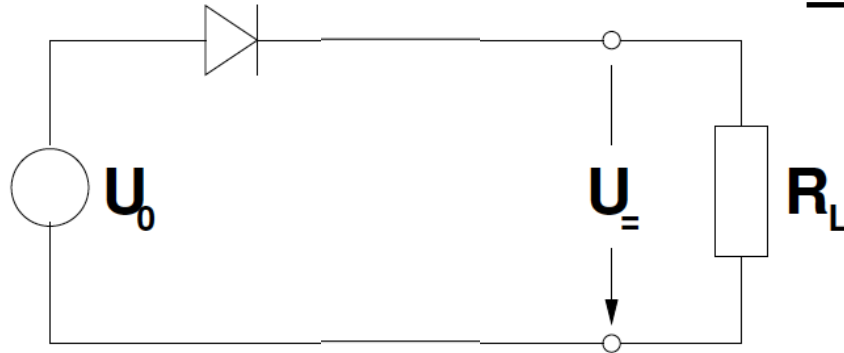


Blocks negative half waves

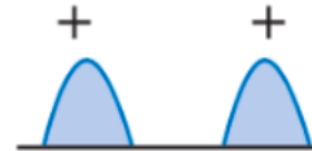


# Circuits with diodes (1)

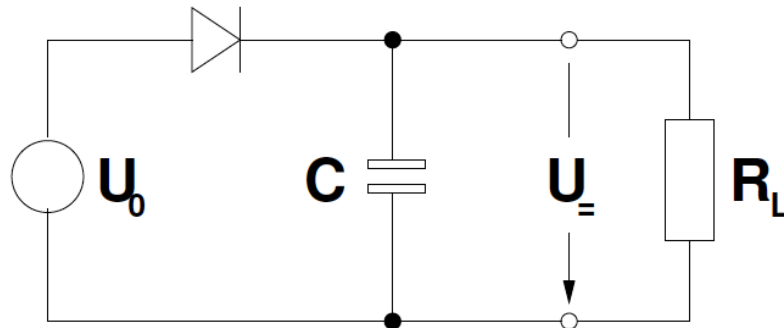
## Half-wave rectifier



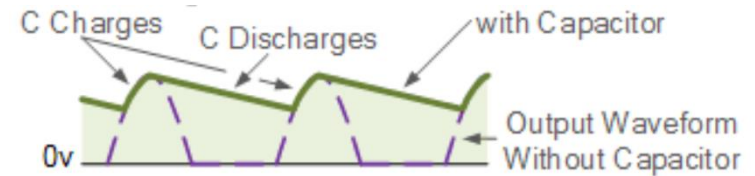
Blocks negative half waves



## Half-wave rectifier with smoothing capacitor

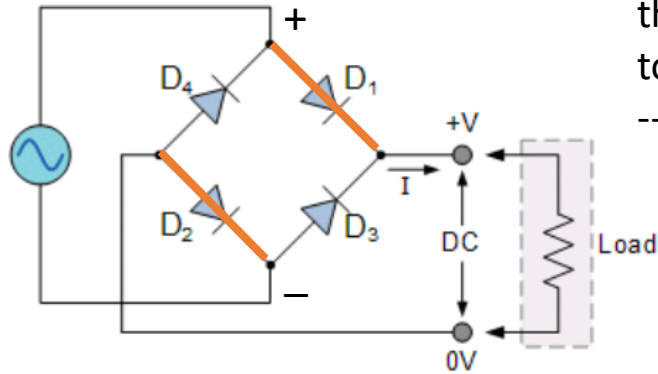


Half waves smoothed



# Circuits with diodes (2)

## Full-wave Bridge rectifier



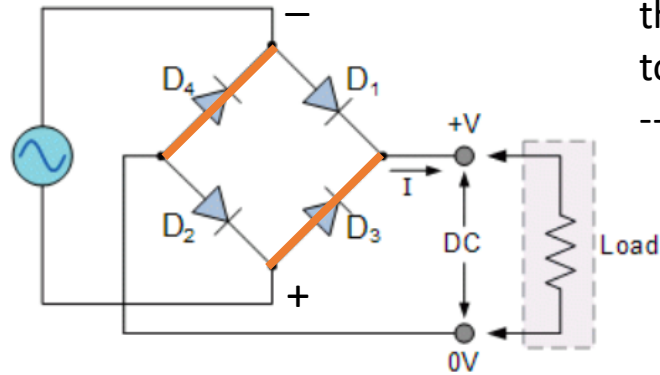
Diodes are arranged such that the positive pole is always connected to the same point.

--> Inverts negative half waves



# Circuits with diodes (2)

## Full-wave Bridge rectifier



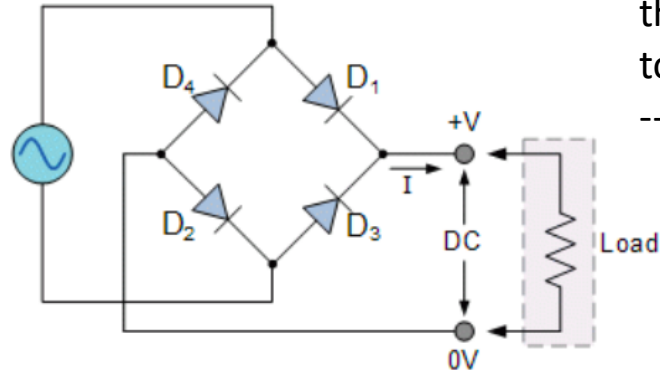
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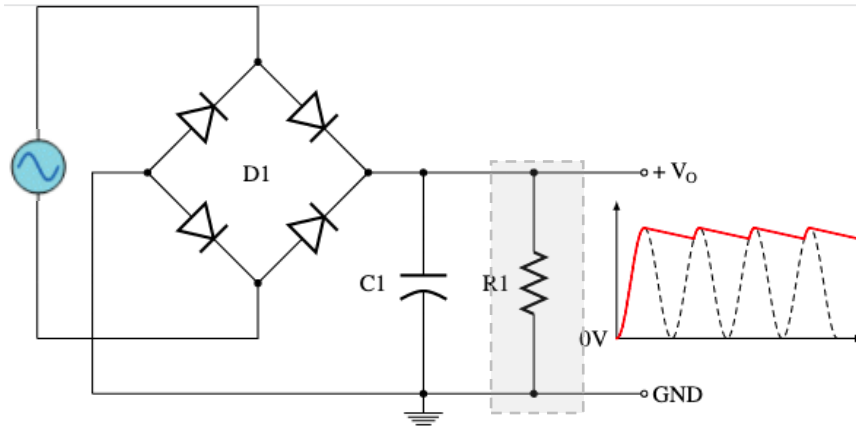


Diodes are arranged such that the positive pole is always connected to the same point.

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## Bridge rectifier with smoothing capacitance

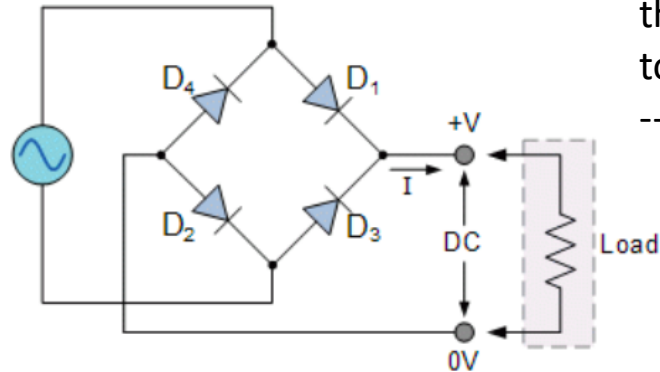


+

-

# Circuits with diodes (2)

## Full-wave Bridge rectifier

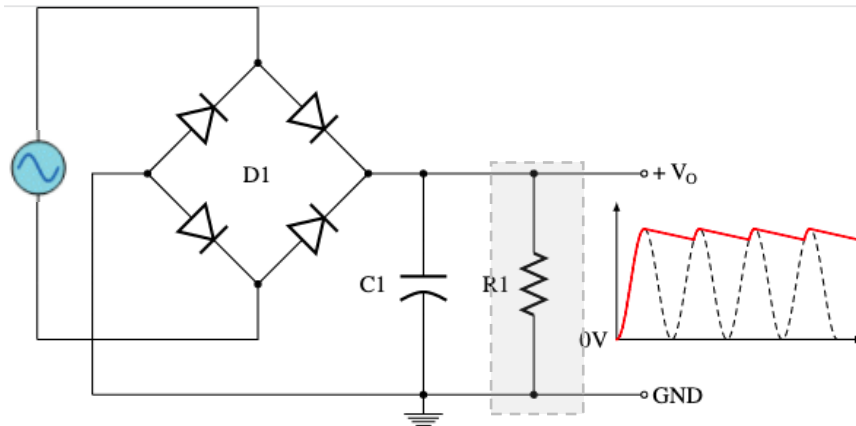


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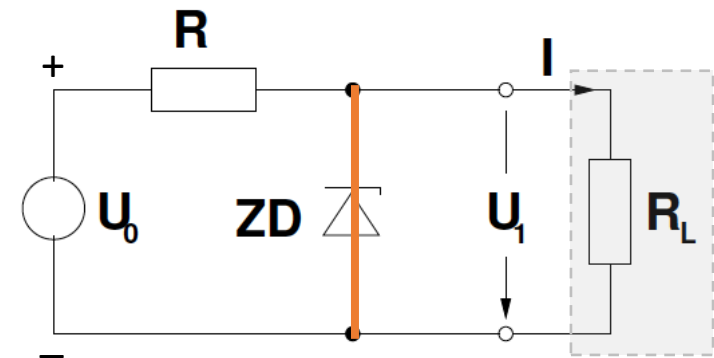


## Bridge rectifier with smoothing capacitance



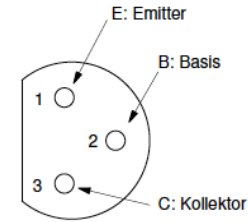
## Voltage regulation/limitation:

If the initial voltage becomes larger than the Zener voltage the Zener current increases  $\rightarrow$  resistance drops



# Transistors

- Active, controllable semiconductor devices.
- Amplify and switch signals and power
- Main types:
  - **Bipolar junction transistor (BJT)**
    - here: **npn transistor**
    - pnp transistor: works in an analogous manner

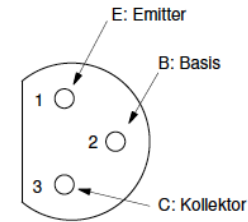


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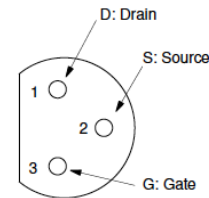
- **Bipolar junction transistor (BJT)**

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- **Field Effect Transistor (FET)**

- MOSFET: **NMOS/PMOS**
- CMOS: combines NMOS and PMOS

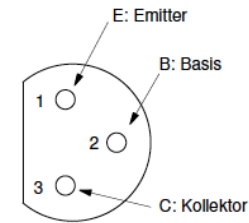


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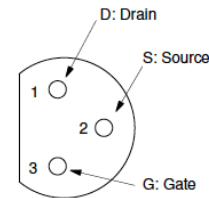
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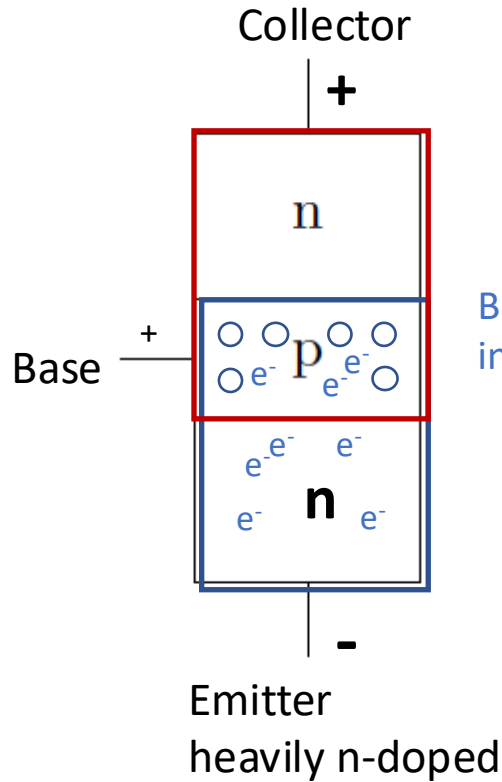
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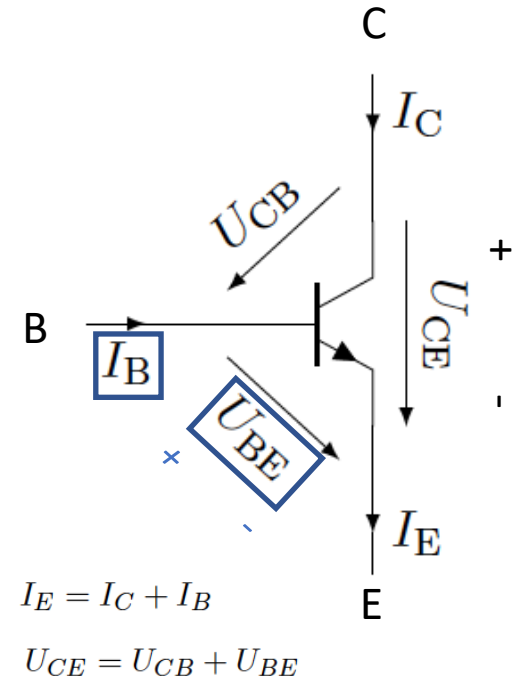


*Contemporary Integrated Circuits (IC) are in general not build from discrete transistors but need to understand the transistor principle to understand IC*

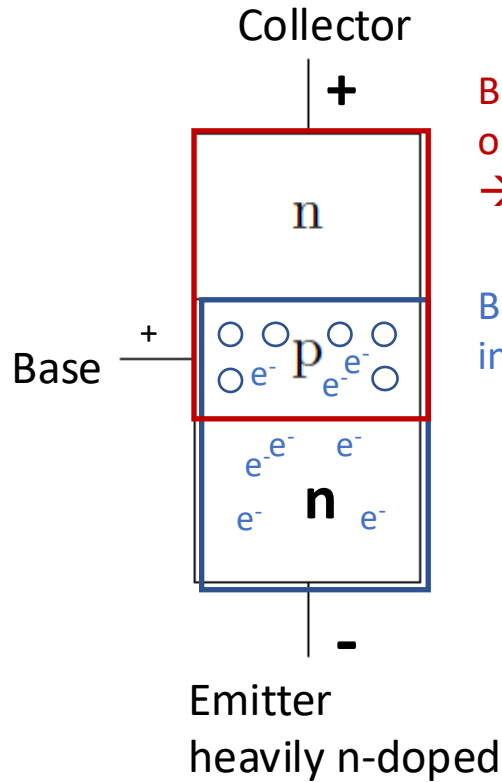
# Bipolar Junction Transistor



Base-Emitter diode: operated  
in forward direction

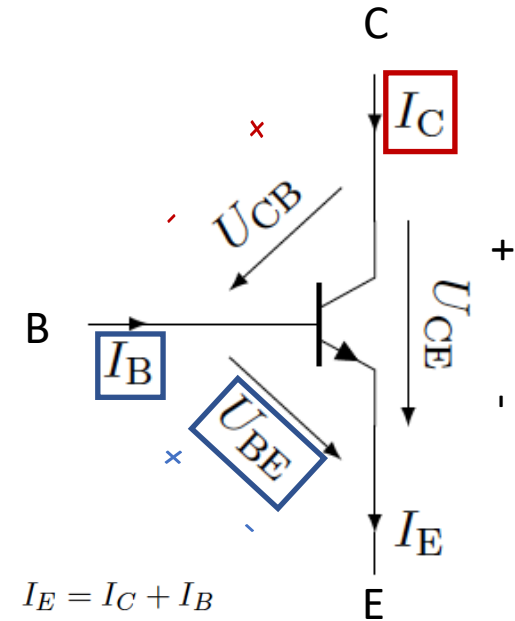


# Bipolar Junction Transistor



Base-Collector diode:  
operated in reverse bias  
→ “leakage” collector current  $I_C$

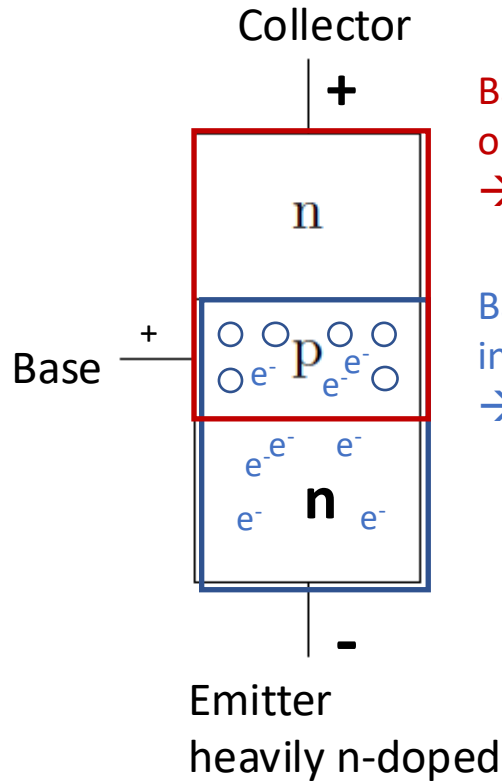
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$$I_E = I_C + I_B$$

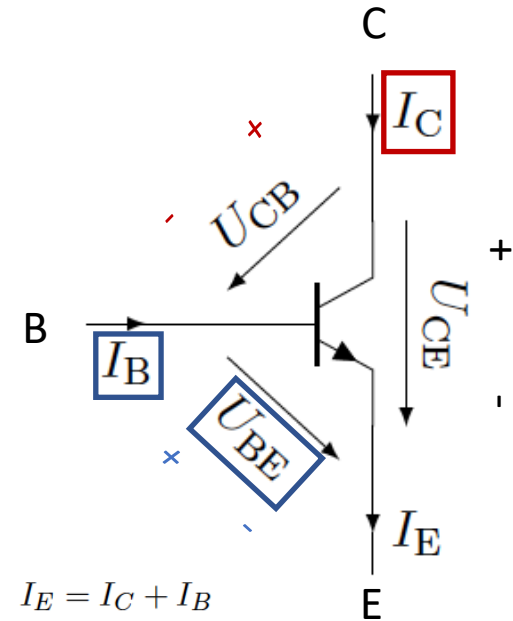
$$U_{CE} = U_{CB} + U_{BE}$$

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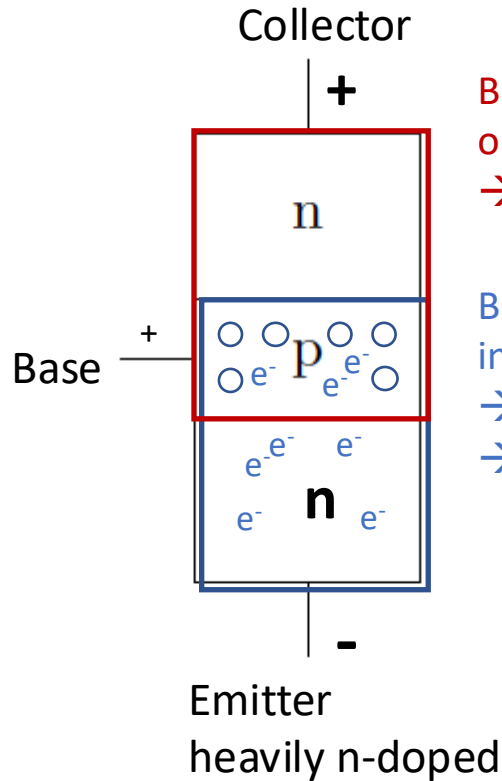
Base-Emitter diode: operated  
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→ electrons drift into the base



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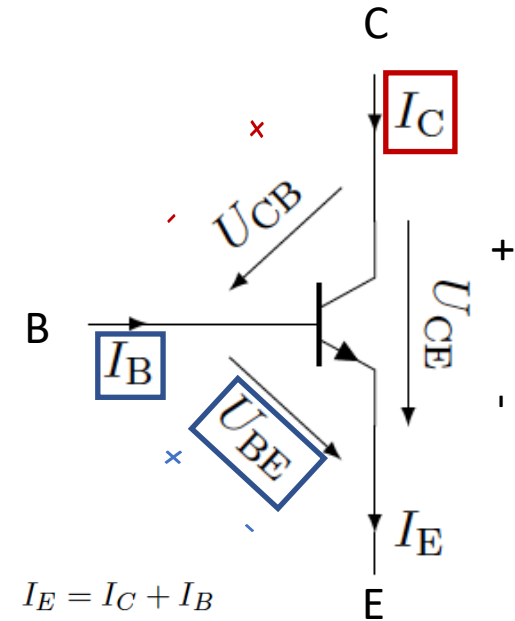
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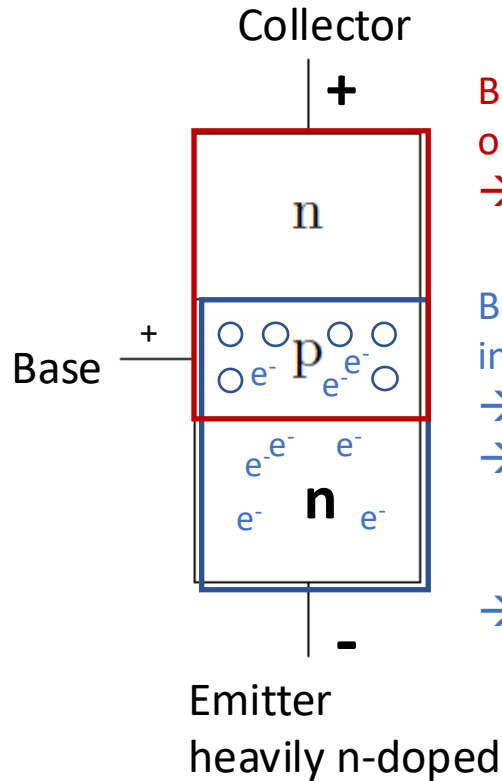
Base-Emitter diode: operated  
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→ electrons drift into the base  
→ some electrons reach the  
p-n transition region of the  
Base-Collector diode



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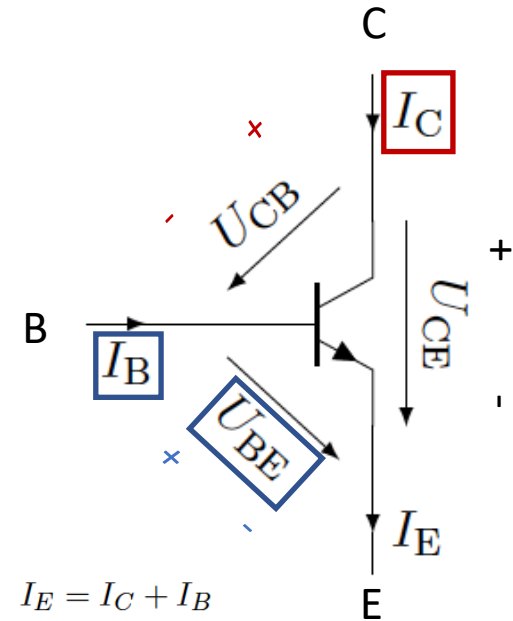
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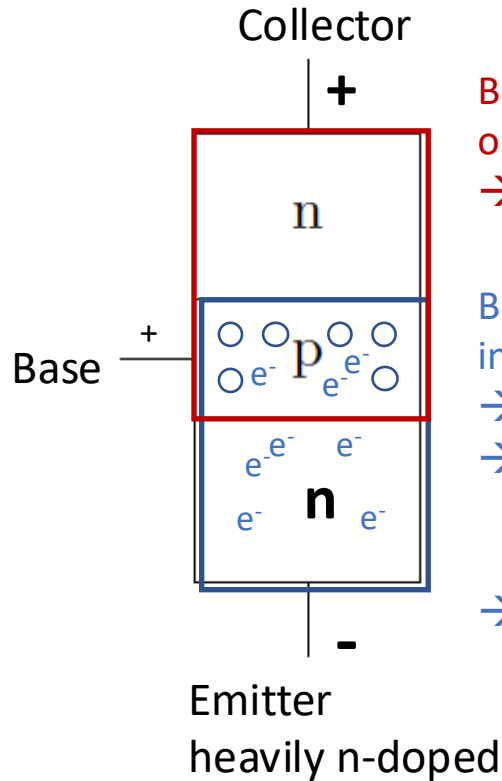
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Base-Collector diode  
→ increase collector current  $I_C$



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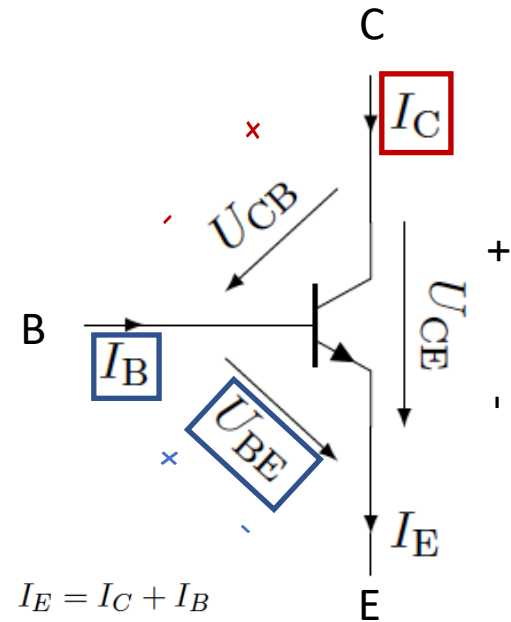
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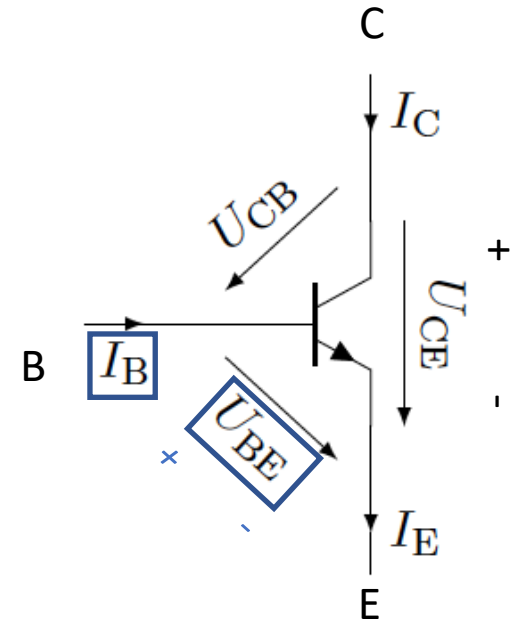
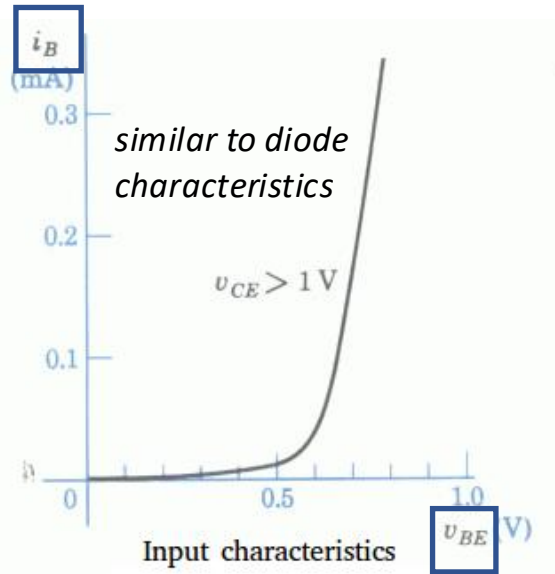
$$I_E = I_C + I_B$$

$$U_{CE} = U_{CB} + U_{BE}$$

$$I_B / U_{BE} \rightarrow \text{control} \rightarrow I_C$$

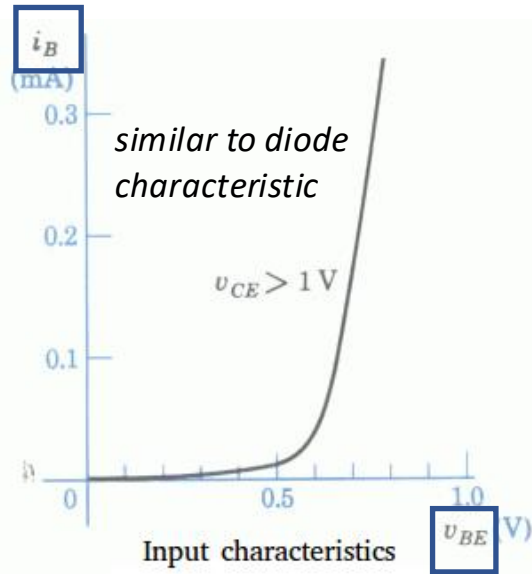
# npn BJT: characteristics (1)

## Input characteristics

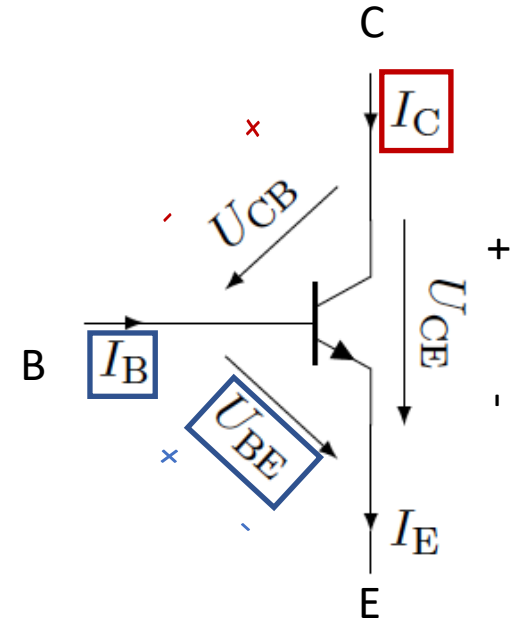
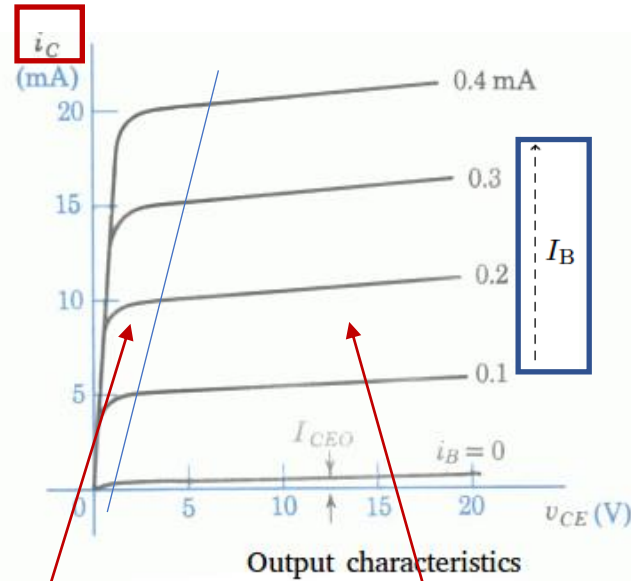


# npn BJT: characteristics (1)

## Input characteristics



## Output characteristics

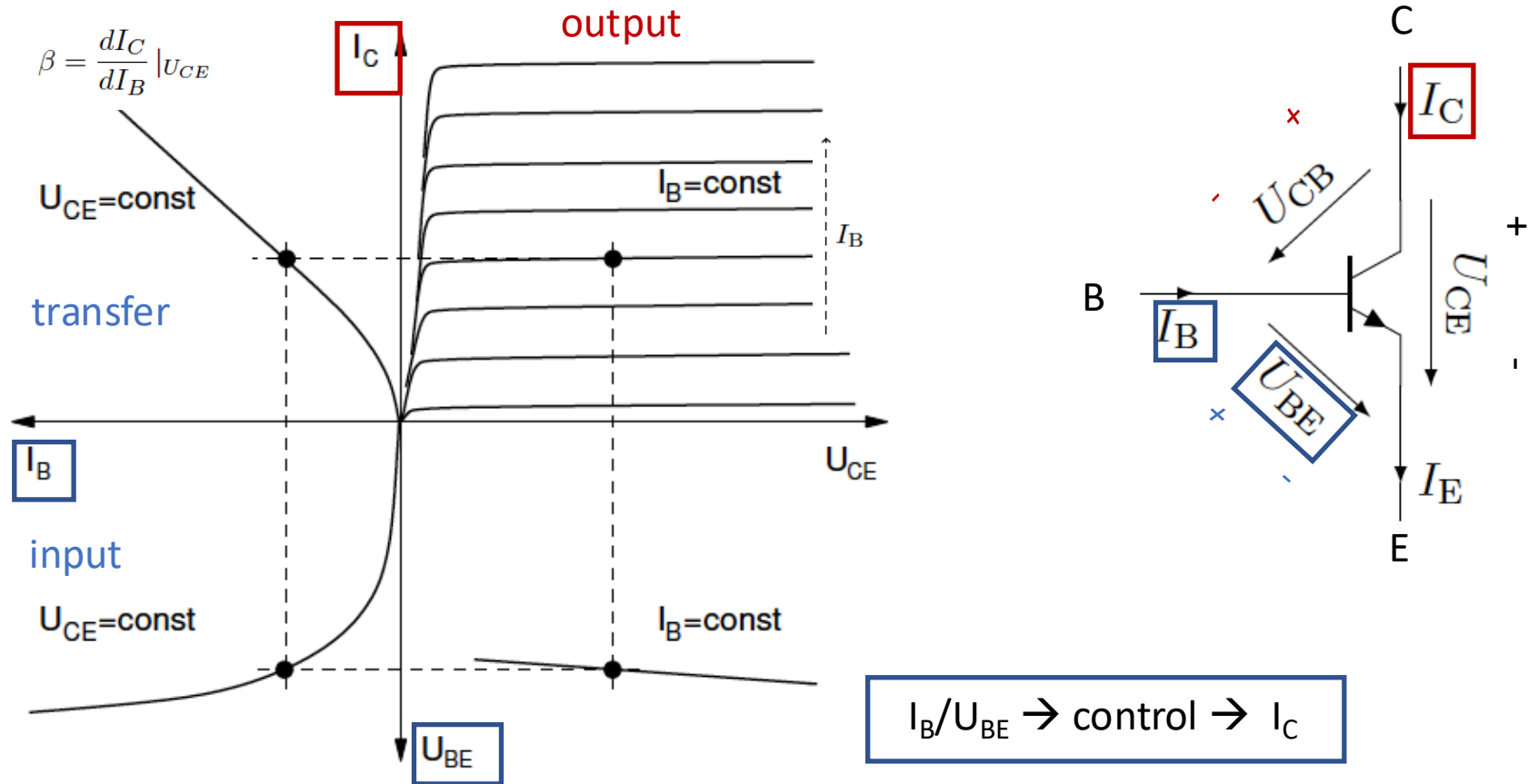


**Saturation region:**  
Small changes in  $U_{CE}$  lead to large change in  $I_C$   
→ switches etc.

**Active region:**  
Small change in base current  $I_B$  lead to large change in collector current, nearly independent of  $U_{CE}$   
→ Current amplification etc.

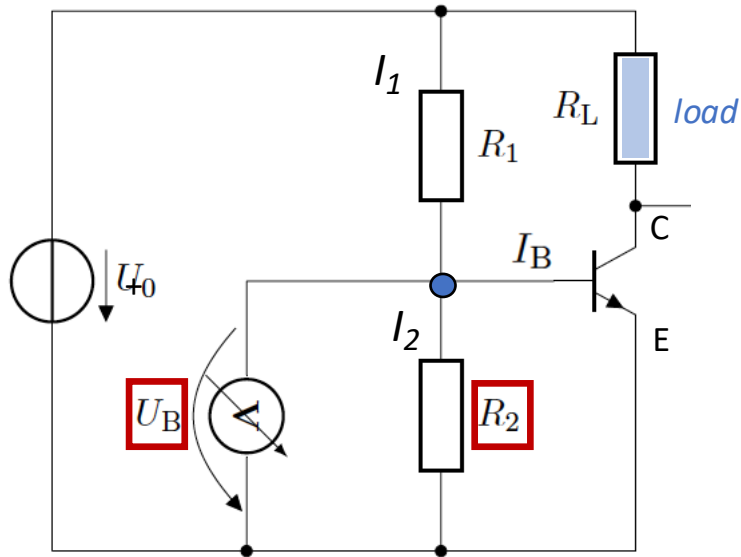
# npn BJT: characteristics (2)

- working point in active region



# Selecting the working point

## Example circuit

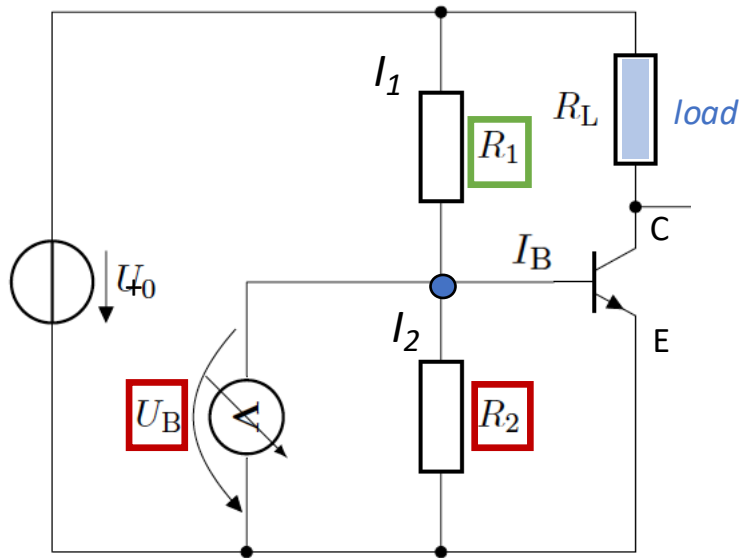


## Voltage divider biasing

The voltage  $U_B$  across  $R_2$  forward-biases the BE junction

# Selecting the working point

## Example circuit



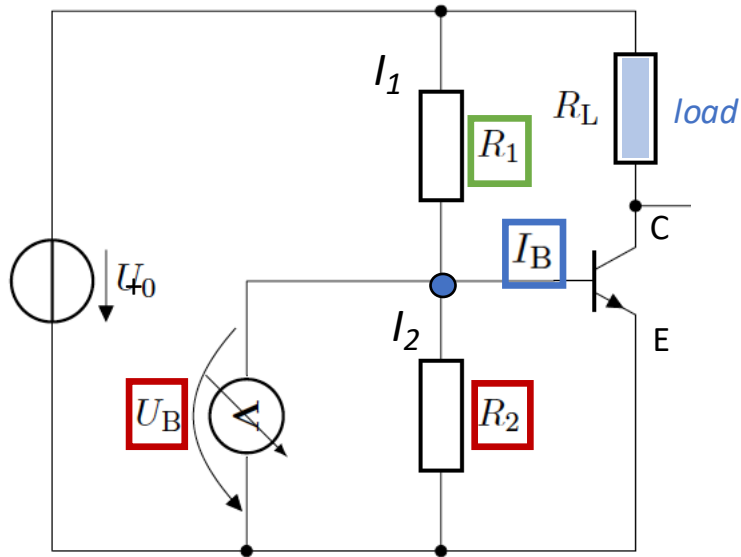
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$$U_B = U_0 \cdot \frac{R_2}{R_1 + R_2} - I_B \cdot \frac{R_1 R_2}{R_1 + R_2}$$

# Selecting the working point

## Example circuit



(Calculation: see next lecture: circuit analysis)

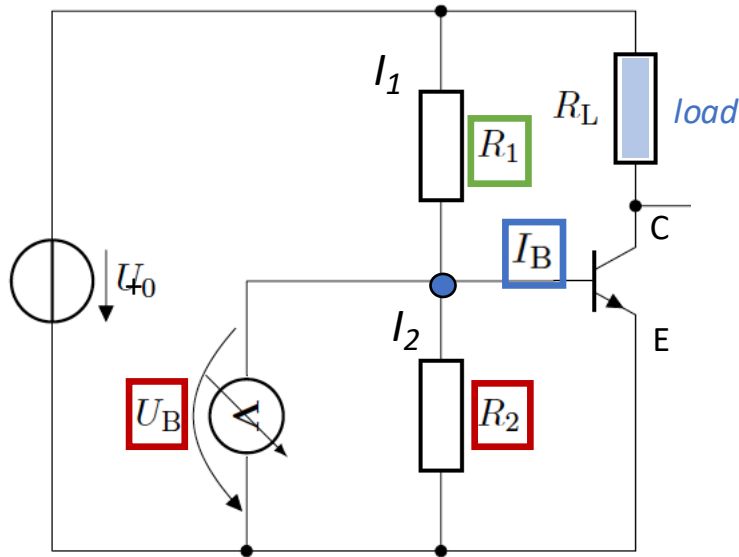
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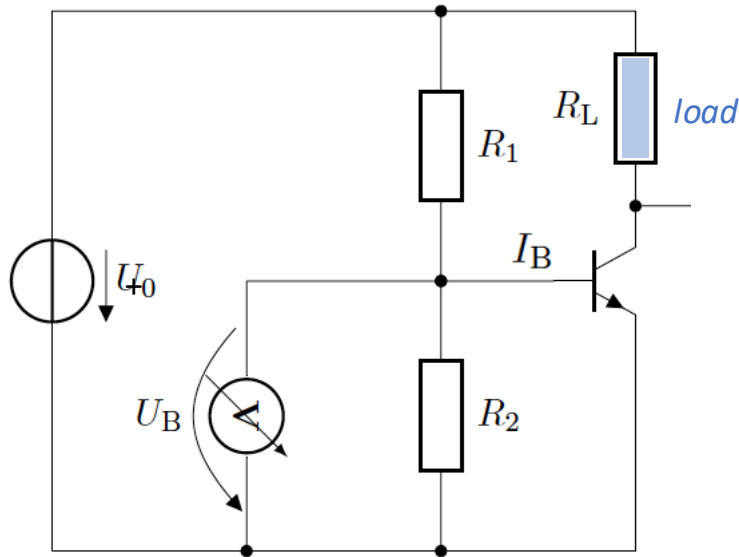
$$U_B = U_0 \cdot \frac{R_2}{R_1 + R_2} - I_B \cdot \frac{R_1 R_2}{R_1 + R_2}$$

If  $R_1, R_2$  are sufficiently small, the base current does not impact the base voltage

$$I_B \cdot R_1 \ll U_0 \quad \rightarrow \quad U_B \approx U_0 \cdot \frac{R_2}{R_1 + R_2}$$

# Selecting the working point

## Example circuit



(Calculation: see next lecture: circuit analysis)

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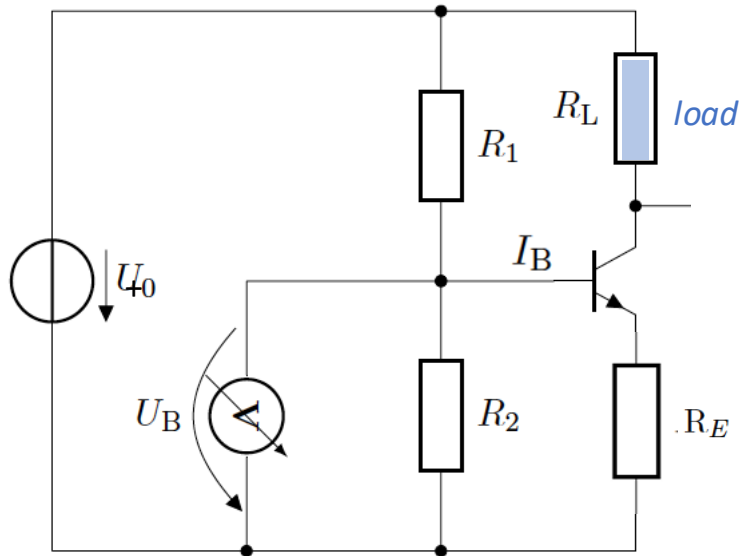
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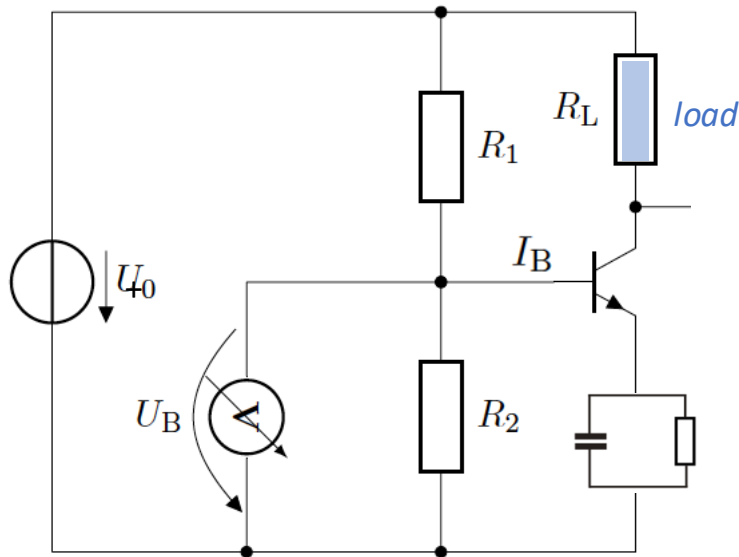
$$I_B \cdot R_1 \ll U_0 \quad \rightarrow \quad U_B \approx U_0 \cdot \frac{R_2}{R_1 + R_2}$$

## Stabilizing WP by adding emitter resistance $R_E$

Reduces  $U_{BE}$  if base current  $I_B$  becomes too large.

# Selecting the working point

## Example circuit



## Voltage divider biasing

The voltage  $U_B$  across  $R_2$  forward-biases the BE junction

$$U_B = U_0 \cdot \frac{R_2}{R_1 + R_2} - I_B \cdot \frac{R_1 R_2}{R_1 + R_2}$$

If  $R_1, R_2$  are sufficiently small, the base current does not impact the base voltage

$$I_B \cdot R_1 \ll U_0 \quad \rightarrow \quad U_B \approx U_0 \cdot \frac{R_2}{R_1 + R_2}$$

## Stabilizing WP by adding emitter resistance $R_E$

Reduces  $U_{BE}$  if base current  $I_B$  becomes too large.

Effect on AC signal can be mitigated by adding a capacitor in parallel

$\rightarrow R_E \parallel R_C$  reduced for high frequencies,  $R \approx R_E$  for low frequencies

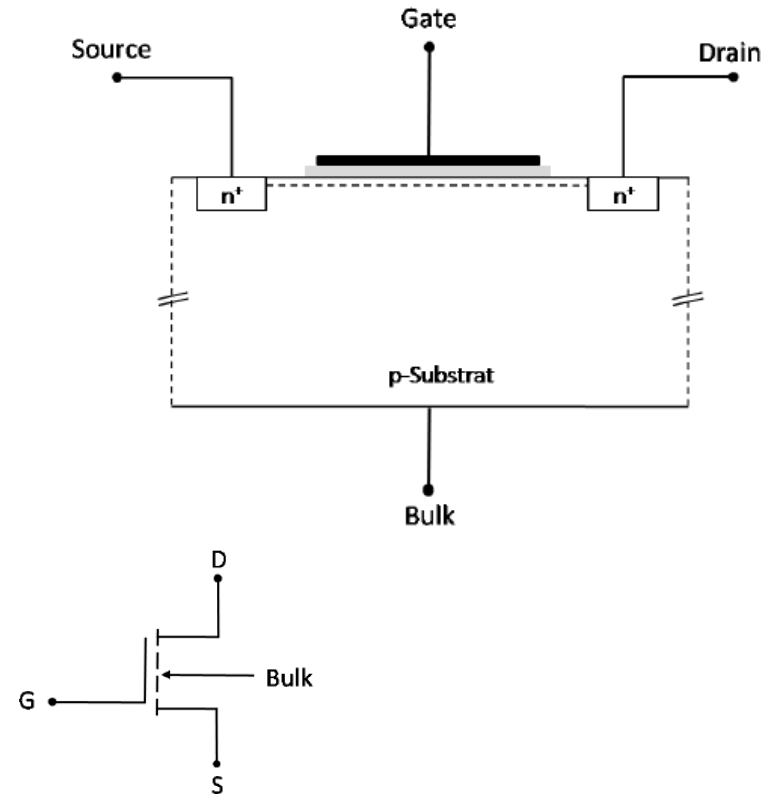
$$X_C = \frac{1}{i\omega C}$$

# FET

BJT not suited for Integrated Circuits (IC): base currents would overheat the IC

→ use FETs: similar operation as with BJT but:

- controlled with negligible currents
- smaller area
- transfer characteristics more linear
- less noise



# FET

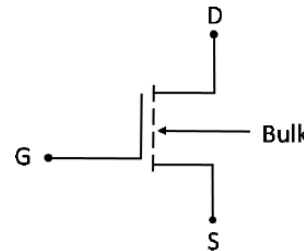
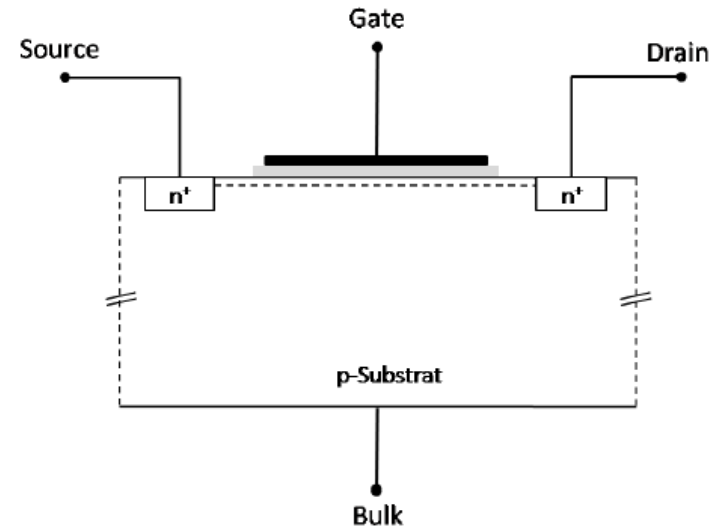
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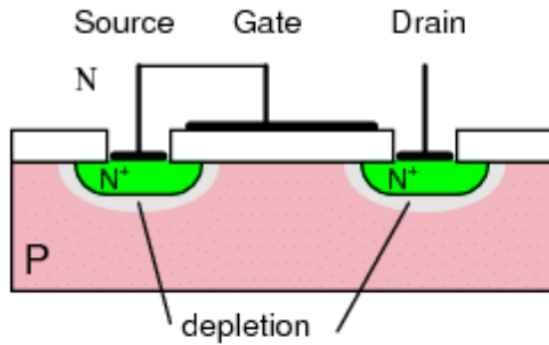
- controlled with negligible currents
- smaller area
- transfer characteristics more linear
- less noise

Example n-channel MOSFET (Metal-Oxide-Silicon FET)

- p-doped substrate
- n-doped channels: Source, Drain
- Gate isolated from substrate by e.g.  $\text{SiO}_2$ 
  - → no Gate-Source/Drain currents

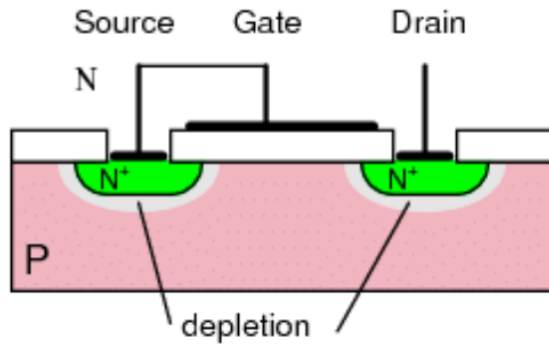


# N-channel MOSFET: operation

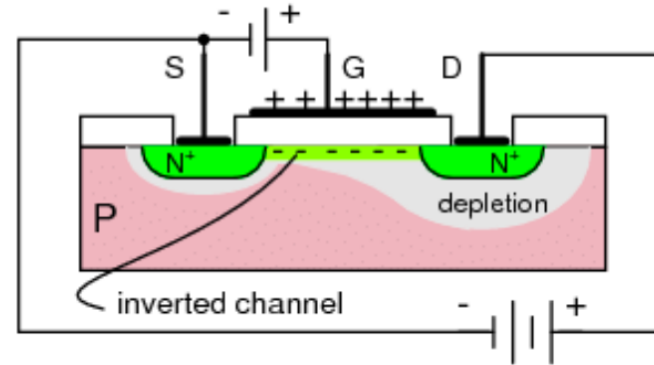


- No source drain current

# N-channel MOSFET: operation

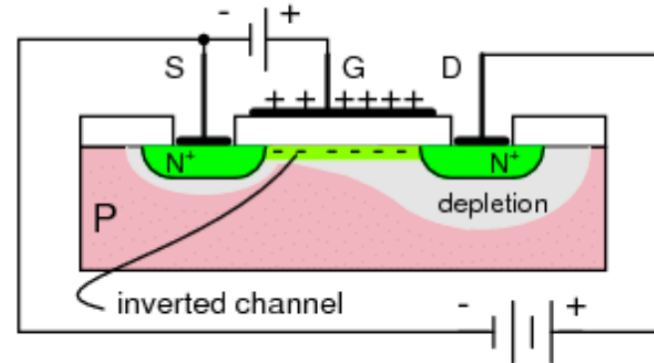
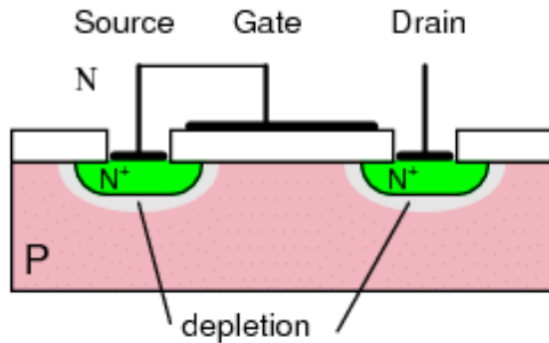


- No source drain current



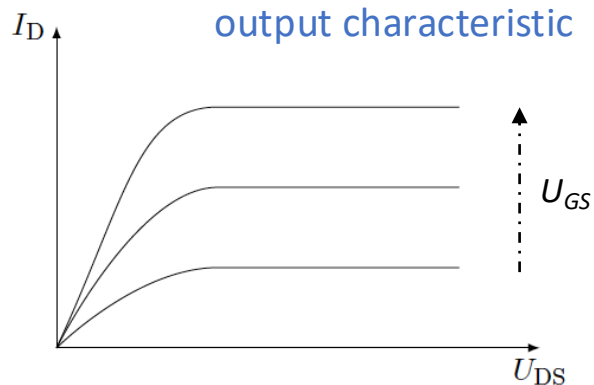
- Electrons from p-doped substrate drawn towards positively charged gate
- → channel allows for S-D current  $I_D$

# N-channel MOSFET: operation



- No source drain current

- Electrons from p-doped substrate drawn towards positively charged gate
- → channel allows for S-D current  $I_D$



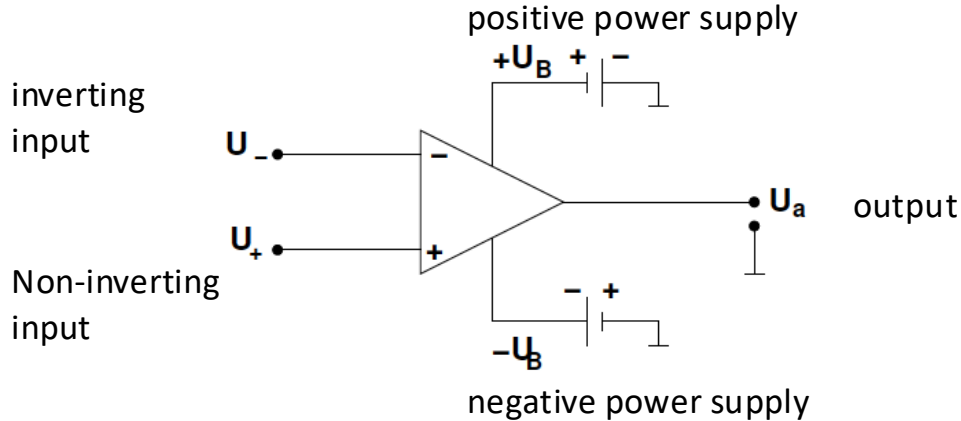
Typically, smaller transconductance than BJT (output current /input voltage)



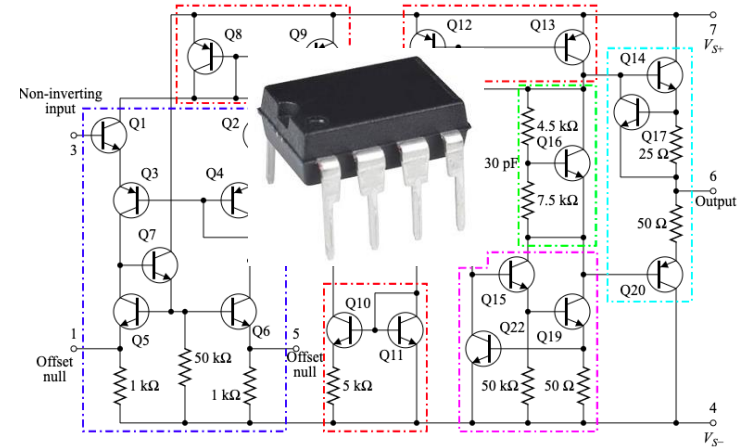
(2) Analog electronics:  
2.2: Integrated circuits  
Example: Operation Amplifier

# Operational amplifier (op amp)

Difference amplifier with two inputs and one output



Circuit diagram:



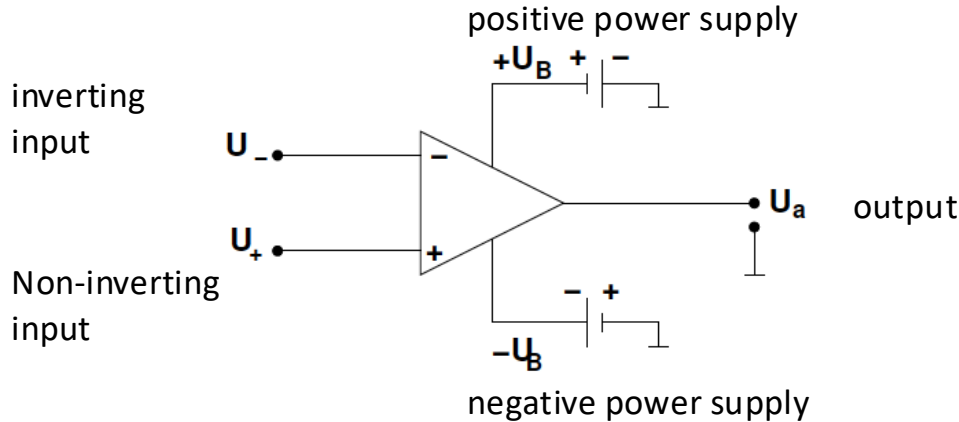
Characteristics:

- Output voltage proportional to the difference between the input voltages: very high amplification ( $> 10000-100000$ )

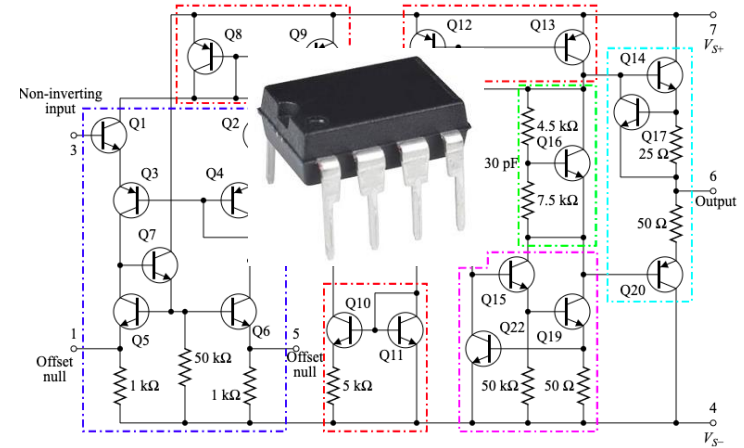
$$U_a = v_0 \cdot (U^+ - U^-)$$

# Operational amplifier (op amp)

Difference amplifier with two inputs and one output



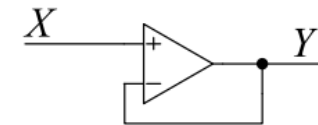
Circuit diagram:



Characteristics:

- Output voltage proportional to the difference between the input voltages: very high amplification (> 10000-100000)
- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]

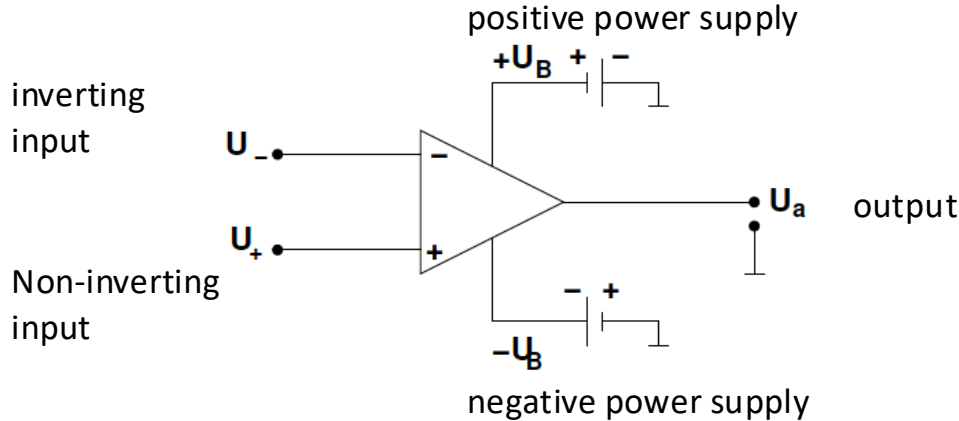
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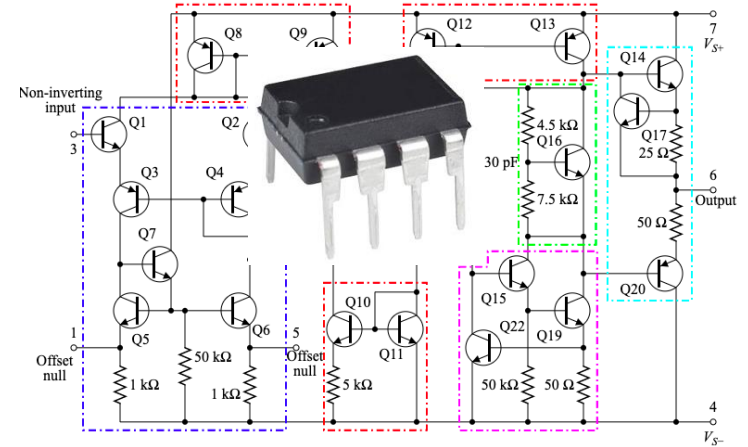
negative feedback

# Operational amplifier (op amp)

Difference amplifier with two inputs and one output



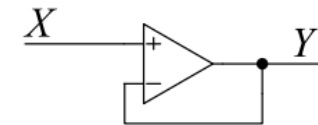
Circuit diagram:



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- Negligible input current (into the op amp) [2]

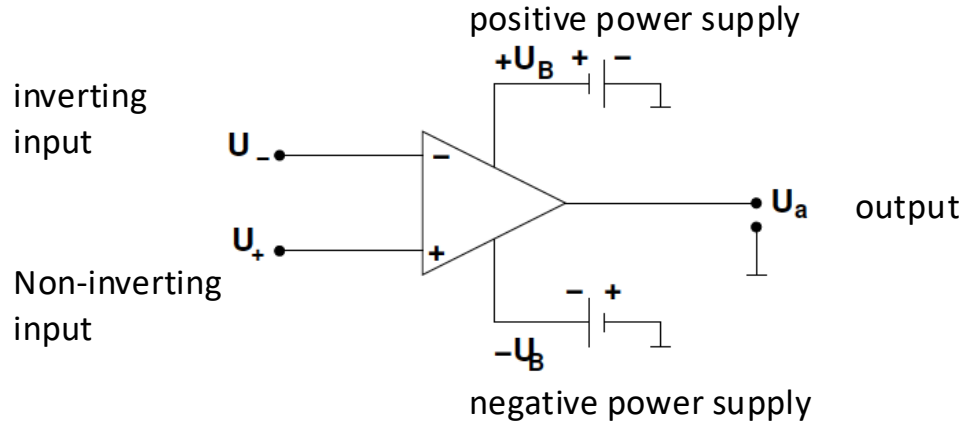
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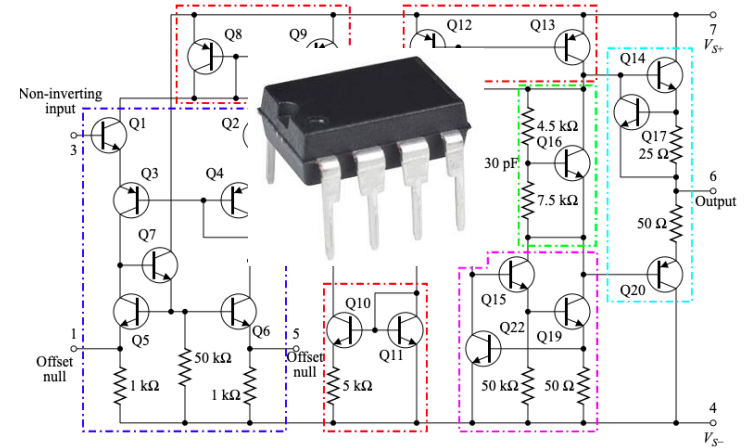
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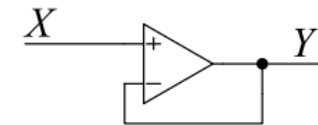
Circuit diagram:



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- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]
- Negligible input current (into the op amp) [2]
- The maximum output voltage is the power supply voltage

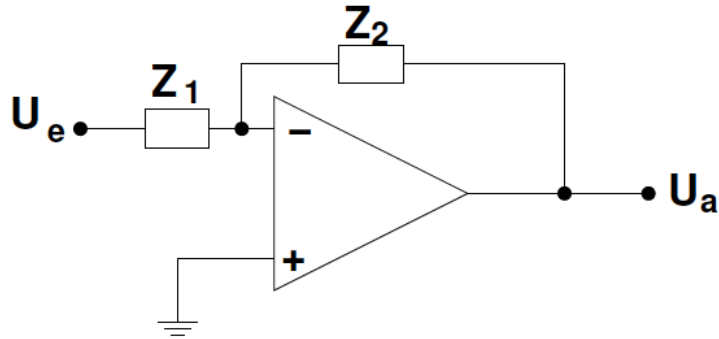
$$U_a = v_0 \cdot (U^+ - U^-)$$



negative feedback

# Op amp circuits

Inverting amplifier (negative feedback)

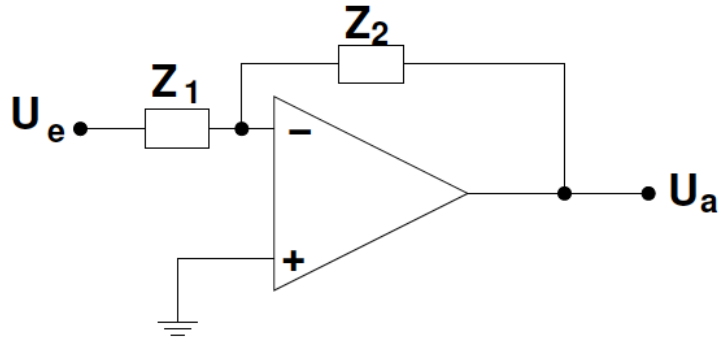


$$[2] \rightarrow I_1 = \frac{U_e - U^-}{Z_1} = \frac{U^- - U_a}{Z_2} = I_2$$

- If used with negative feedback ( $U_a$  connected with  $U^-$ ) the op amp regulates  $U^+ = U^-$  [1]
- Negligible input current (into the op amp) [2]

# Op amp circuits

Inverting amplifier (negative feedback)



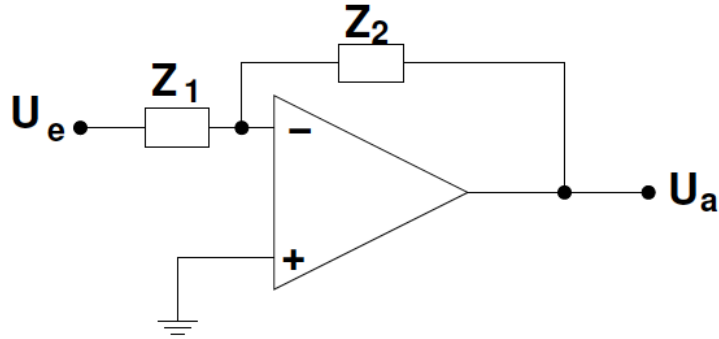
$$[2] \rightarrow I_1 = \frac{U_e - U^-}{Z_1} = \frac{U^- - U_a}{Z_2} = I_2$$

$$[1] \rightarrow U^- = 0 \text{ V (virtual ground)}$$

- If used with negative feedback ( $U_a$  connected with  $U^-$ ) the op amp regulates  $U^+ = U^-$  [1]
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# Op amp circuits

Inverting amplifier (negative feedback)



$$[2] \rightarrow I_1 = \frac{U_e - U^-}{Z_1} = \frac{U^- - U_a}{Z_2} = I_2$$

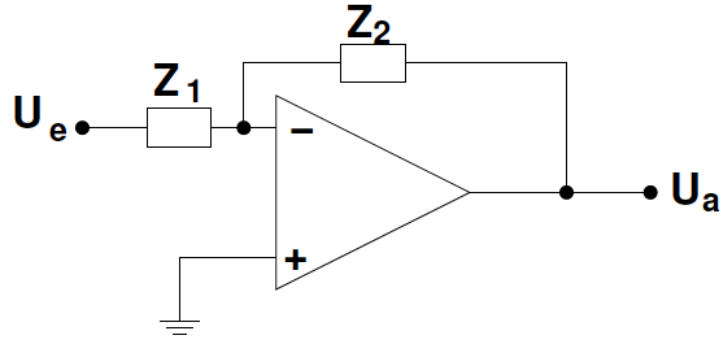
$$[1] \rightarrow U^- = 0 \text{ V (virtual ground)}$$

$$\rightarrow U_a = -\frac{Z_2}{Z_1} U_e$$

- If used with negative feedback ( $U_a$  connected with  $U^-$ ) the op amp regulates  $U^+ = U^-$  [1]
- Negligible input current (into the op amp) [2]

# Op amp circuits

Inverting amplifier (negative feedback)



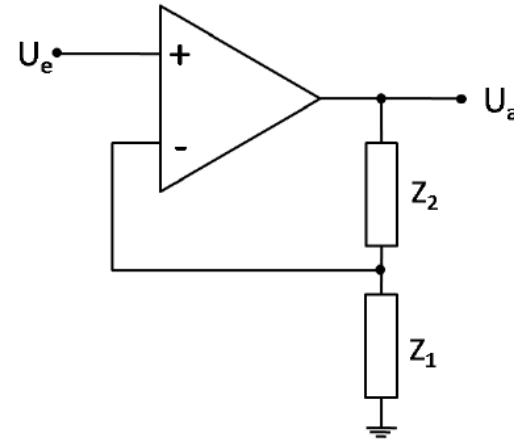
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- If used with negative feedback ( $U_a$  connected with  $U^-$ ) the op amp regulates  $U^+ = U^-$  [1]
- Negligible input current (into the op amp) [2]

Non-inverting amplifier (negative feedback)

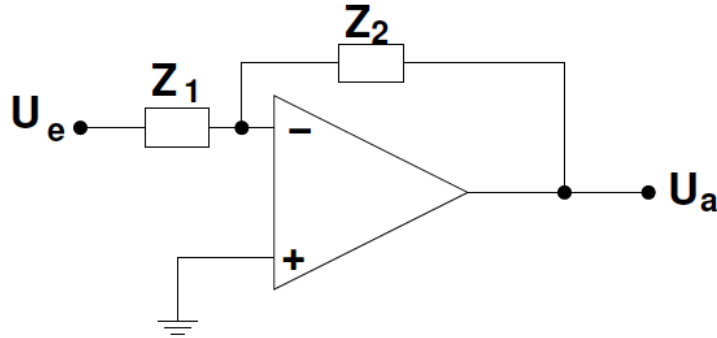


Negative feedback from voltage divider:

$$[1] \rightarrow U_e = U^- = \frac{Z_1}{Z_1 + Z_2} U_a$$

# Op amp circuits

Inverting amplifier (negative feedback)



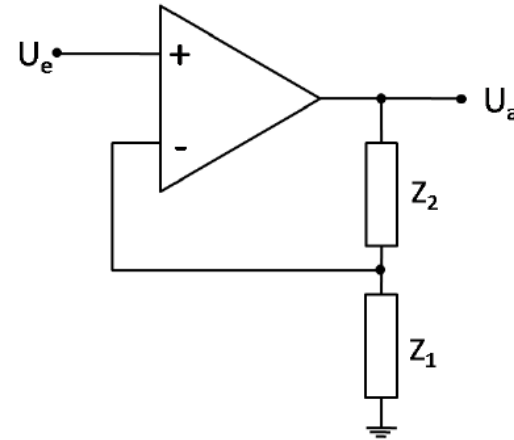
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Non-inverting amplifier (negative feedback)



Negative feedback from voltage divider:

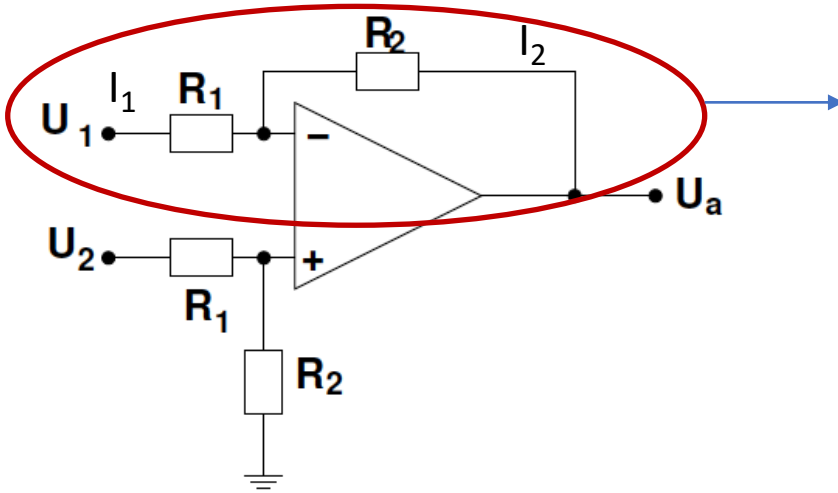
$$[1] \rightarrow U_e = U^- = \frac{Z_1}{Z_1 + Z_2} U_a$$

$$\rightarrow U_a = \left( \frac{Z_2}{Z_1} + 1 \right) U_e$$

# Op amp circuits

Differential amplifier (negative feedback)

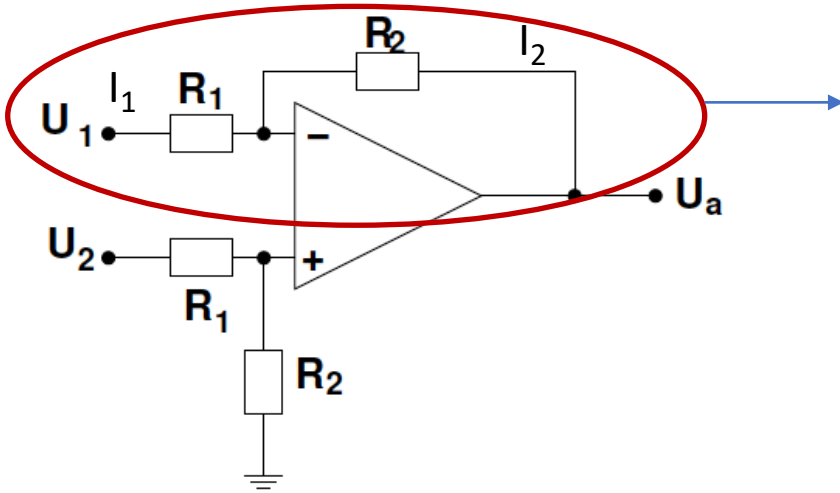
$$[1] \quad U_- = U_+ = U$$



- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]
- Negligible input current (into the op amp) [2]

# Op amp circuits

Differential amplifier (negative feedback)



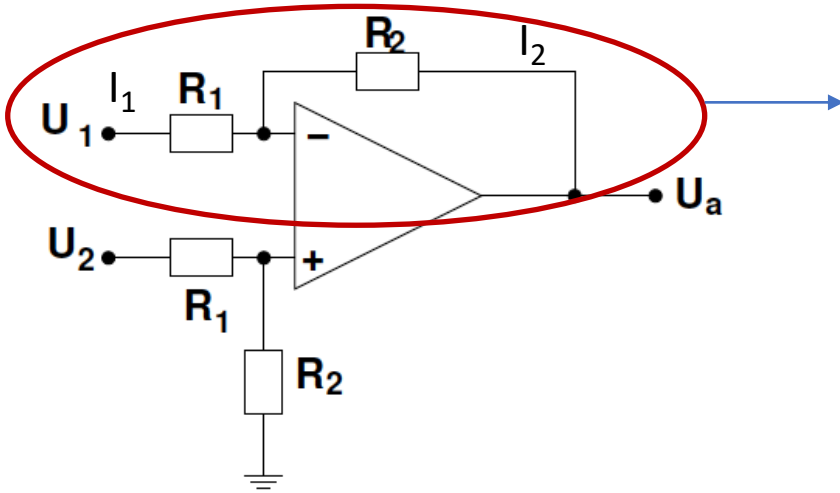
$$[1] U_- = U_+ = U$$

$$[2] I_1 = \frac{U_1 - U}{R_1} = I_2 = \frac{U - U_a}{R_2}$$

- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]
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# Op amp circuits

Differential amplifier (negative feedback)



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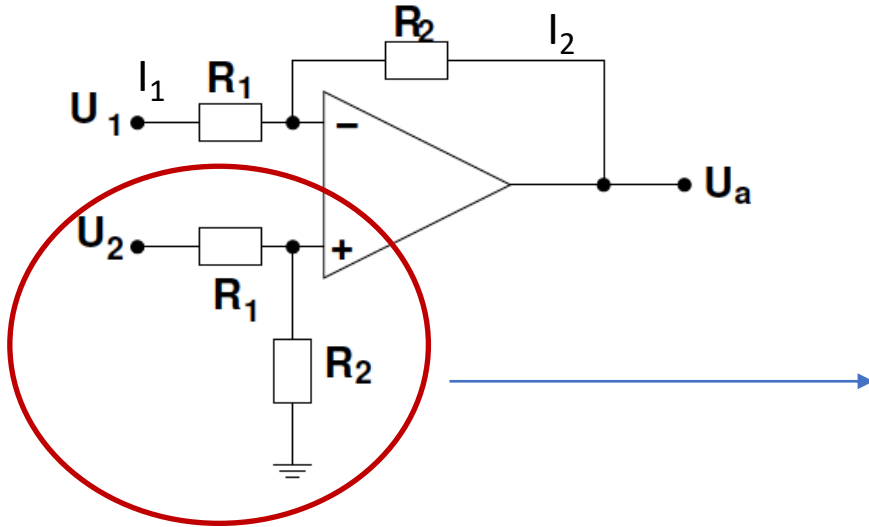
$$\rightarrow \frac{U_1 R_2}{R_1} - \frac{U R_2}{R_1} = U - U_a$$

$$\rightarrow U_a = U \frac{R_2 + R_1}{R_1} - U_1 \frac{R_2}{R_1} \quad (*)$$

- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]
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# Op amp circuits

Differential amplifier (negative feedback)



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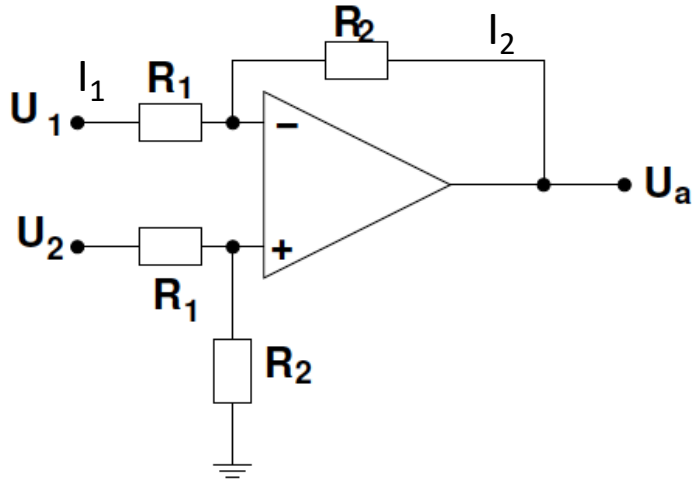
$$\rightarrow U_a = U \frac{R_2 + R_1}{R_1} - U_1 \frac{R_2}{R_1} \quad (*)$$

$$U = U_2 \frac{R_2}{R_1 + R_2} \quad (\text{voltage divider}) \quad (**)$$

- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]
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# Op amp circuits

Differential amplifier (negative feedback)



$$[1] \quad U_- = U_+ = U$$

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(\*\*) in (\*)

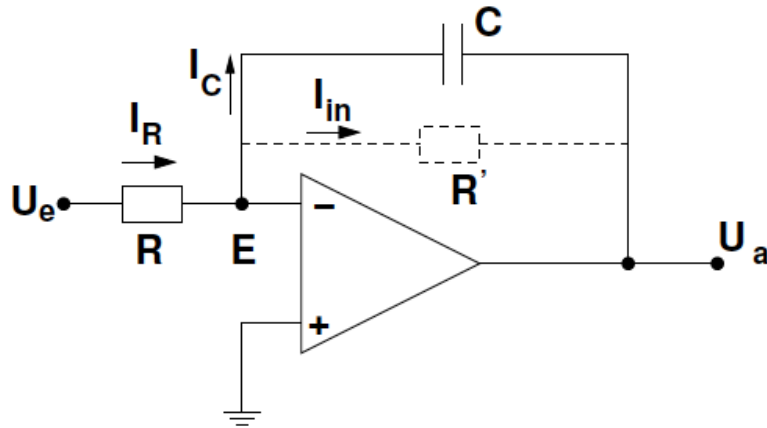
$$\rightarrow U_a = U_2 \frac{R_2}{R_1 + R_2} \frac{R_1 + R_2}{R_1} - U_1 \frac{R_2}{R_1}$$

$$\rightarrow U_a = \frac{R_2}{R_1} (U_2 - U_1)$$

- If used with negative feedback ( $U_a$  connected with  $U_-$ ) the op amp regulates  $U_+ = U_-$  [1]
- Negligible input current (into the op amp) [2]

# Op amp circuits

Integrator (negative feedback)

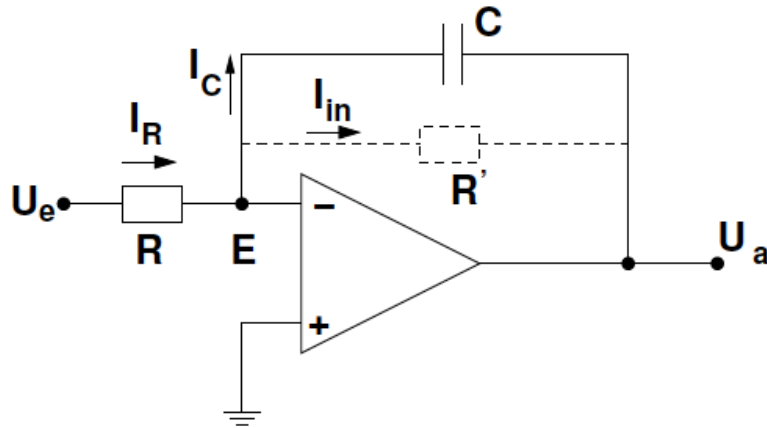


Virtual ground offset by input current  
→ op amp passes a current that charges the capacitor to maintain the virtual ground

$$[2] \quad I_R = \frac{U_e}{R} \approx I_C$$

# Op amp circuits

Integrator (negative feedback)



Virtual ground offset by input current  
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$$[2] \quad I_R = \frac{U_e}{R} \approx I_C$$

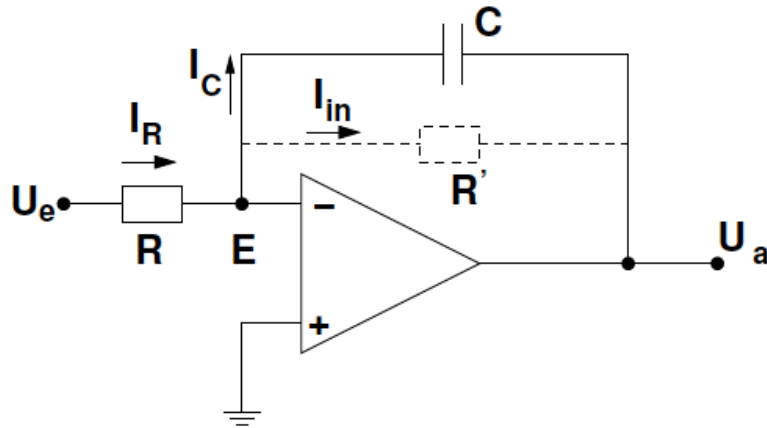
Capacitor equation:

- Differential:  $I = C \frac{dU}{dt}$

- Integrated:  $U = \frac{1}{C} \int I dt \quad (*)$

# Op amp circuits

Integrator (negative feedback)



Capacitor equation:

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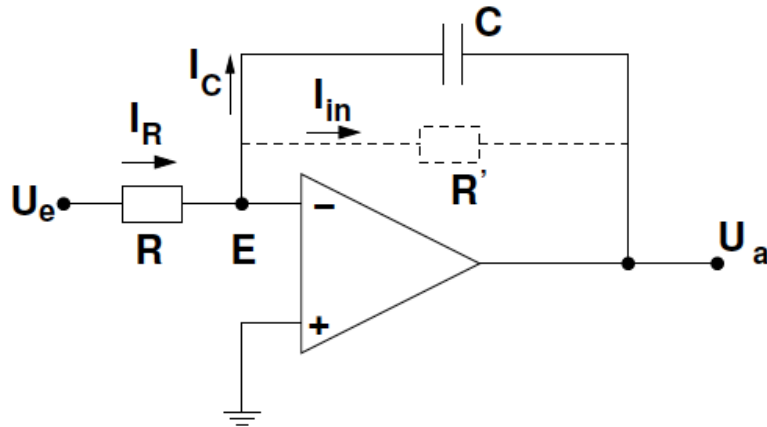
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with(\*):

$$U_a = -\frac{1}{C} \int_0^t I_c dt$$

# Op amp circuits

## Integrator (negative feedback)



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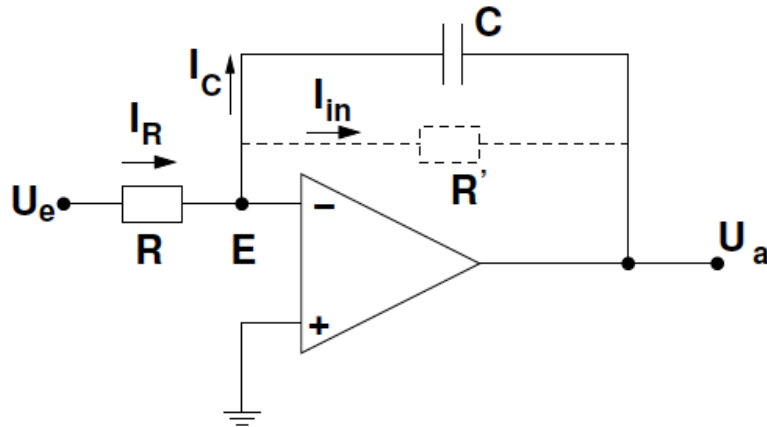
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$$U_a = -\frac{1}{C} \int_0^t I_c dt = -\frac{1}{RC} \int_0^t U_e dt$$

# Op amp circuits

## Integrator (negative feedback)



Capacitor equation:

- Differential:  $I = C \frac{dU}{dt}$

- Integrated:  $U = \frac{1}{C} \int I dt$  (\*)

Virtual ground offset by input current  
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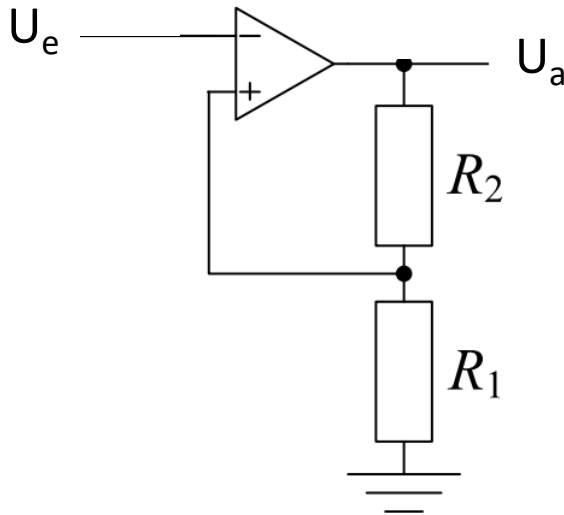
$$U_a = -\frac{1}{C} \int_0^t I_c dt = -\frac{1}{RC} \int_0^t U_e dt$$

→ The output voltage is proportional to the time integrated input voltage

# Op amp circuits

Schmitt trigger: positive feedback

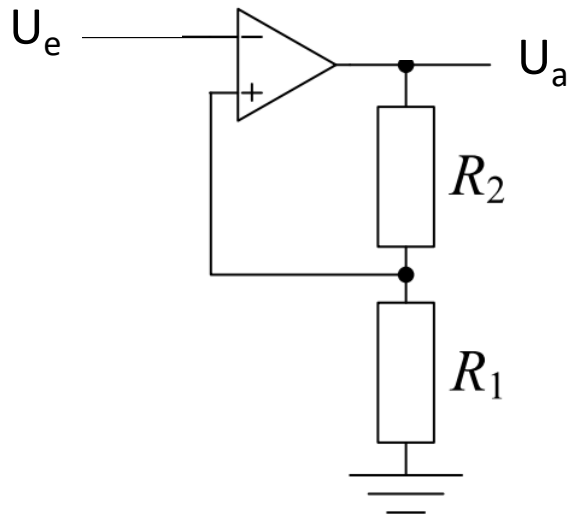
If  $U_a$  rises, the difference between  $U_-$  and  $U_+$  will rise. This causes  $U_a$  to rise even further until maximum output voltage (given by the power supply voltage) is reached



$$U_a = v_0 \cdot (U^+ - U^-)$$

# Op amp circuits

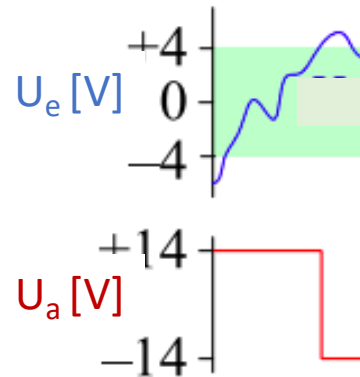
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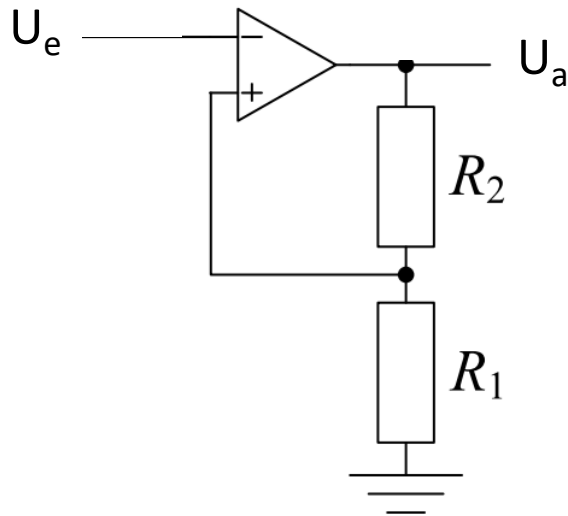
If  $U_a$  rises, the difference between  $U_-$  and  $U_+$  will rise. This causes  $U_a$  to rise even further until maximum output voltage (given by the power supply voltage) is reached

Example:  $U_{\max} = 14\text{V}$ ,  $R_1 = 10\Omega$ ,  $R_2 = 4\Omega$   
If  $U_a = 14\text{V}$ ,  $U_+ = 4\text{V}$ .



# Op amp circuits

## Schmitt trigger: positive feedback



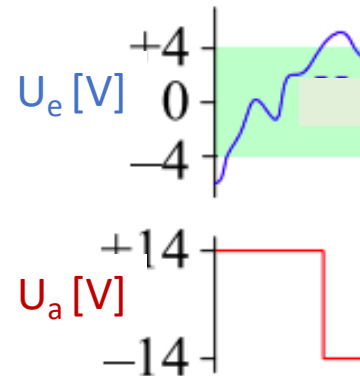
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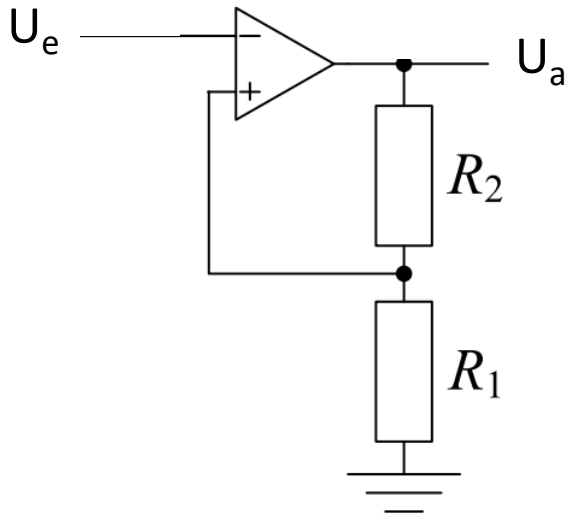
If  $U_a = 14\text{V}$ ,  $U_+ = 4\text{V}$ .

If  $U_e$  exceeds 4V,  $U_- > U_+$  and  $U_a$  flips to  $-14\text{V}$



# Op amp circuits

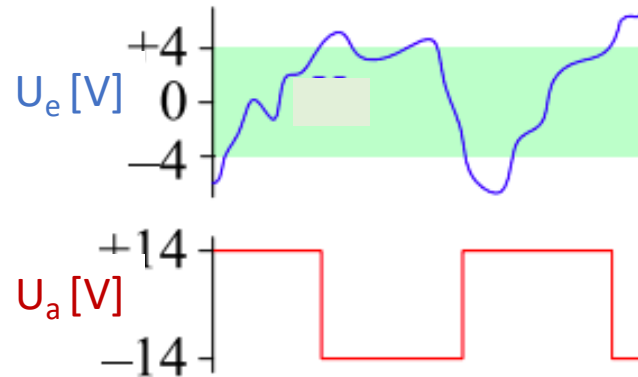
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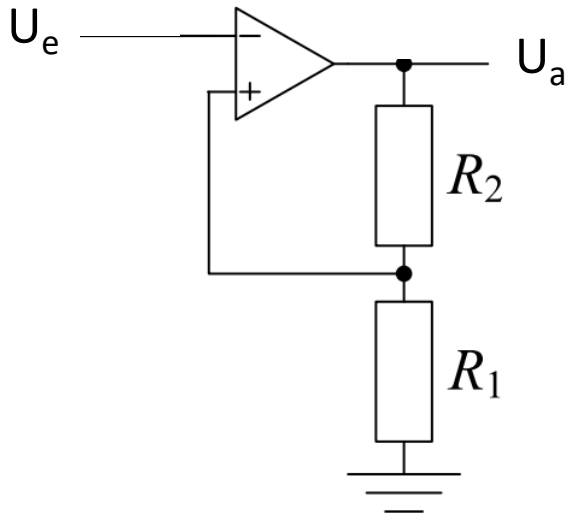
If  $U_a$  rises, the difference between  $U_-$  and  $U_+$  will rise. This causes  $U_a$  to rise even further until maximum output voltage (given by the power supply voltage) is reached

Example:  $U_{\max} = 14\text{V}$ ,  $R_1 = 10\Omega$ ,  $R_2 = 4\Omega$   
If  $U_a = -14\text{V}$ ,  $U^+ = -4\text{V}$ .



# Op amp circuits

Schmitt trigger: positive feedback



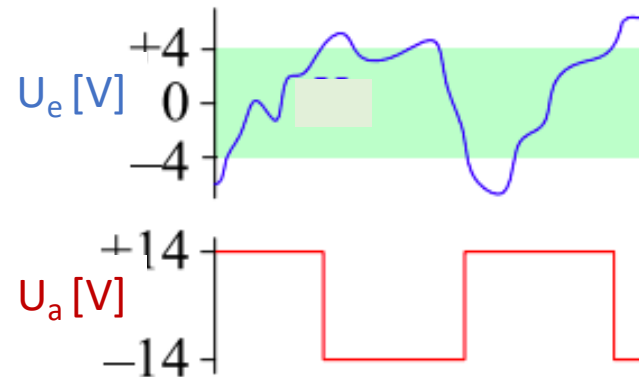
$$U_a = v_0 \cdot (U^+ - U^-)$$

If  $U_a$  rises, the difference between  $U_-$  and  $U_+$  will rise. This causes  $U_a$  to rise even further until maximum output voltage (given by the power supply voltage) is reached

Example:  $U_{\max} = 14\text{V}$ ,  $R_1 = 10\Omega$ ,  $R_2 = 4\Omega$

If  $U_a = -14\text{V}$ ,  $U^+ = -4\text{V}$ .

If  $U_e$  exceeds  $-4\text{V}$ ,  $U_- < U_+$  and  $U_a$  flips to  $+14\text{V}$





## (3) Digital electronics

# Digital electronics

Work with only two **voltage levels** (depend on type and input/output)

- High: 1, typically 2-5V
- Low : 0, typically 0-1.5V

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○ **Hexadecimal 4-bit groups:**

0000	0	0100	4	1000	8	1100	C
0001	1	0101	5	1001	9	1101	D
0010	2	0110	6	1010	A	1110	E
0011	3	0111	7	1011	B	1111	F

Example:

- Decimal: 2025
- Binary: 0111 1110 1010
- Hexadecimal: 7EA

# Digital electronics

Work with only two **voltage levels** (depend on type and input/output)

- High: 1, typically 2-5V
- Low : 0, typically 0-1.5V

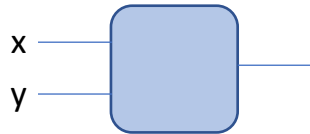
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Example:

- Decimal: 2025
- Binary: 0111 1110 1010
- Hexadecimal: 7EA

○ **Boolean algebra**



AND OR

$x$	$y$	$x \wedge y$	$x \vee y$
0	0	0	0
1	0	0	1
0	1	0	1
1	1	1	1

NOT

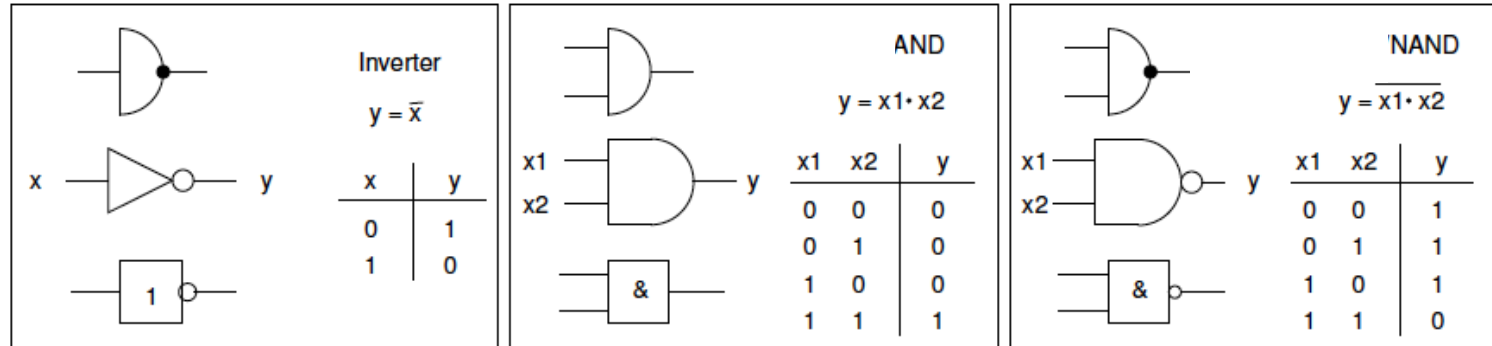
$x$	$\neg x$
0	1
1	0

Laws:

- Associativity
- Commutativity
- Distributivity

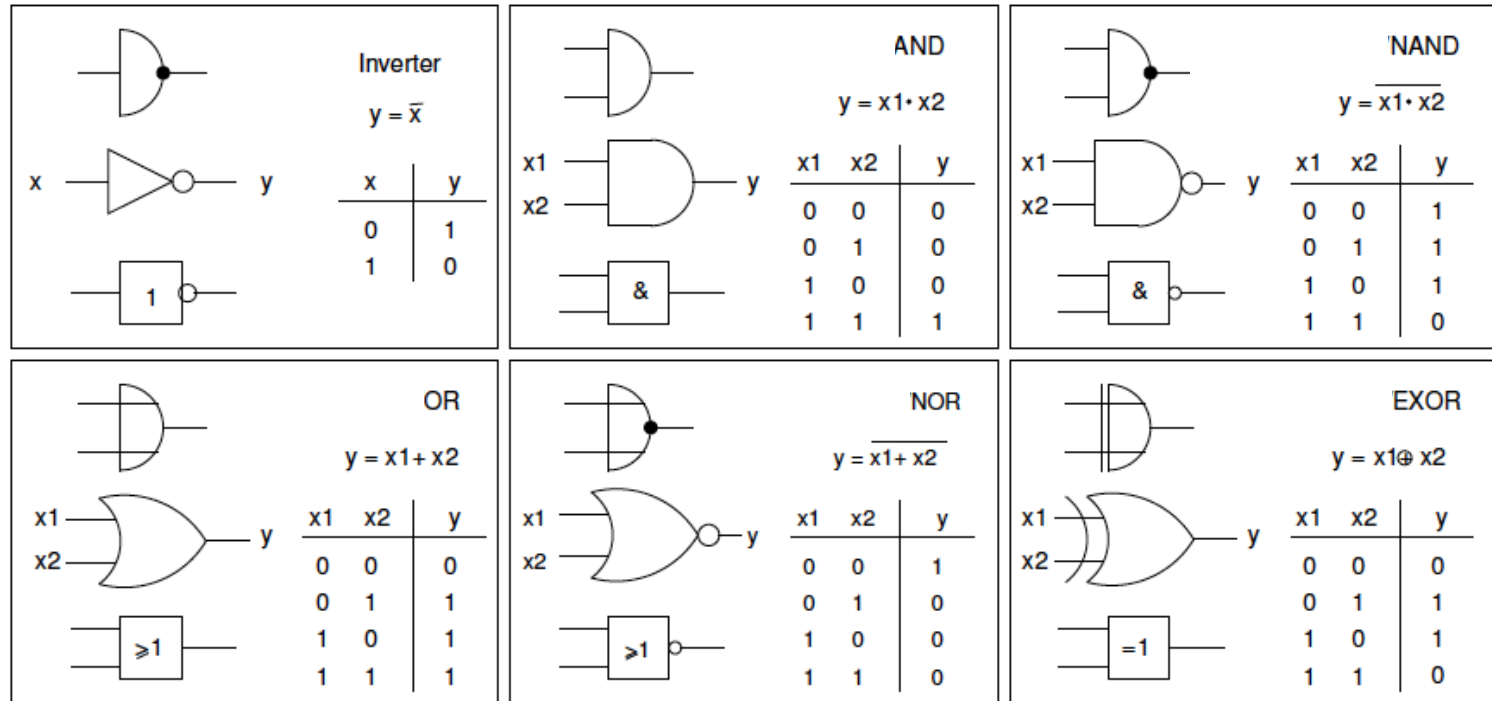
# Logical operations

Full table of symbols, including secundar operations



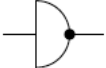
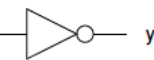
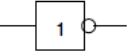
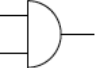

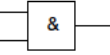
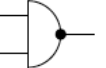

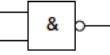
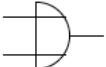
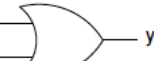
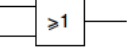
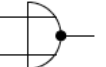

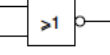

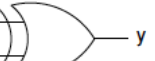
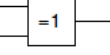
# Logical operations

Full table of symbols, including secundar operations

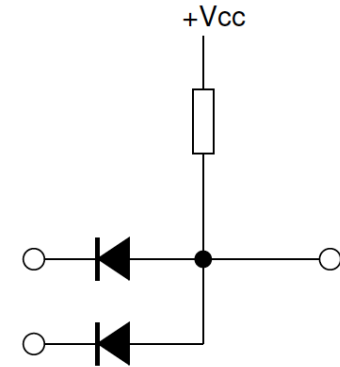


# Logical operations

Full table of symbols, including secundar operations

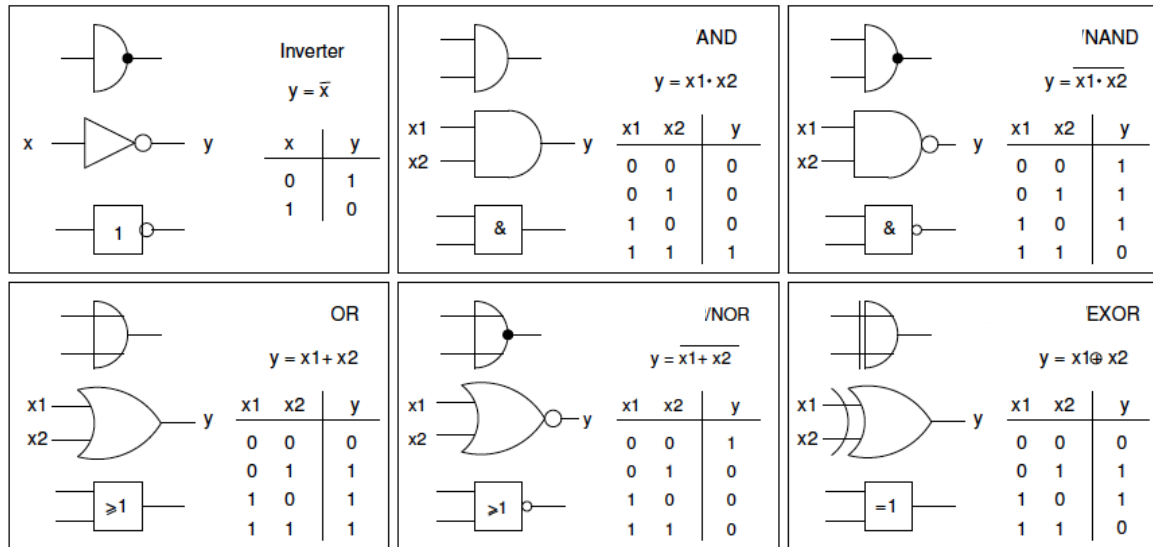
 <p>Inverter <math>y = \bar{x}</math></p> <p><math>x</math>  <math>y</math></p> <table border="1" data-bbox="343 539 459 615"> <thead> <tr> <th>x</th> <th>y</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table> <p></p>	x	y	0	1	1	0	 <p>AND <math>y = x_1 \cdot x_2</math></p> <p><math>x_1</math> <math>x_2</math>  <math>y</math></p> <table border="1" data-bbox="697 515 846 659"> <thead> <tr> <th><math>x_1</math></th> <th><math>x_2</math></th> <th><math>y</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p></p>	$x_1$	$x_2$	$y$	0	0	0	0	1	0	1	0	0	1	1	1	 <p>'NAND <math>y = \overline{x_1 \cdot x_2}</math></p> <p><math>x_1</math> <math>x_2</math>  <math>y</math></p> <table border="1" data-bbox="1089 515 1238 659"> <thead> <tr> <th><math>x_1</math></th> <th><math>x_2</math></th> <th><math>y</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p></p>	$x_1$	$x_2$	$y$	0	0	1	0	1	1	1	0	1	1	1	0									
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 <p>OR <math>y = x_1 + x_2</math></p> <p><math>x_1</math> <math>x_2</math>  <math>y</math></p> <table border="1" data-bbox="324 791 459 935"> <thead> <tr> <th><math>x_1</math></th> <th><math>x_2</math></th> <th><math>y</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table> <p></p>	$x_1$	$x_2$	$y$	0	0	0	0	1	1	1	0	1	1	1	1	 <p>/NOR <math>y = \overline{x_1 + x_2}</math></p> <p><math>x_1</math> <math>x_2</math>  <math>y</math></p> <table border="1" data-bbox="697 791 846 935"> <thead> <tr> <th><math>x_1</math></th> <th><math>x_2</math></th> <th><math>y</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p></p>	$x_1$	$x_2$	$y$	0	0	1	0	1	0	1	0	0	1	1	0	 <p>EXOR <math>y = x_1 \oplus x_2</math></p> <p><math>x_1</math> <math>x_2</math>  <math>y</math></p> <table border="1" data-bbox="1089 791 1238 935"> <thead> <tr> <th><math>x_1</math></th> <th><math>x_2</math></th> <th><math>y</math></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table> <p></p>	$x_1$	$x_2$	$y$	0	0	0	0	1	1	1	0	1	1	1	0
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Simple diode-based  
AND gate

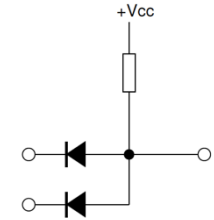


# Logical operations

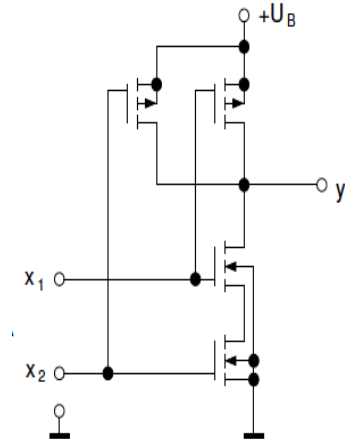
## Full table of symbols, including secundar operations



## Simple diode-based AND gate



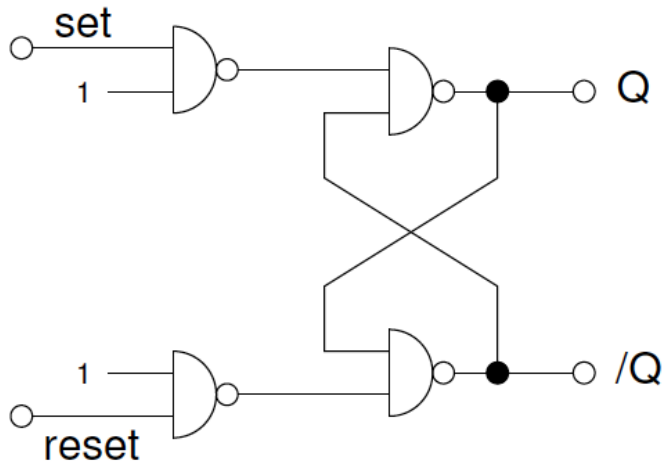
## CMOS-based NAND gate



# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

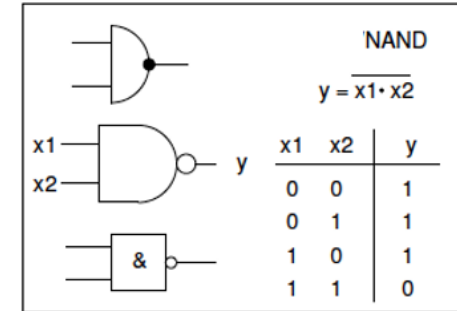
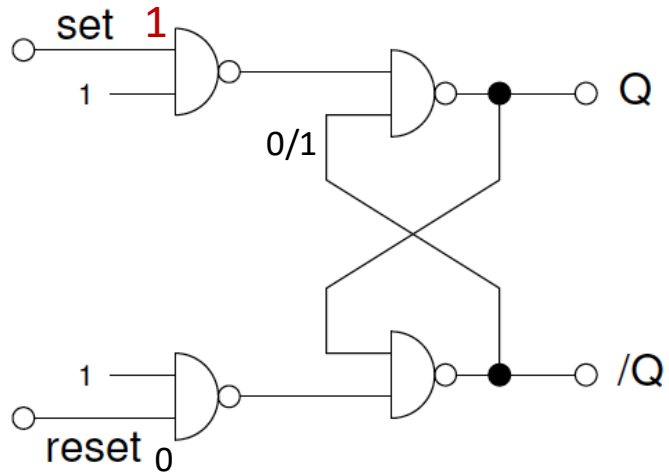
## Simple SR (set-reset) Latch



# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

## Simple SR Latch

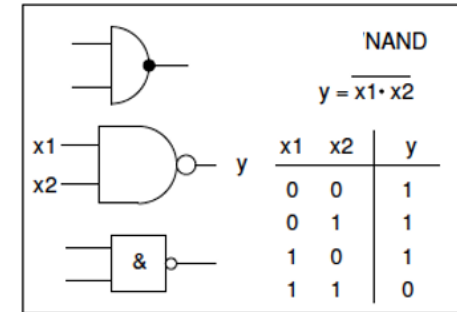
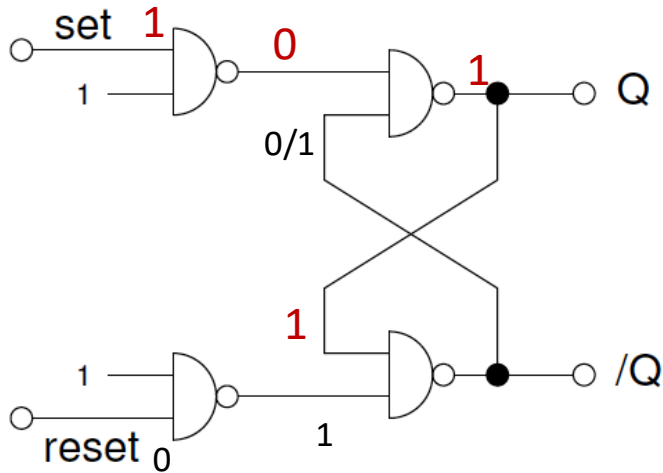




# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

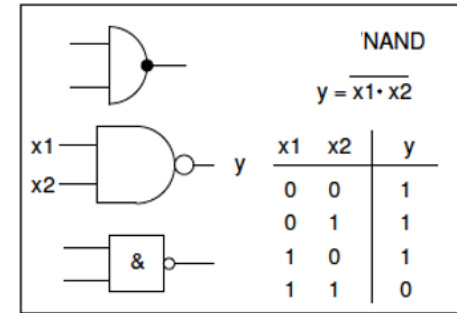
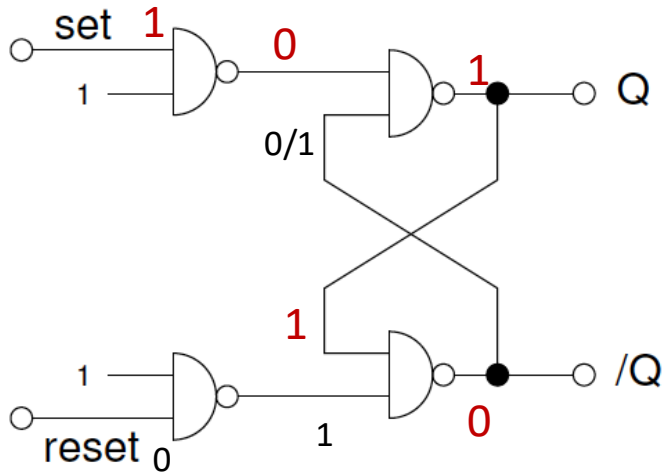
## Simple SR Latch



# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

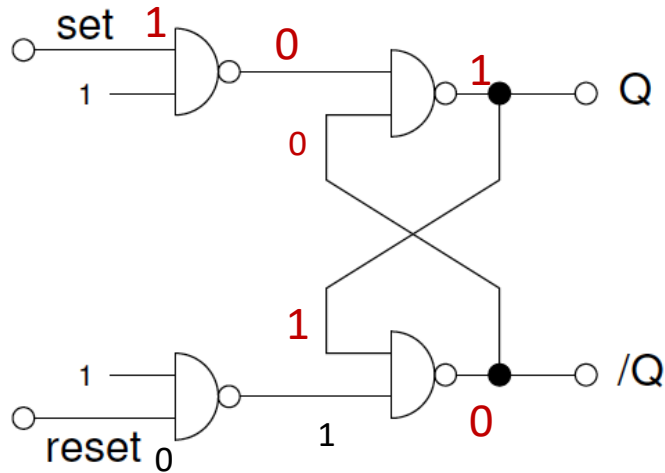
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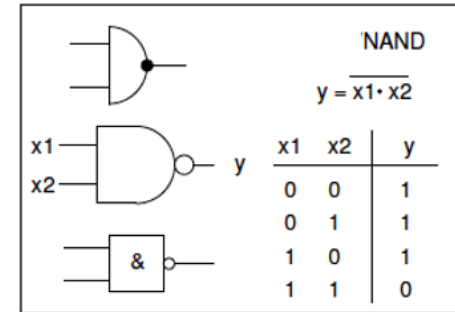
# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

## Simple SR Latch



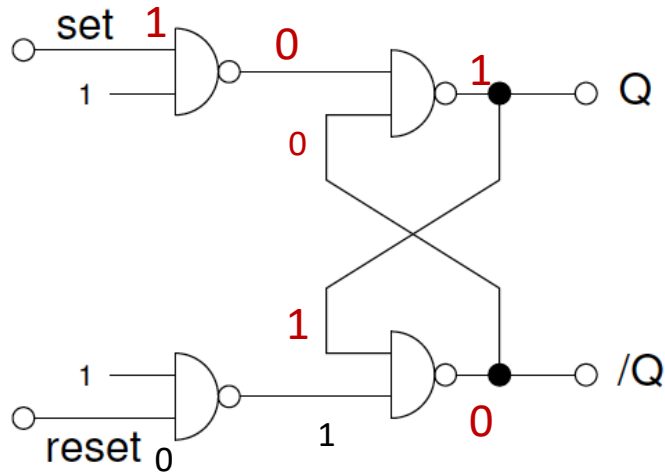
*stable situation*



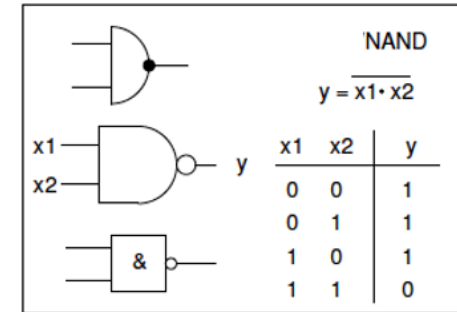
# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

## Simple SR Latch



*stable situation*

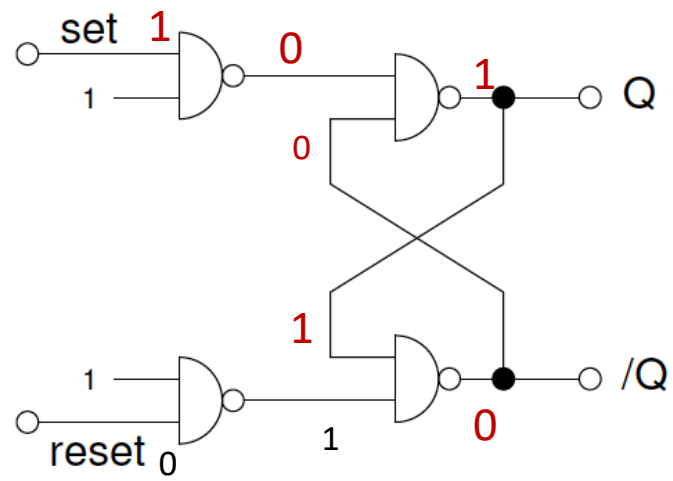


*Likewise, setting the reset to 1 and the set to 0, will lead to the inverse stable Situation*

# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

## Simple SR Latch



*stable situation*

		NAND	
		$y = \overline{x1 \cdot x2}$	
x1	x2	y	
0	0	1	
0	1	1	
1	0	1	
1	1	0	

*Likewise, setting the reset to 1 and the set to 0, will lead to the inverse stable situation*

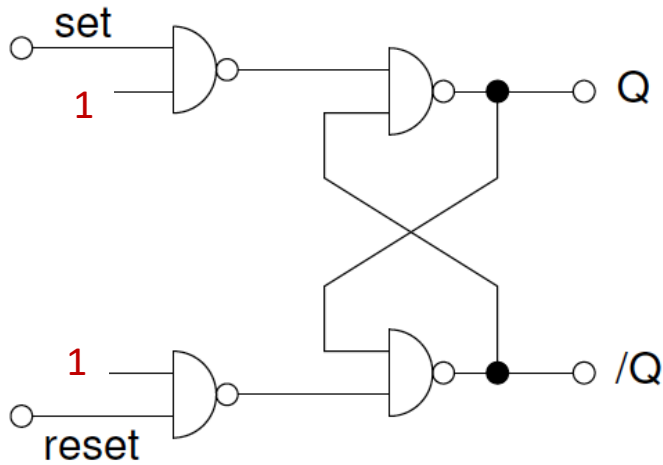
*If the second inputs are 0, Q does not change latch is "opaque"*

*→ Gated or clocked SR latch*

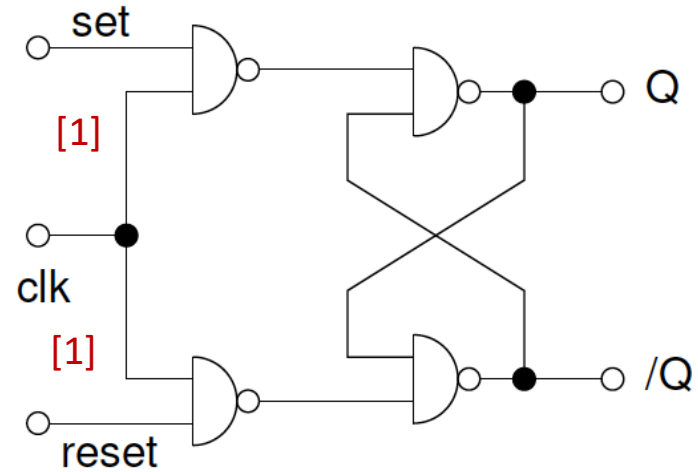
# Flip Flop: SR latch

Flip flops (latches) are digital circuits with two stable states → store information

## Simple SR Latch



## Clocked SR Latch

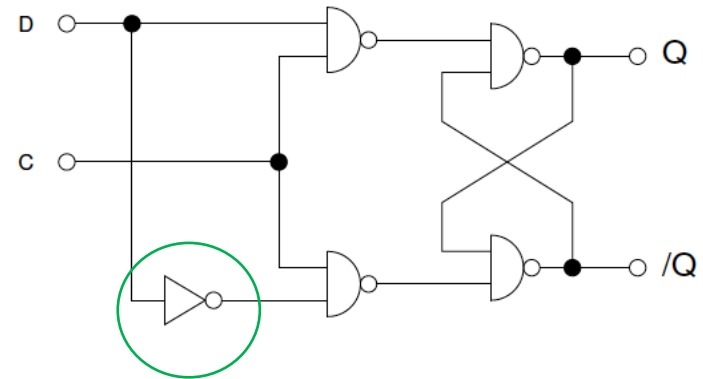


*clk provides "1" in a clocked way*

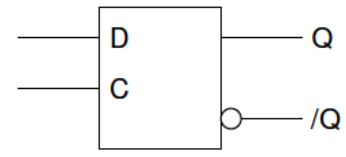
# D-latch and serial register

Flip flops (latches) are digital circuits with two stable states → store information

D- Latch: only “set” input needed, due to inverter



symbol:



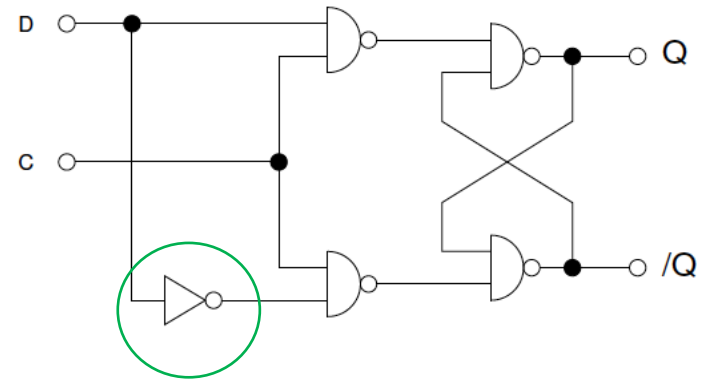
Truth table:

C	D	Q	$\bar{Q}$	Comment
0	X	$Q_{prev}$	$\bar{Q}_{prev}$	No change
1	0	0	1	Reset
1	1	1	0	Set

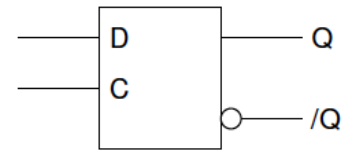
# D-latch and serial register

Flip flops (latches) are digital circuits with two stable states → store information

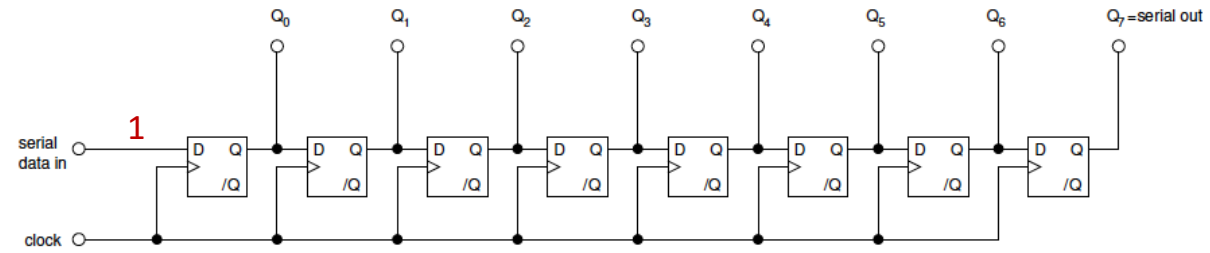
D- Latch: only “set” input needed, due to inverter



symbol:



.... can be used to construct serial shift register

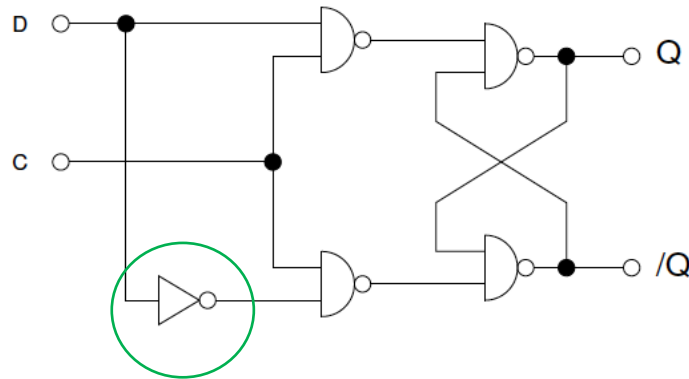


Goal:  
store “0101”

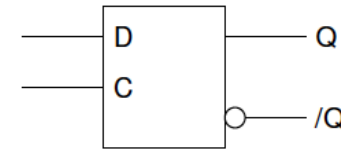
# D-latch and serial register

Flip flops (latches) are digital circuits with two stable states → store information

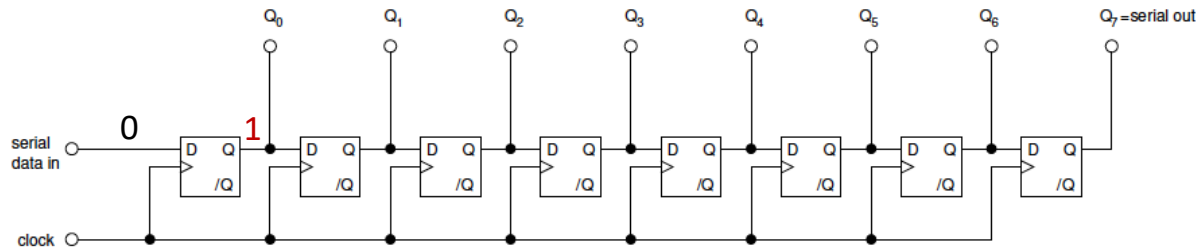
D- Latch: only “set” input needed, due to inverter



symbol:



.... can be used to construct serial shift register

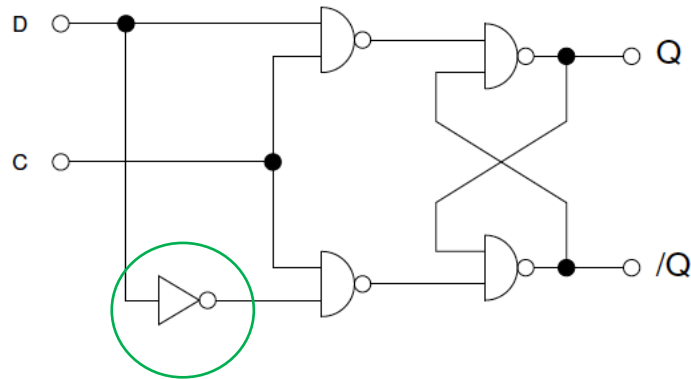


Goal:  
store “0101”

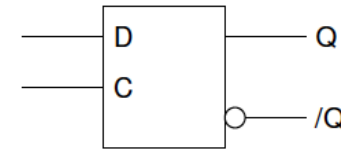
# D-latch and serial register

Flip flops (latches) are digital circuits with two stable states → store information

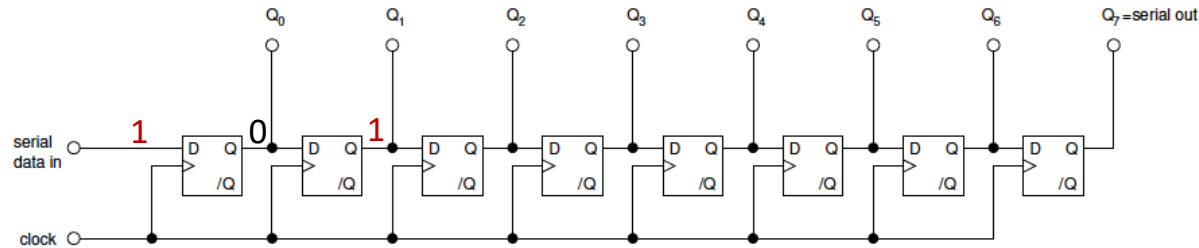
**D- Latch:** only “set” input needed, due to **inverter**



symbol:



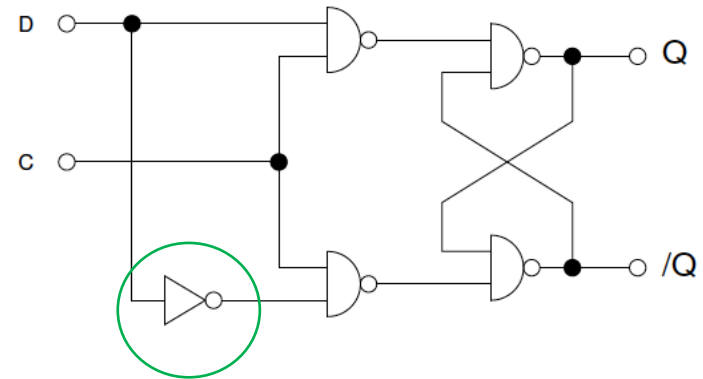
.... can be used to construct **serial shift register**



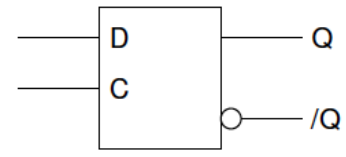
# D-latch and serial register

Flip flops (latches) are digital circuits with two stable states → store information

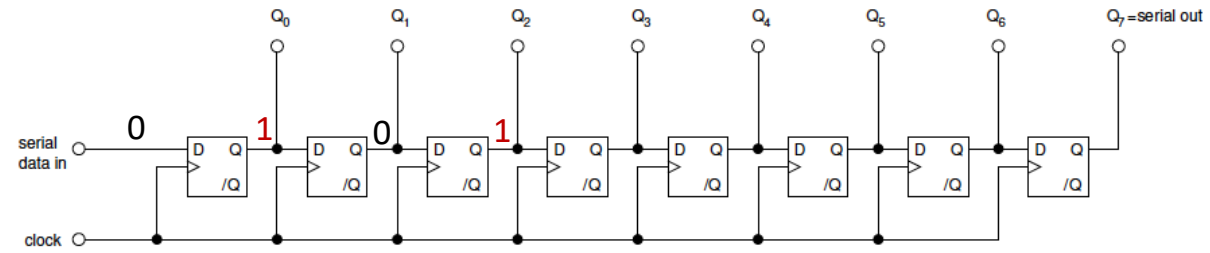
D- Latch: only “set” input needed, due to inverter



symbol:



.... can be used to construct serial shift register





Many thanks for attending!

Any questions?



## (4) Circuit analysis, topologies

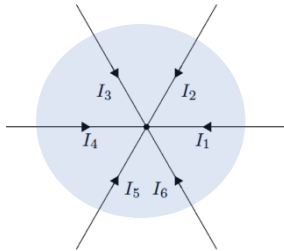
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Basic circuit analysis can be performed based on the two Kirchhoff laws:

## Junction rule or Kirchhoff's Current Law (KCL):

The currents flowing out of any closed  
Region of a circuit sum to 0

$$\sum_{k=1}^n I_k = 0$$



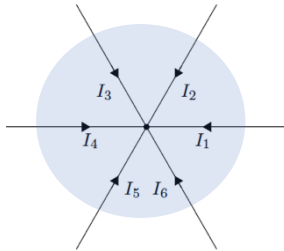
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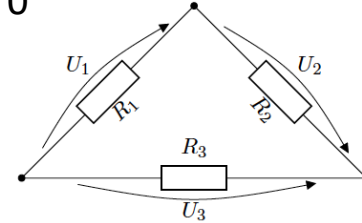
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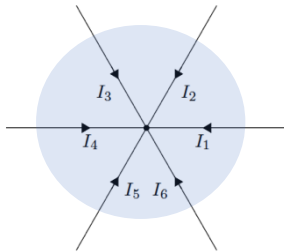
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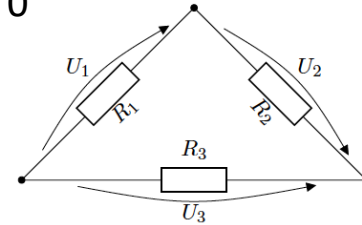
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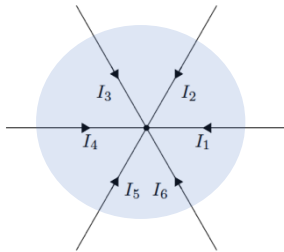
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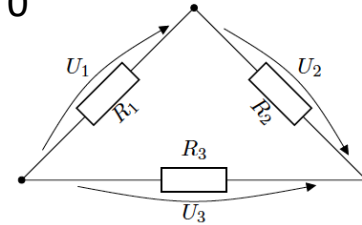
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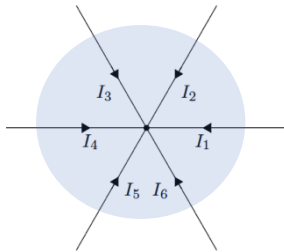
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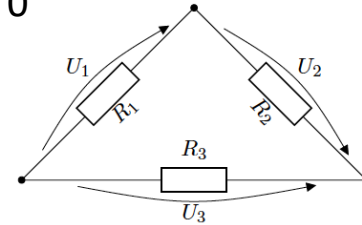
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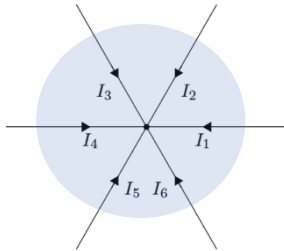
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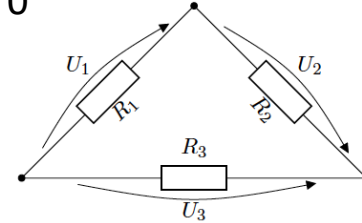
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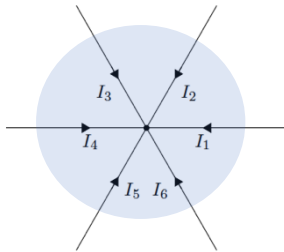
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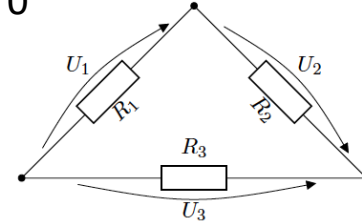
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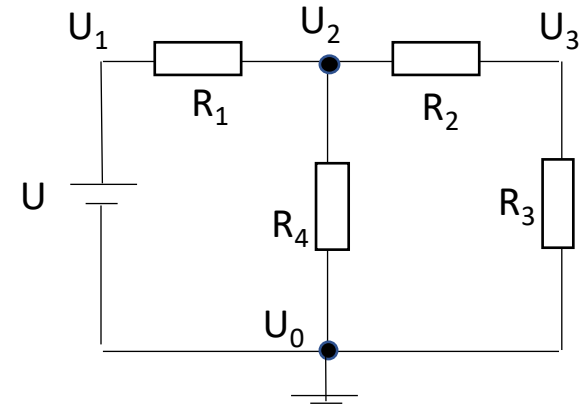
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- Norton equivalent: replace part of the network by source and resistance in parallel

# Nodal Analysis

Node: section of the circuit which connects components.

Aim: determine the voltage at each node relative to a reference node, then use them to derive the other relevant quantities



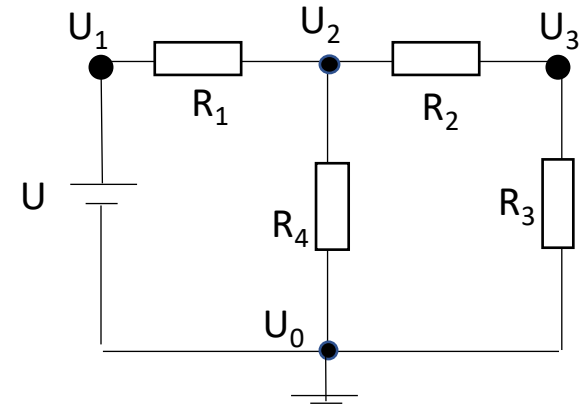
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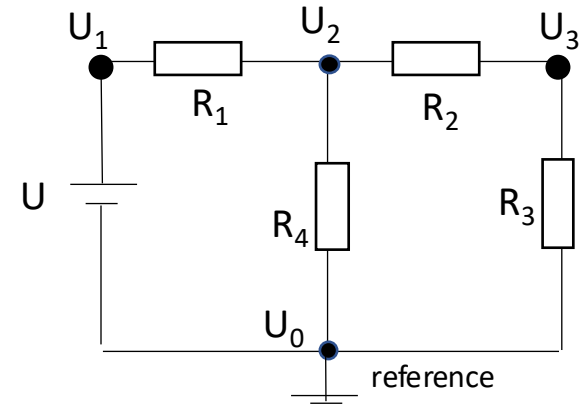
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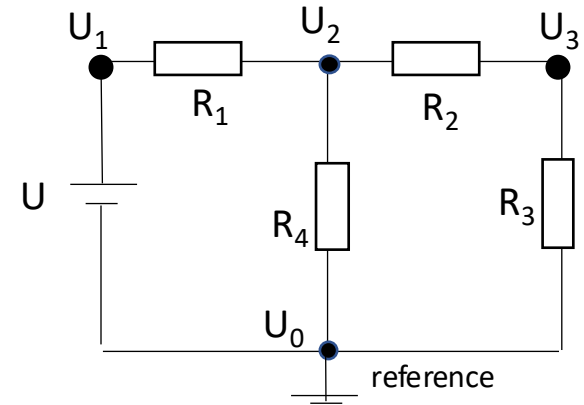
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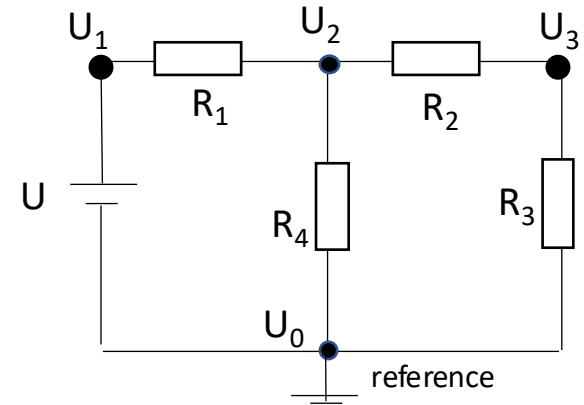
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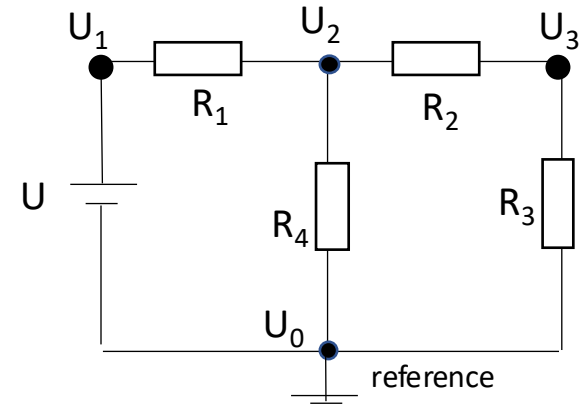
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Example:  $U_0$ :  $U_0 = 0V$

$U_1$ :  $U_1 = U$

$U_2$  KCL:  $\frac{U_1 - U_2}{R_1} = \frac{U_2 - U_0}{R_4} + \frac{U_2 - U_3}{R_2}$

$U_3$  KCL:  $\frac{U_2 - U_3}{R_2} = \frac{U_3 - U_0}{R_3}$



# Nodal Analysis

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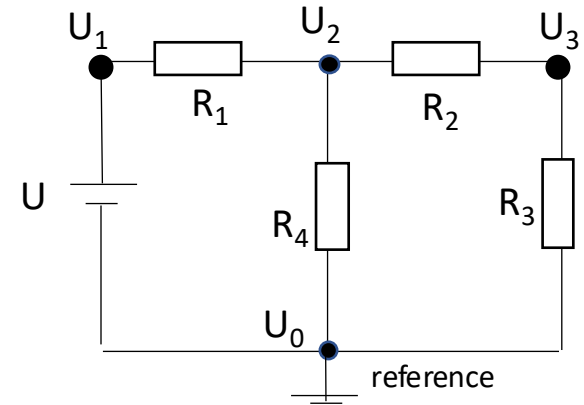
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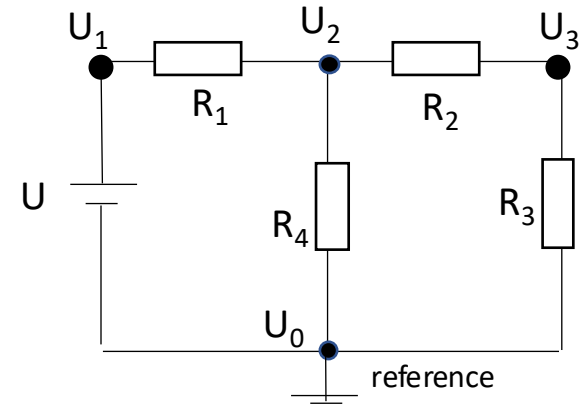
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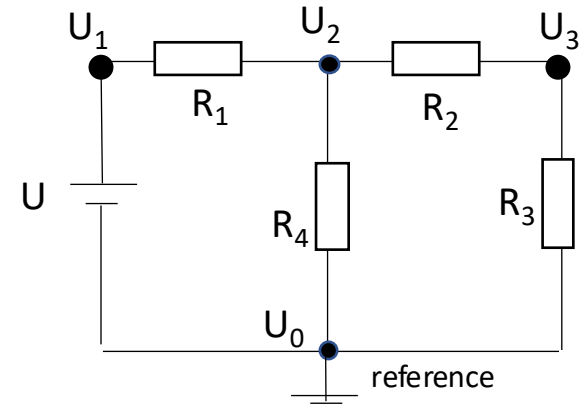
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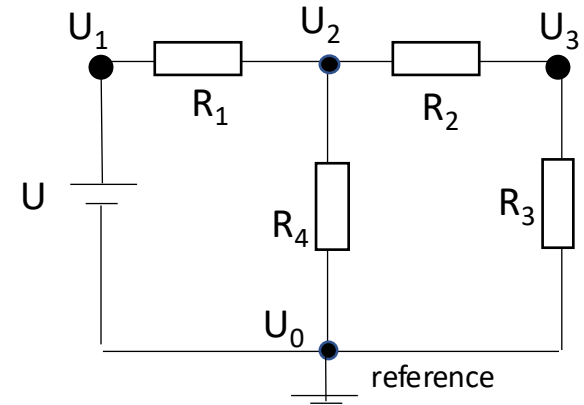
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$$\rightarrow U_3 = \frac{G_1 G_2 U}{G_2(G_1 + G_4) + G_3(G_1 + G_2 + G_4)}$$

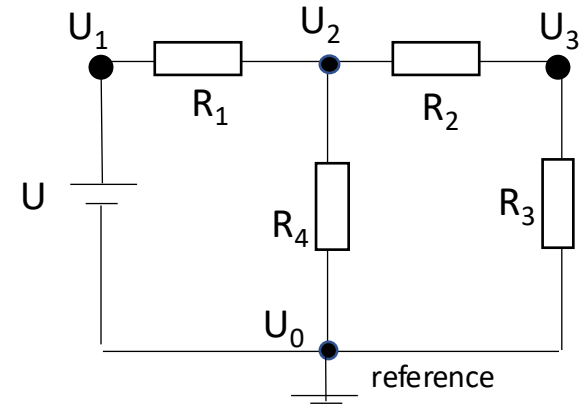
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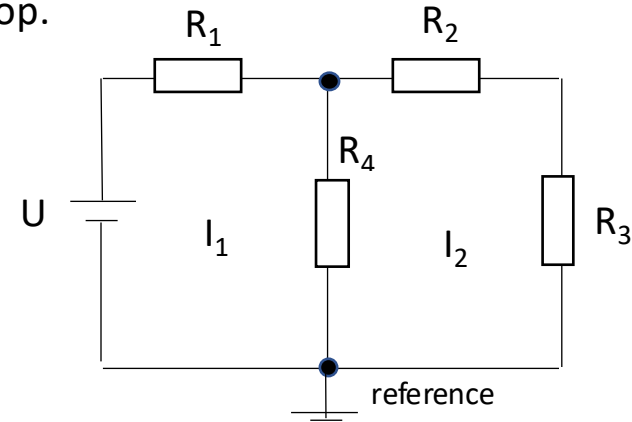
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# Mesh current Analysis

Essential mesh: loop in the circuit that does not contain any other loop.  
Aim: determine the current through each mesh



# Mesh current Analysis

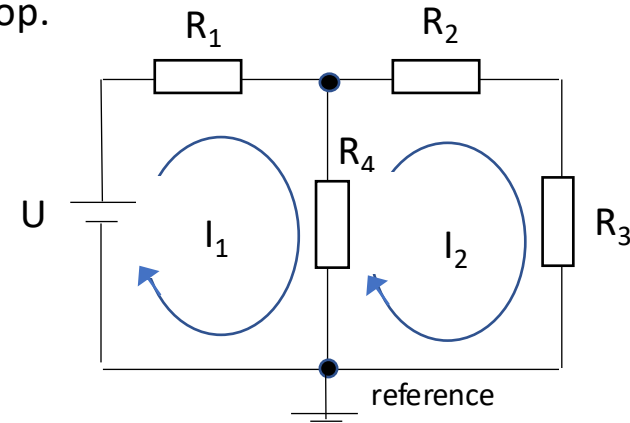
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Steps:

- Identify all essential meshes and assign mesh current (special treatment for dependent sources and current sources which are part of two meshes)
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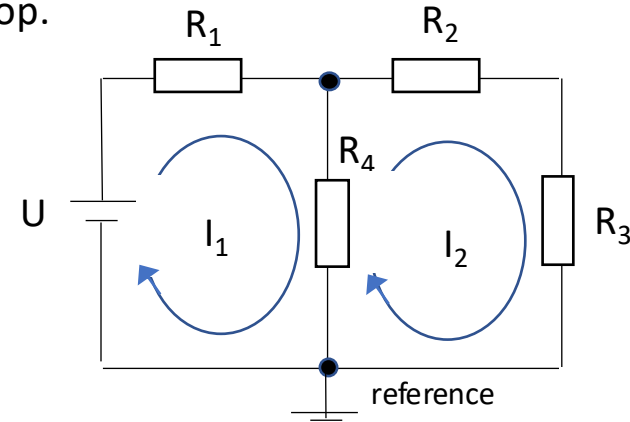
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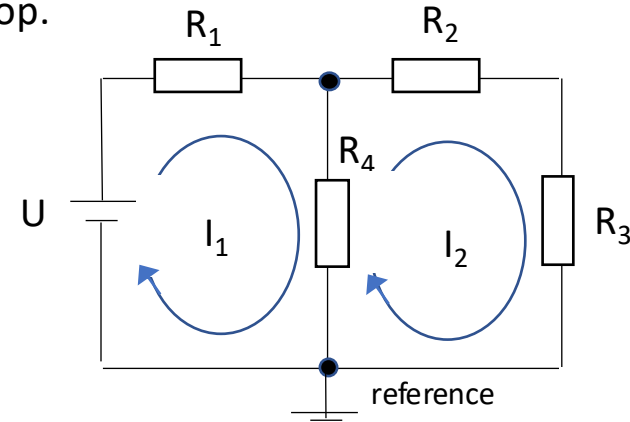
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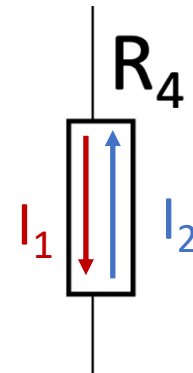
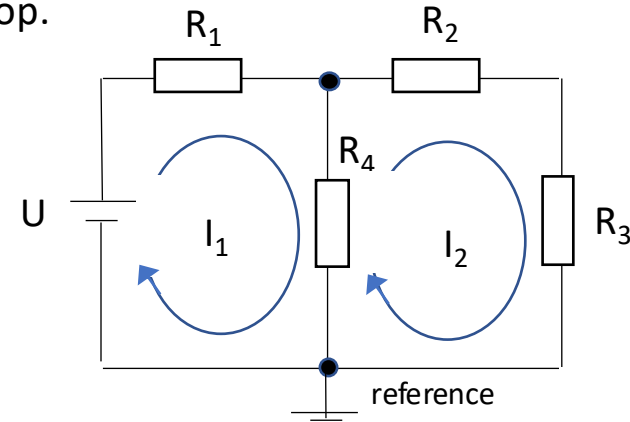
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Mesh 2:  $R_4(I_2 - I_1) + R_2 I_2 + R_3 I_2 = 0$



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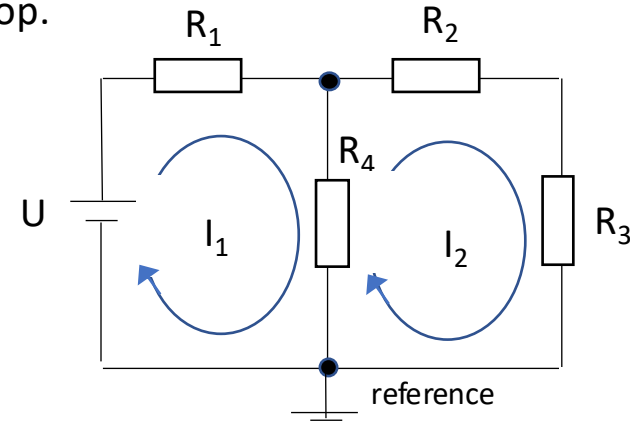
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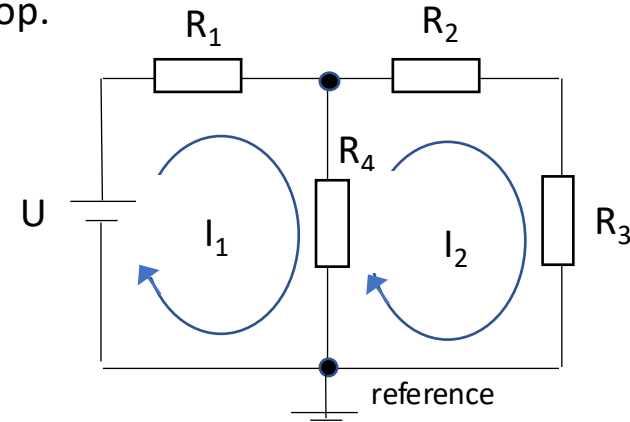
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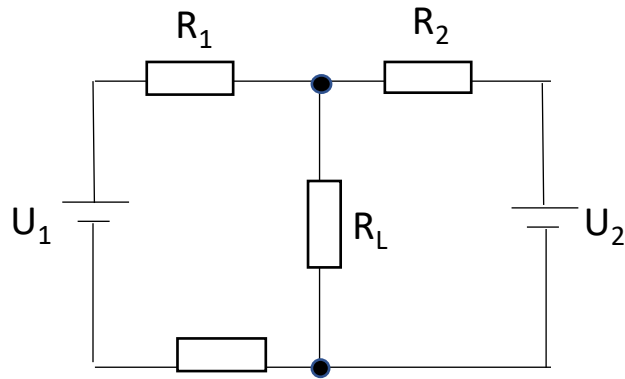
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$$\rightarrow I_1 = \frac{(R_2 + R_3 + R_4) U}{(R_1 + R_4)(R_2 + R_3 + R_4) - R_4^2} \rightarrow I_2$$

# Thevenin equivalent circuit

*Thevenin's theorem: Any linear circuit containing several voltage sources and resistances can be replaced by a single voltage in series with a single resistance connected across the load“*

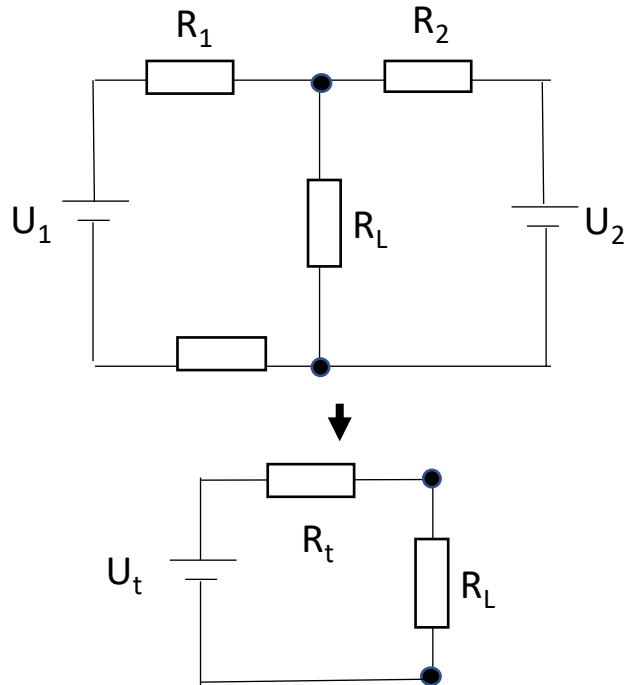
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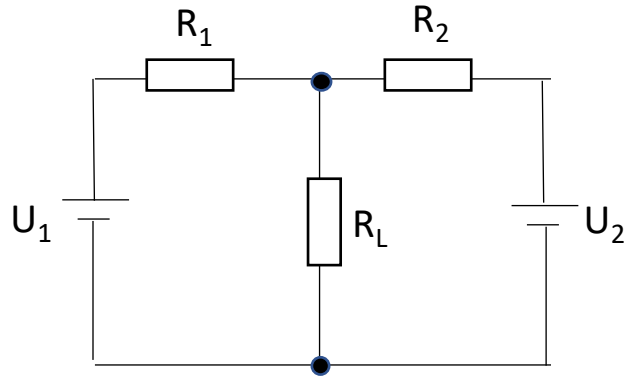
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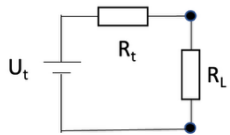
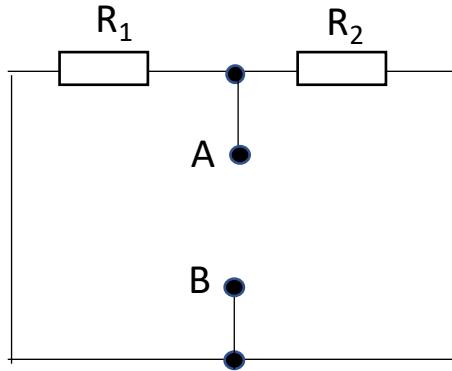
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Example circuit:



Step1: remove load and shorten sources. Then calculate total Thevenin resistance  $R_T$  wrt A/B

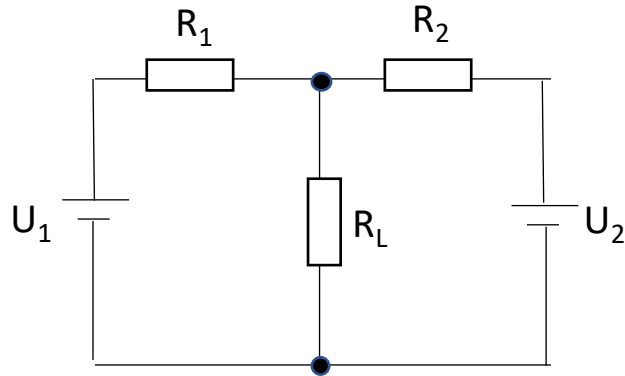


$$R_T = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

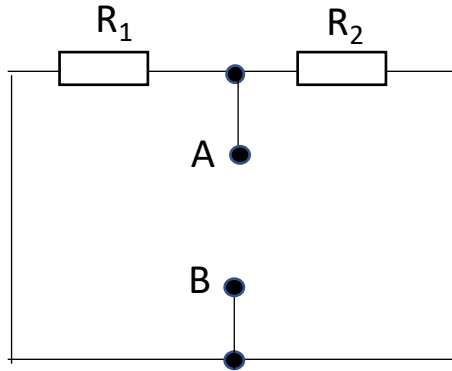
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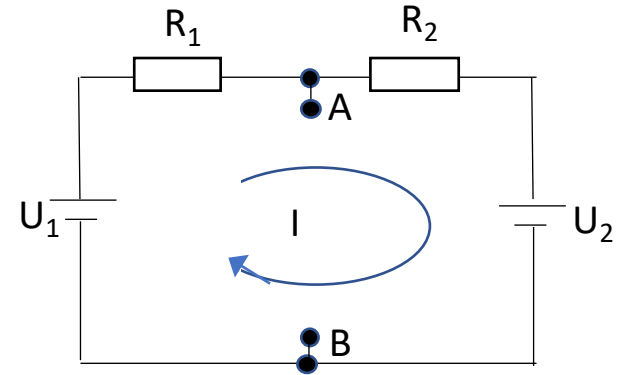


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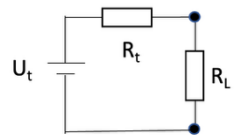
$$R_T = R_1 || R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Step2: Reconnect sources. Calculate Thevenin voltage  $U_T$



$$I = \frac{U_1 - U_2}{R_1 + R_2} \quad (*)$$

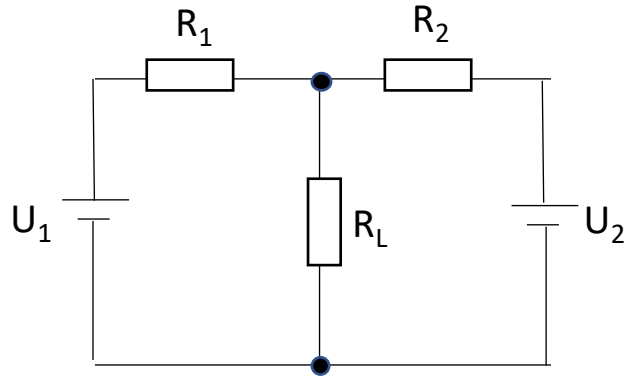
$$U_T = U_{AB} = U_1 - IR_1 = U_2 + IR_2$$



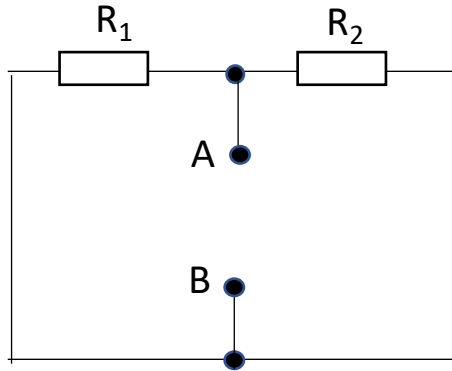
# Thevenin equivalent circuit

*Thevenin's theorem: Any linear circuit containing several voltage sources and resistances can be replaced by a single voltage in series with a single resistance connected across the load“*

Example circuit:

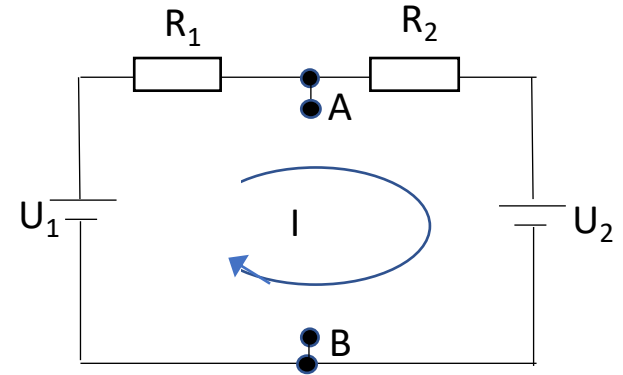


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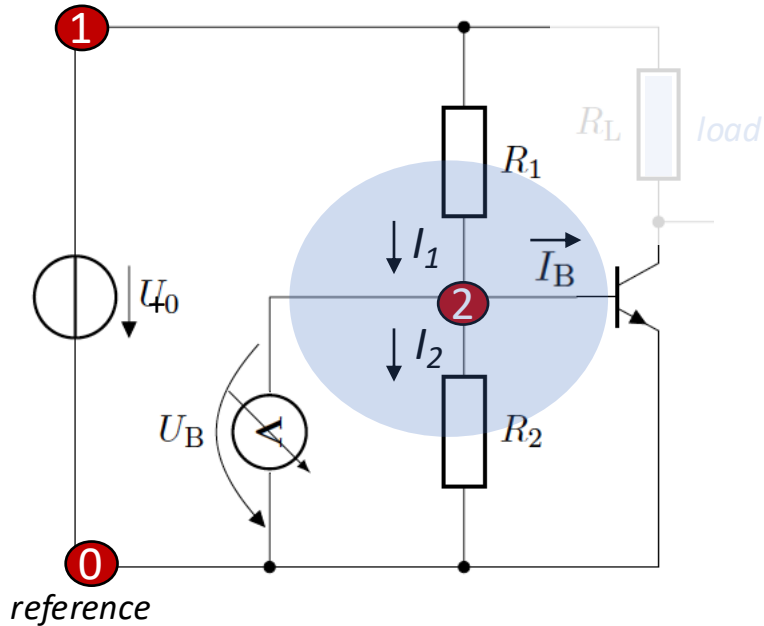


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# Example: nodal analysis

## Revisiting Voltage divider biasing circuit



Reminder: The voltage  $U_B$  across  $R_2$  forward-biases the BE junction

Here: can use **nodal analysis**:

Apply Kirchhoff's current law (KCL) at **node 2**

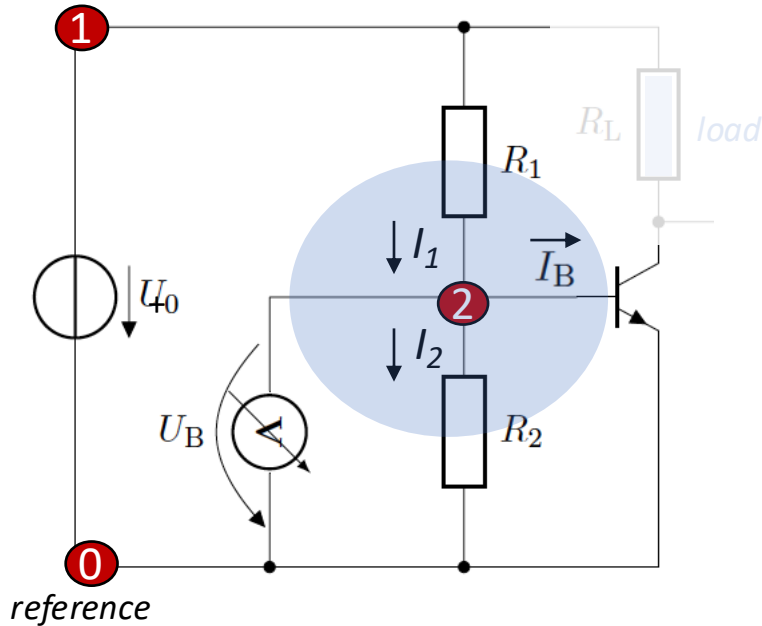
*Reminder the  $I_B - U_B$  relation does not follow Ohms law but a diode-like input characteristics (which for this exercise, we pretend not to know)*

$$U_1: \quad U_1 = U_0 \quad (1)$$

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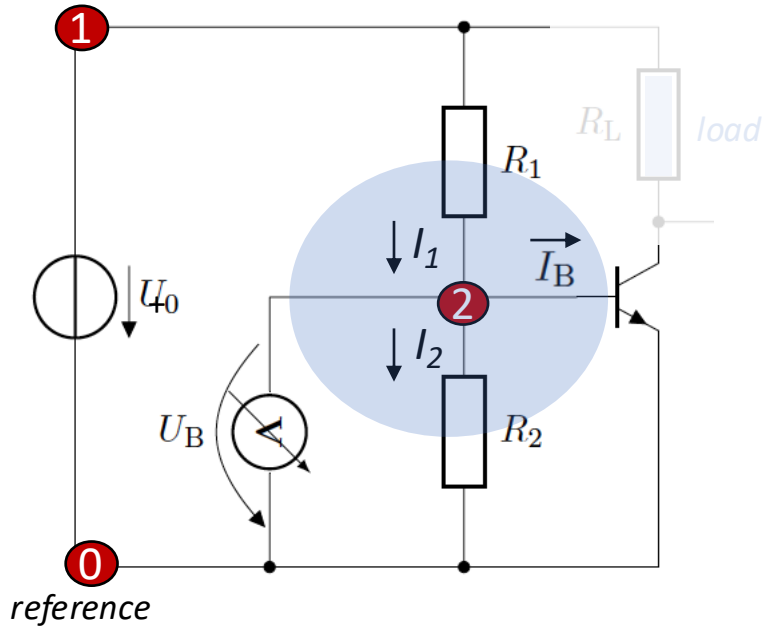
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$$(1) \ \& \ (2) \ \Rightarrow \ \frac{U_0 - U_B}{R_1} = \frac{U_B}{R_2} + I_B \ \Rightarrow \ U_0 - U_B = U_B \frac{R_1}{R_2} + I_B R_1 \ \Rightarrow \ U_B \frac{R_1 + R_2}{R_2} = U_0 - I_B R_1$$

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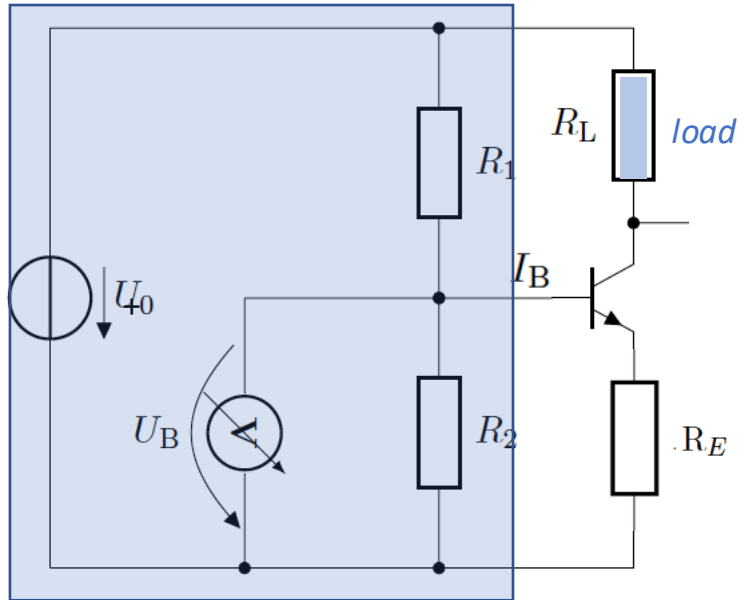
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$$\Rightarrow \ U_B = U_0 \frac{R_2}{R_1 + R_2} - I_B \frac{R_1 R_2}{R_1 + R_2}$$

# Example: Thevenin equivalent

*Voltage divider biasing with emitter resistance*

Reminder: We can stabilize the working point by adding an emitter resistance

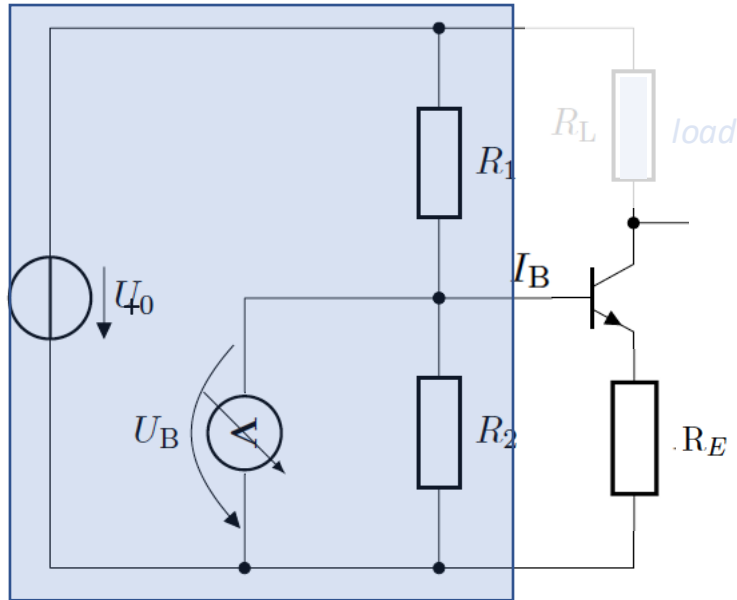


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# Example: Thevenin equivalent

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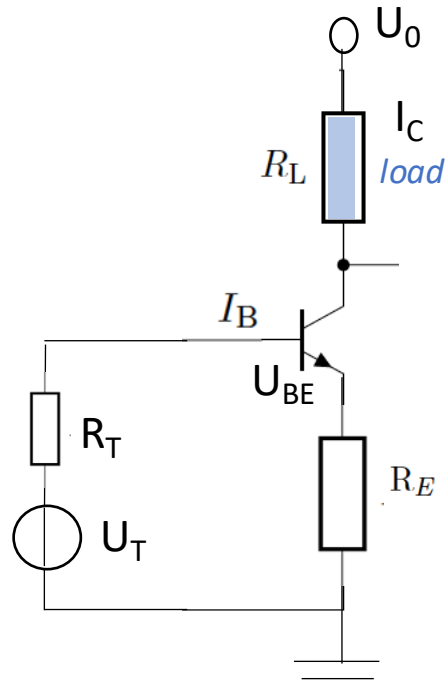
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- Thevenin voltage:  $U_T = U_0 \frac{R_2}{R_1 + R_2}$
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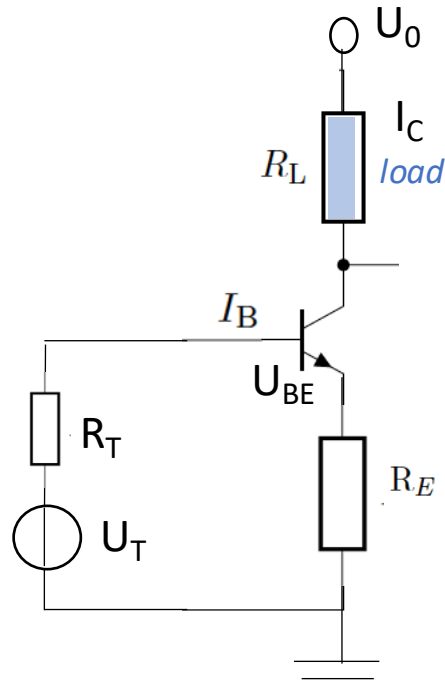
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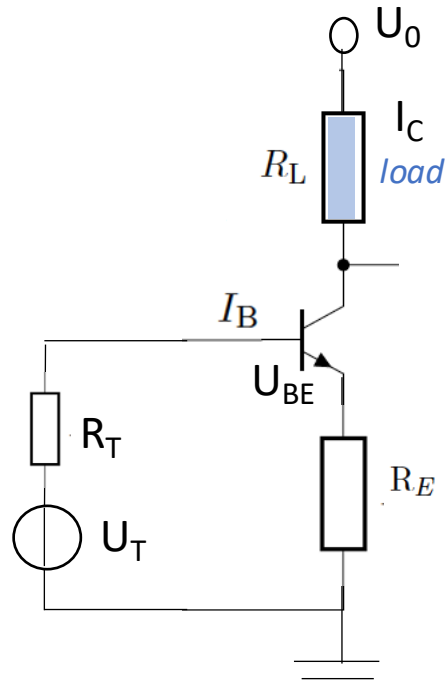
Now we can analyze the mesh (KVL):

$$U_T = I_B R_T + U_{BE} + R_E (I_B + I_C)$$

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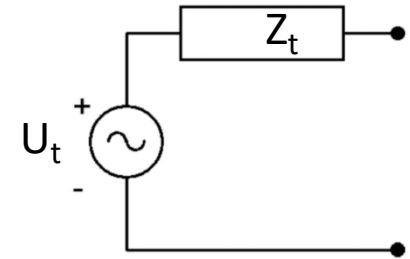
with  $I_C = \beta I_B$  (transfer characteristics):

$$U_T = I_B R_T + U_{BE} + R_E I_B (1 + \beta)$$

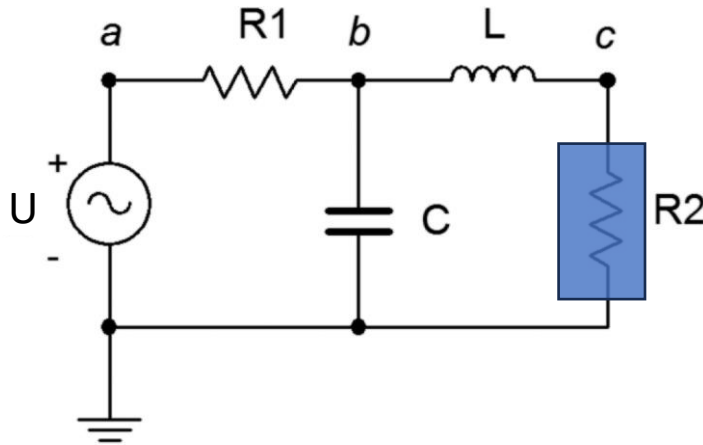
$$\rightarrow I_B = \frac{U_T - U_{BE}}{R_T + R_E (1 + \beta)} \rightarrow I_C = \beta I_B \rightarrow \dots$$

# AC Circuits

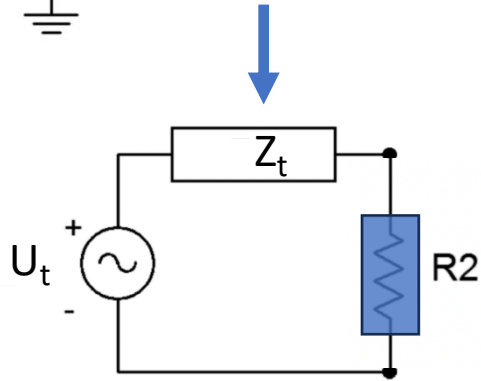
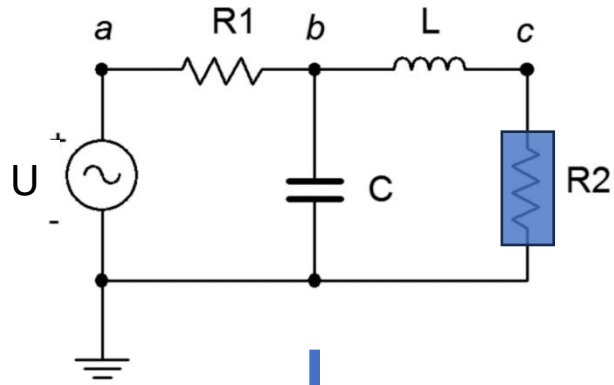
*“Any linear circuit containing several voltage sources and impedances can be replaced by a single voltage source in series with a single impedance connected across the load”*



Example: Find the Thevenin equivalent that drives  $R_2$

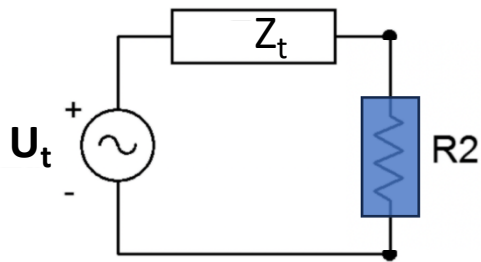
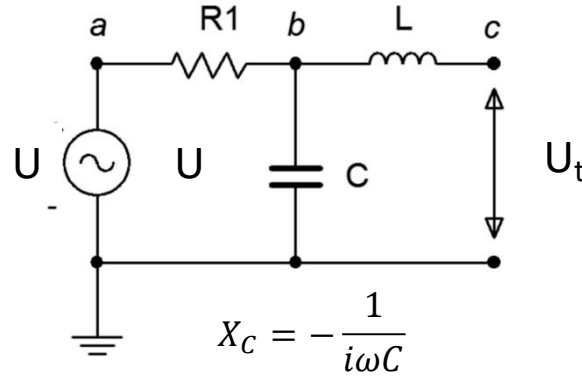
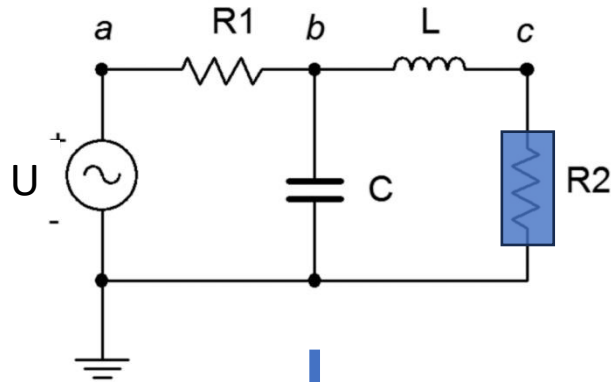


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$$U_2 = U \frac{R_2}{Z_t + R_2}$$

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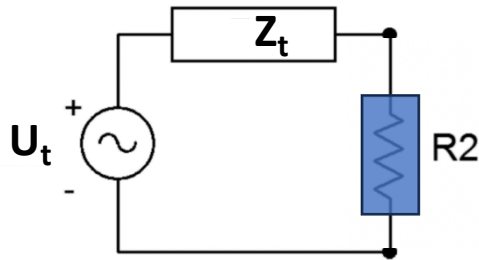
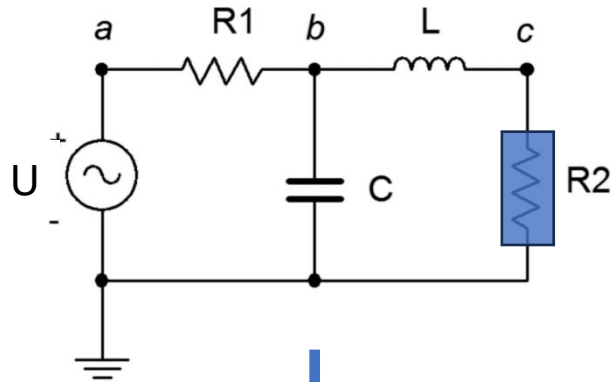
**Thevenin voltage  $U_t$ :**

No current through L

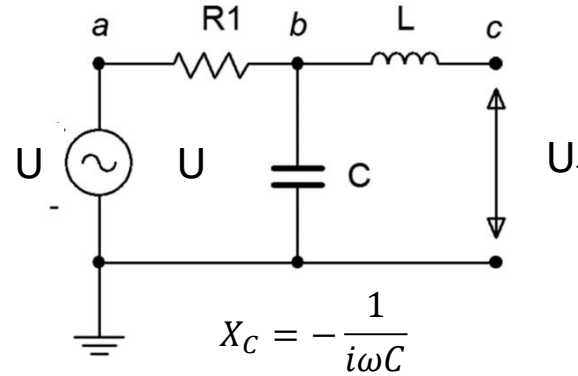
$$\rightarrow U_L = 0$$

$$U_t = U \frac{X_C}{X_C + R_1}$$

# AC Circuits



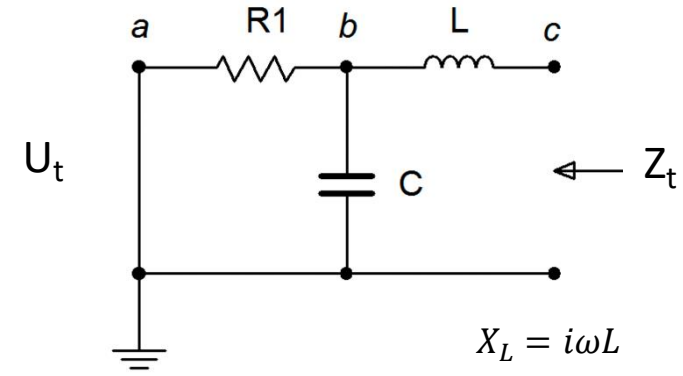
$$U_2 = U \frac{R_2}{Z_t + R_2}$$



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No current through L  
 $\rightarrow U_L = 0$

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**Thevenin impedance  $Z_t$ :**

L in series with  $R_1 \parallel C$

$$\begin{aligned} X_t &= X_L + R_1 \parallel X_C \\ &= X_L + \frac{R X_C}{R + X_C} \end{aligned}$$

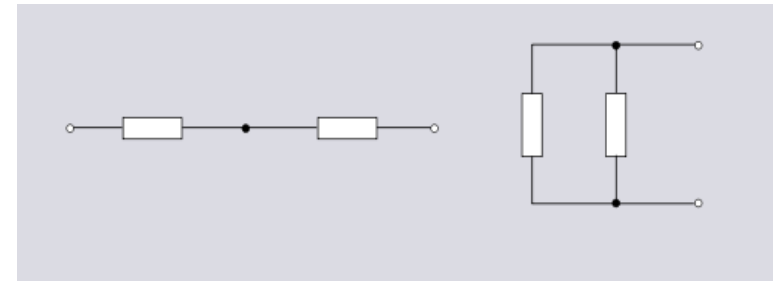
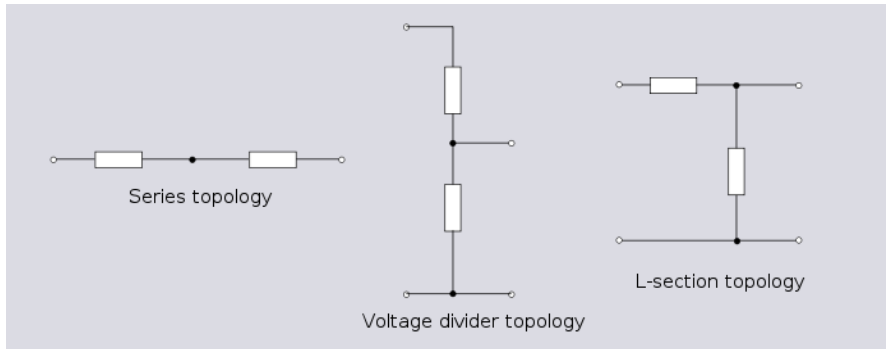
# Circuit topologies

*The formal layout of the equations following the application of Kirchhoff's rules applied to a circuit does not depend on the type of device connected in the branches. It only depends on the topology of the circuit.*

**Circuit Topology** describes how components in a network are connected. Circuits with different physical layout can have the same topology.

Example: three circuits with the same topology:

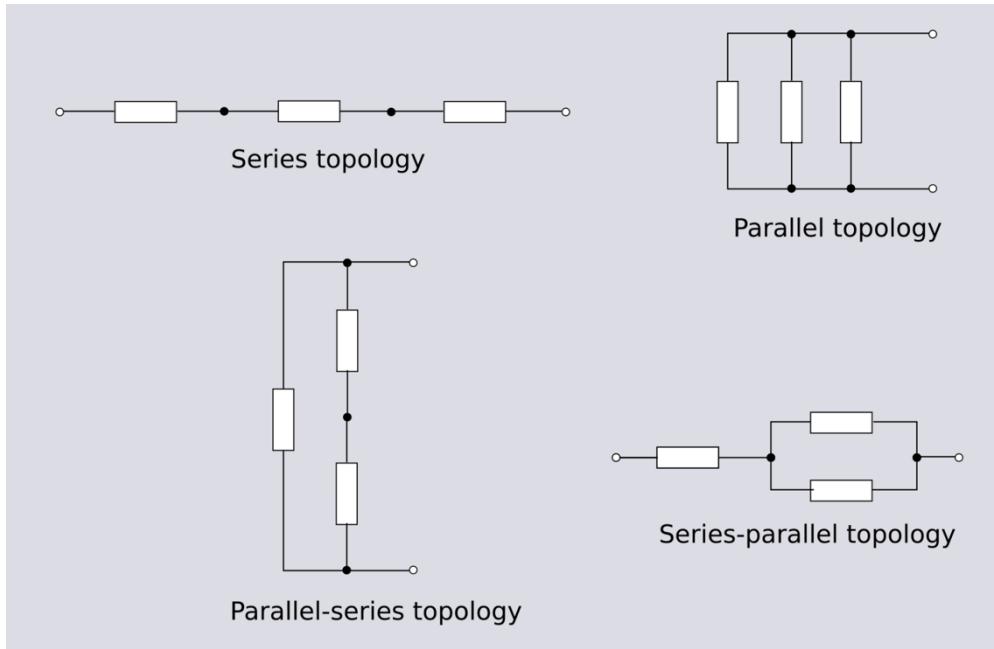
Example: There are only two topologies for a network with 2 branches: series and parallel.



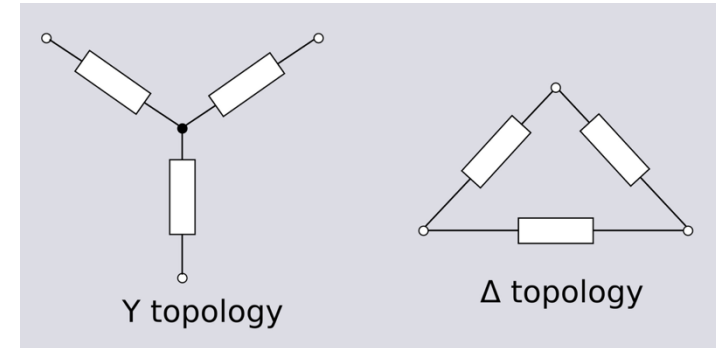
# Circuit topologies

Example: topologies with 3 branches:

2 terminals



3 terminals



# Graph theory

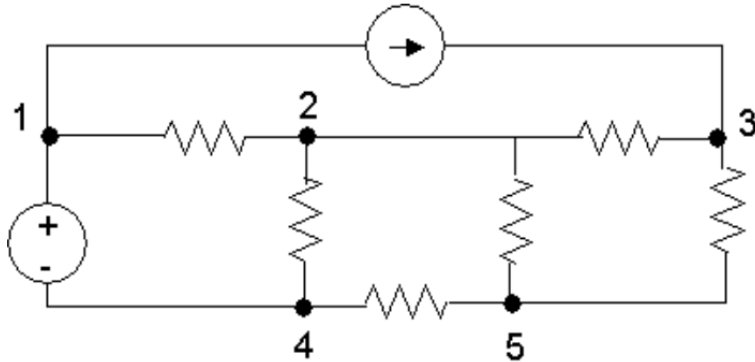
Mathematical **Graph theory** is used to analyze the topology:

Graphs represent the aspects of a network connected to its topology. The devices are left out.

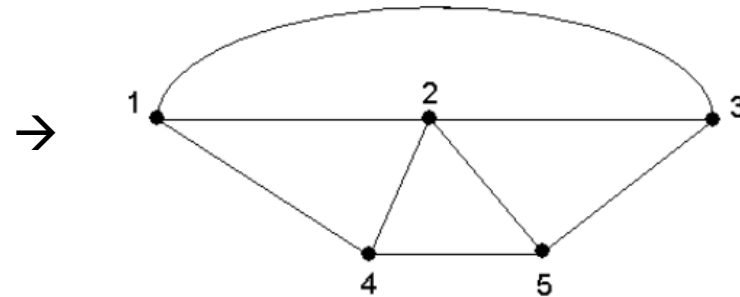
→ a line represents a device. A node represents all points at the same potential.

Example:

**circuit**



**graph**



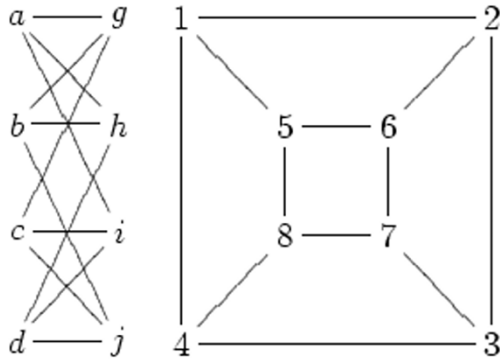
The graph representation makes it easier to analyze complex circuits.

Graphs are **equivalent** if they can be transformed into each other by translation, rotation, reflection, stretching or crossing/knotting the branches,

# Graph theory

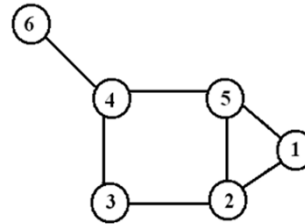
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Isomorphism  
 Example:



$f(a)=1$   $f(b)=6$   $f(c)=8$   $f(d)=3$   
 $f(g)=5$   $f(h)=2$   $f(i)=4$   $f(j)=7$

Representation:



Example: Adjacency matrix

	1	2	3	4	5	6
1	0	1	0	0	1	0
2	1	0	1	0	1	0
3	0	1	0	1	0	0
4	0	0	1	0	1	1
5	1	1	0	1	0	0
6	0	0	0	1	0	0

Topological distance:

Distance matrix

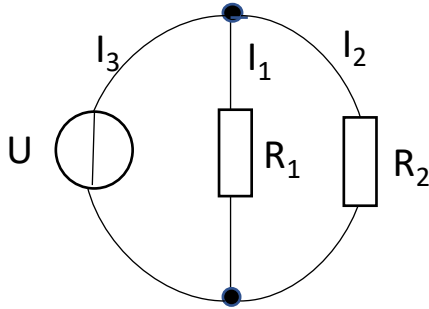
	1	2	3	4	5	6
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5	1	1	2	1	0	2
6	3	3	2	1	2	0

# Graph theory: dual graph

Each graph has a **dual graph** with the following elements exchanged:

- $R \leftrightarrow 1/R$
- $L \leftrightarrow C$
- $U \leftrightarrow I$
- $U \text{ source} \leftrightarrow I \text{ source}$
- $\text{mesh} \leftrightarrow \text{node}$

graph

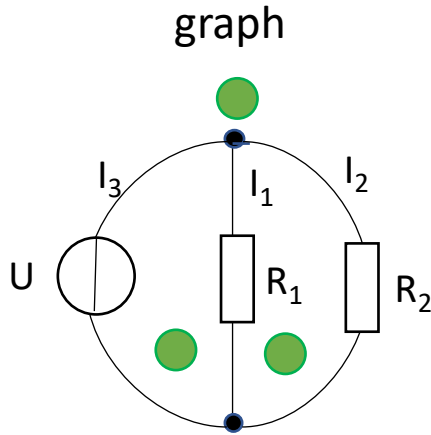


$$I_3 = -I_1 - I_2 = U \left( \frac{1}{R_1} + \frac{1}{R_2} \right)$$

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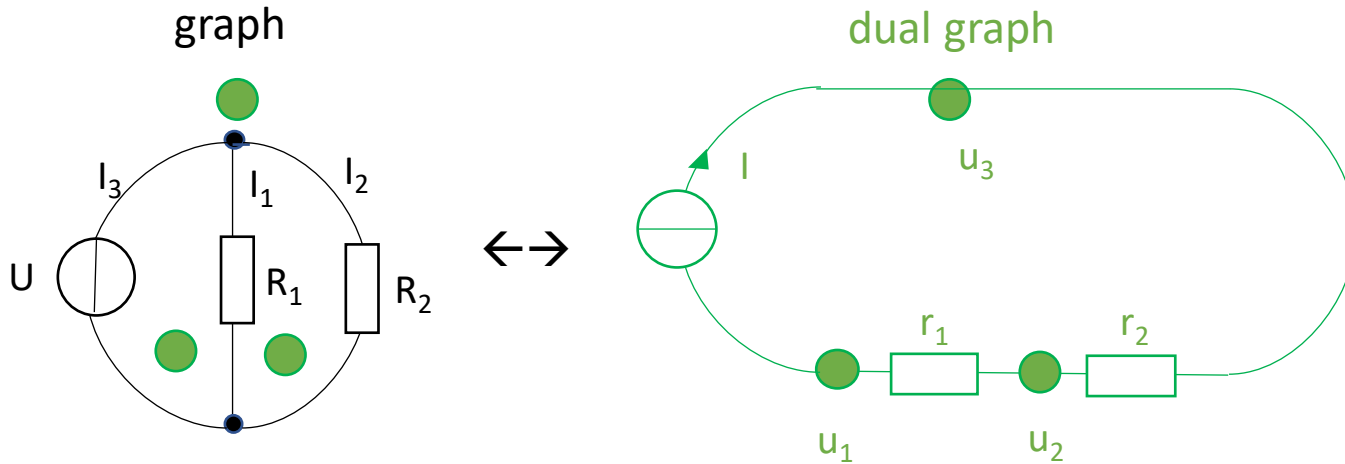


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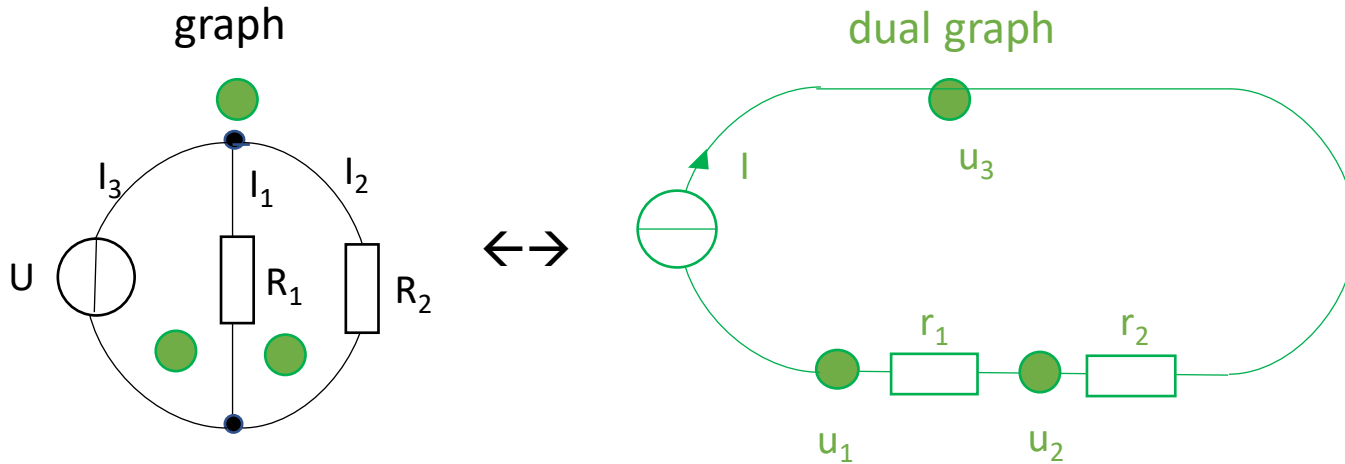
*converted parallel  
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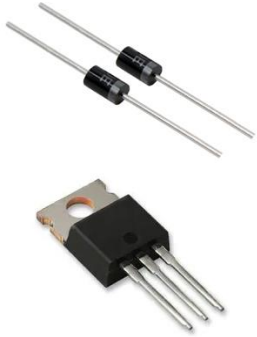
*converted parallel circuit into serial circuit*

*both solutions are equivalent as  $U \leftrightarrow I$*

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$$u_3 - u_1 = I(r_1 + r_2) = I \left( \frac{1}{R_1} + \frac{1}{R_2} \right)$$

# Literature



- (1) Reminder: Electrical circuits
- (2) Analog electronics
- (3) Digital electronics
- (4) Circuit analysis, circuit topologies



## Literature:

Paul Horowitz, Winfield Hill  
The Art of Electronics  
Cambridge University Press (2015)

D. Sundararajan  
Introductory Circuit Theory  
Springer (2019)

