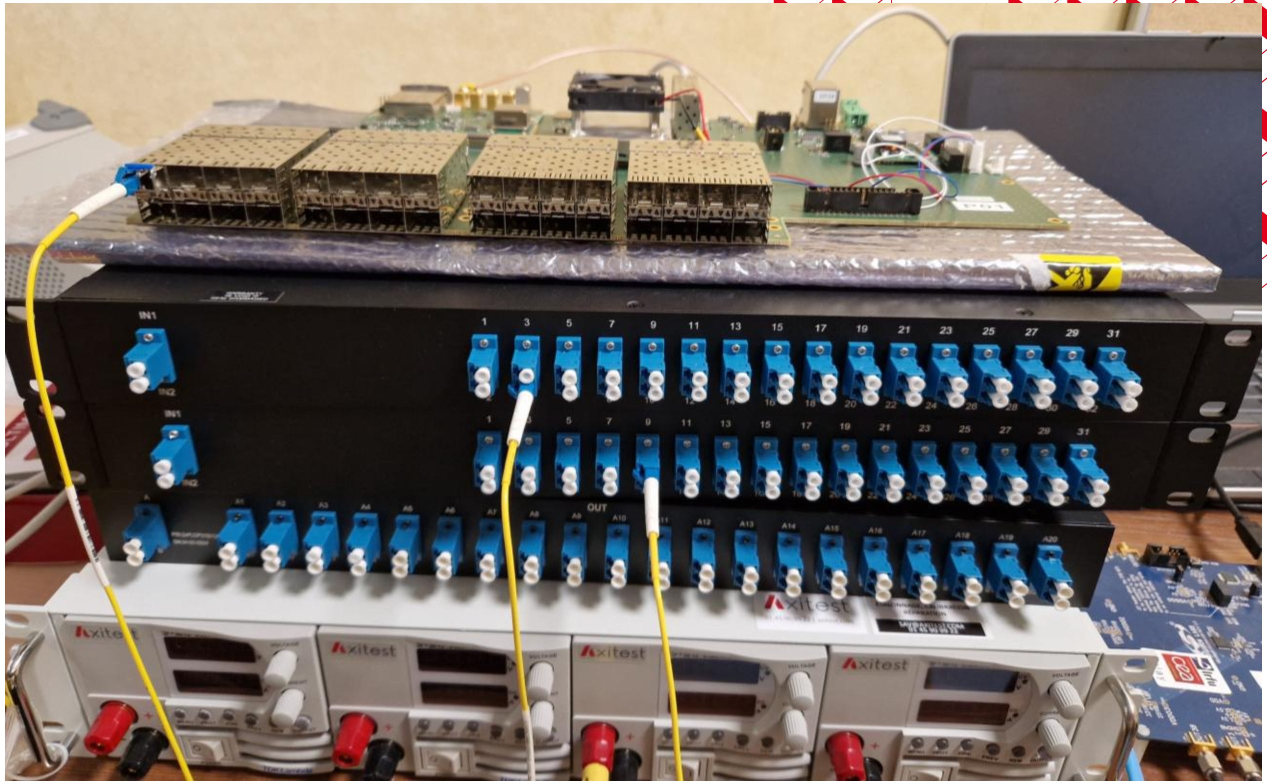
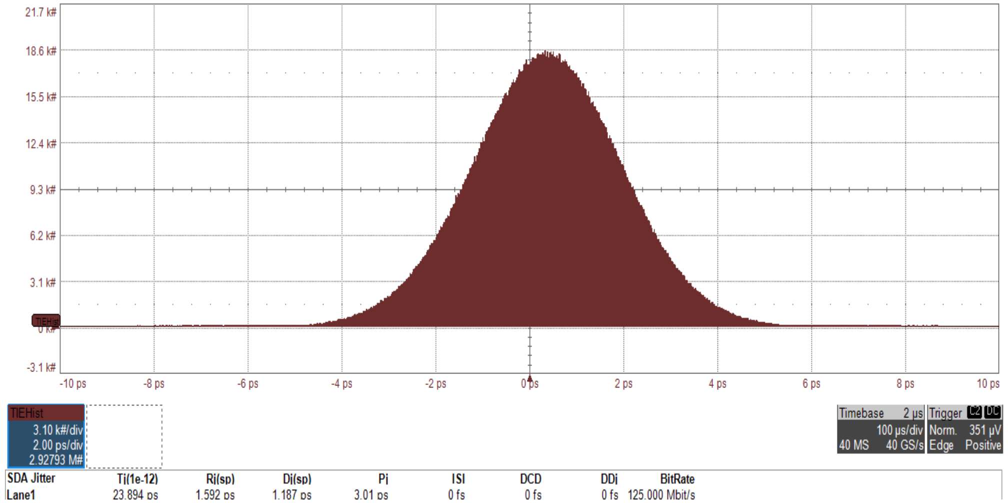


PRR:
FSCD prototype comments and updates

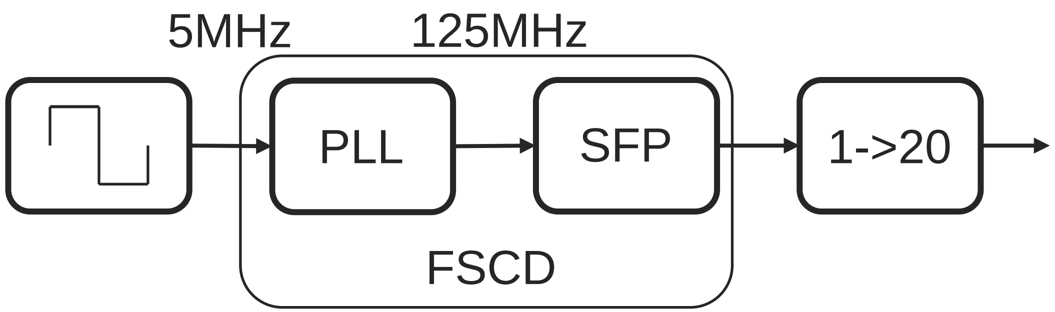
Sara Bolognesi, Denis Calvet, Emmanuel Molina Gonzalez, **Guillaume Soudais**

26/03/2026

First stage clock distribution



FSCD Port	Rj (ps rms)	Dj (ps rms)
0	1.59	1.19
1	1.67	0.92
2	1.67	0.75
3	1.70	1.13
4	1.62	1.79
5	1.73	1.03
6	1.68	1.40
7	1.60	1.17

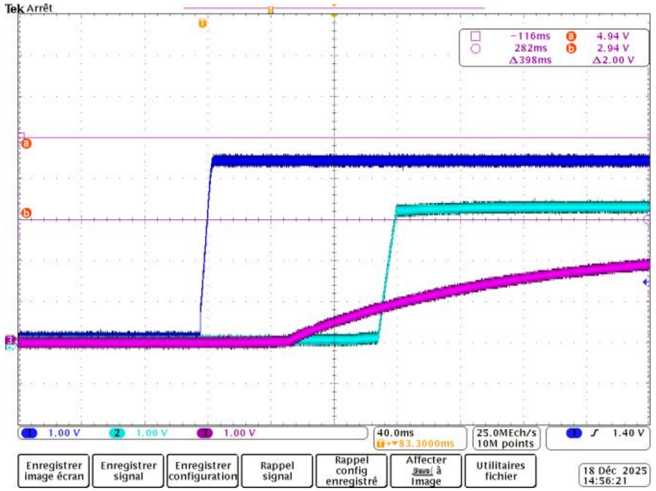
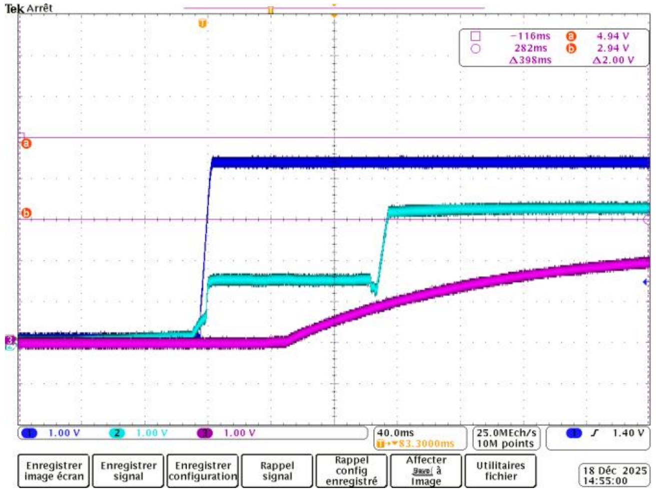
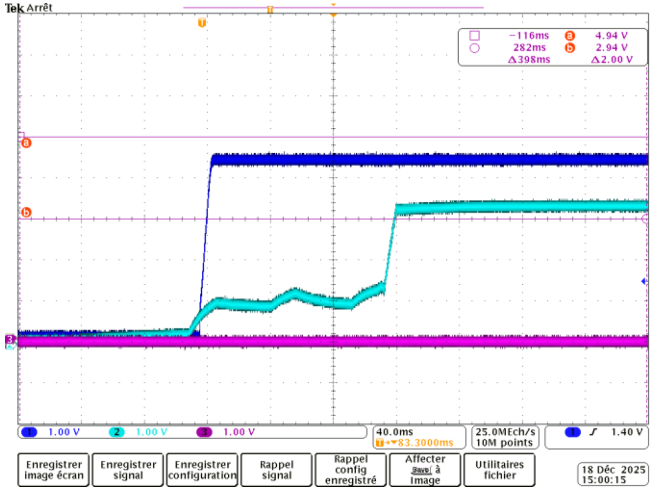


- All outputs of the main clock group have bellow **2 ps rms** of random and deterministic jitter.
- This quality is reached by having sending the PLL clock signal through fanout chip and directly to the SFP.
- **15 ps** of delay variation upon reset
- 90% eye opening in synchronous data transmission of PRBS at 500 Mbps.

Updates on previous results

- Source of the power anomaly during start up.
- Redundant power supply mechanism.
- Justifications for using a square clock input for testing.
- Clock quality with a received signal, offset between output after resets.
- Synchronous data transmission eye diagram with PRBS.
- New optical splitter performance and power.
- Updated and improved optical architecture.
- Sources of fixed delay difference between endpoints.

Power up sequencing

	P01	P03 (Denis')
No screen	Not captured	
Screen		

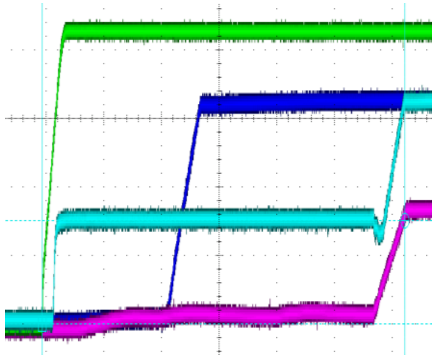
- V_POW
- 3V3_IO
- unused

2 different power issues during boot sequence:

- Power delay on Vpow
- Screen reverse powering FPGA bank

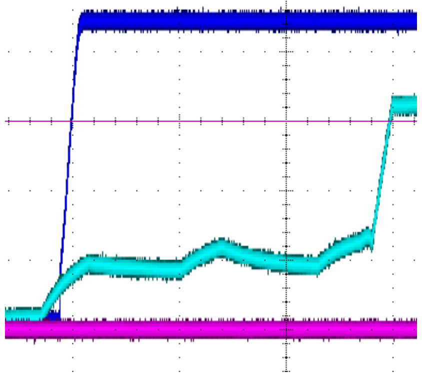
Power sequencing

P03 + no screen
Before V_pow fix



+

P03 + screen
After V_pow fix



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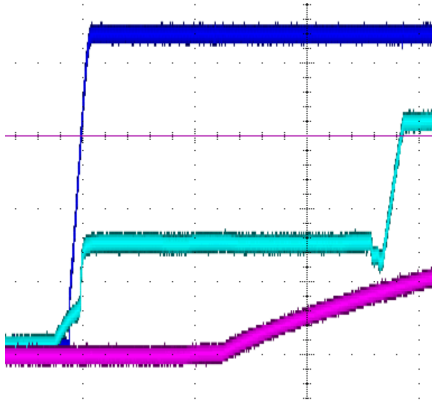


P01 + screen

- V_POW
- 3V3_IO
- unused

"Delay is introduced in the micro-controller software so that V_POW is started well after 24V_FS is established." –Denis

First issue can be solved by updating the micro controller software.

The second issue was not mentioned by Denis.
It seems to come from a reverse powering of an FPGA bank.

Screen is powered before the FGPA, pulls up its communication line to the FPGA for a short duration. This line may be powering the FPGA bank hence seeing tension on 3V3_io line.

Maybe the screen software can be changed, we need to look into it.

Redundant power supply

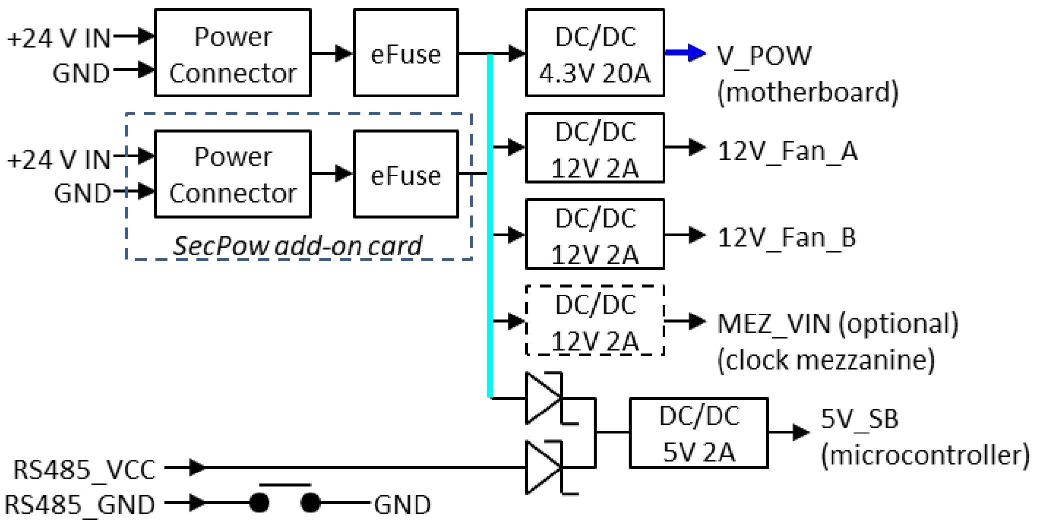
A transistor is used next to the eFuse to detect reverse voltage.

➢ The used power supply is the one with the highest voltage.

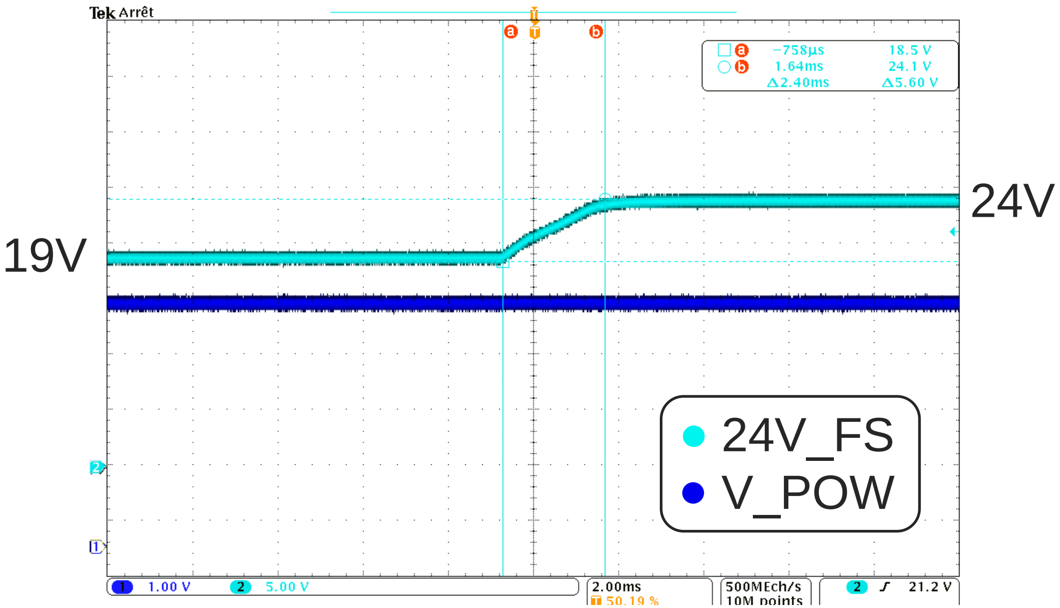
During run time, the main and spare power supply will be set at 24 V and 23 V respectively.

No power will be drown from the spare power supply until the main is deactivated.

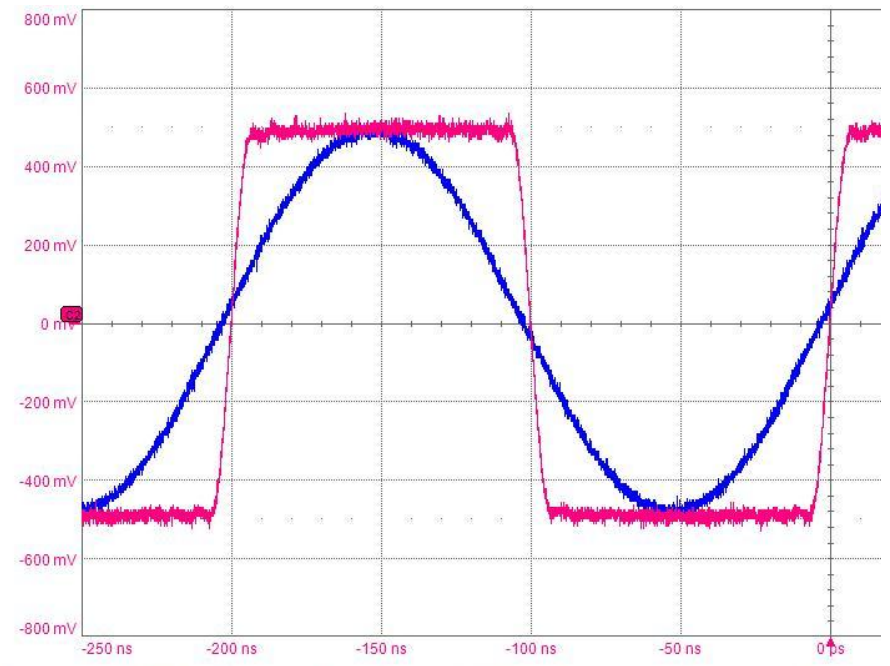
Automatic and seamless switch between power supplies.



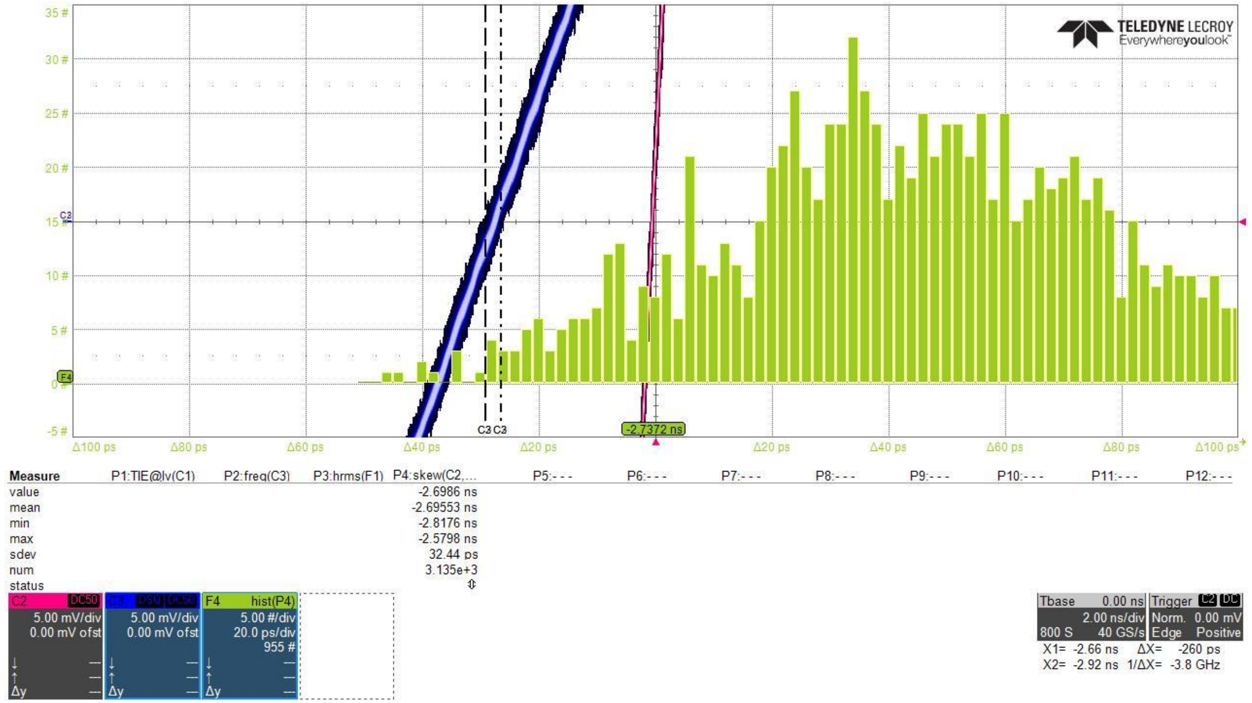
General on board power scheme



Rising edge of slow signal on oscilloscope



AWG output 1 : Square 5MHz 1Vpp
AWG output 2 : Sinusoidal 5MHz 1Vpp



Phase offset between the square and sinusoidal clock output of the arbitrary waveform generator.

Std dev = 32.44 ps

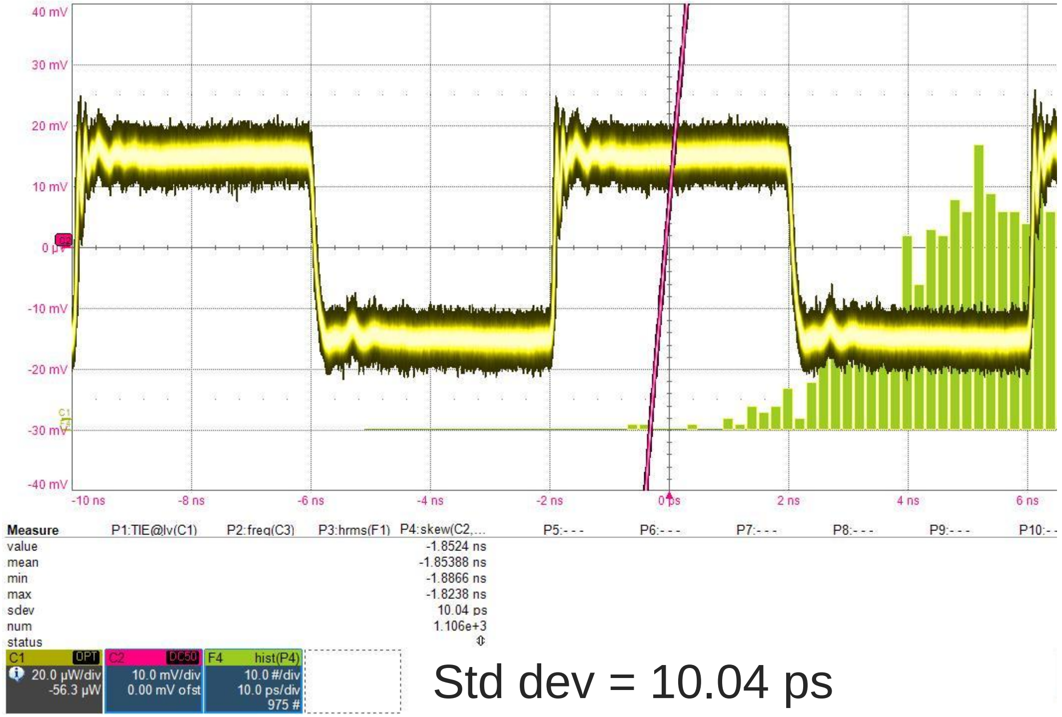
Pk-pk = 238 ps

Even with a large vertical scale, the oscilloscope cannot perform a precise measurement.

Retesting sinusoidal input on FSCD

AWG output 1 : Square 5MHz 1Vpp -> Oscilloscope
AWG output 2 : Sinusoidal 5MHz 1Vpp -> FSCD mezz clk input

reset	avg skew [ns]	std dev [ps]
1	-1.855	10.1
2	-1.853	10.04
3	-1.859	9.48
4	-1.862	9.17
5	-1.856	9.5
6	-1.861	9.15
7	-1.864	9.18
8	-1.865	9.88
9	-1.864	9.48
10	-1.87	9.62



Std dev = 10.04 ps
Pk-pk = 63 ps

Upon 10 reset, FSCD always find the same offset compared to the 5MHz clock though it is using the sinusoidal input.
If it had issue I would expect a far larger phase variation than the 17 ps peak to peak here.

- Therefore I think the scope struggles to find the rising edge of a slow signal (sinusoidal).

Phase offset and clock quality

Phase offset between outputs after board resets.

Reset	Skew P1 P2 [ns]
1	-1.237
2	-1.237
3	-1.237
4	-1.236
5	-1.236

Phase variation is either slow variation over time or unknown fixed phase variation added by components.

Clock quality when SFP emitting receives a clock signal to monitor.

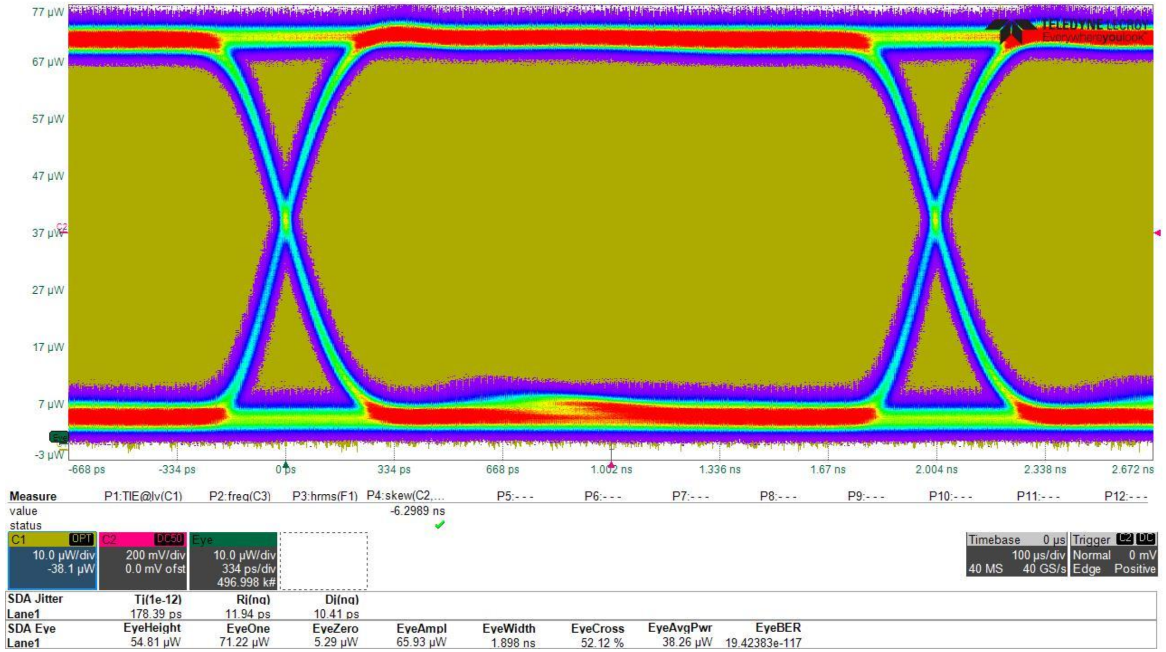
Measured using the SFP I/O board.

	Rj	Dj	TIE
Rx ON	8.22	12.68	9.206
Rx OFF	8.47	5.69	8.19

Dj varies a lot when redoing the measurement.

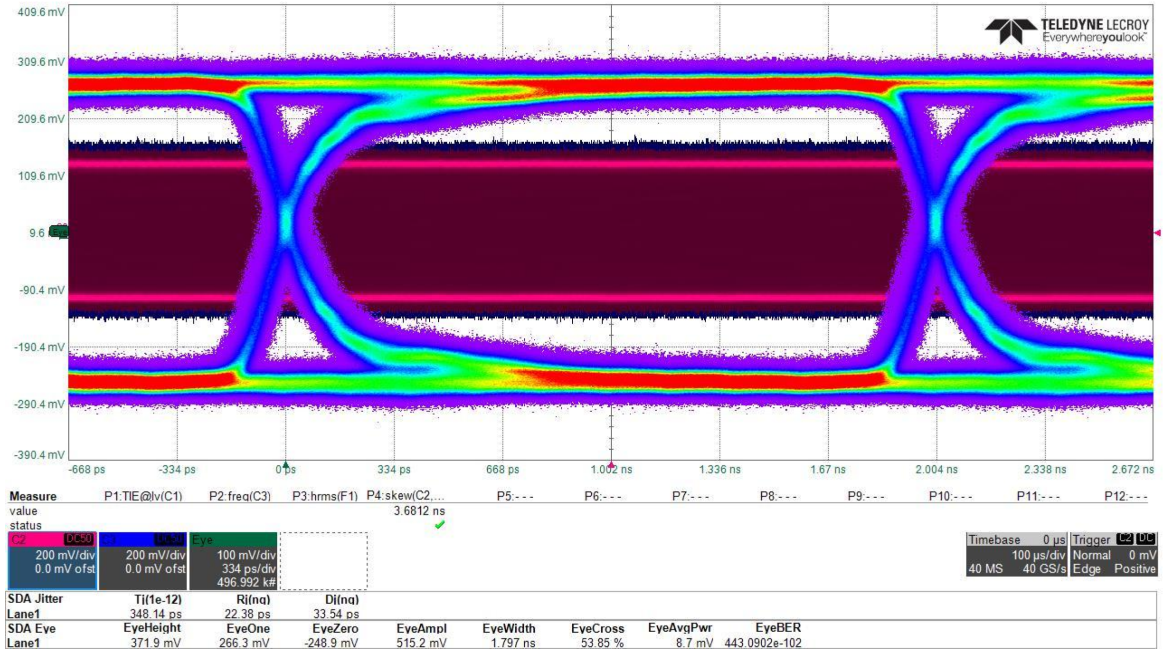
The difference in Rj and TIE does not seem significant.

Eye diagram of the sync data link with PRBS



PRBS 15 at 500 Mbps
SFP 80km through 2x32 splitter
Optical probe

Eye width : 1.898 ns

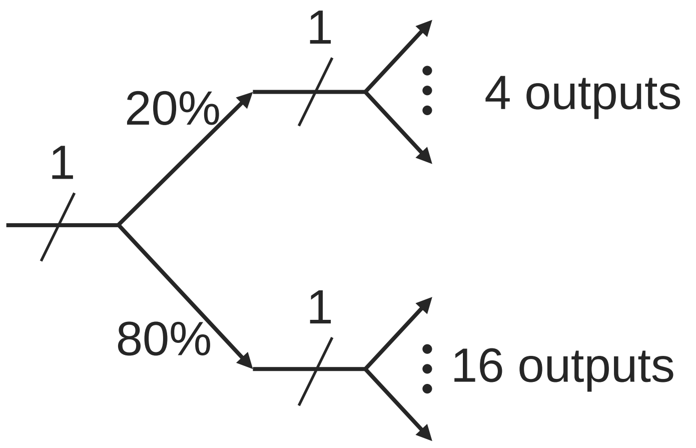


PRBS 15 at 500 Mbps
SFP 80km through 2x32 splitter
SFP I/O board

Eye width : 1.797 ns

ACPhotonics 2 – 1x20 PLC splitter

3 ACPhotonics procured for testing, custom built optical splitters



Power budget:

80 km SFP : 0 – 5 dBm

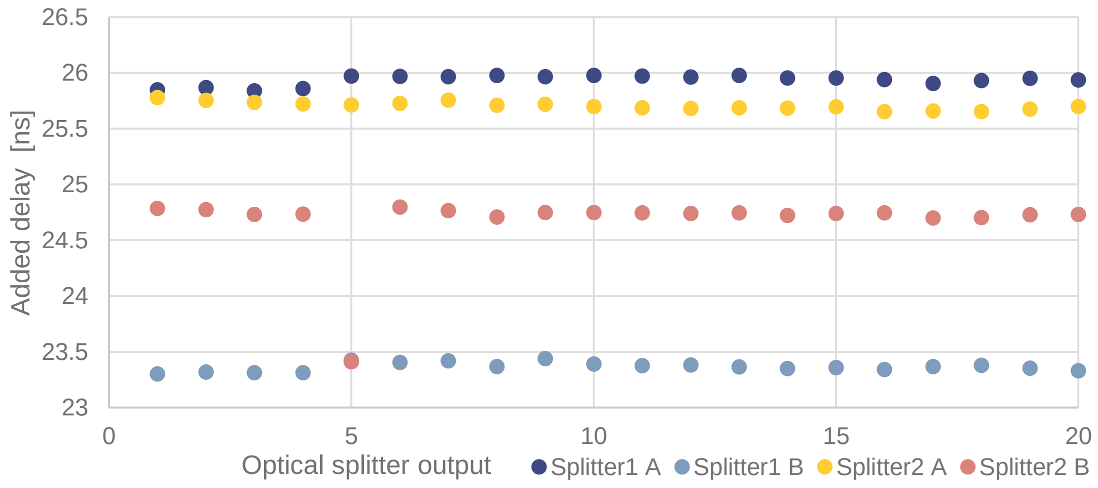
Optical splitter : -14 dB (theoretical -13 dB)

Fiber and connectors : <1 dB

10km SFP receiver detection : -20 dBm

- ~5 dB margin

- 3 ns transmission delay difference between splitters
- Splitters output are not aligned



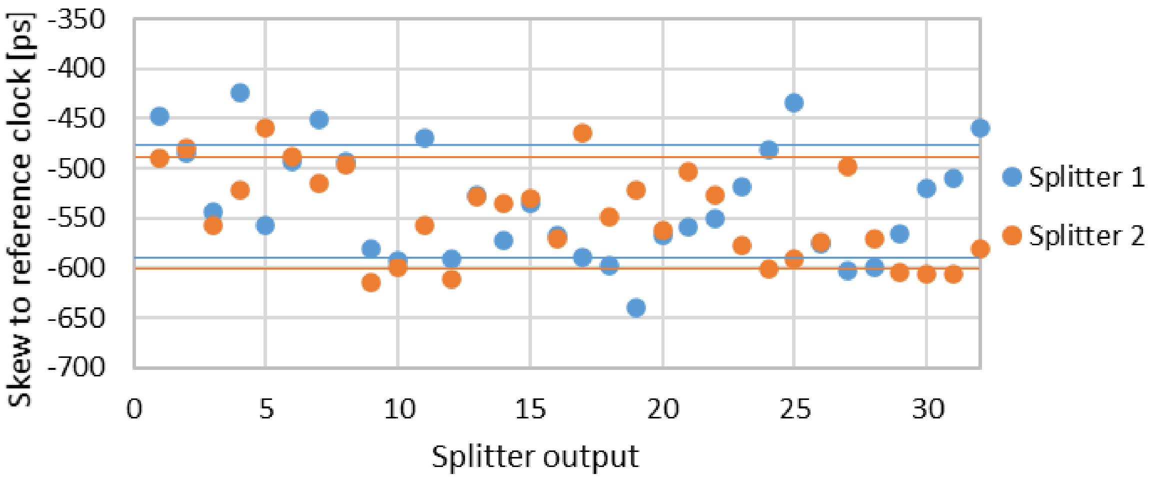
Transmission delay of four optical splitters

FS.com PLC 2x32

2 sample procured for testing.

2x32 means 2 input to 32 output

The 2 input are merged into one and then splitted into 32 output.



- 215ps, and 154ps maximum variation of skew between splitter output and reference clock, and 110 ps when selected.
- 2nd inputs of the splitters has a 30ps and 15ps offset with the 1st input.

Optical splitter PLC 2X32

Power budget:

- 80 km SFP : 0 – 5 dBm
- Optical splitter : -17 dB (theoretical -15 dB)
- Fiber and connectors : <1 dB
- 10km SFP receiver detection : -20 dBm

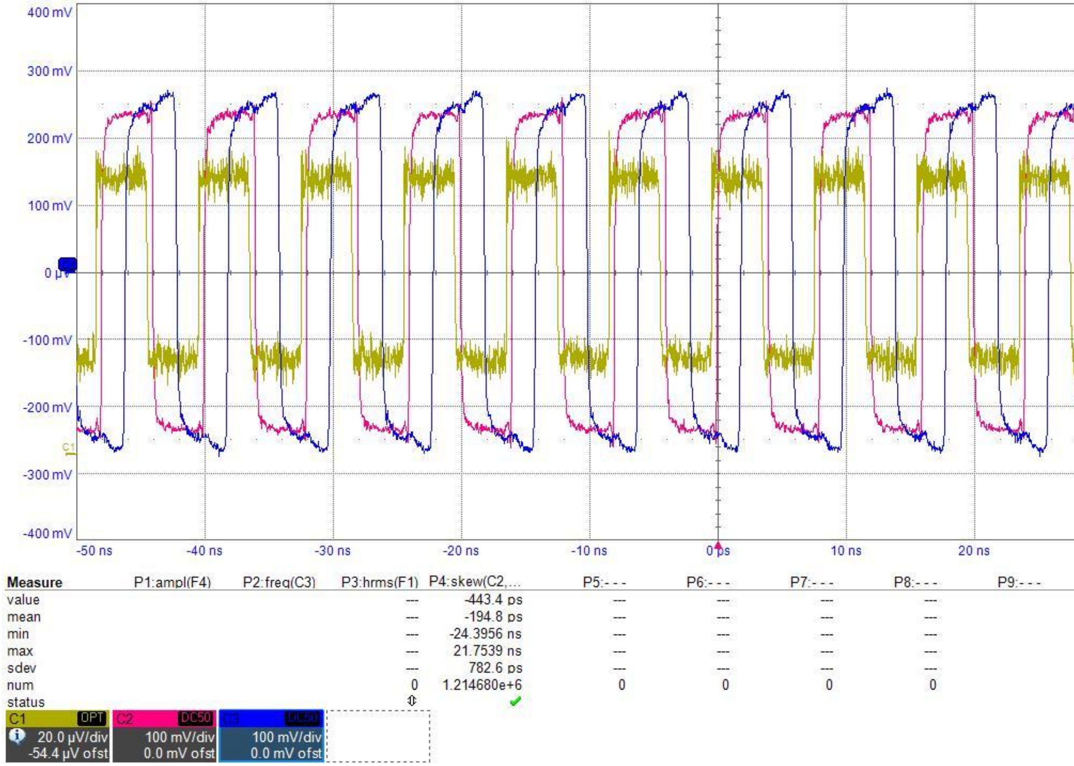
➢ **2 dB margin**

This is the expected safety margin by the end of life of the components.

The additional outputs can be used if one fiber inside is broken and for a direct feedback loop to FSCD to monitor phase and optical power.

Optical splitter PLC 2X32

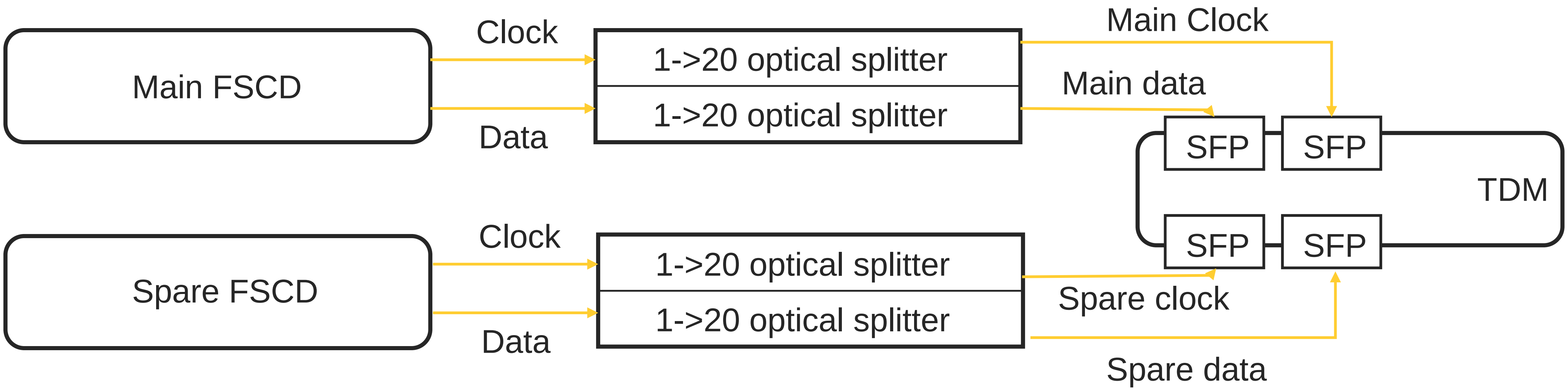
output	1->20 splitter	2x32 splitter Input 1	2x32 splitter Input 2
1	-11.49 dBm	-13.61 dBm	-14.36 dBm
2	-12.21 dBm	-13.94 dBm	-14.28 dBm
3	-11.93 dBm	-13.83 dBm	-14.31 dBm
4		-14.2 dBm	-14.8 dBm



- ~3dB more of attenuation with new splitter but we are still far from SFP detection minimum
- Below 10 ps jitter measured on SFP output with -24dBm of power. 22 ps jitter measured with -29 dBm power.
- Attenuation should not be an issue with such a splitter, and can be monitored, with an alarm raised if power is too low.

- Ref clock from SMA
- Optical probe
- SFP I/O board

Current clock distribution topology

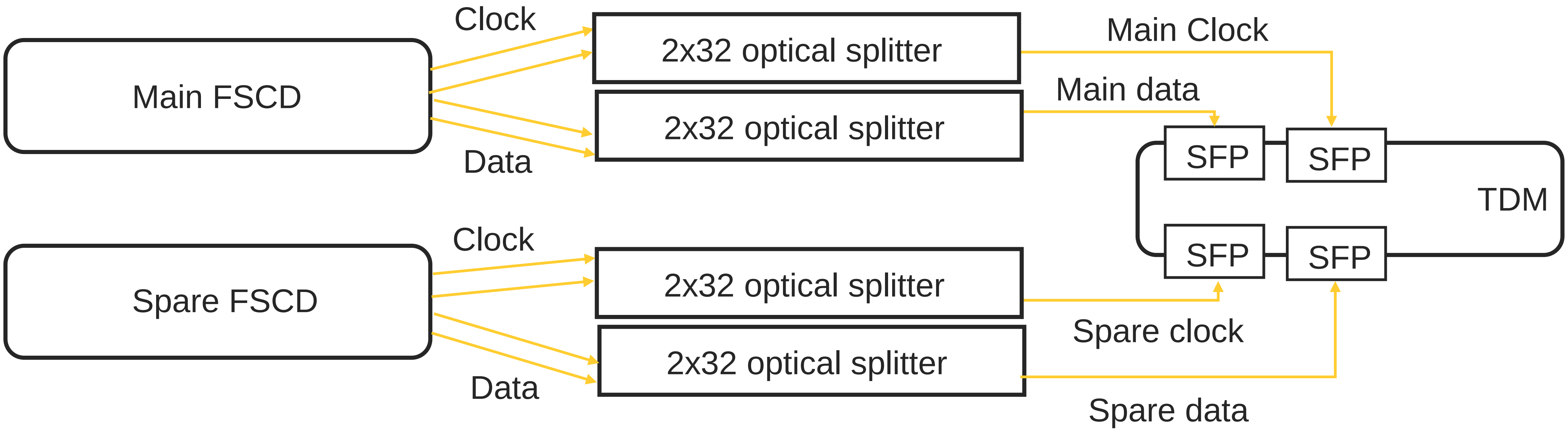


Unknown procedure for switching FSCD in case of failure.

But requires actions from TDM board, switching PLL input from one SFP to another.

➢ We can slightly modify this architecture using 2x32 optical splitters.

Proposed clock distribution topology



- ➢ Using the second input of the splitter for a backup SFP.

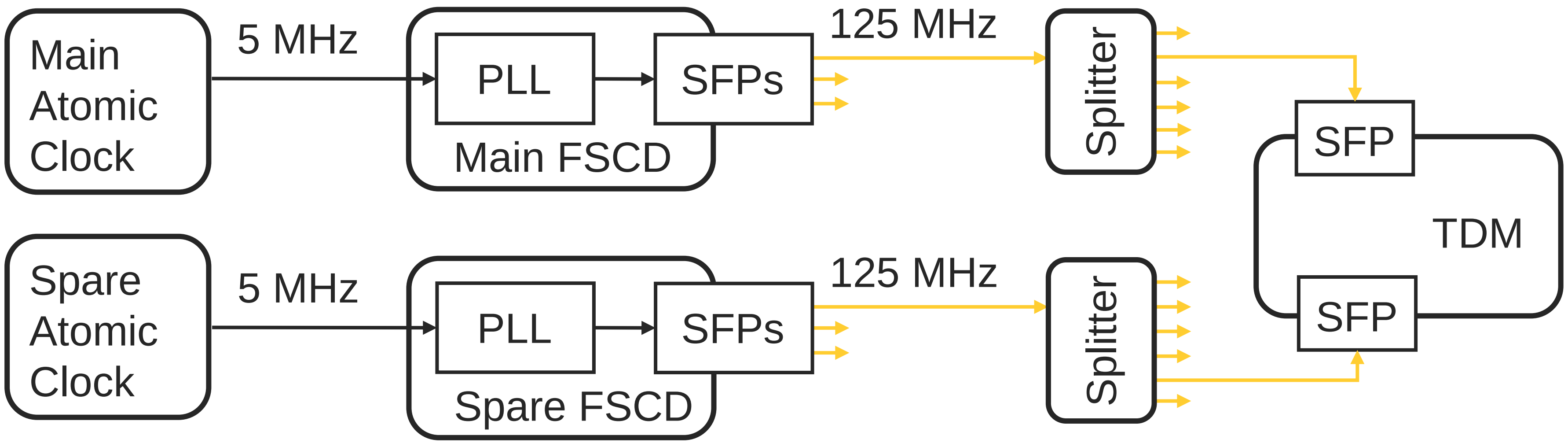
+

Only 1 SFP emitting light per optical splitter, the other laser should not age.
Allow for redundancy before switching to secondary FSCD board.

–

There may be a 150 ps phase shift when switching splitter input. (~100ps SFP + 30 ps splitter input)
Uses 4 units of space in the side hut rack.

Fixed phase offset



Each TDM boards will have an unknown phase with the reference clock due a small variability in the delay added by each components in the clock distribution:

- PCB trace adds **150 ps** delay difference.
- SFP Tx adds **100 ps** delay difference.
- Optical splitter adds ~**200 ps** (100 ps with selection) of delay difference.
- Optical fibers adds **50 ps** of delay difference if length are matched to 1 cm.
- SFP Rx adds **150 ps** delay difference.

Around **700 ps** delay difference may be added. Below the 1 ns target.

Summary

- Source of the power bug is understood, and should be fixed with different software in components.
- A fixed phase after reset was observed using a sinusoidal input to the FSCD.
- The Tx clock signal is not deteriorated when receiving a monitored clock.
- 90% eye opening in the synchronous data transmission at 500 Mbps
- New optical tested, introducing below 200 ps fixed phase variation.
- Low power safety margin at end of life of components, but the power can be monitored.
- Updated and improved optical architecture enabling low impact change instead of moving to spare clock distribution.
- Around 700 ps fixed phase difference at TDM level, below the 1 ns target.

Open points

- The procedure to switch from main to spare clock distribution is not clearly defined, but should not create modifications to the board design.

- The interface with the calibration system is not clearly defined. From the last discussion with the calibration team, there should not be any direct link between FSCD board and calibration board. The communication will be done with another system.
  We will keep in the design all the ports thought to be used in this case.