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High-Speed Data Transmission and Serial Powering IP's in 65nm CMOS Image Sensor Process at the Electron Ion Collider

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High-Speed Data Transmission and Serial Powering IP's in 65nm CMOS Image Sensor Process at the Electron Ion Collider
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ABSTRACT:
Next generation particle physics experiments like Electron Ion Collider demand high-speed data communication and lower mass designs for its detectors. Thanks to the availability of smaller technologies and innovative designs techniques, novel scientific detectors will be based on high speed and energy efficient sensor systems. This paper therefore presents circuits designed to meet the EIC powering and high-speed data requirements. These include a shunt LDO to support serial powering in EIC vertex tracker, a dual-frequency PLL that supports two frequency modes of operation, a 5GHz PRBS Generator for system testing, an I2C block and a high speed CML receiver.
Shunt LDO is a novel design technique that is used for the implementation of highly efficient, low mass, current based serial powering scheme. In this paper, we describe our initial work on a Shunt LDO architecture for the implementation of serial powering in the EIC. Shunt LDO employs several protection-features like over voltage protection and under shunt protection.
Phase locked loops which generate on-chip clock/carrier are an essential part of every communication system. In this paper we are proposing a flexible PLL design that supports existing data read out systems (where the supporting infrastructure imposes a speed limit) and future systems (where the infrastructure can be designed to support higher rates). Special schemes and design techniques are employed to make the design radiation tolerant and area efficient.
As a part of ITS3 upgrade, high speed I/O 's were designed and fabricated. They are i) High speed CML Receiver, which can operate up to 8GHz. ii) I2C IP, which supports serial communication iii) PRBS Generator, which can produce a random sequence up to 10Gbps to enable system testing.
The supporting LVDS receiver and CML line driver were already fabricated as part of the CERN Experimental Physics R&D Programme (EP R&D WP1.2) and have been shown to be functional on silicon up to 2Gbps .

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