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Evaluation and simulation of High Voltage-CMOS chips for high radiation environments

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High Voltage-CMOS (HV-CMOS) sensors are gaining steam as a capable, radiation tolerant, and cost effective solution for silicon based detectors in current and future experiments. These devices can be biased to high voltage, for radiation tolerance, and due to their monolithic nature they can also meet a low material budget. Additionally, they do not require external processing, such as bump-bonding, which can be expensive and limit pixel granularity. Although an attractive option further development is still needed to meet anticipated targets for experiments such as the High Luminosity LHC (HL-LHC) upgrades.

The UKRI-MPW1 is the next iteration in a series of proof-of-concept chips designed to increase radiation tolerance through high biasing voltages. Designed in the LFoundry 150 nm HV-CMOS technology, the chip has a dedicated cross-section consisting of a 3.0 kΩ cm high resistivity backside biased p-type substrate with a Voltage Terminating Scheme (VTS) ring structure, and a new low dose p-type current blocking layer jointly developed with LFoundry. This builds upon the previous UKRI-MPW0 which had a measured breakdown voltage of 600 V, and a 50 μm depletion depth after a fluence of 1×10^{16} 1 MeV n_{eq} cm^{-2}; however, the design suffered from a high leakage current of 4 mA. The new design seeks to reduce the leakage current by way of the VTS, and the new p-layer placed around each pixel, to prevent current flow between pixels.

This contribution presents experimental measurements of the UKRI-MPW0 and varying TCAD evaluations used to develop the new chip cross-section for the UKRI-MPW1. These include Current Voltage (IV) breakdown and inter-pixel current measurements and simulations. As well as, 2D cross-section simulations of current flow, electric field, and breakdown of the new UKRI-MPW1 chip design.

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