

A 4-Gbps serializer circuit in a 180 nm technology for monolithic pixel sensor prototypes developed for the CEPC vertex detector

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Monolithic CMOS Pixel Sensor (CPS) is one of the promising candidates for the Circular Electron Positron Collider (CEPC) Vertex detector, due to its good performance and trade-off of granularity, readout speed, material budgets and power consumption. A full-scale TaichuPix chip, including a matrix of 512×1024 pixels with a size of $25 \times 25 \mu\text{m}^2$ is developed to provide a spatial resolution better than $5 \mu\text{m}$. It requires a raw data rate up to 3.84 Gbps and power consumption less than 25mW/Gbps for the serializer circuit. Based on one of the small-scale prototypes, the highest serial data rate is tested to be 3.36 Gbps with a peak-to-peak jitter of about 150 ps and large current consumption. Moreover, the 32-bit parallel data width of the serializer isn't suitable for the 8B10B encoder. Therefore, two 4-Gbps serializers (20:1 and 40:1) have been designed and optimized to meet these requirements based on the same process node of 180 nm as the TaichuPix, considering the funding and time costs. The serializer consists of a phase locked loop (PLL), 5:1 sub-multiplexers based on a shift-register chain, a 4:1 or 8:1 sub-multiplexer based on the binary-tree structure, a clock distributor and a high-speed driver. A ring-oscillating PLL with a simulated frequency tuning range (TR) of 0.34~3.12 GHz and a 1-MHz -offset phase noise (PN-1M) of -103dBc/Hz is integrated in the 20:1 serializer. We also tried an LC-tank PLL with a narrower TR (1.8~2.3 GHz) and a better PN-1M (-118 dBc/Hz) in the 40:1 serializer. The total current is 71 and 82 mA for the 20:1 and 40:1 serializer operating at 4 Gbps, respectively. The simulation results indicate that both circuits meet the data rate and the power consumption requirements. The serializers will be characterized and reported in the presentation.

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