

# A 5.12-Gbps serializer circuit for front-end fast readout electronics of silicon pixel detectors

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The advanced synchrotron radiation sources are major facilities to analyze the formation and evolution of material structure for multidisciplinary researches, in terms of its high luminosity, low emittance, wide energy bandwidth and so on. Several advanced synchrotron radiation sources are under construction in China, involving the HEPS (High Energy Photon Source) and SHINE (Shanghai high repetition rate X-ray Free Electron Laser and extreme light facility). They will be major multidisciplinary-researches platforms in China. To meet the requirements of pixel detectors in these facility, dedicated pixel readout chips are being developed, such as HEPS-BPIX and HYLITE. In this paper, we present a high-speed serializer circuit developed in a commercial 130-nm CMOS technology for the full-scale (128×128) pixel readout chip of HYLITE, which requires a data rate of 4 Gbps. The serializer adopts a 16-to-1 binary-tree multiplexer, a ring-oscillating based phase-locked loop (PLL) and a current mode logic driving stage with a multi-stage pre-amplifier. The test results show that it functions as expected with a wide operating range from 0.52 Gbps to 5.5 Gbps and satisfies the data-rate requirement. The measured jitter values at 5.12 Gbps are about 2 ps and 20 ps for the random and deterministic jitter, and 47 ps for the total jitter, and the horizontal and vertical eye openings are 0.84 UI and 72%. At the maximal 5.504 Gbps, the eye is still open and clear with the total jitter of about 52.2 ps. Several modules (the previous version of the PLL) has already been verified working normally after taking 130 Mrad (Si) X-ray irradiation. The full-scale HYLITE chip integrated the serializer has been fabricated in an engineering run. More detailed designs and tests will be reported.

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