

Serial Powering Scheme and Performance Analysis for Innermost Layer (L0) for ATLAS ITk modules

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After ten years of massive success, the Large Hadron Collider (LHC) at CERN is going for an upgrade to the next phase, the High Luminosity Large Hadron Collider (HL-LHC) which is planned to start its operation in 2029. This is expected to have a fine boost to its performance, with an instantaneous luminosity of $5.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ (ultimate value $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) with 200 average interactions per bunch crossing which will increase the fluences up to more than 10^{16} neq/cm^2 , resulting in high radiation damage in ATLAS detector [1]. To withstand this situation, it was proposed to make the innermost layer [L0] of the new Inner Tracker (ITk) with 3D silicon sensor modules, which will have a radiation tolerance of more than $1 \times 10^{16} \text{ neq/cm}^2$ with a TID of 9.9 MGy [2].

Each 3D sensor is bump-bonded to a FrontEnd (FE) chip to form a bare module, and three bare modules are powered in parallel in a triplet module. The L0 layer will have 396 triplet modules. To reduce cable material and improve detector performance, 3 to 5 triplets (depending on the location in the detector) will be powered in series. The FE chip implements a number of features (like a shunt-low-dropout regulator and over-voltage and under-shunt protection) needed to guarantee stable operation of the detector with this powering scheme. In this study, we powered in series 5 triplets based on the pre-production ATLAS FE chip for HL-LHC. We ensured that the chosen operational parameters are within our theoretical specs and result in stable operation of the modules within the serial power chain. Triplets were also powered in Low Power mode (LP), used to operate the module at a lower current, and their performance was tested without cooling requirements. The performance of the under-shunt and over-voltage protection were also analyzed.

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