LHCb VELO upgrade 2 readout

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On behalf of the LHCb VELO upgrade 2 groups
Position Sensitive Detectors
University of Oxford
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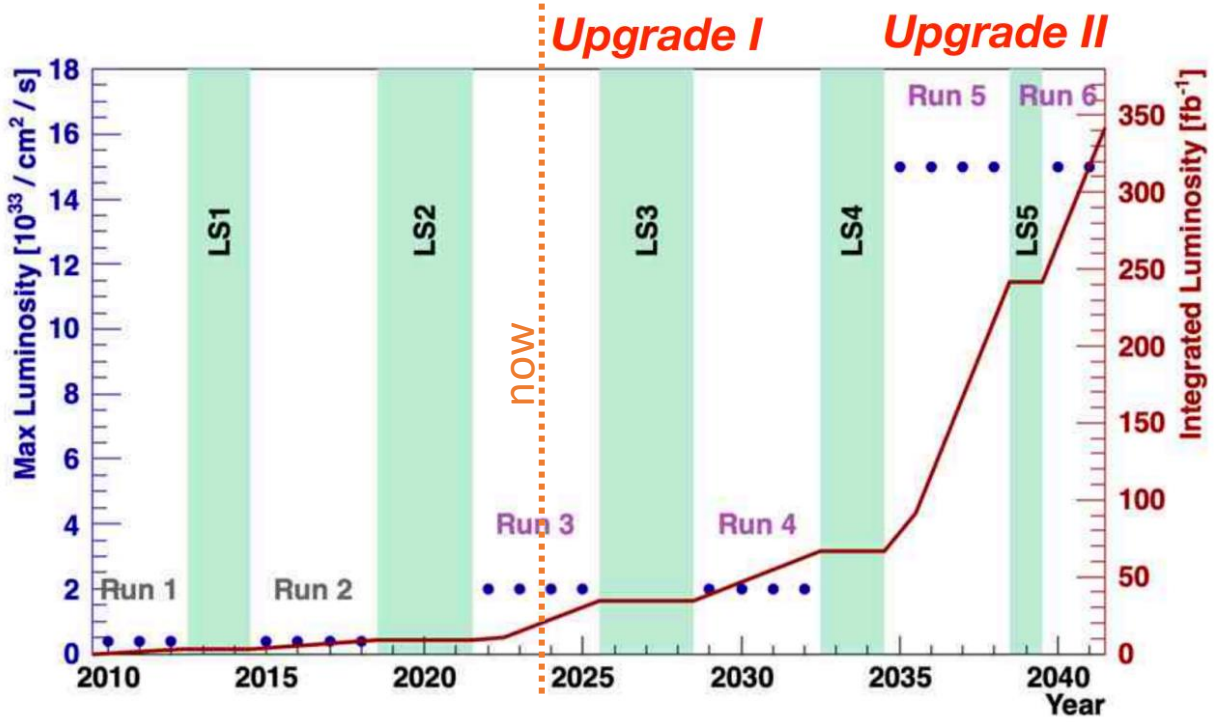
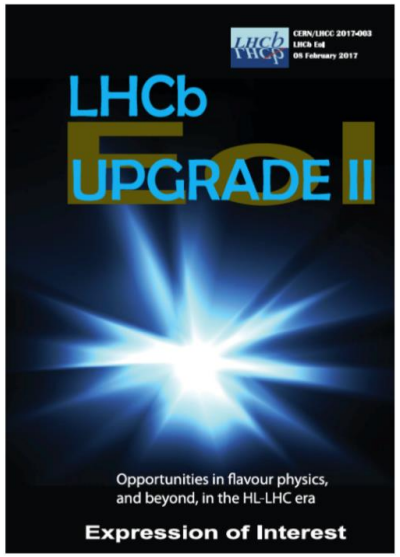
LHCb Upgrade 2 Schedule

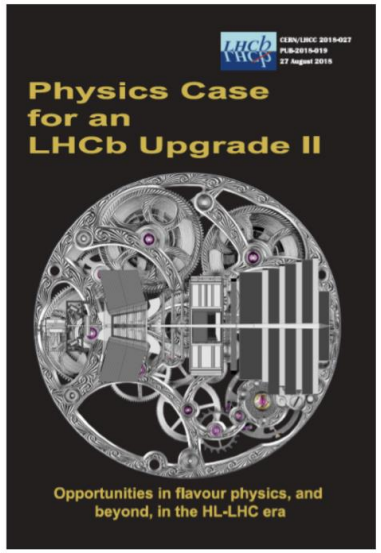
Current: Upgrade I being finalised/commissioning

2017: Expression of interest
2018: Physics case
2022: Framework Technical design report

2021-2024: Research and Development phase
2024: Technical design reports
2025-2026: LHCb Upgrade Ib
2025-2030: (R&D+) Production phase
2032: LHCb Upgrade II / Start of Run 5

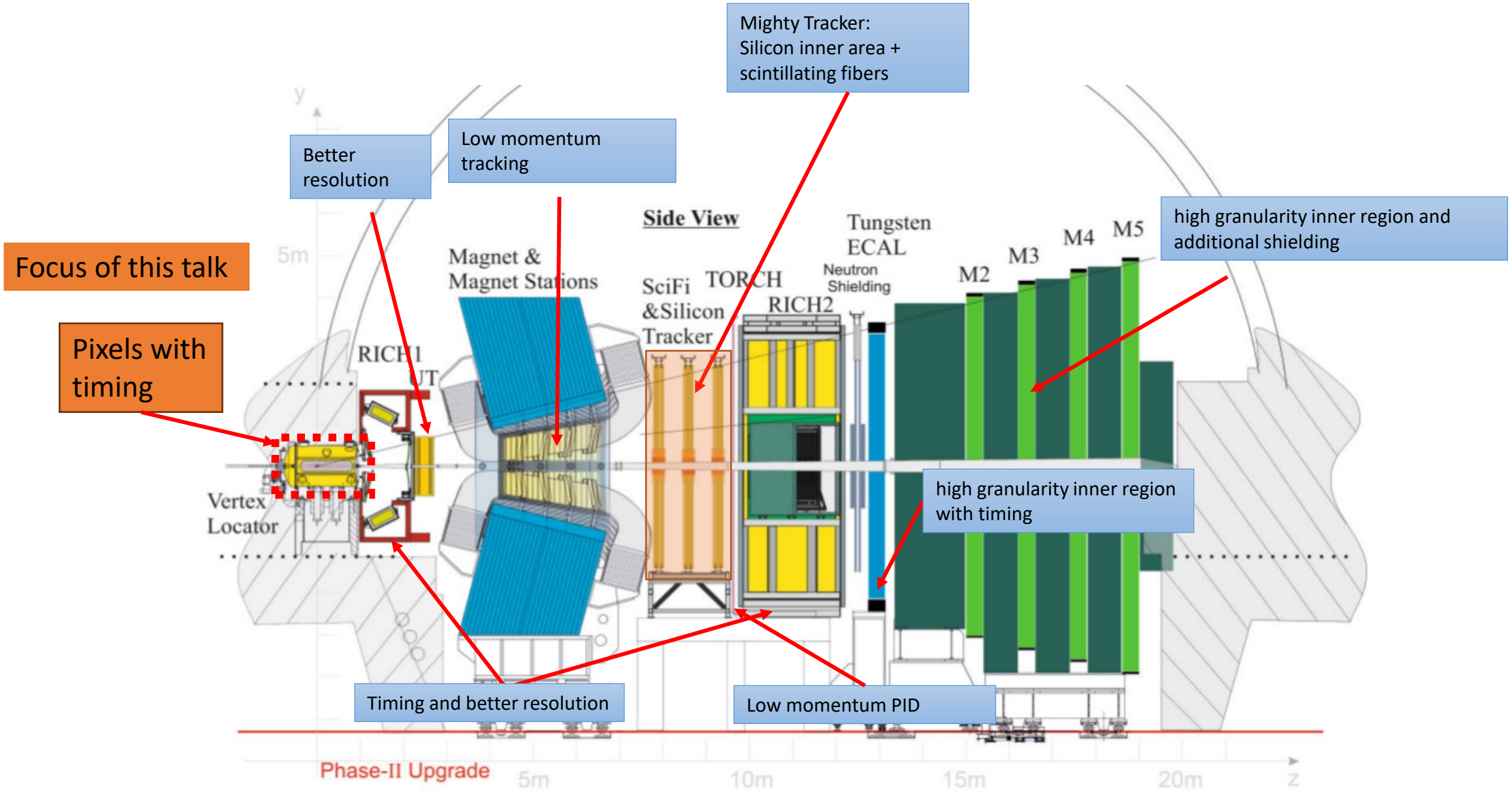






LHCb Upgrade II

CERN-LHCC-2021-012

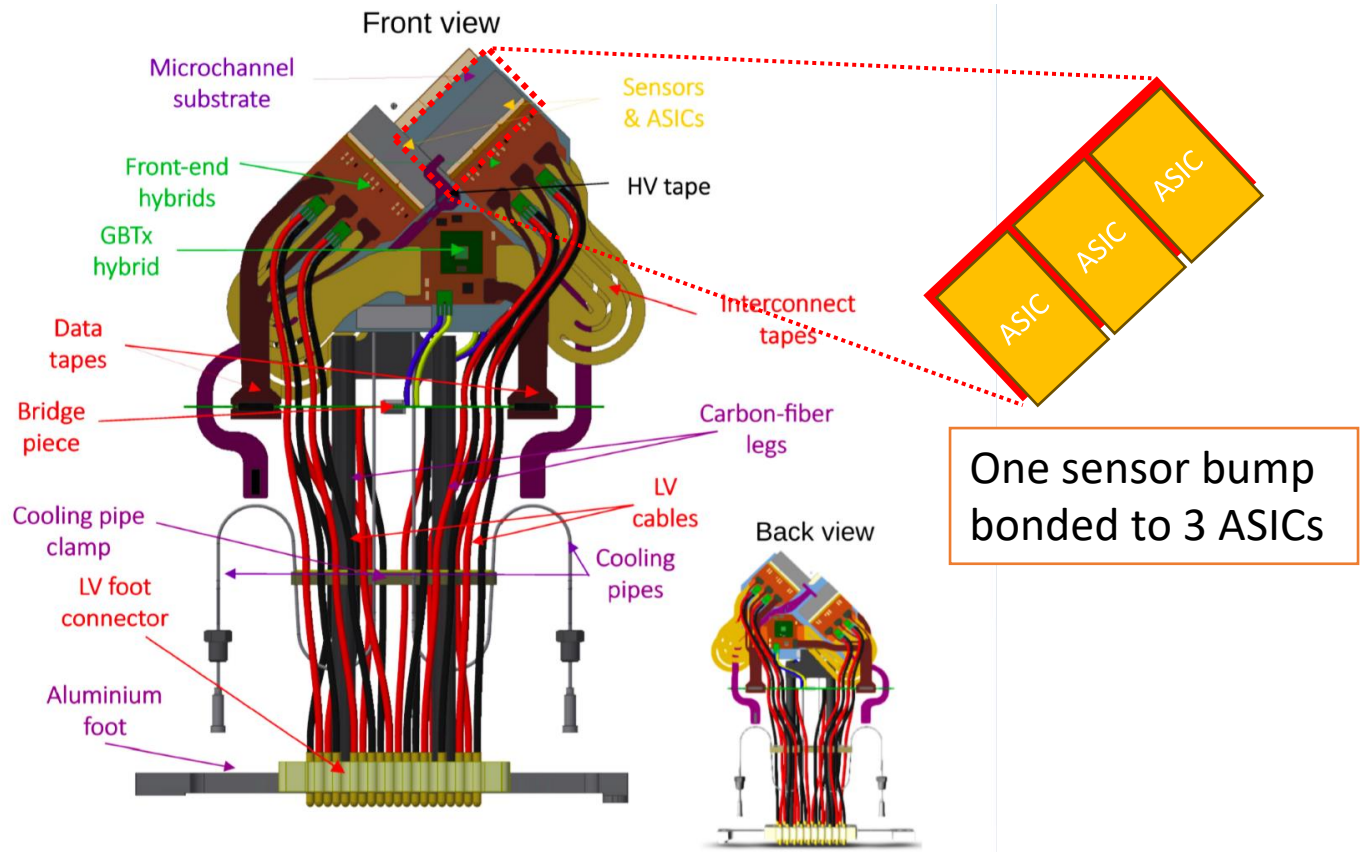


LHCb VELO Upgrade 1

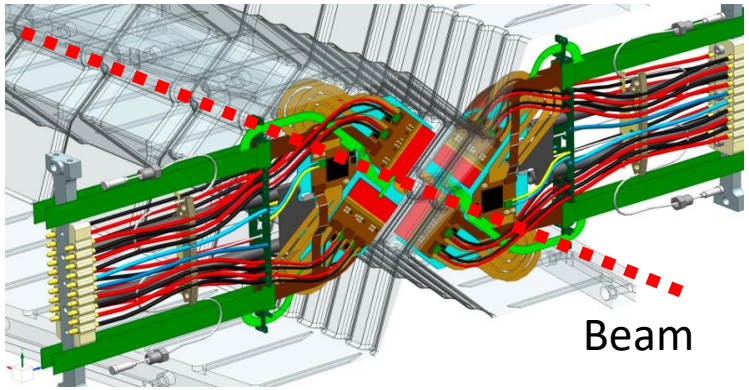
Modules key features

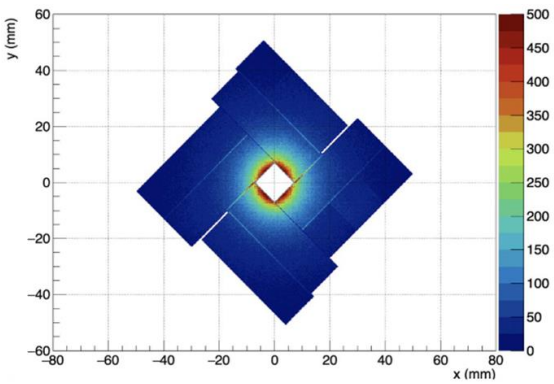
- The closest distance to LHC beam will be 5.1 mm
- Very high (8×10^{15} neq/cm^2) and non-uniform radiation (~r^{-2})
- Vacuum operation
- ASIC power dissipation ~1W/cm2
- Silicon microchannels CO_2 evaporative cooling J.NIMA.2022.166874
  - Sensor temperature < $-20^{\circ}C$ to mitigate radiation damage

More details on Pawel's Talk on Monday



One sensor bump bonded to 3 ASICs

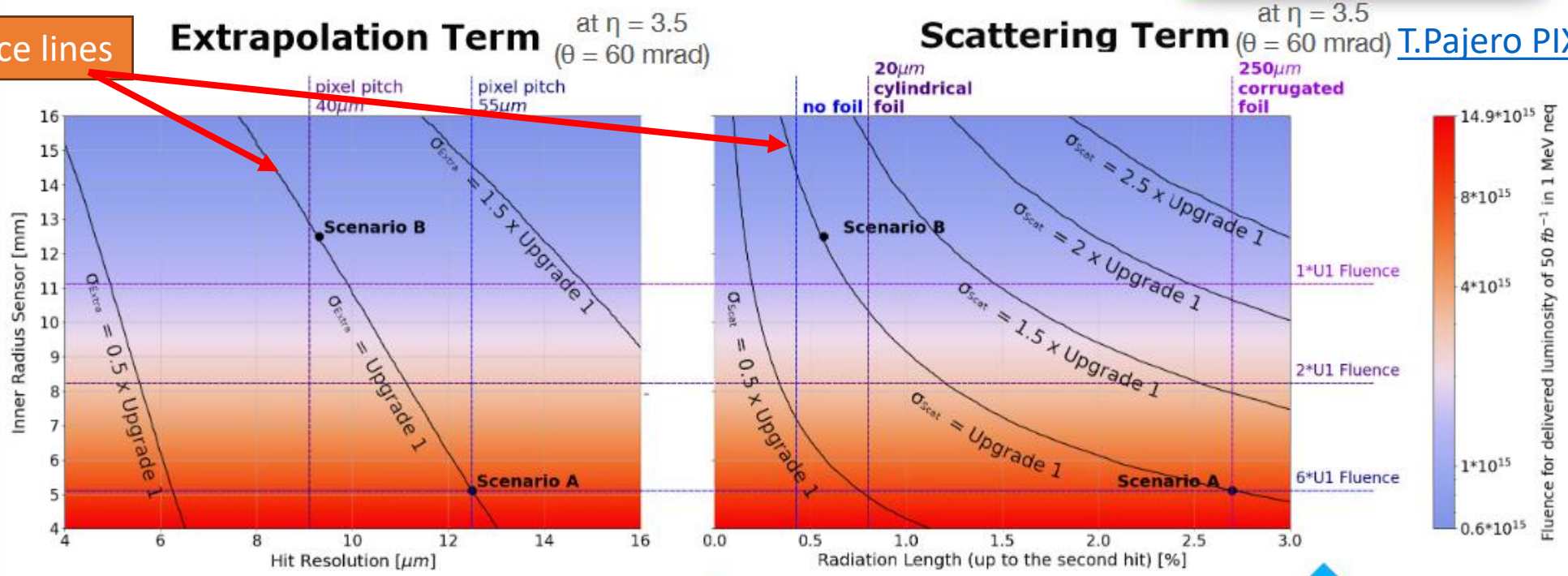




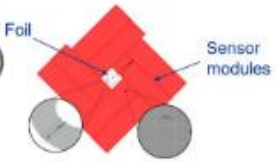
LHCb VELO Upgrade 2

$$\sigma_{IP} = \sigma_{extra} \oplus \frac{\sigma_{scat}}{p_T}$$

Iso-performance lines



Scenario A (S_A) (same as in UI, at 7.5× lumi)



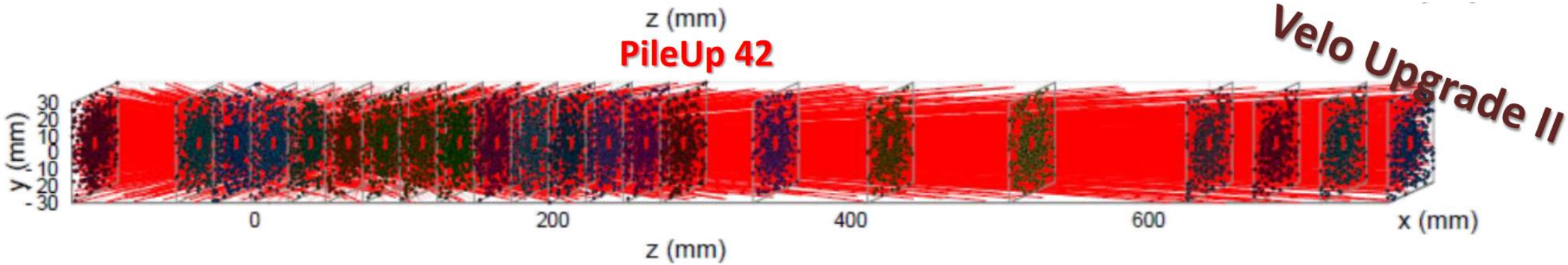
- 5.1 mm inner radius
- 55 × 55 μm pixels
- 6 × 10^{16} 1 MeV n_{eq} cm^{-2} maximum fluence, 3 Grad ionising dose
  - highly non homogeneous
  - radiation harder sensors or regular replacement
- >250 Gb/s ASIC bandwith (900 Mtracks/cm^2/s)

Scenario B (S_B)

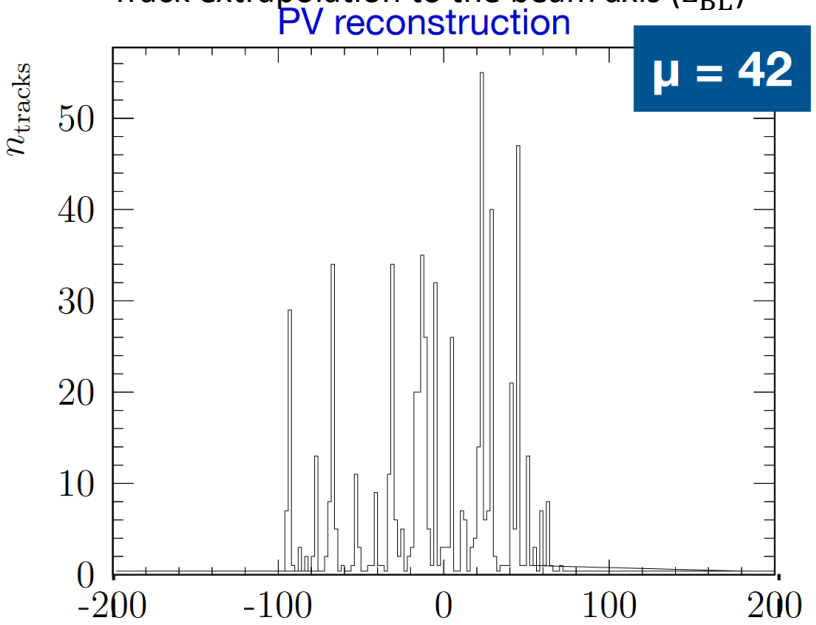
- 12.5 mm inner radius
- 42 × 42 μm pixels
- 5× reduction of material budget before 2nd hit
  - much thinner RF foil or substitution with wires
- 8 × 10^{15} 1 MeV n_{eq} cm^{-2} maximum fluence, 400 Mrad ionising dose
- >94 Gb/s ASIC bandwith

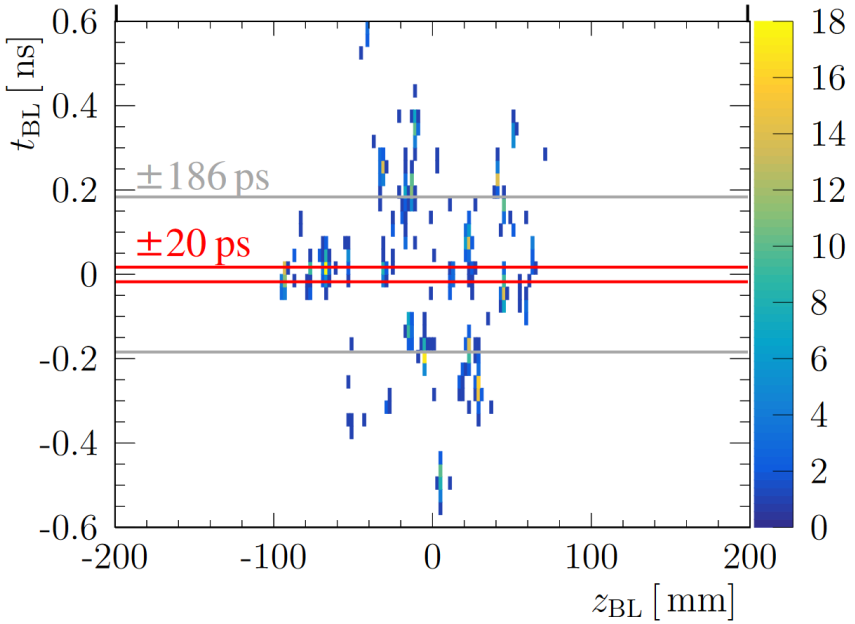
LHCb-PUB-2022-001

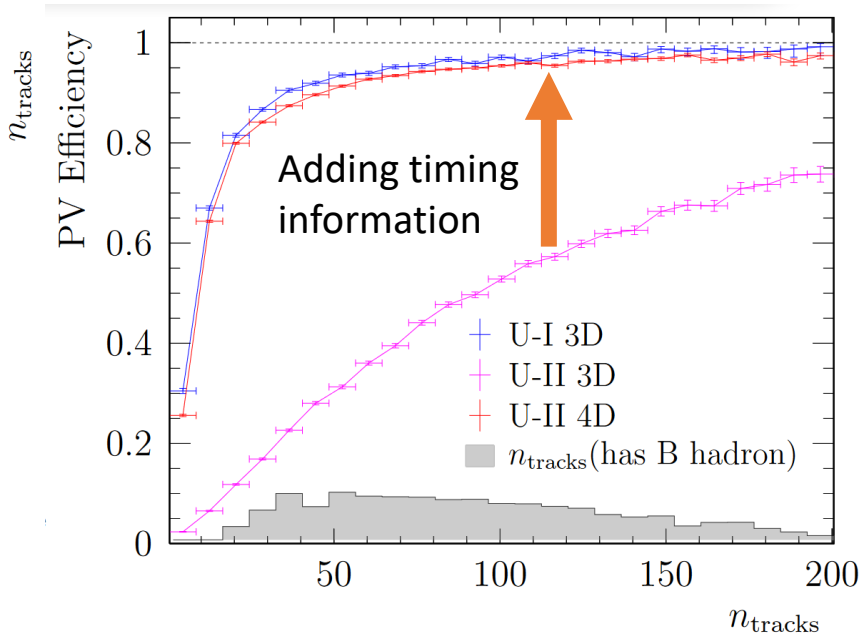
Pile-Up challenge (VELO U2)



Track extrapolation to the beam axis (z_{BL})







The time resolution of 20 ps per track (50 ps per hit) restores the upgrade 1 detector performance

LHCb VELO Upgrade 2 (time resolution)

$\sigma_t(\text{hit})$ - required to be $< 50\text{ps}$ due to the track reconstruction efficiency.

$$\sigma_t^2 = \sigma_{\text{Landau}}^2 + \sigma_{\text{distortion}}^2 + \sigma_{\text{jitter}}^2 + \sigma_{\text{TDC}}^2$$

Sensor contribution

σ_{Landau} - fluctuations along the particle path, depends on the sensor thickness and integrated signal charge

$\sigma_{\text{distortion}}$ - non-uniform weighting field and non-saturated drift velocity in the sensor

σ_{jitter} - signal to noise ratio can be improved with on sensor gain

Sensor contribution evaluated to be of order of $\lesssim 40$ ps (3D trench sensor, Planar 50um sensors, LGADs)

ASIC contribution

σ_{jitter}- it can be improved with a faster amplifier rise (ASIC)

σ_{TDC} - depends on **T**ime-to-**D**igital **C**onverter implementation in the ASIC

Timepix4 has a 200ps TDC ($200\text{ps}/\sqrt{12}$ => $\sigma_{\text{TDC}} \sim 60\text{ps}$).

ASIC R&D is needed.

LHCb VELO Upgrade 2 (R&D)

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	$\leq$55	$\leq$42
Matrix size	256×256	335×335
Time resolution RMS [ps]	$\leq$ 30	$\leq$ 30
Loss of hits [%]	$\leq$ 1	$\leq$ 1
TID lifetime [MGy]	$>$ 24	$>$ 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	$\leq$ 500	$\leq$ 500
Pixel rate hottest pixel [kHz]	$>$ 350	$>$ 40
Max discharge time [ns]	$<$ 29	$<$ 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	$>$ 250	$>$ 94

Priority

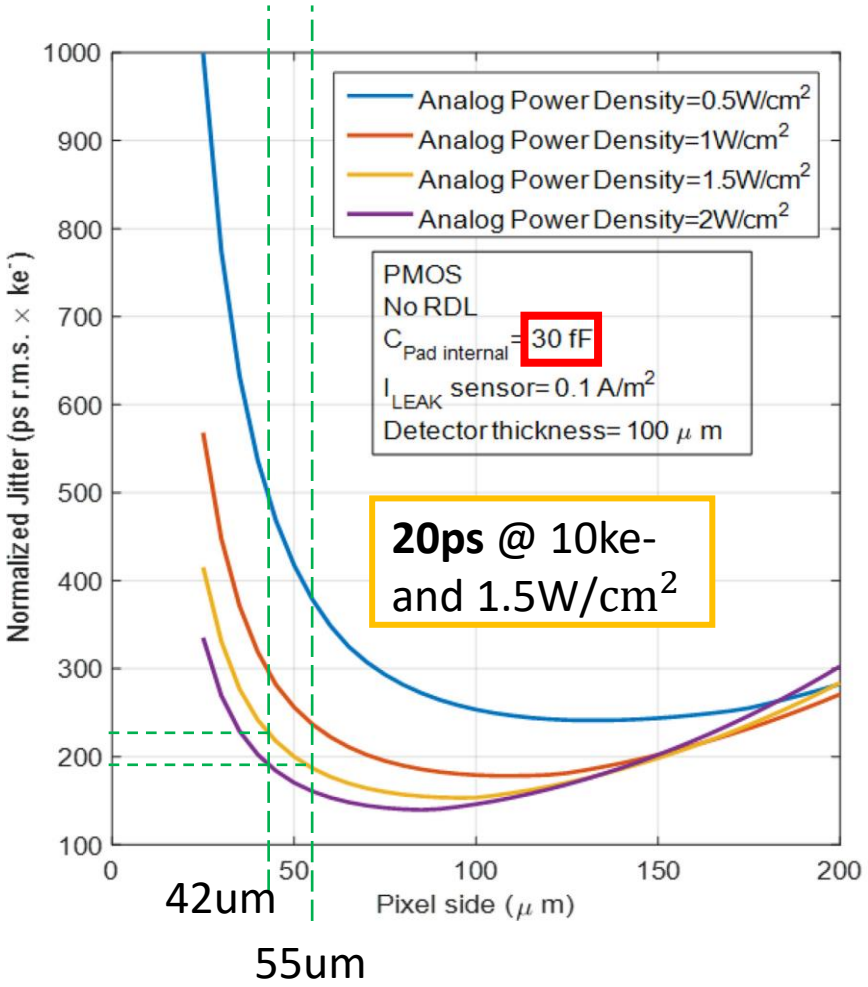
Challenging!

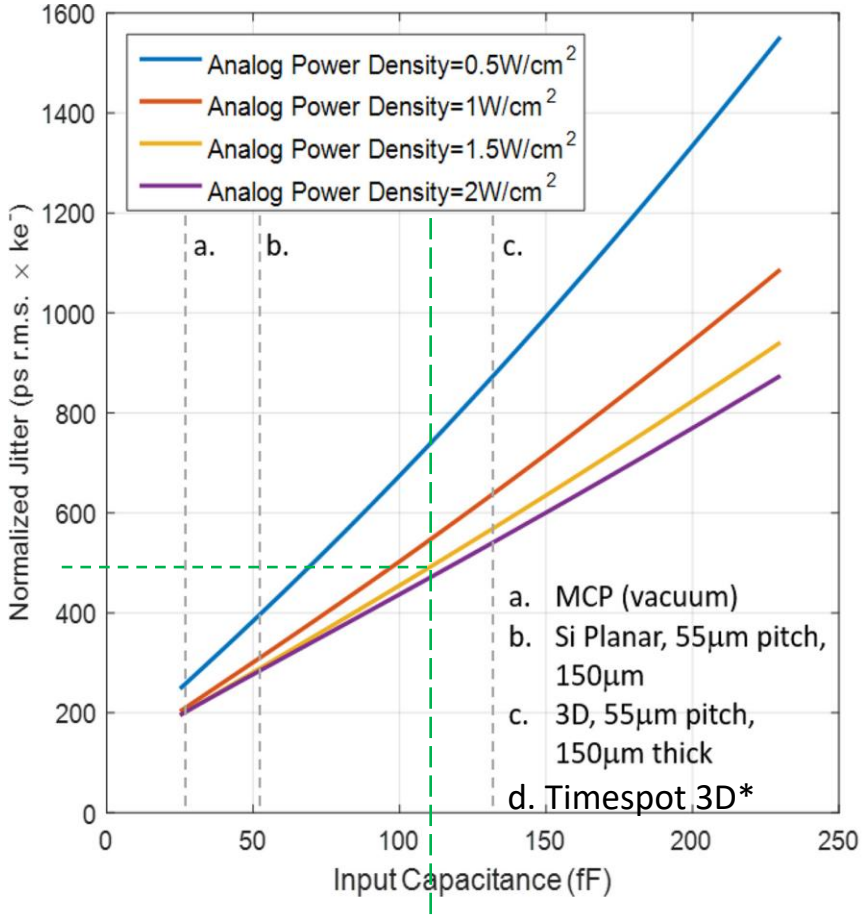
doable

Lessons learnt from the Timepix4 design

R. Ballabriga et al

$$\frac{dv_{out}(t)}{dt} = \frac{Q_{in} g_m}{C_O(C_{IN}+C_{FB})} \frac{\frac{Q_{in}}{C_{FB}} - V_{th}}{\frac{Q_{in}}{C_{FB}}}$$





*F. Borgato et al

Larger signals improves the time resolution (sensor technology)

Larger pixels increases the capacitance (noise increase)

Very small pixels limits the current for the transistor (decreases rise time)

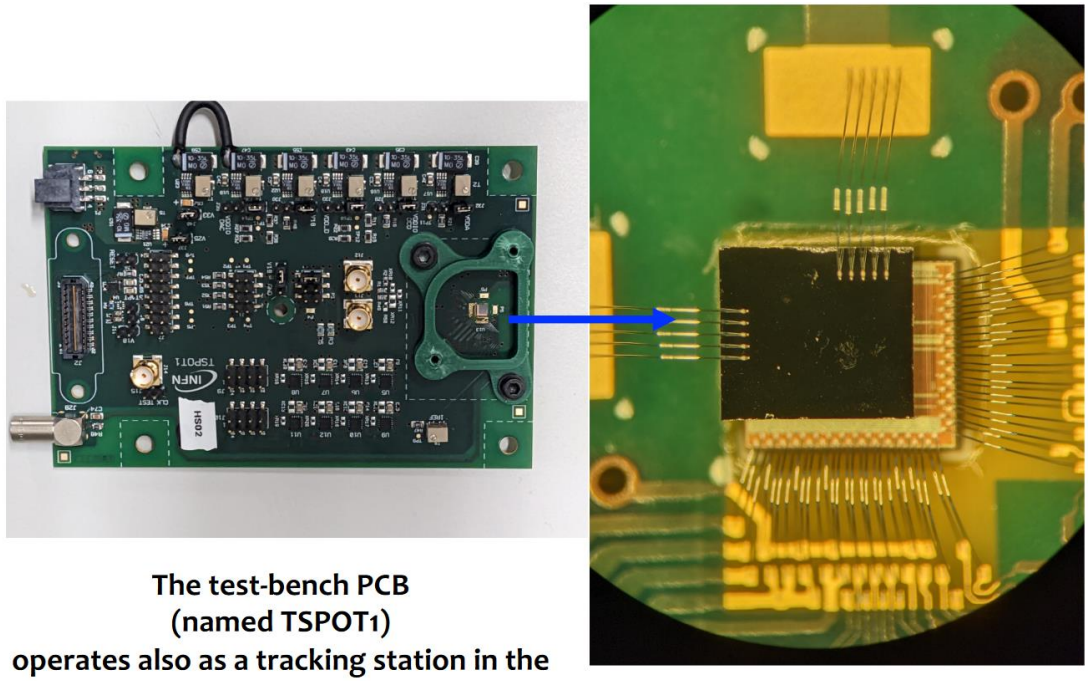
Smaller capacitance improves the time resolution

Why not more power? Vacuum operation and maximum sensor temperature (cooling)

R&D efforts

TimeSpot (14 INFN sites)

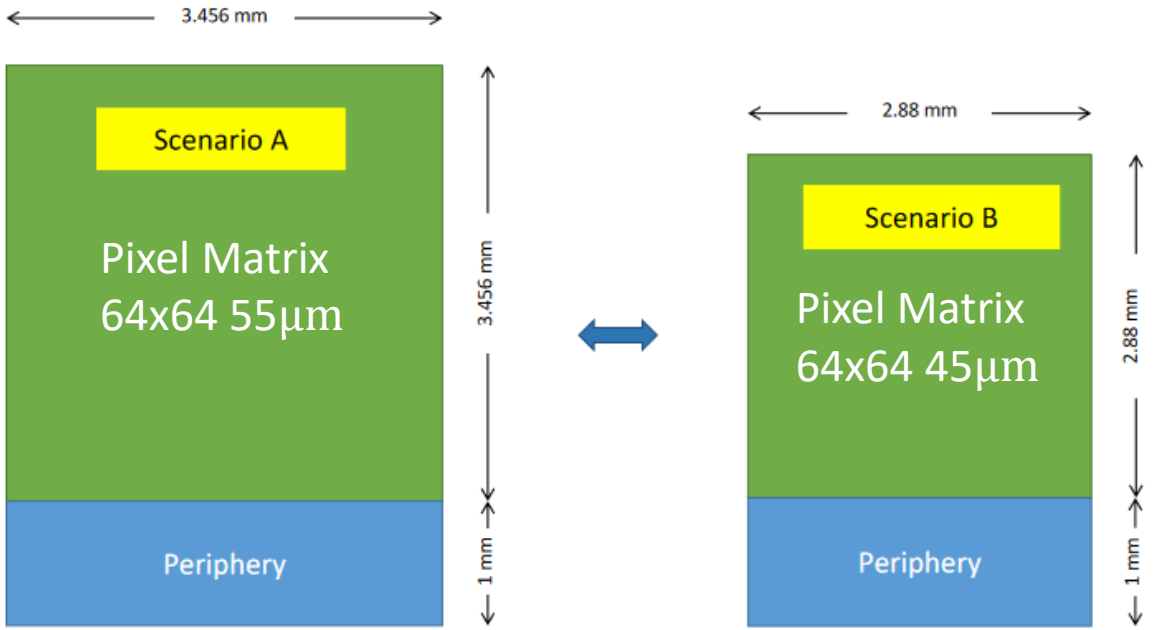
28 nm CMOS
First submission (single test-cells)
Second submission of the ASIC (32x32 pixels, 55 um pixels)
Manufactured and tested



The test-bench PCB
(named TSPOT1)
operates also as a tracking station in the demonstrator (test beam at SPS)

PicoPix (CERN, NIKHEF, IGFAE)

28 nm CMOS
Timepix4 Experience
Aiming for a large-scale prototype chip (64x64 pixels)
In line with scenario A and B (55µm or 45µm)

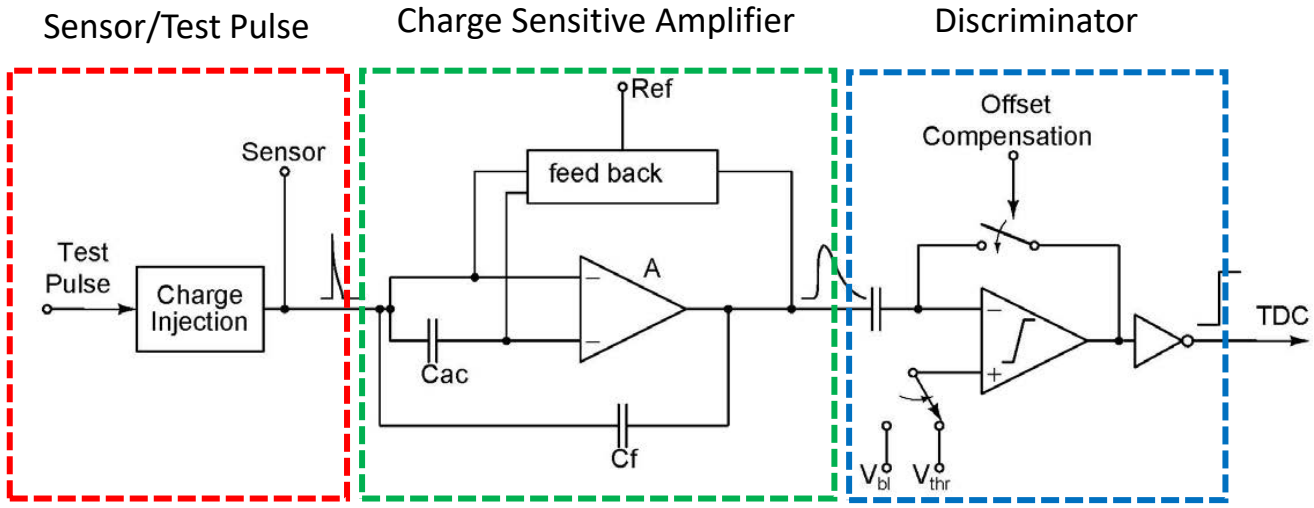


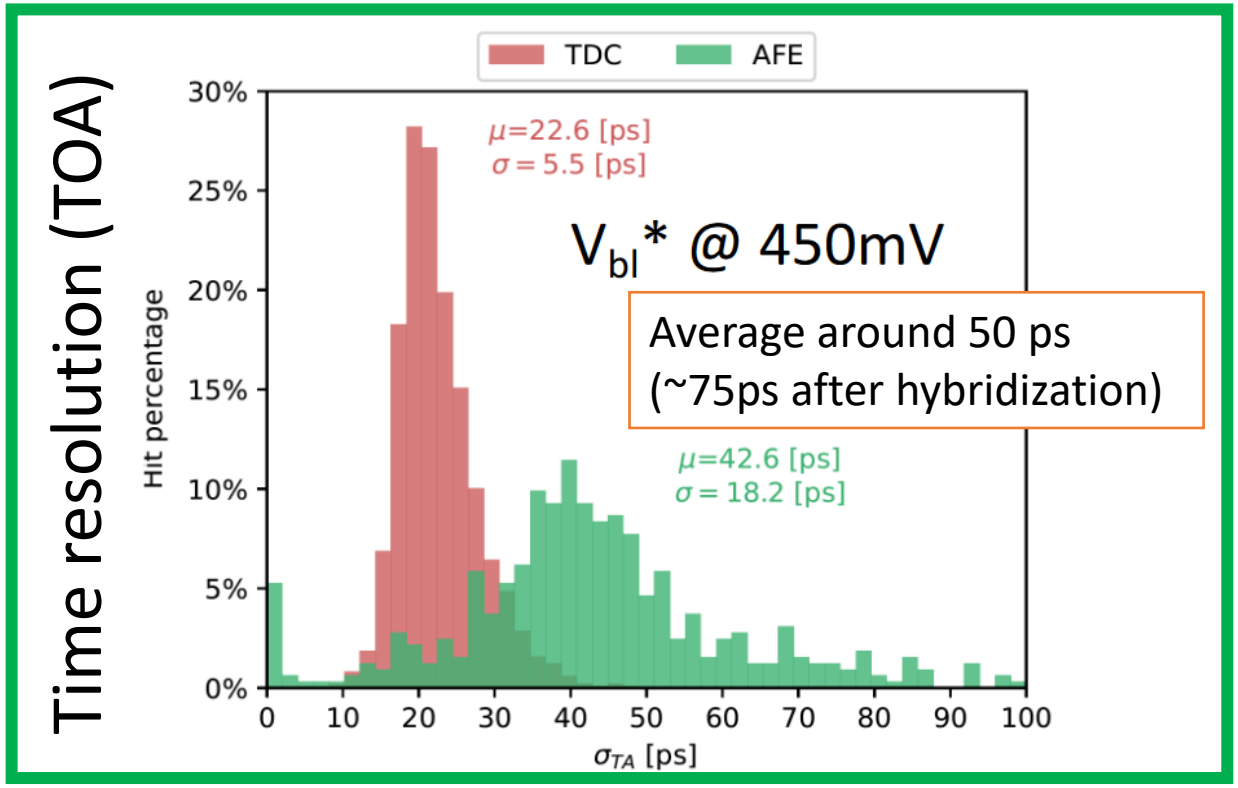
TimeSpot

Sandro Cadeddu et al

- Full functionality demonstrator (TimeSpot1)
- 32x32 pixels, 6 mm2 (55 um pitch)
  - 2 x 512 pixels
- Signal and TDC test pulse capabilities allow time resolution measurements for the analogue and TDC contributions
  Digital and analogue services distributed to 2x16 pixel blocks
- Read Out Trees -> every 128 channels globally timestamped and sent to the serializer
- Data out after serialization via LVDS

Covered in detail on Lorenzo's talk on Tuesday





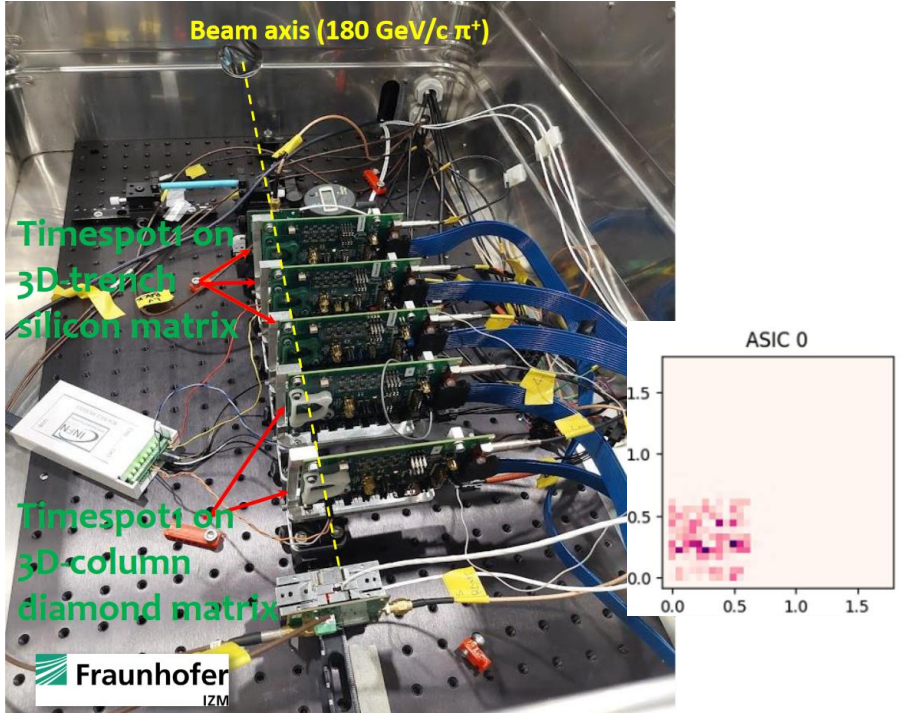
TimeSpot

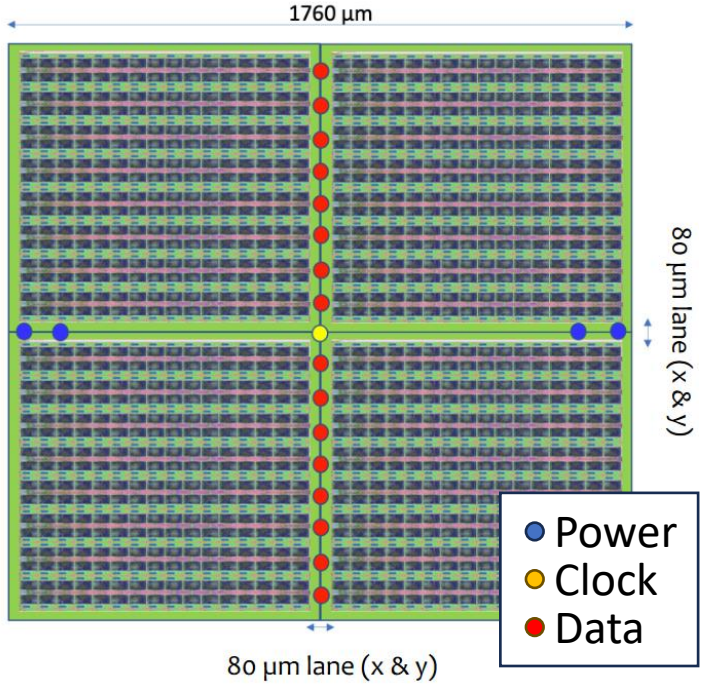
- Tracks with 28nm technology were acquired and reconstructed
  - Several lessons learnt (DAQ, matrix, TDCs, …)

- Challenges:
  - High expected power per pixel (LHCb @ 350kHz, $38\mu W/ch$)
  - Better clock distribution (reference clock jitter)
  - Time resolution of the analogue front-end is better than 20ps or below by design

Covered in detail on Lorenzo's talk on Tuesday

- Next step:
  - Efforts will be continued by the IGNITE
  - IGNITE0 submitted in July/2023 (8x4 chip, expected in Nov/2023)
  - Larger matrix (64x64) submission on end of 2023 – beginning of 2024
  - Through Silicon Vias (TSV) being investigated for power and clock distribution, and data transmission



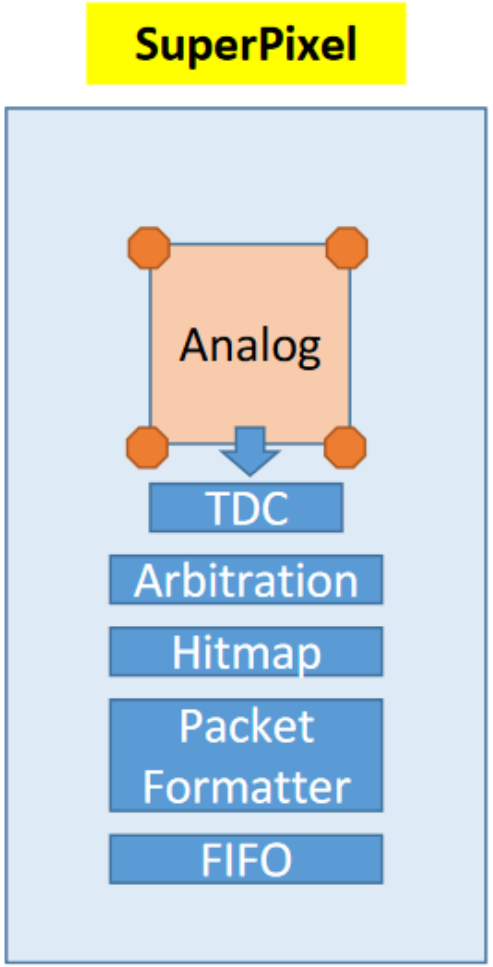


PicoPix

EP R&D Seminar (V. Sriskaran) and Challenges with fast timing on large pixel matrices (X. Llopart)

"Exploration" phase
Being designed to be a large-scale prototype on the first submission

- Analog FE, Pixel readout, Pixel data clustering
- dDLL clock distribution (as in Timepix4)
- Low power clock distribution
- Superpixel and superpixel groups (similar to Timepix4)
- Single event effect robust architecture
- On-chip bandgap and biasing DACs



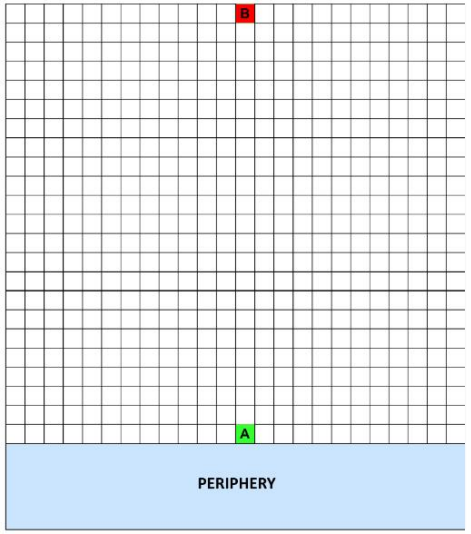
- 1 analog island
  - 4 Front-end and 4 discriminators
- Disc. Inputs are OR-ed
  - one TDC measurement per SuperPixel
- Free running DCO (2-3 GHz) with 10 phases:
  - Time bin size: 50-33 ps
  - Time resolution: 14.4-9.5 ps

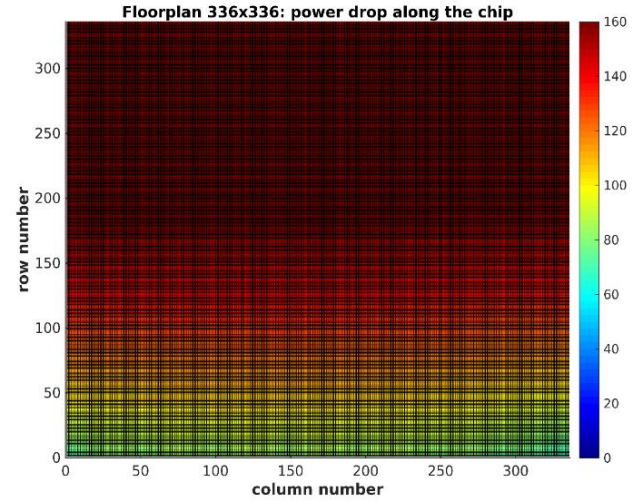
PicoPix

EP R&D Seminar (V. Sriskaran) and Challenges with fast timing on large pixel matrices (X. Llopart)

Simulated power drop in a 336x336 array of 45 µm pixels having 2 $\mathrm{W/cm^{-2}}$ analogue power density

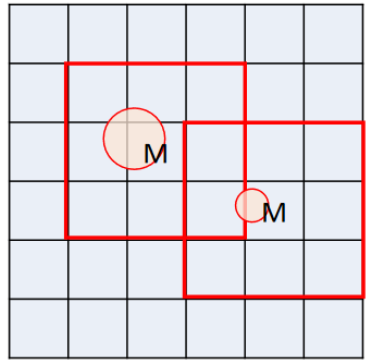
- $\sigma_{\mathrm{TOA}}(\mathrm{Pixel\ B}) > 2 \times \sigma_{\mathrm{TOA}}(\mathrm{Pixel\ A})$
- Non-uniformity observed on the Timepix4 VCO frequency due to the power drop before TSVs





On-pixel and on-chip clustering (most events are cluster of 1-4 pixels)

- Readout only the largest event in cluster (charge) and veto large clusters (>3x3)
  - Best time (TOA) and energy (TOT) resolution and cluster hitmap
- Data rate reduction by around a factor x7 (preliminary)
  - 600 Gbps -> 86 Gbps per ASIC



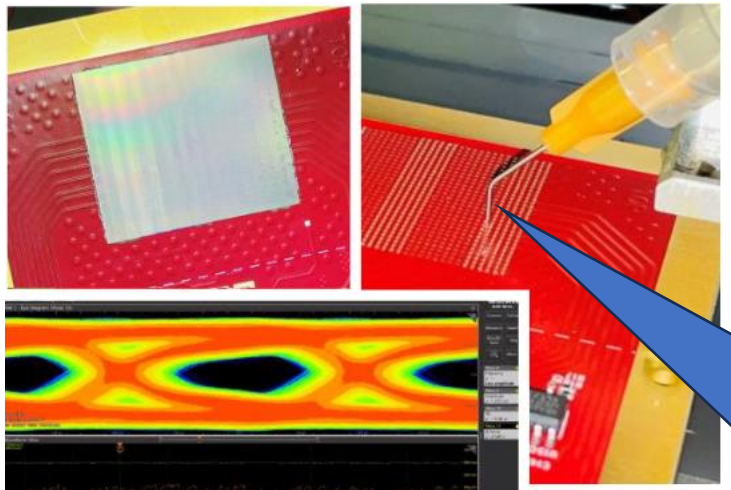
- TSMC 28 nm CMOS: Provides great level of integration at pixel level, good radiation tolerance (LHCb U2 workshop)
- Two possible designs being considered in-line with the scenario A and B
- Submission expected on Q2/2024

Integration and data rates

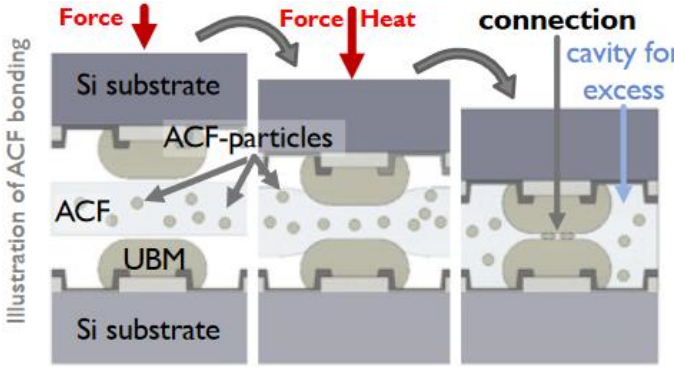
ACF and ACP

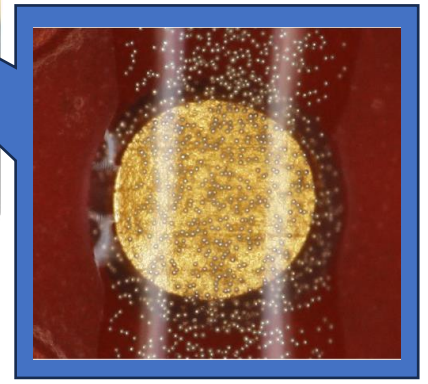
- Anisotropic Conducting Film or Paste
- Conduction stablished via conductive particles
- Encouraging results with early version of Timepix4v0
- Good communication with the chip

[VELO U2 workshop]



(Jerome & Xavi Llopart)



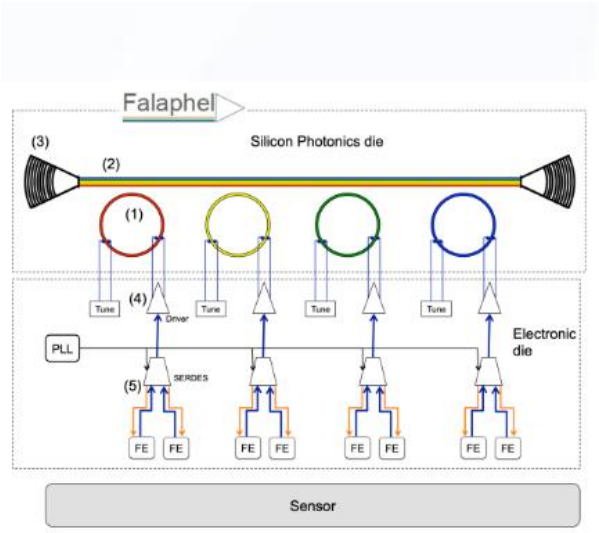


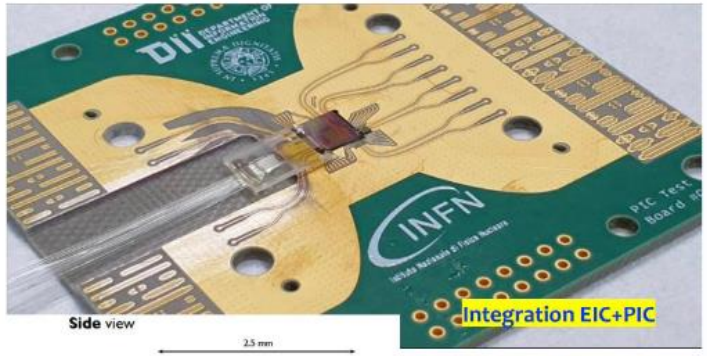
CERN EP-ESE and UNIGE (Université de Genève)

FALAPHEL

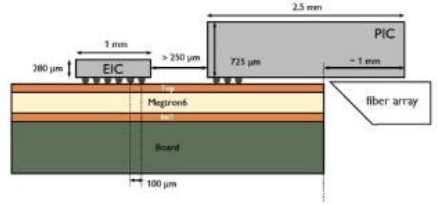
- CMOS 28nm EIC + Photonic IC (PIC)
- Driver 25 Gbps
- Target: 10^{16} neq MeV/cm^2 radiation tolerance

[VELO U2 workshop], [DRD7 workshop]





Side view



Conclusion

LHCb VELO upgrade 2

- ASIC time resolution below 30ps required for the track reconstruction
- High data rates (250Gb/s per ASIC, Scenario A)
- Limited power due to the operation in vacuum/cooling (up to $1.5 - 2\mathrm{W/cm^2}$)
- Non-uniform radiation environment (up to $6 \times 10^{16}\ \mathrm{MeV\ neq/cm^2}$)

TimeSpot → IGNITE

- Second interaction of the chip reached an overall time resolution around 50ps (75ps after hybridization)
- New test chip submitted in July/23 (Expected by Nov/23)
- Larger matrix design of 64 x 64 or 128 x 128 is being prepared

PicoPix

- “Exploration Phase” based on the timepix4 experience
- Aiming for a large-scale prototype on the first submission (64x64 pixels)
- Expected submission by Q2/2024

Integration and data rates

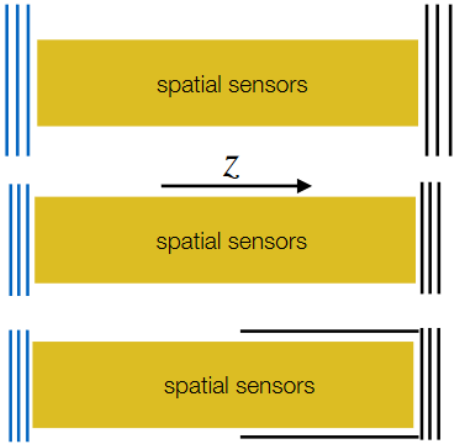
- ASIC integration via anisotropic conducting film or paste being studies (encouraging results with timepix4v0)
- Falaphel (Silicon photonics, 25Gbps, target $10^{16}\ \mathrm{neq\ MeV/cm^2}$)

Thank you for your attention!

Backup slides

Why not just timing layers?

T.Pajero PIXEL 2022



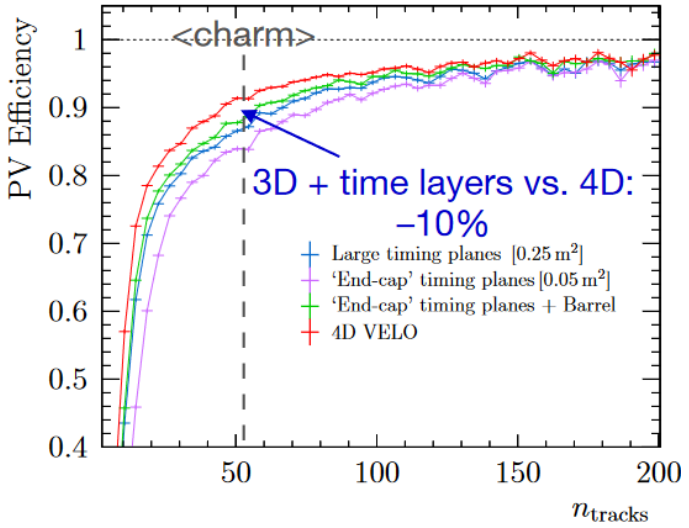
3D VELO + timing layers

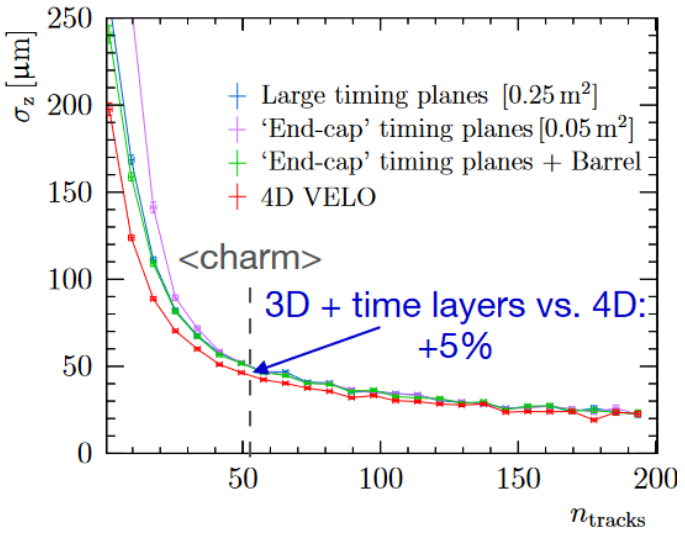
- at least 3 layers for efficiency and and combinatorics removal
- larger pitch (100 μm)
- 25 ps per layer
- lower radiation tolerance acceptable
- very large area required compared to VELO ($$$)

	VELO *(à la U1)*	Large endcaps	Endcaps	Endcaps + barrel
Covered range	$2 < \eta < 5$	$2 < \eta < 5$	$2.8 < \eta < 5$	$2 < \eta < 5$
Area [m²]	**0.15**	**1**	**0.3**	**1.35**

4D VELO

- 50 ps single-hit resolution
- better performance (efficiency, ghost rate)
- lower cost
  - single sensor technology and ASIC
  - easier event reconstruction





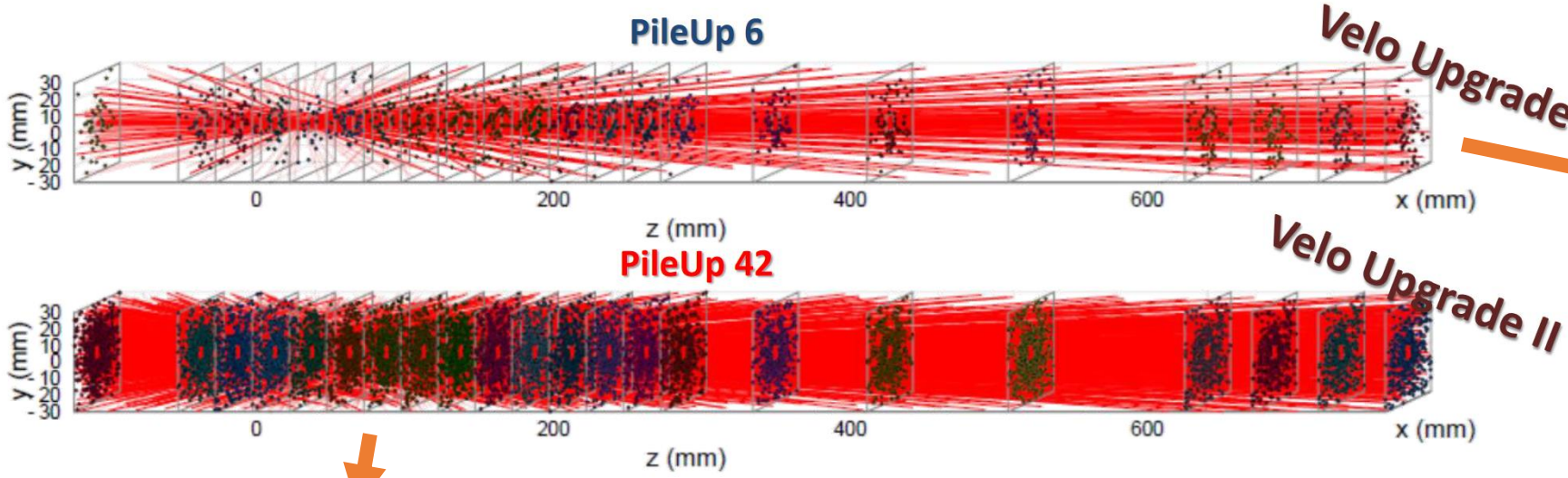
LHCb-PUB-2022-001

Timepix4

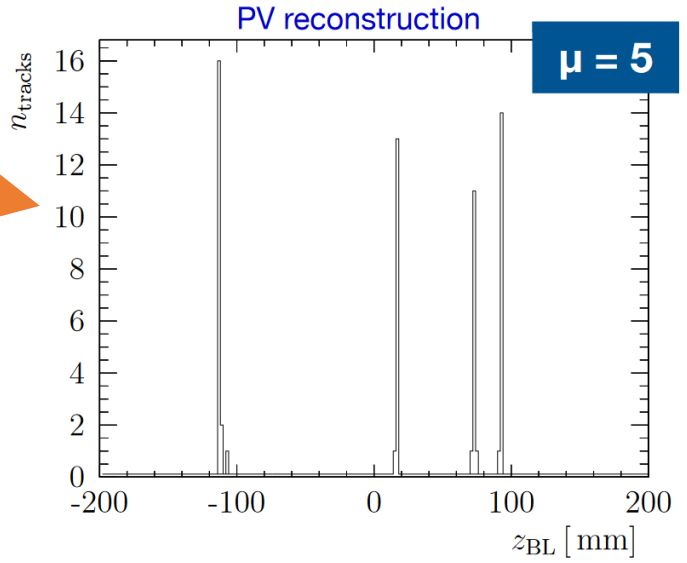
			Timepix3 (2013)	Timepix4 (2019)	
Technology			130nm – 8 metal	65nm – 10 metal	
Pixel Size			55 x 55 µm	55 x 55 µm	
Pixel arrangement			3-side buttable 256 x 256	4-side buttable 512 x 448	
Sensitive area			1.98 cm^2	6.94 cm^2	3.5x
Readout Modes	Data driven (Tracking)	Mode	TOT and TOA		
		Event Packet	48-bit	64-bit	33%
		Max rate	0.43x10^6 hits/mm^2/s	**3.58x10^6 hits/mm^2/s**	8x
		Max Pix rate	1.3 KHz/pixel	**10.8 KHz/pixel**	
	Frame based (Imaging)	Mode	PC (10-bit) and iTOT (14-bit)	CRW: PC (8 or 16-bit)	
		Frame	Zero-suppressed (with pixel addr)	Full Frame (without pixel addr)	
		Max count rate	~0.82 x 10^9 hits/mm^2/s	~5 x 10^9 hits/mm^2/s	
TOT energy resolution			< 2KeV	< **1Kev**	2x
TOA binning resolution			1.56ns	**195ps**	8x
TOA dynamic range			409.6 µs (14-bits @ 40MHz)	**1.6384 ms** (16-bits @ 40MHz)	4x
Readout bandwidth			≤5.12Gb (8x SLVS@640 Mbps)	**≤163.84 Gbps (16x @10.24 Gbps)**	32x
Target global minimum threshold			<500 e^-	<500 e^-	

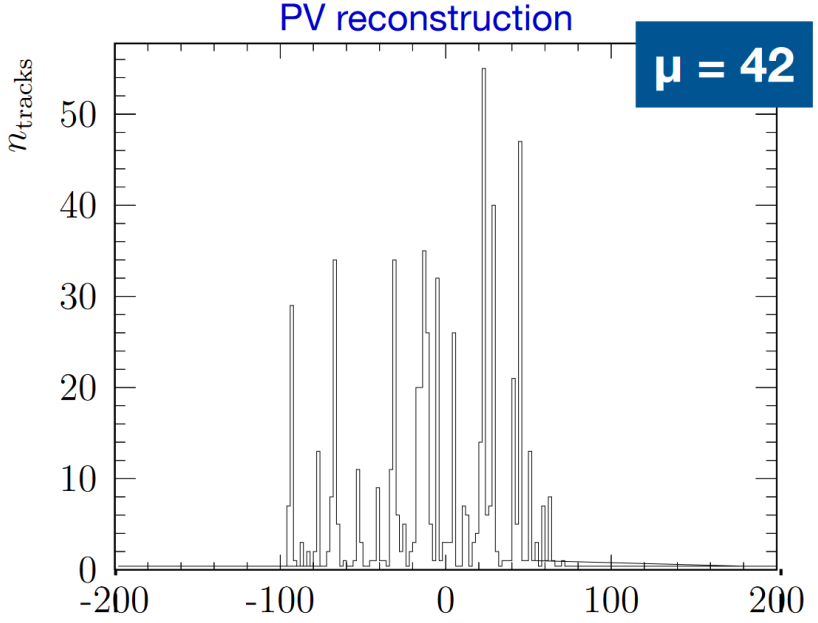
28.2 x 25.6 mm^2

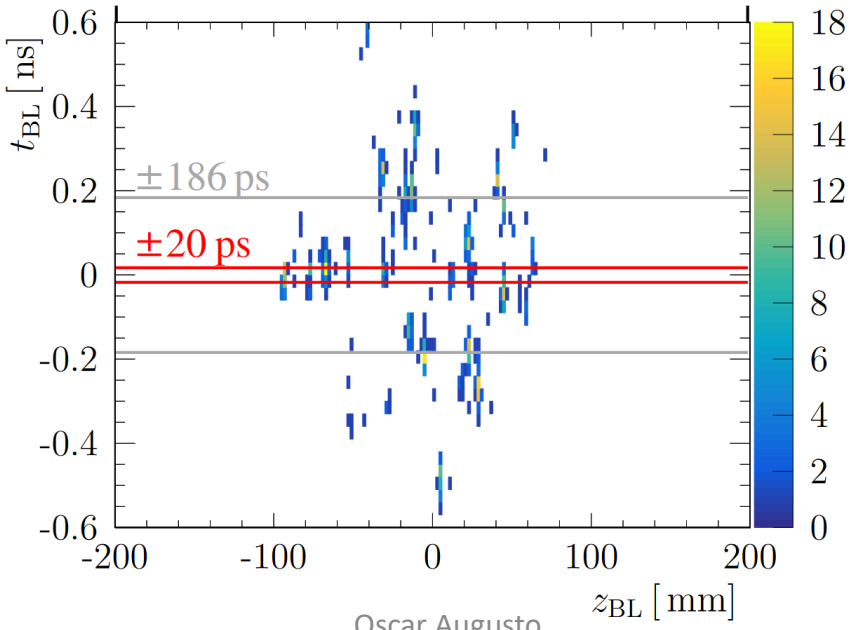
LHCb VELO Upgrade 2

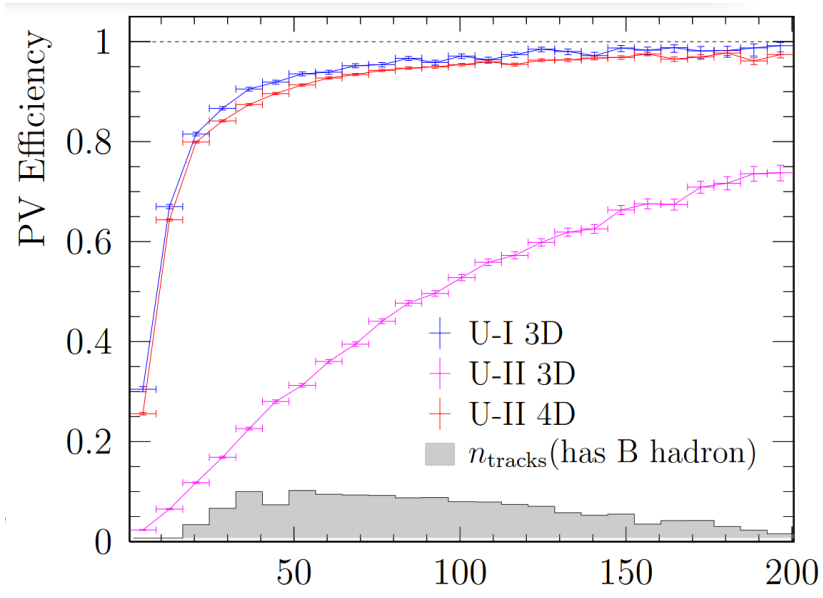


Track extrapolation to the beam axis (z_{BL})









LHCb VELO Upgrade 2

Requirement	5.1 mm distance	12.5 mm distance	VeloPix (2022)
Technology [nm]	28nm?	28nm?	130
Pixel matrix	256x256	335x335	256x256
Pixel pitch [um]	≤ 55	≤ 42	55
RMS Time resolution [ps]	≤ 50	≤ 50	~ 7200
Power per area [W/cm^2]	1.5	1.5	< 0.8
Power per pixel [uW]	23	14	5
TID lifetime [MGy]	> 24	> 3	4
Pixel rate hottest pixel [kHz]	> 350	> 40	50
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94	20

This talk will focus on the latest results from the R&D programs TimeSpot and PicoPix.

LHCb VELO Upgrade 2 (R&D)

Requirement	scenario S_A	scenario S_B
Pixel pitch [µm]	≤55	≤42
Matrix size	256×256	335×335
Time resolution RMS [ps]	≤ 30	≤ 30
Loss of hits [%]	≤ 1	≤ 1
TID lifetime [MGy]	> 24	> 3
ToT resolution/range [bits]	6	8
Max latency, BXID range [bits]	9	9
Power budget [W/cm^2]	1.5	1.5
Power per pixel [µW]	23	14
Threshold level [e$^-$]	≤ 500	≤ 500
Pixel rate hottest pixel [kHz]	> 350	> 40
Max discharge time [ns]	< 29	< 250
Bandwidth per ASIC of 2 cm^2 [Gb/s]	> 250	> 94

Priority

Challenging!

doable

Main (preliminary) requirements in next-generation (4D)trackers

Requirement	LHCbU2 Run5 (Scenario A)	LHCbU2 Run5 (Scenario B)	NA62++ (HIKE)	CMSPPS/ run4(5)	CMS run5 forward	FCC–hh (VERY preliminary)
Pixel pitch [μm]	55	42	≤300	50-100	≈100	10
Hit time resolution RMS [ps] (electronics stage)	30	30	30	30	30	< 20
NIEL lifetime for sensors [n/cm^2]	6 x 10^{16}	8 x 10^{15}	n x 10^{16}	10^{16}	n x 10^{15}	10^{18}
TID lifetime for electronics [Grad]	2.4	0.3	2	1	0.05	x10 ?
Power budget [W/cm^2]	1.5	1.5	≈ 4.5	1-2	1	TBD
Power per pixel [μW]	25	14	300	25-50	100	TBD
Hit rate [GHz/cm^2]	12 (max)	2.5	10	6	6	30
Data BW [Gbps/ASIC]	250	94	10-20	100	10	x10 ?
Material budget (per station)	<0.8% X_0	<0.8% X_0	<0.5% X_0	< 1	1	≈1
Trigger scheme/peculiarities	triggerless	triggerless	Tbd (triggerless?)	Tbd (triggered?)	triggered, serial pwr	TBD

Further upcoming interests on 4D tracking (with similar specs): high intensity/ rare effects (e.g. PIONEER proposal @PSI, π rare decays), neutrino tagging techniques in LBL experiments, Muon colliders (background rejection).