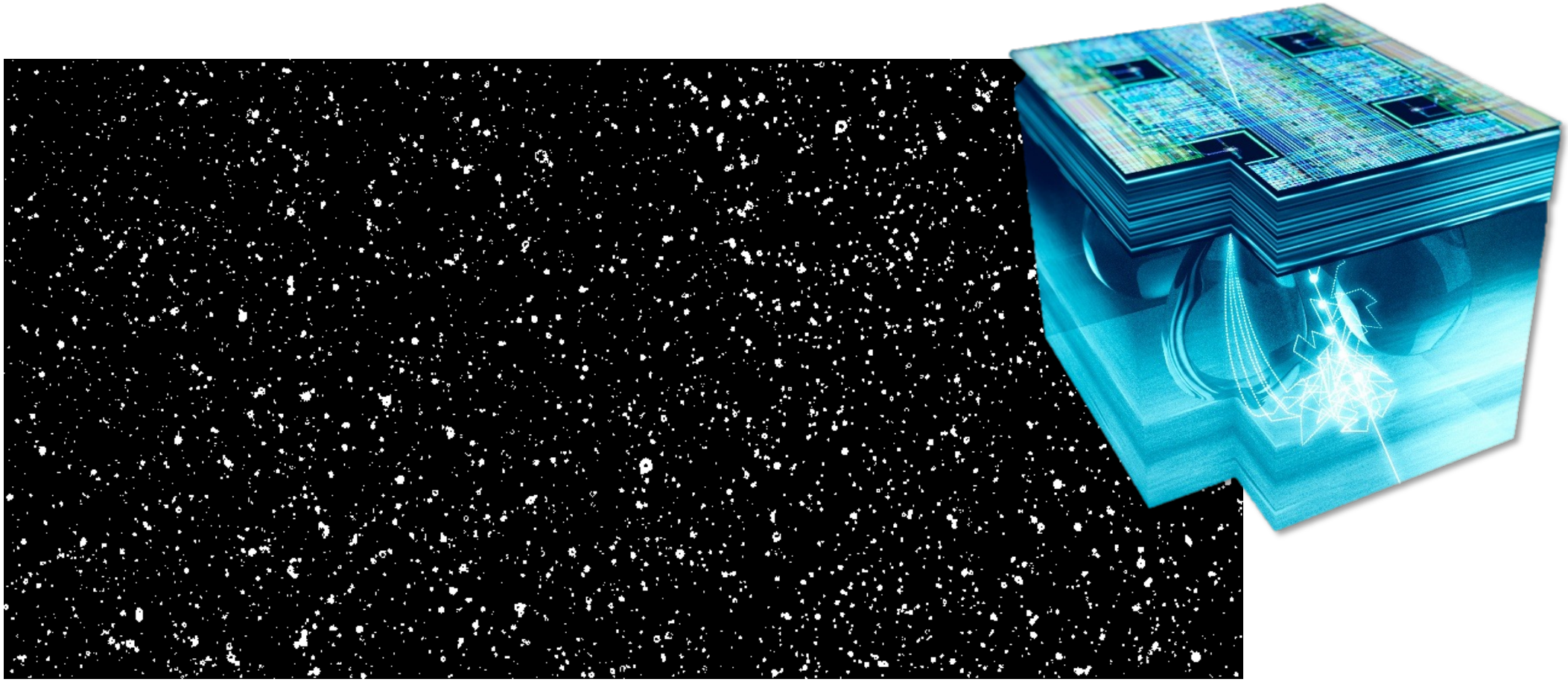
Advances in (monolithic) pixel detectors



ALPIDE prototype: 200 MeV protons at PSI

W. Snoeys
Geneva, Switzerland

PSD13, Oxford, UK, September 7th, 2023

walter.snoeys@cern.ch

Acknowledgements

- D. Bortoletto and the workshop organizers

- Colleagues from CERN, the ALICE ITS and ITS3 upgrade, ATLAS ITk, WP1.2 …

CMOS Monolithic Active Pixel Sensors revolutionized the imaging world

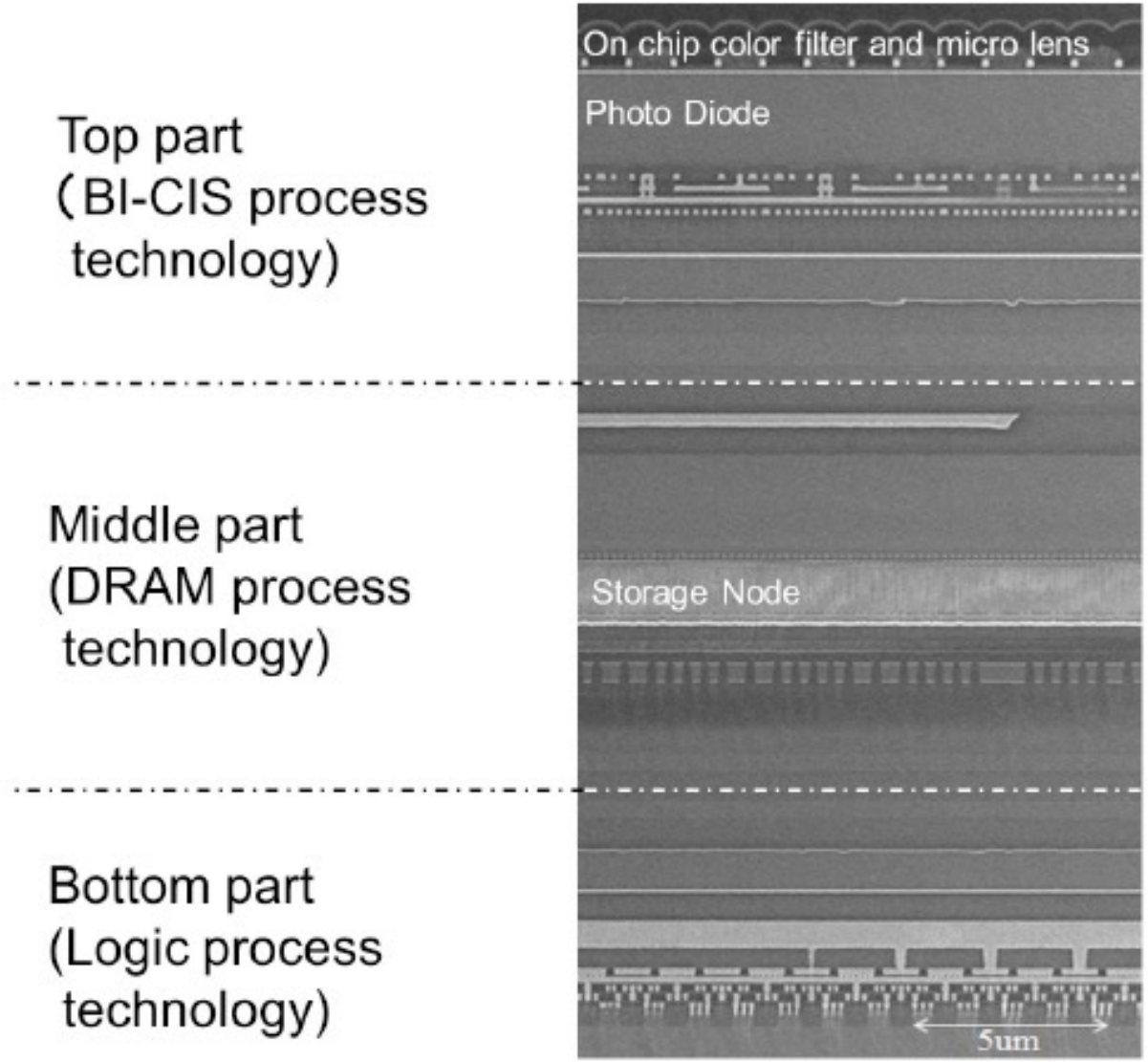
reaching:

- less than 1 e^- noise
- > 40 Mpixels
- Wafer scale integration
- Wafer stacking (now offered by foundries)
- …

Silicon has become the standard in tracking applications both for sensor and readout

… and now CMOS MAPS make their way in High Energy Physics !

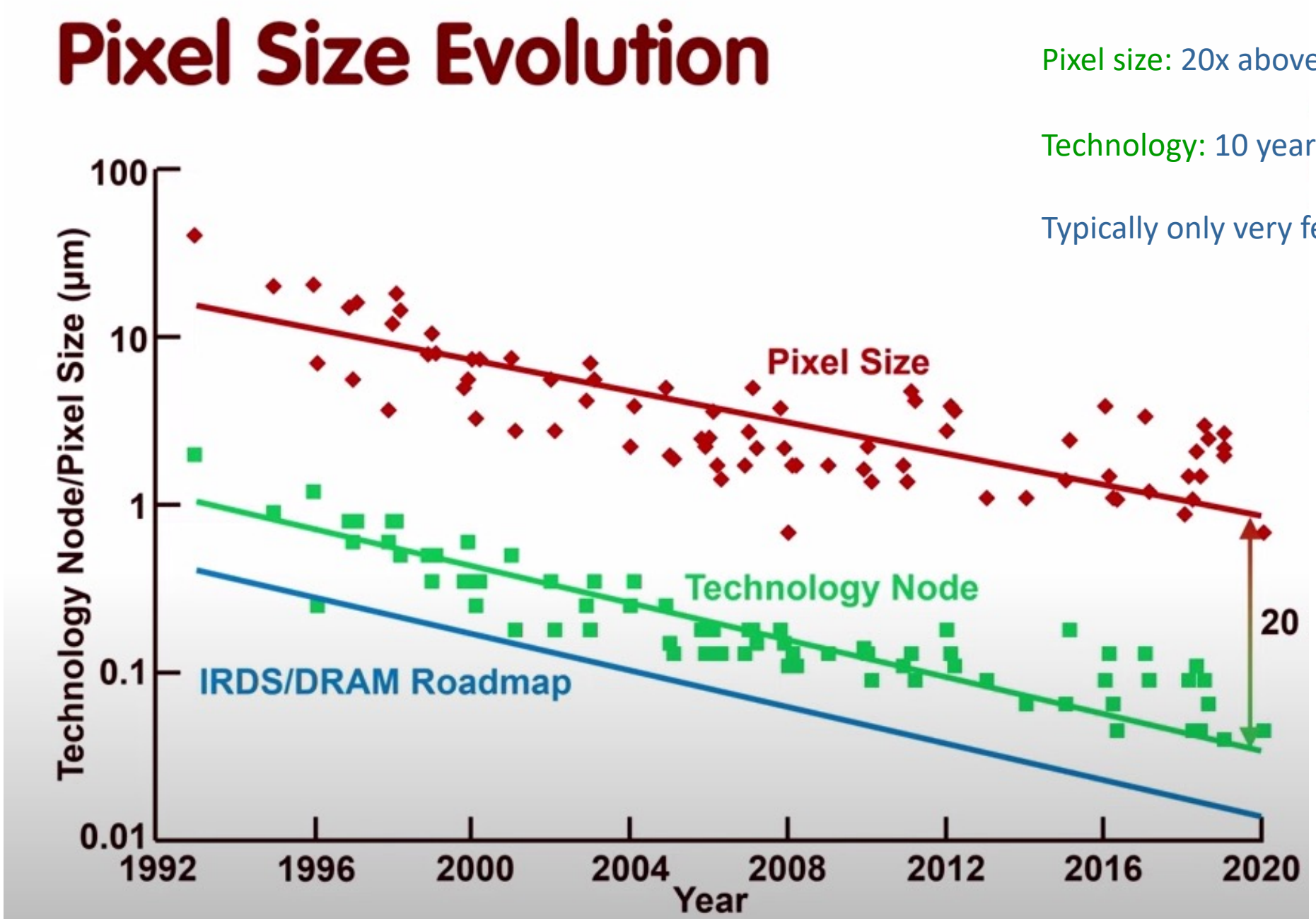
Hybrid still in majority in presently installed systems



Sony, ISSCC 2017

New technologies (TSV's, microbumps, wafer stacking…) make the distinction between hybrid and monolithic more vague.

Evolution of pixel size and technology node for visible:



Pixel size: 20x above technology feature size

Technology: 10 years behind DRAM technology

Typically only very few (1-4) transistors per pixel

Many more transistors per pixel for HEP !

Albert Theuwissen, ISSCC 2021

Requirements for High Energy Physics

	Dose (Mgy)	Fluence (10^{16} 1MeVn_{eq}/cm^2)
ALICE ITS	**0.01**	**10^{-3}**
LHC	**1**	**0.1…0.3**
HL-LHC 3ab^{-1}	**5**	**1.5**
FCC	**10-350**	**3-100**

Radiation tolerance

- CMOS circuit typically more sensitive to ionizing radiation
- Sensor to non-ionizing radiation (displacement damage)

Single particle hits instead of continuously collected signal in visible imaging

- Sparse images < or << 1% pixels hit per event
- Near 100% efficiency, full CMOS in-pixel needed, often circuit (much) more complex

Position resolution (~µm)

Low power consumption is the key for low mass

- Now tens of mW/cm^2 for silicon trackers and hundreds of mW/cm^2 for pixels
- Despite enhanced detector functionality for upgrades, material penalty limits power consumption increase

More bandwidth

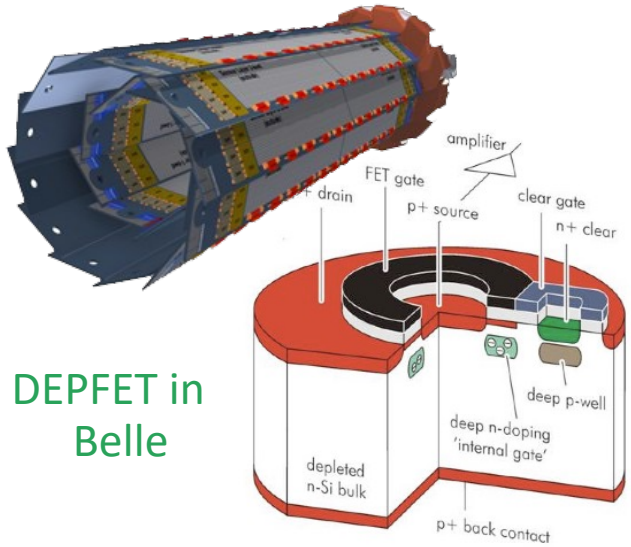
Time resolution

- Time stamping ~ 25 ns or even lower, ... much lower (10s of ps)

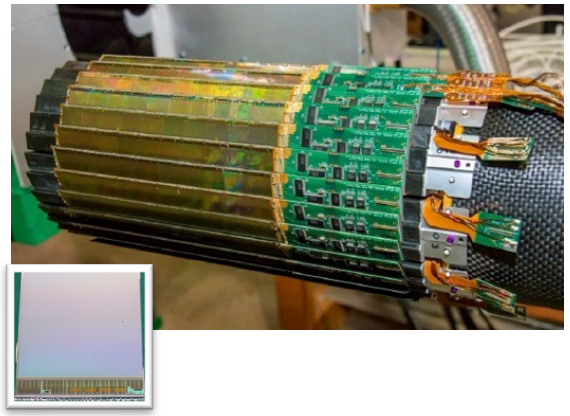
Larger and larger areas

- ALICE ITS2 10 m^2, discussions on hundreds to even thousands square m^2,
- Interest for versatile sensors programmable for different applications (P. Allport CERN EP seminar 2020)

Monolithic sensors in HEP move into mainstream CMOS technology



DEPFET in Belle



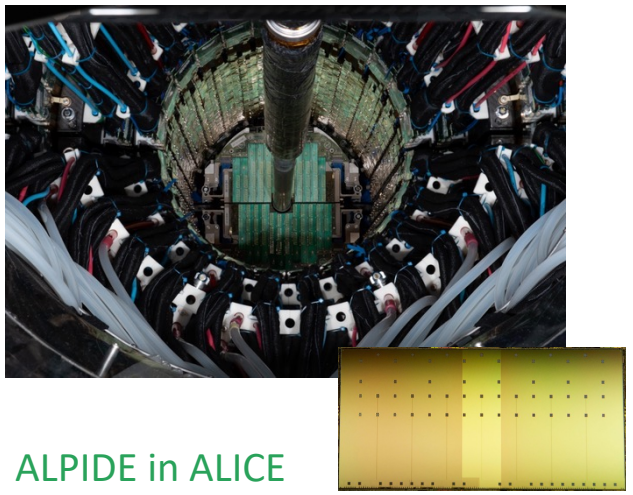
MIMOSA28 (ULTIMATE) in STAR

IPHC Strasbourg

First MAPS system in HEP

Twin well 0.35 µm CMOS

- Integration time 190 µs
- No reverse bias -> NIEL few 10^{12} 1 MeV n_{eq}/cm^2
- Rolling shutter readout



ALPIDE in ALICE

First MAPS in HEP with sparse readout similar to hybrid sensors

Quadruple well 0.18 µm CMOS

- Integration time <10 µs
- Reverse bias but no full depletion -> NIEL ~10^{14} 1 MeV n_{eq}/cm^2

DEPLETED MAPS for better time resolution and radiation tolerance

Large collection electrode

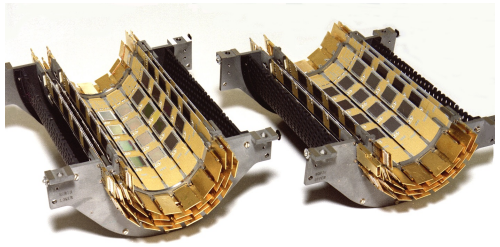
LF Monopix, MuPix,…

Extreme radiation tolerance and timing uniformity, but large capacitance

Small collection electrode

ARCADIA LF, TJ Malta, TJ Monopix, Fastpix, CLICTD, …

- Sub-ns timing
- NIEL >10^{15} 1 MeV n_{eq}/cm^2 and beyond

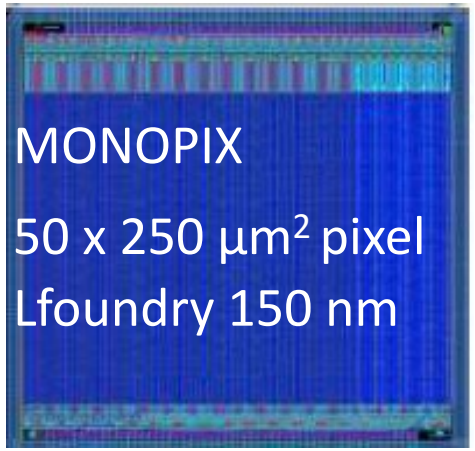


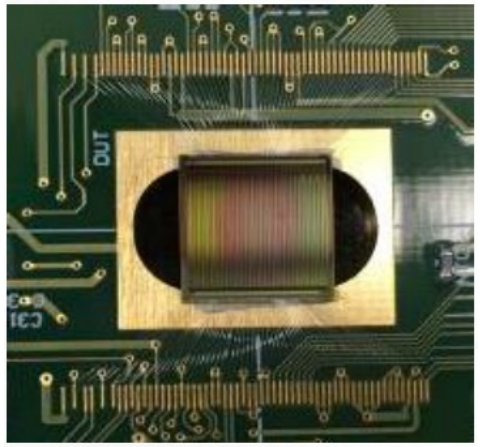
CCDs in SLD detector at SLAC, C. Damerell et al.

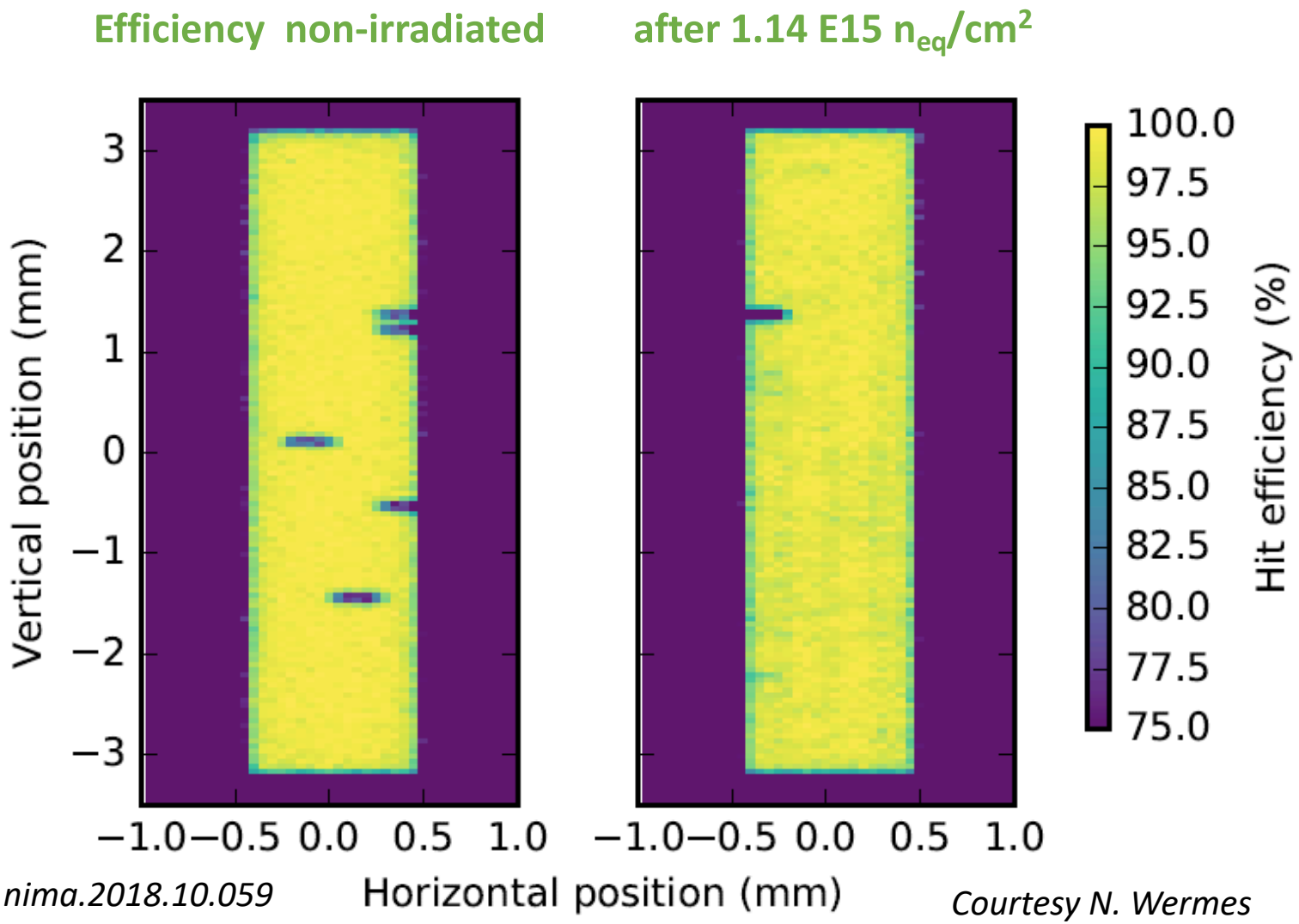
Commercial deep submicron CMOS technology evolved “naturally” towards

- Very high tolerance to ionizing radiation, some caveats, cfr G. Borghello, F. Faccio, requires extensive irradiation campaigns
- Availability of substrates compatible with particle detection
- Imaging technology not absolutely required, but some flexibility/features very beneficial for sensor optimization, both for small and large collection electrode structures.

Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)







T. Hirono et al., https://doi.org/10.1016/j.nima.2018.10.059

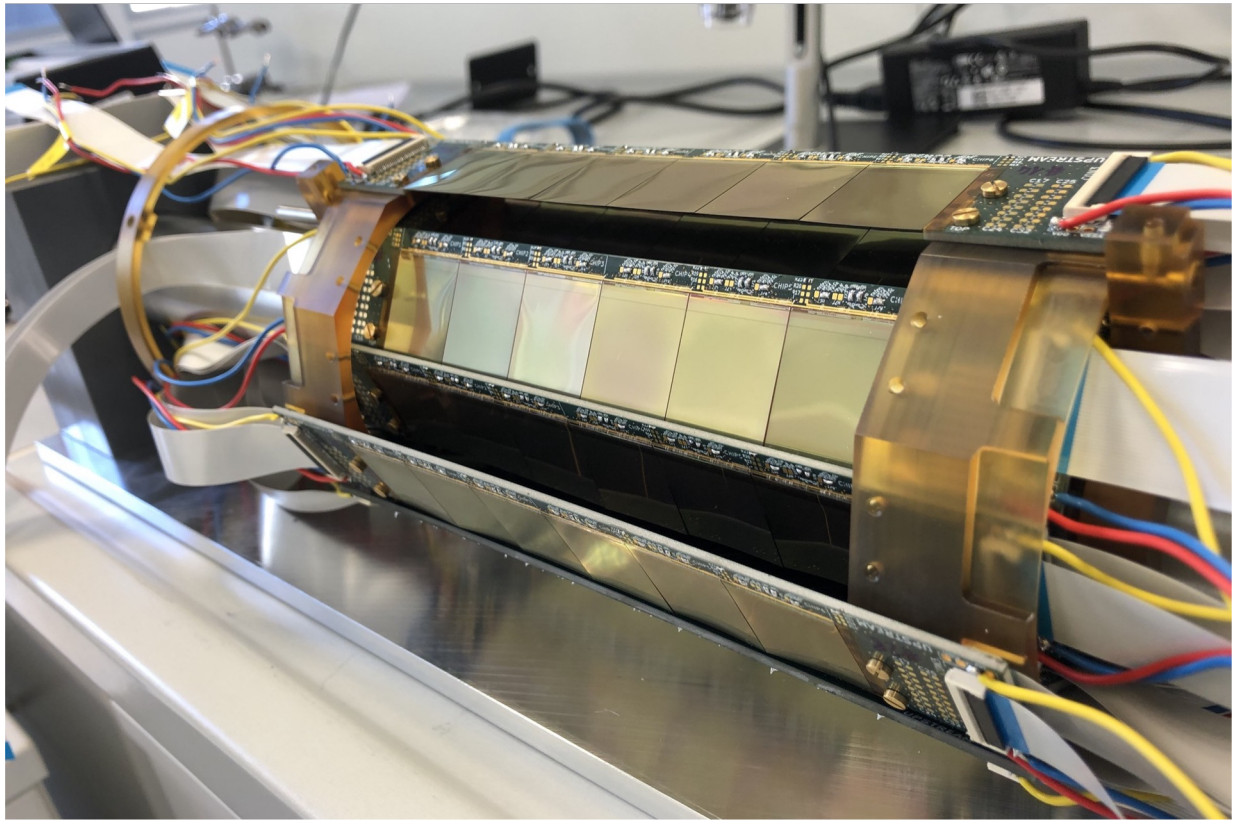
Courtesy N. Wermes

Other developments in same technology:

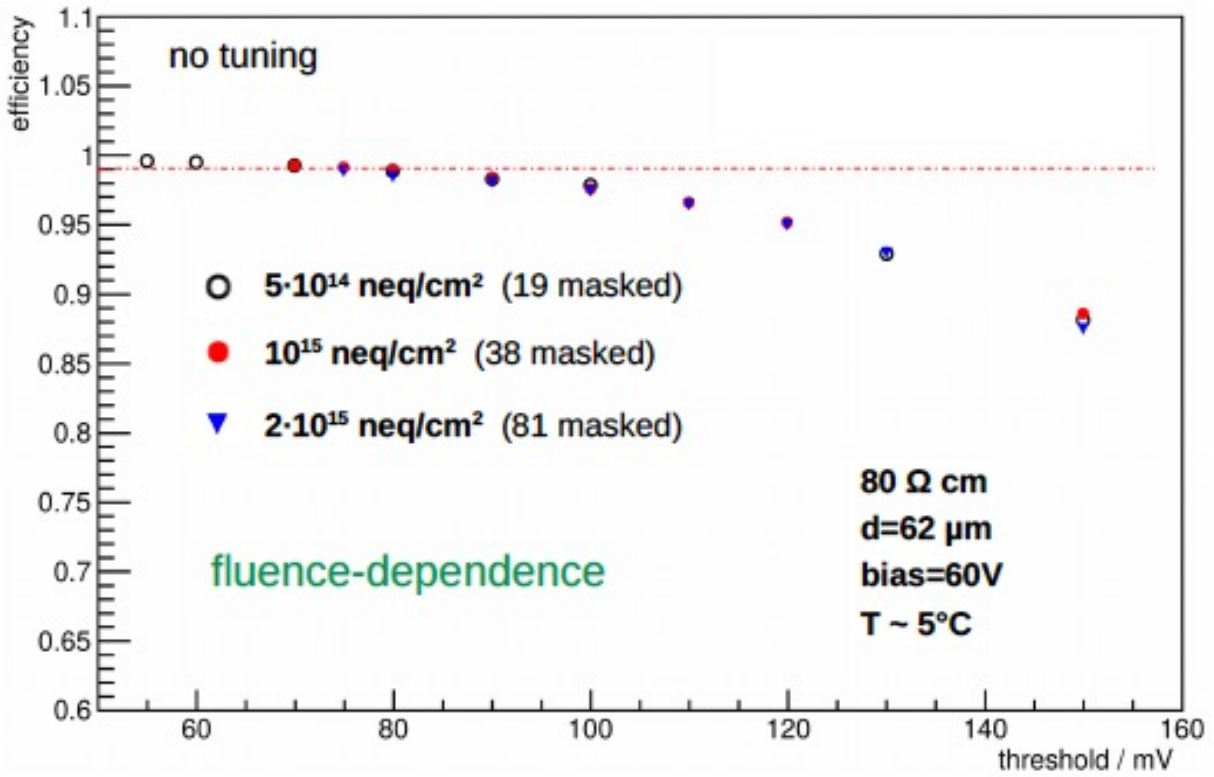
CACTUS Y. Degerli et al. doi:10.1088/1748-0221/15/06/P06011, VCI 2022, NIM A 1039 (2022) 167022

RD-50 E. Vilella et al. doi:10.22323/1.373.0019

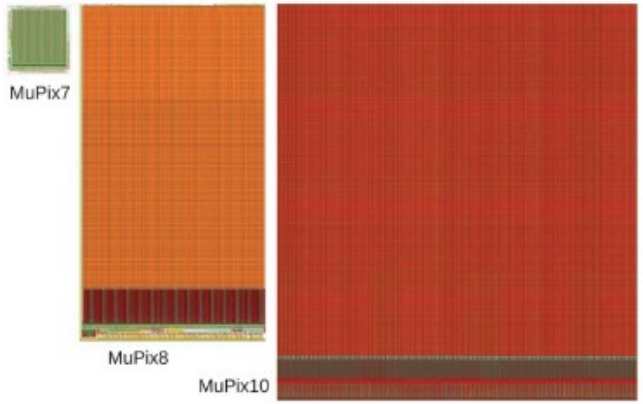
Better sensor radiation tolerance and timing: Large collection electrode: rad hard, but large C (100fF or more)



MuPix vertex detector prototype

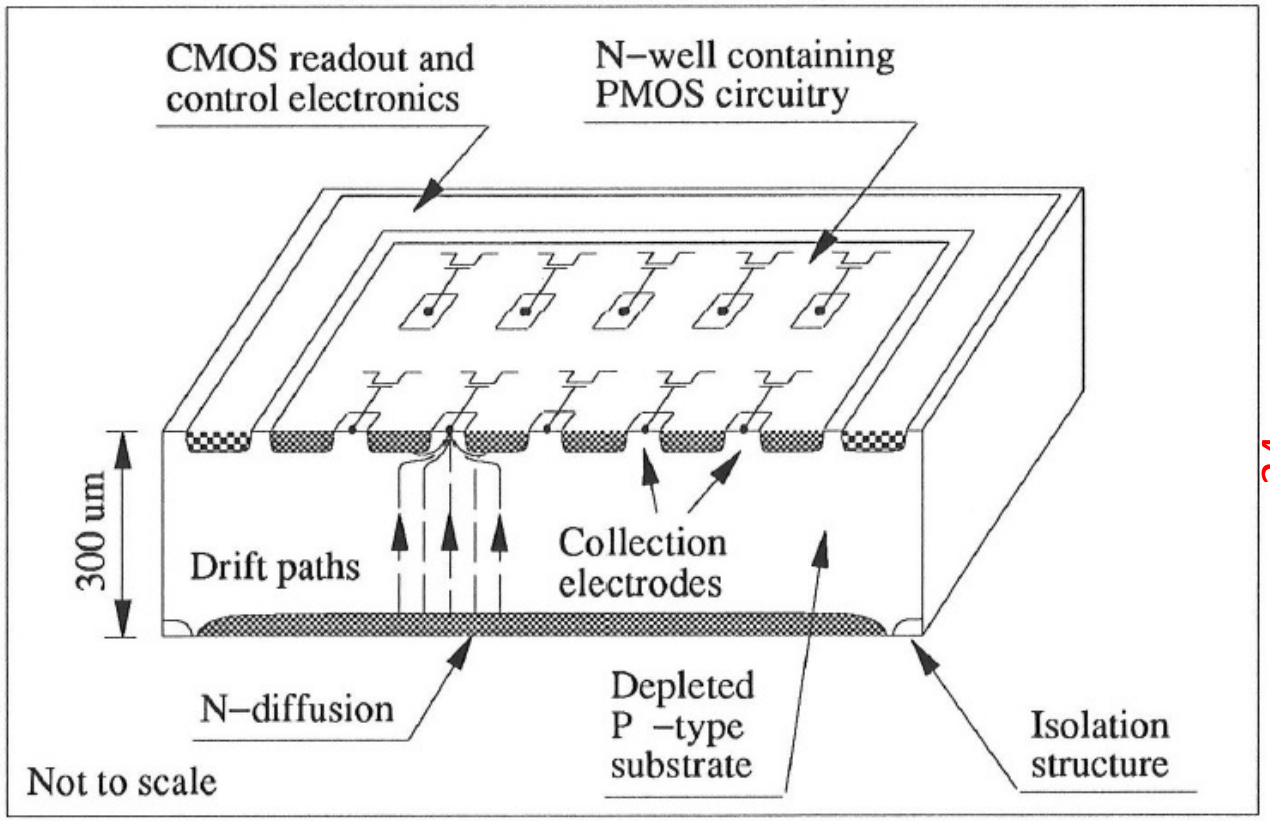


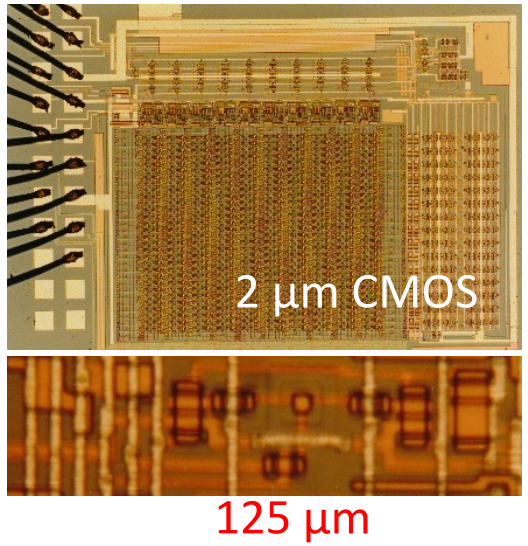
Courtesy I.Peric and A. Schoening

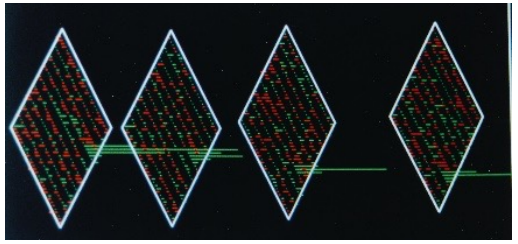


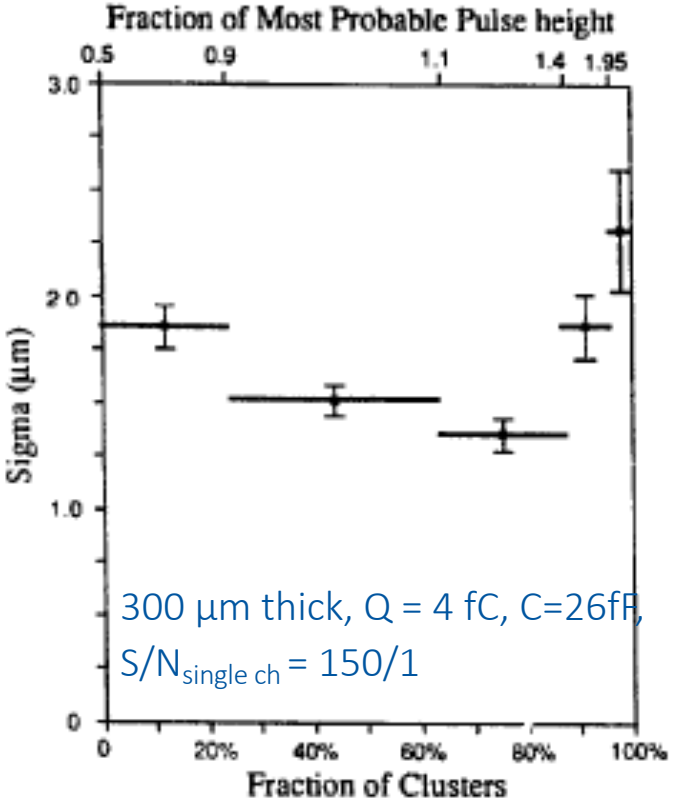
AMS/TSI 180nm, also used for ATLASPIX

Small collection electrodes, this example CMOS but double sided process

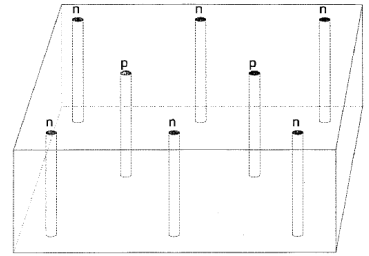








- Separation of junction from collection electrode
- Better than 2 µm position resolution even at large pitch due to good S/N
- Improved back side trench isolation lead to sensors with 3D electrodes (S.Parker, J. Segal)

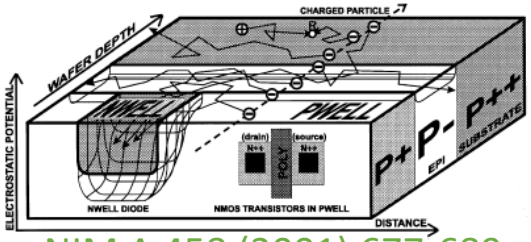


C. Kenney, S. Parker, J. Plummer, J. Segal, W. Snoeys et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

Other examples: ~ 1 µm resolution: SOI sensor, pitch 13.75 µm *M. Battaglia et al. NIM A 654 (2011) 258-265, NIM A 676 (2012) 50-53*

Position resolution: good S/N for interpolation Junction separation and back side processing: see below

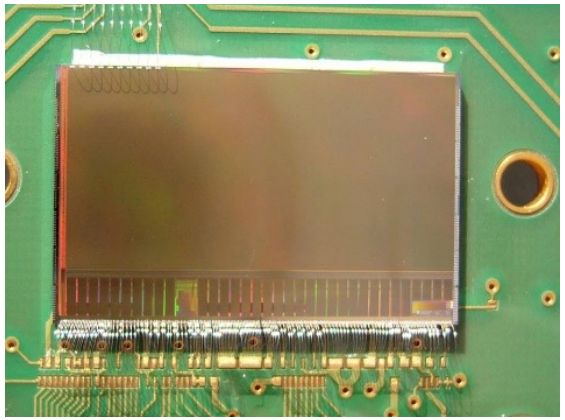
Mimosa series – IPHC Strasbourg – standard CMOS



NIM A 458 (2001) 677-689

A monolithic active pixel sensor for charged particle tracking and imaging using standard VLSI CMOS technology

R. Turchetta[a,*], J.D. Berst[a], B. Casadei[a], G. Claus[a], C. Colledani[a], W. Dulinski[a], Y. Hu[a], D. Husson[a], J.P. Le Normand[a], J.L. Riester[a], G. Deptuch[b,1], U. Goerlach[b], S. Higueret[b], M. Winter[b]



Rolling shutter readout

Mimosa26 – 2008

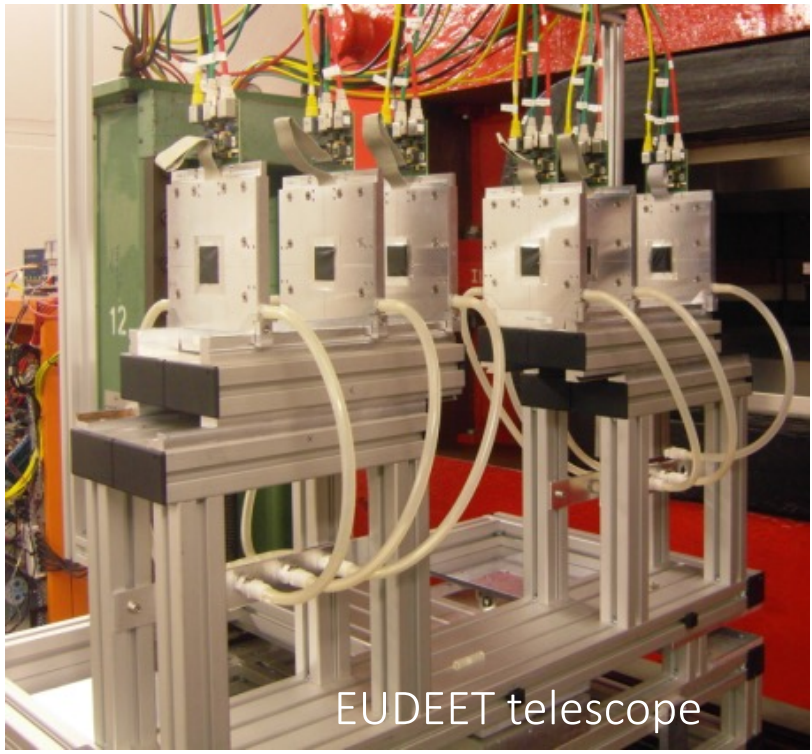
Courtesy of C. Hu IPHC Strasbourg

AMS 0.35 µm

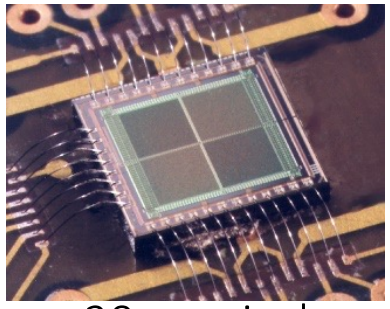
18.4 µm pixel pitch 576x1152 pixels

First MAPS with integrated zero-suppressed readout

First MAPS used for several applications, also for EUDEET telescope



Mimosa1 – 1999
AMS 0.6 µm

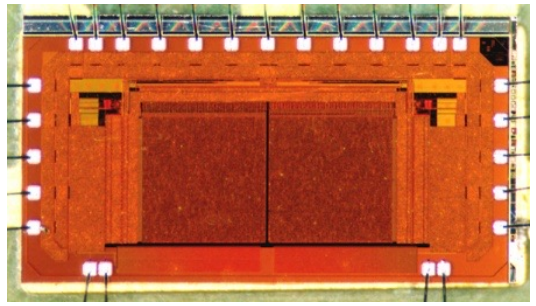


20µm pixel

Mimosa2 – 2000
MIETEC 0.35 µm

20µm pixel

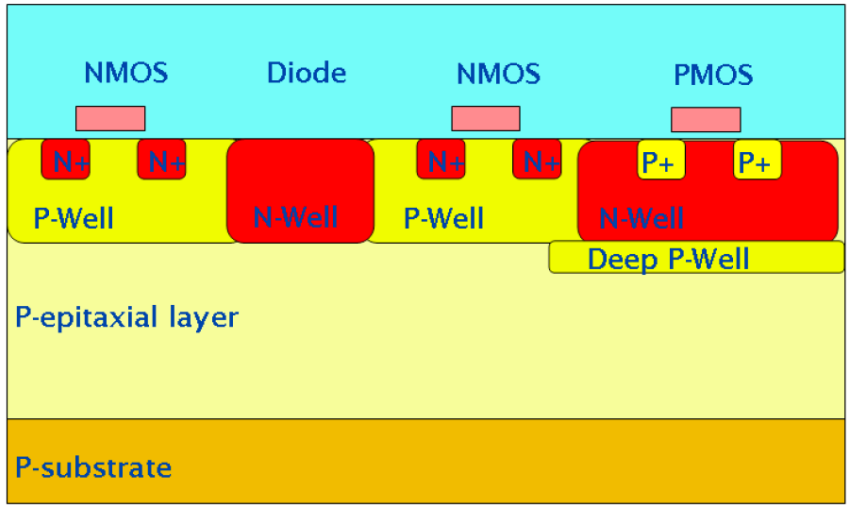
Mimosa3 – 2001
IBM 0.25 µm



8µm pixel

....

The INMAPS process: quadruple well for full CMOS in the pixel



STFC development, in collaboration with TowerJazz A game changer

Additional deep P-well implant allows complex in-pixel CMOS and 100 % fill-factor

New generation of CMOS sensors for scientific applications (TowerJazz CIS 180nm)

Sensors 2008 (8) 5336, DOI:10.3390/s8095336

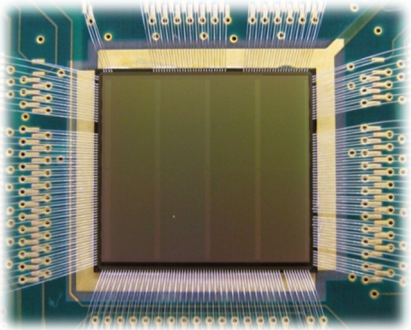
https://iopscience.iop.org/article/10.1088/1748-0221/7/08/C08001/meta

https://iopscience.iop.org/article/10.1088/1748-0221/14/01/C01006/meta

http://pimms.chem.ox.ac.uk/publications.php …

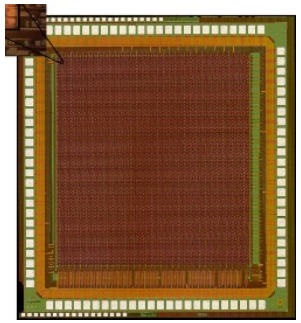
courtesy of N. Guerrini, STFC

TPAC
ILC ECAL (CALICE)



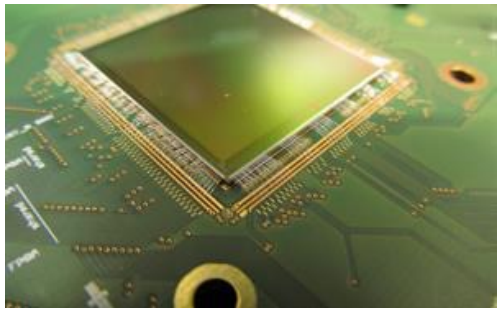
50μm pixel

DECAL
Calorimetry



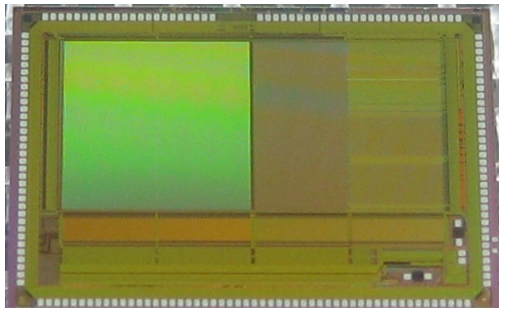
50μm pixel

PIMMS
TOF mass spectroscopy

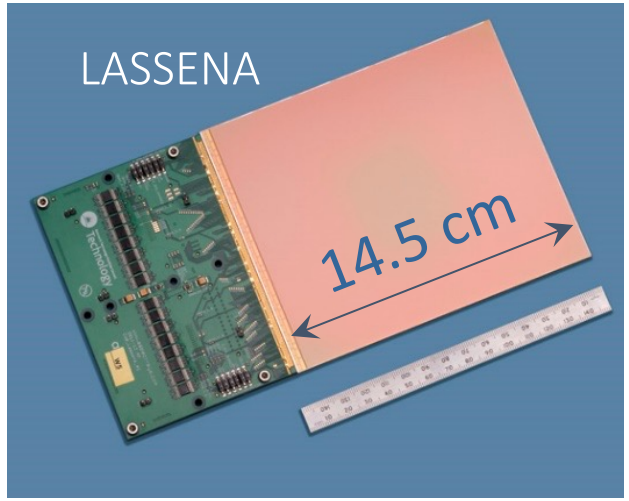


70μm pixel

CHERWELL
Calorimetry/Tracking



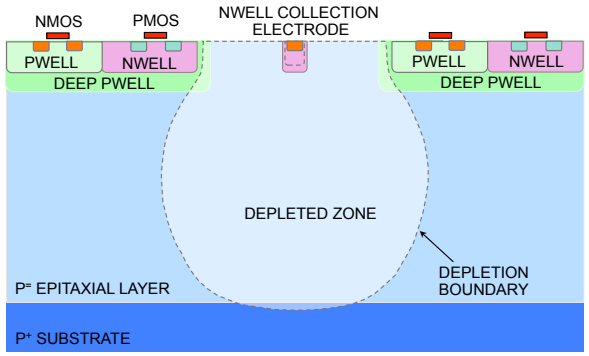
48 μm x 96 μm pixel

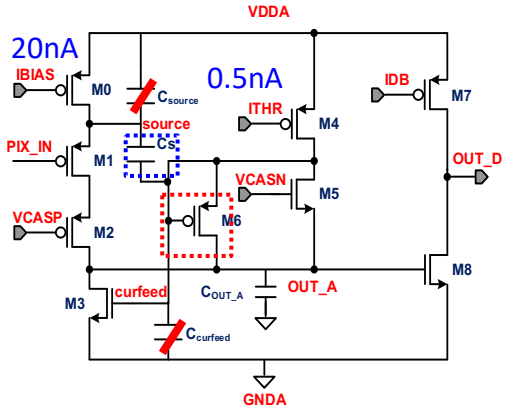


50μm pixel, waferscale

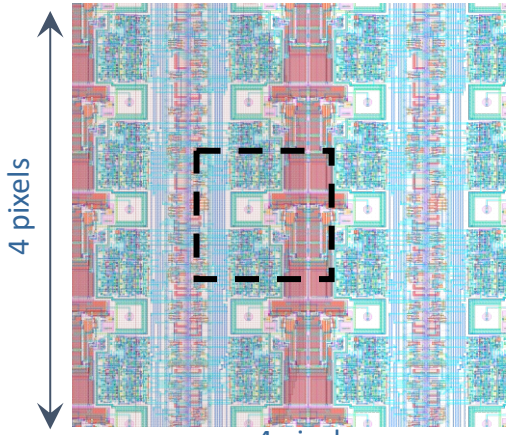
Standard INMAPS process also used for the ALPIDE (27 μm x 29 μm pixel) and MIMOSIS (CBM)

ALPIDE chip in ALICE ITS2

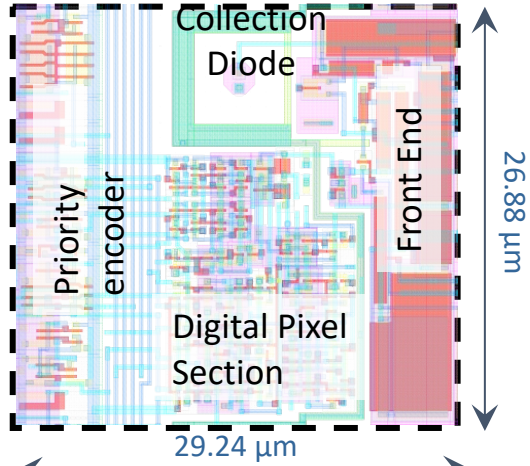




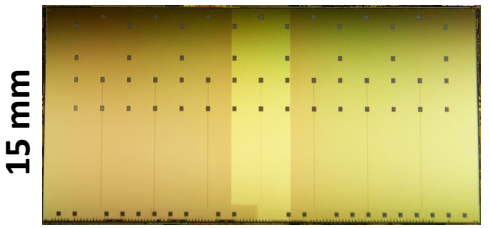
Matrix layout

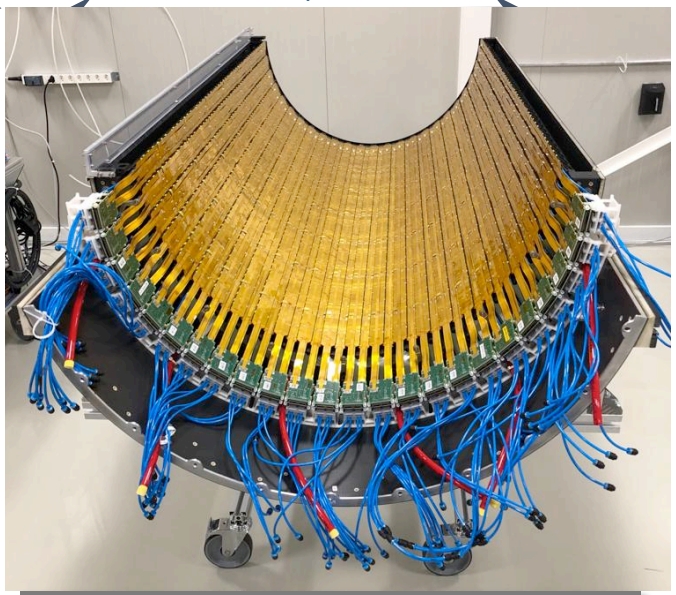


Pixel layout

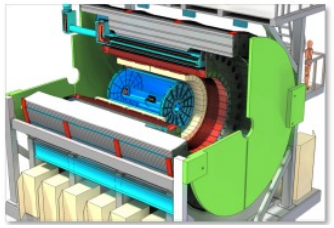


- TJ CMOS 180 nm INMAPS imaging process (TJ) > 1kΩ cm p-type epitaxial layer
- Small 2 µm n-well diode and reverse bias for low capacitance C(sensor+circuit) < 5 fF
- 40 nW continuously active front end D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042
- Q_{in}/C ~ 50 mV, analog power ~ $(Q/C)^{-2}$ NIM A 731 (2013) 125
- Zero-suppressed readout, no hits no digital power G. Aglieri et al. NIM A 845 (2017) 583-587
- Ratio between 15 x 30 mm² and 10 m² in the experiment not ideal -> stitching -> P. Riedler's presentation
- ALPIDE (ALICE Pixel Detector) to be used for several other physics experiments, in space and for medical applications

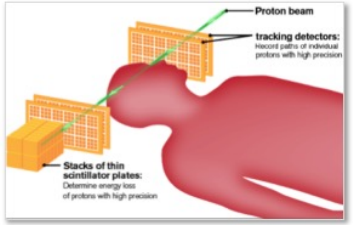




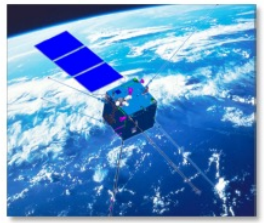
Half outer barrel (layer 6)
~ 2.47 Gpixels covering ~ 2 m² sensitive area



sPHENIX



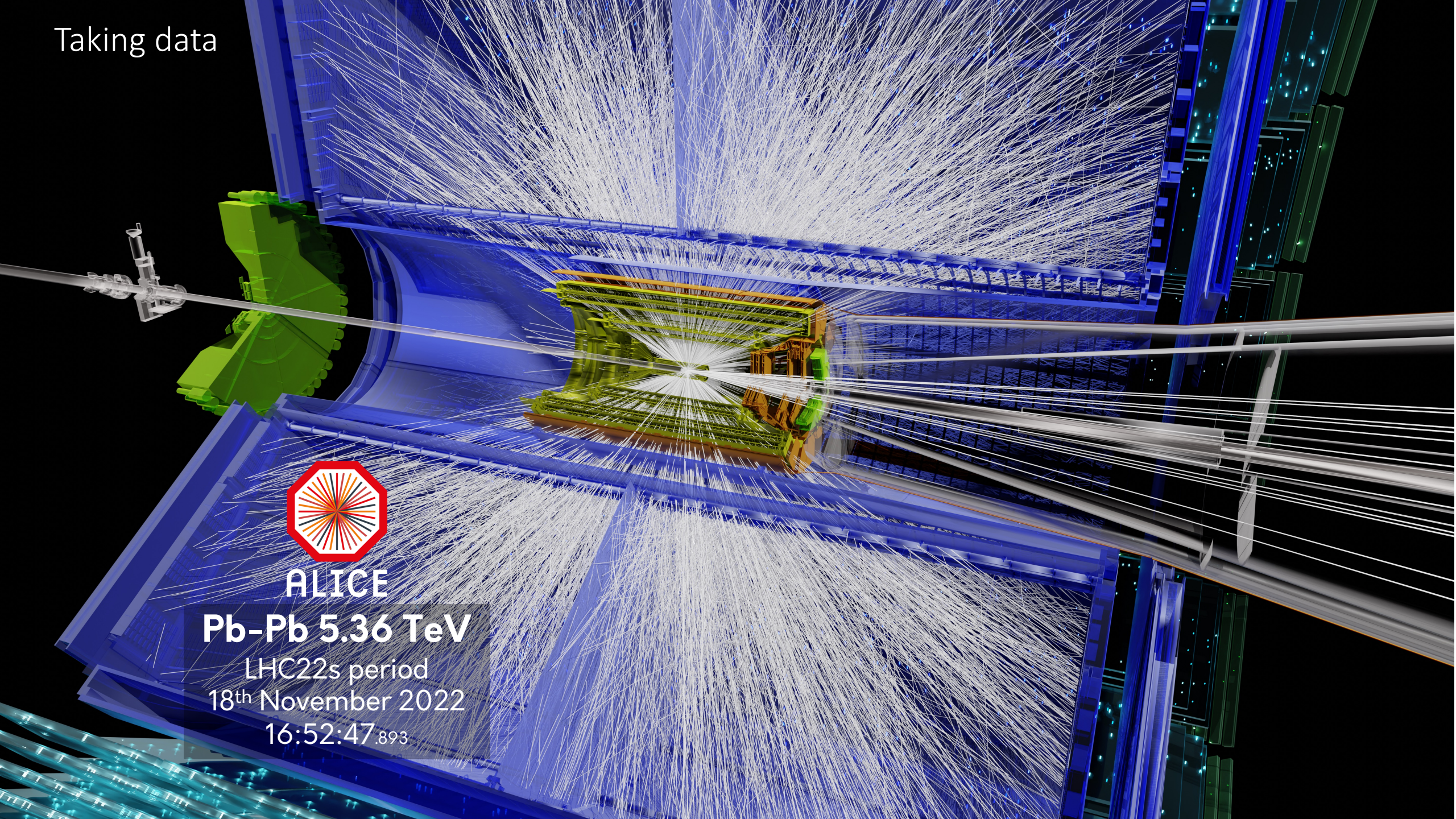
Proton CT (tracking)



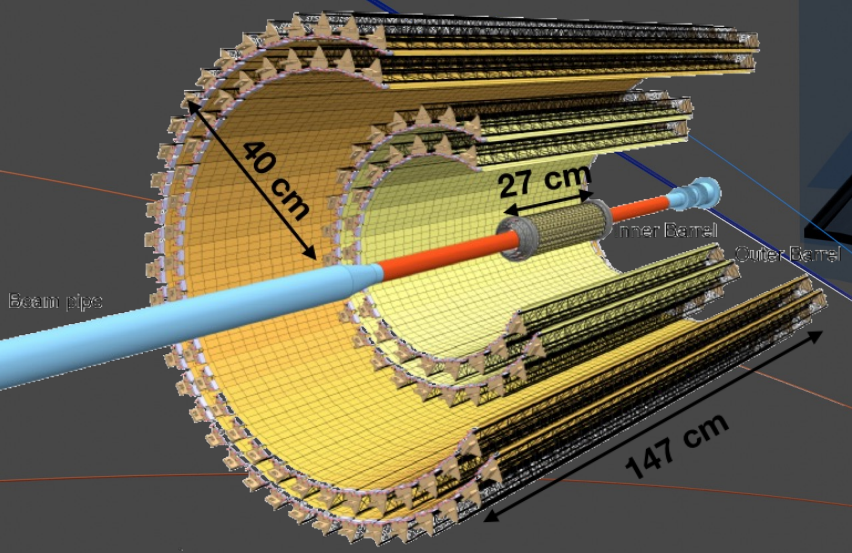
CSES – HEPD2

Design team: G. Aglieri, C. Cavicchioli, Y. Degerli, C. Flouzat, D. Gajanana, C. Gao, F. Guilloux, S. Hristozkov, D. Kim, T. Kugathasan, A. Lattuca, S. Lee, M. Lupi, D. Marras, C.A. Marin Tobon, G. Mazza, H. Mugnier, J. Rousset, G. Usai, A. Dorokhov, H. Pham, P. Yang, W. Snoeys (Institutes: CERN, INFN, CCNU, YONSEI, NIKHEF, IRFU, IPHC) and comparable team for test
1 MPW run and 5 engineering runs 2012-2016, production 2017-2018

Taking data


ALICE
Pb-Pb 5.36 TeV
LHC22s period
18th November 2022
16:52:47.893

ALICE Inner Tracker System 2 (ITS2) taking data



ITS 3 upgrade: replace 3 inner layers with wafer scale stitched sensors[1]

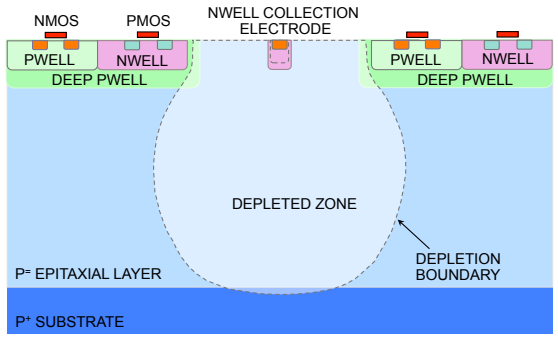
(1) https://indico.cern.ch/event/1071914, *ALICE ITS3 – a next generation vertex detector based on bent, wafer-scale CMOS* sensors, Magnus Mager (CERN)
(1) https://cds.cern.ch/record/2703140/files/LHCC-I-034.pdf - *Letter of Intent for an ALICE ITS Upgrade in LS3*

ALICE

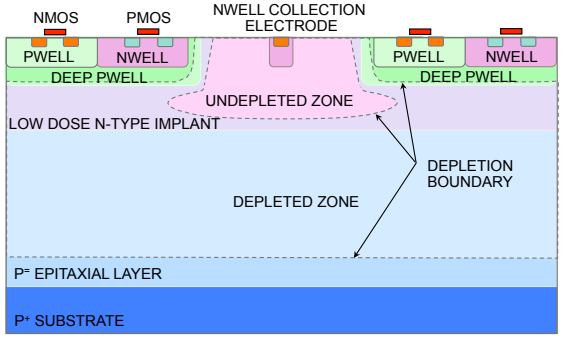
Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors

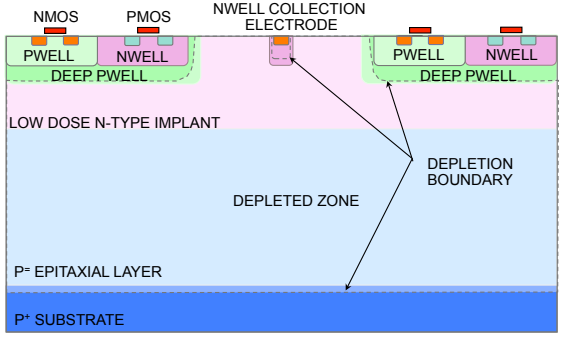
Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…



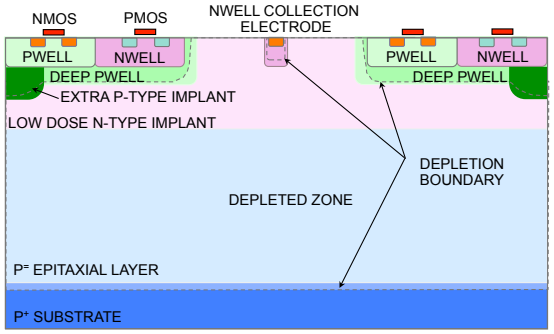
Standard, not fully depleted (ALPIDE)



Not fully depleted at low reverse bias



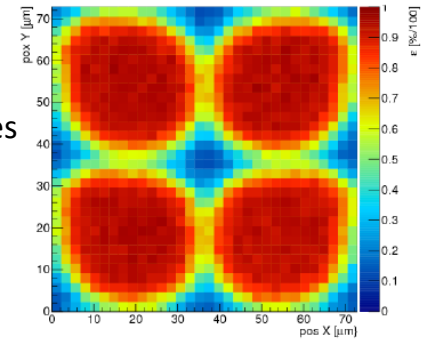
Depletion at higher reverse bias
(MALTA1, MONOPIX)



Further improvements by
influencing the lateral field

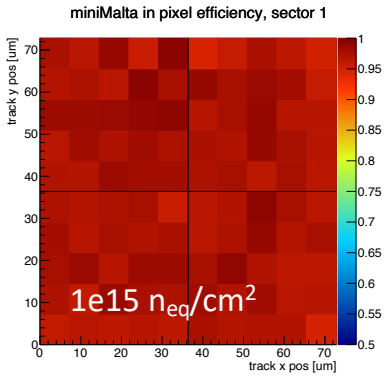
Additional implant for full depletion
=> order of magnitude improvement
Side development of ALICE for ALPIDE
NIMA 871 (2017) pp. 90-96
Triggered development in ATLAS
H. Pernegger et al, 2017 JINST 12 P06008

Efficiency drop at pixel edges
after irradiation
for 36.4 x 36.4 µm^2 pixel
needs improvement
E. Schioppa et al, VCI 2019



3D TCAD simulation
M. Munker et al. PIXEL2018

Significant improvement verified
Also encouraging results with Cz
H. Pernegger et al., Hiroshima 2019
M. Dyndal et al., doi:10.1088/1748-0221/15/02/P02005
M. Van Rijnbach, doi: 10.48550/arXiv.2308.13231



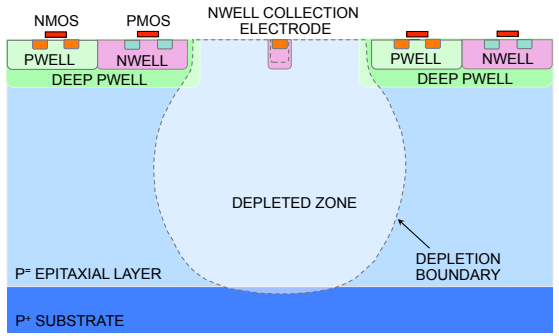
Other similar developments for fast charge collection and depletion:

T.G. Etoh et al., Sensors 17(3) (2017) 483, https://doi.org/10.3390/s17030483
H. Kamehama et al., Sensors 18(1) (2017) 27, https://doi.org/10.3390/s18010027…
L. Pancheri et al., PIXEL 2018, https://doi.org/10.3390/s18010027
C. Kenney et al. NIM A (1994) 258-265, IEEE TNS 41 (6) (1994), IEEE TNS 46 (4) (1999)

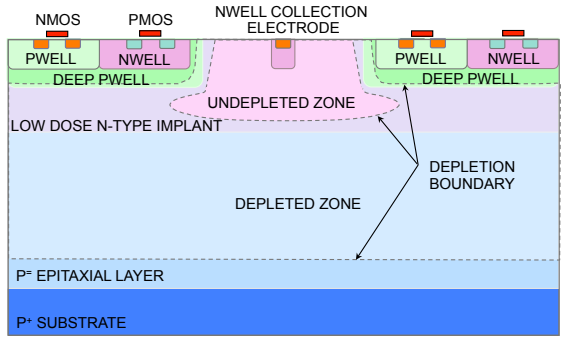
Sensor optimization: Moving the junction away from the collection electrode

for full depletion, better time resolution and radiation hardness… and better efficiency, especially for thin sensors

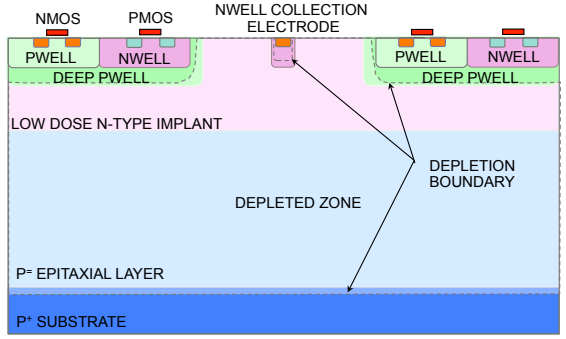
Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…
Also effective doping changes are important.



Standard, not fully depleted (ALPIDE)



Not fully depleted at low reverse bias



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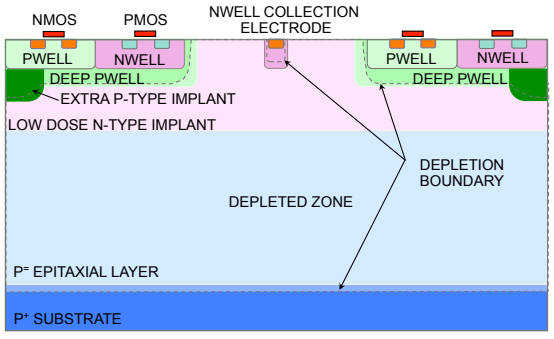
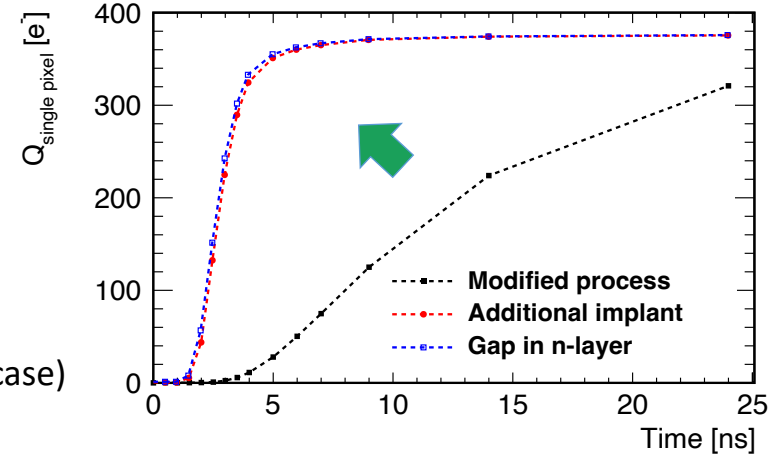


Further improvements by influencing the lateral field

Hit in the pixel corner (= worst case)



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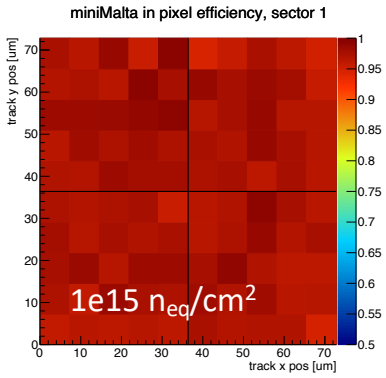

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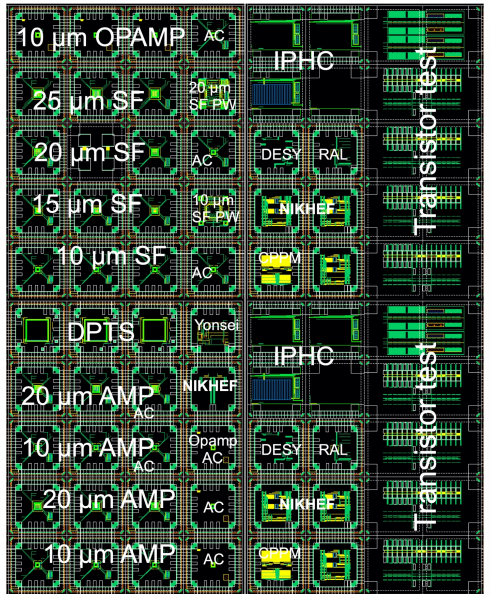
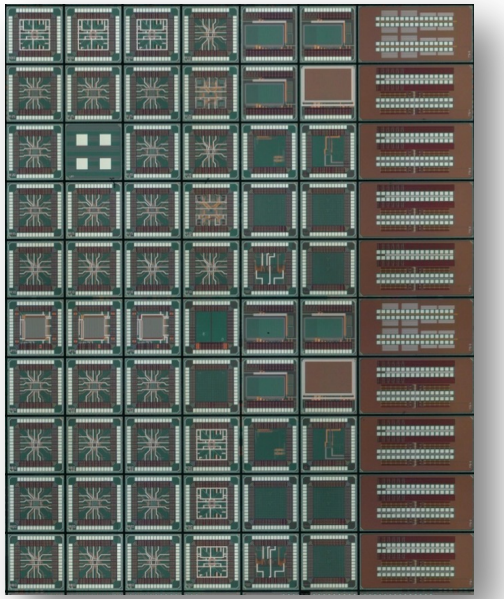
Development of monolithic sensors for high energy physics in TPSCo 65nm ISC technology

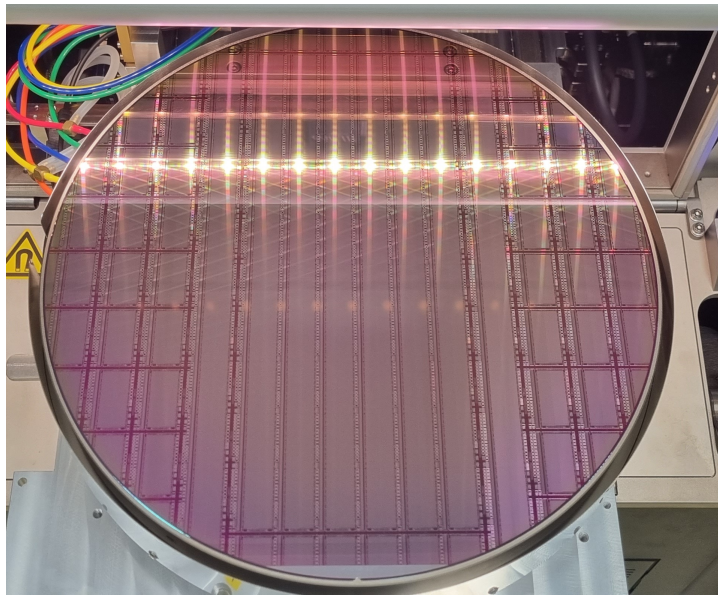
- CERN EP R&D (WP1.2 Monolithic Pixel Detectors) investigating sub 100 nm technologies for HEP
- Many contributors, strong synergy with ALICE ITS3 upgrade, very large measurement team (40-50 people)
- First technology selected TPSC 65 nm ISC, two submissions so far:



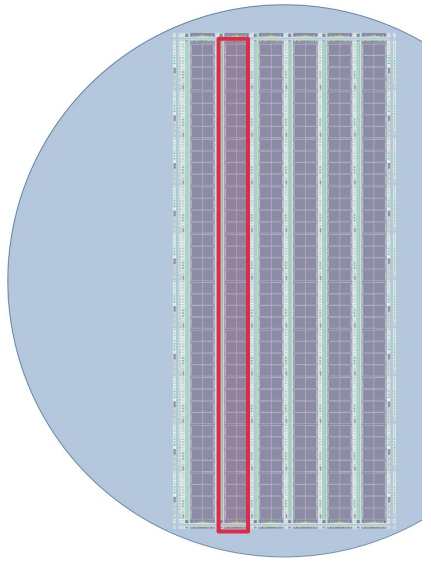


MLR1 (December 2020): 1.5 x 1.5 mm^2 test chips

Learn about the technology, characterize pixels, transistors and building blocks



26cm long single silicon object



ER1 (December 2022): 1.5 x 1.5 mm^2 test chips

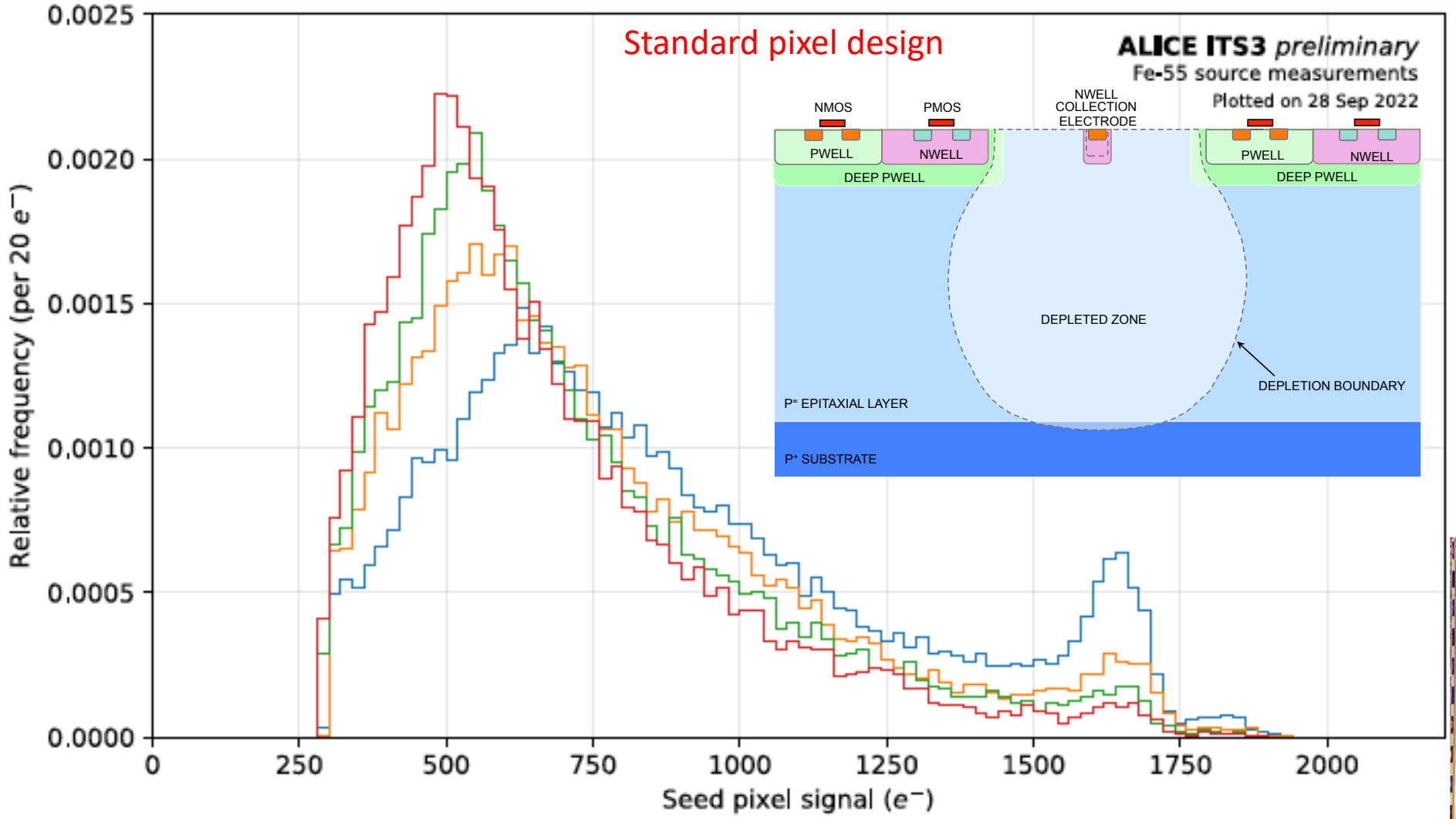
Prove we can design wafer-scale stitched sensors

similar process modifications as in 180 nm, but more needed in 65 nm doi.org/10.22323/1.420.0001

Summary of WP1.2: https://indico.cern.ch/event/1233482/contributions/5264293/attachments/2596131/4482445/EP_RandD_Days_WP1.2_2023_02_20.pdf

Pitch dependence for different variants ^{55}Fe

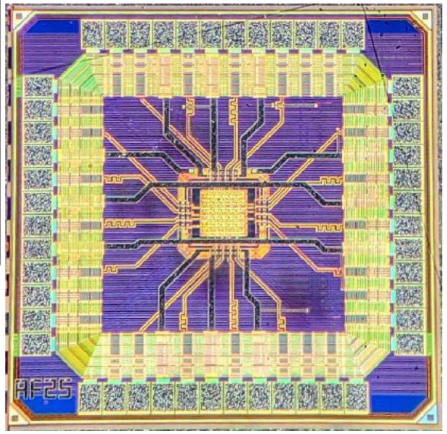
See also: I. Sanna IEEE NSS 2022



APTS SF
type: standard
split: 4
$V_{sub} = V_{pwell} = -1.2$ V
$I_{reset} = 100$ pA
$I_{biasn} = 5$ µA
$I_{biasp} = 0.5$ µA
$I_{bias4} = 150$ µA
$I_{bias3} = 200$ µA
$V_{reset} = 500$ mV

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

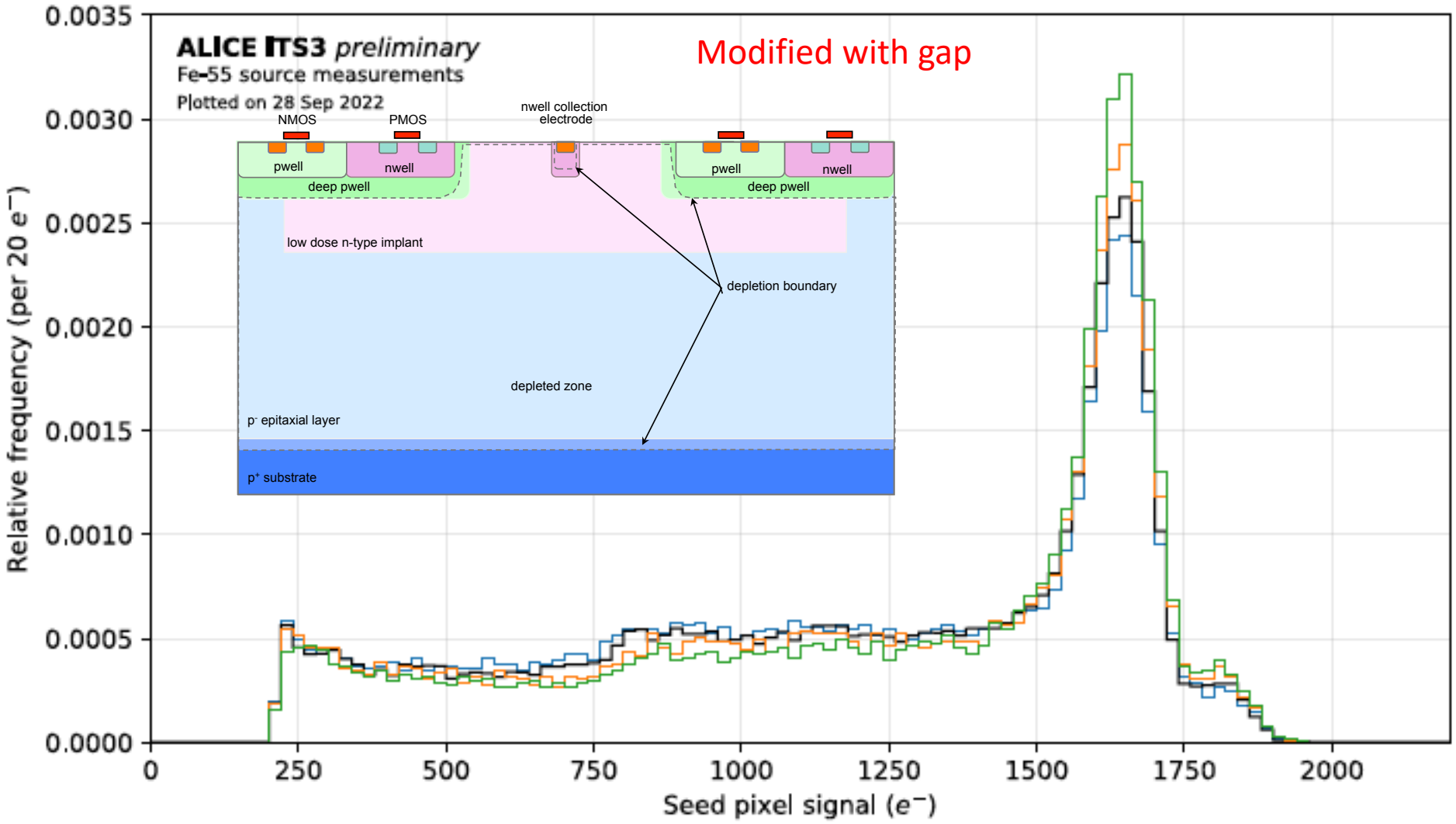
APTS SF



Pitch dependence for different variants ^{55}Fe

See also: I. Sanna IEEE NSS 2022

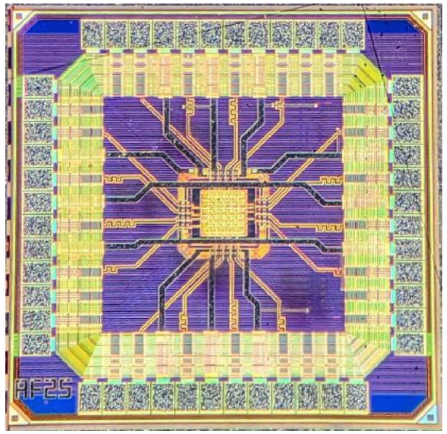
Remarkable result !



APTS SF
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 100\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0.5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$

pitch = 10 µm
pitch = 15 µm
pitch = 20 µm
pitch = 25 µm

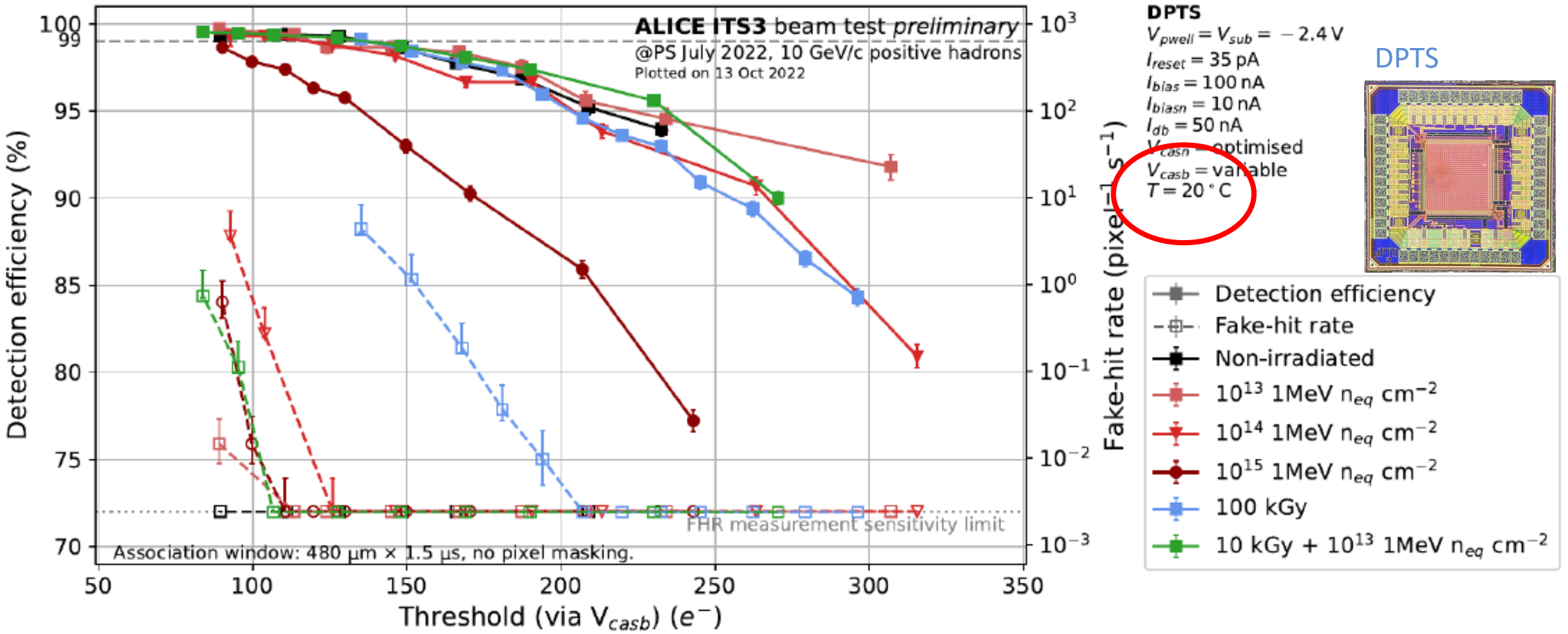
APTS SF



Sensor with gap is only variant conserving efficiency at larger pixel pitches

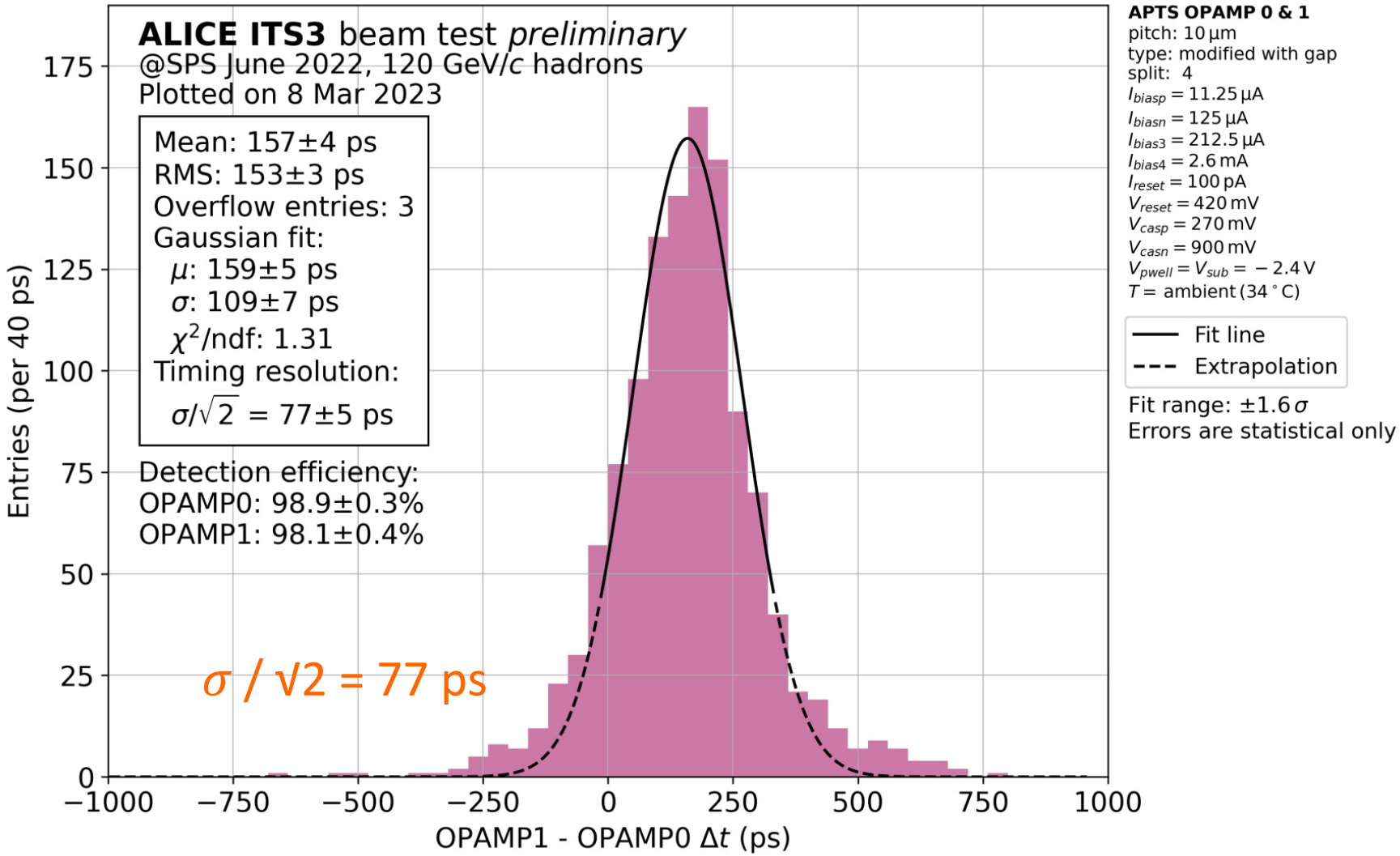
~ 99 % efficiency at 10^{15} n_{eq}/cm^2 … at room temperature

doi: 10.1016/j.nima.2023.168589

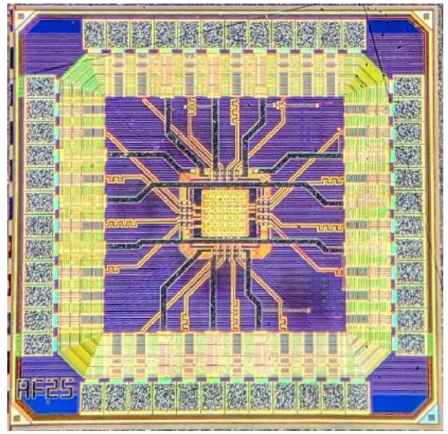


- Fully efficient sensor, analog front end, digital readout chain in 15 x 15 µm² pixel (DPTS) including sensor optimization
- Transistor total ionizing dose tolerance doi: 10.1088/1748-0221/18/02/C02036 and SEU in line with other 65 nm technologies
- KEY ACHIEVEMENT: 65nm ISC qualified for HEP, many features not yet explored (wafer stacking, special imaging devices…)

Sensor timing



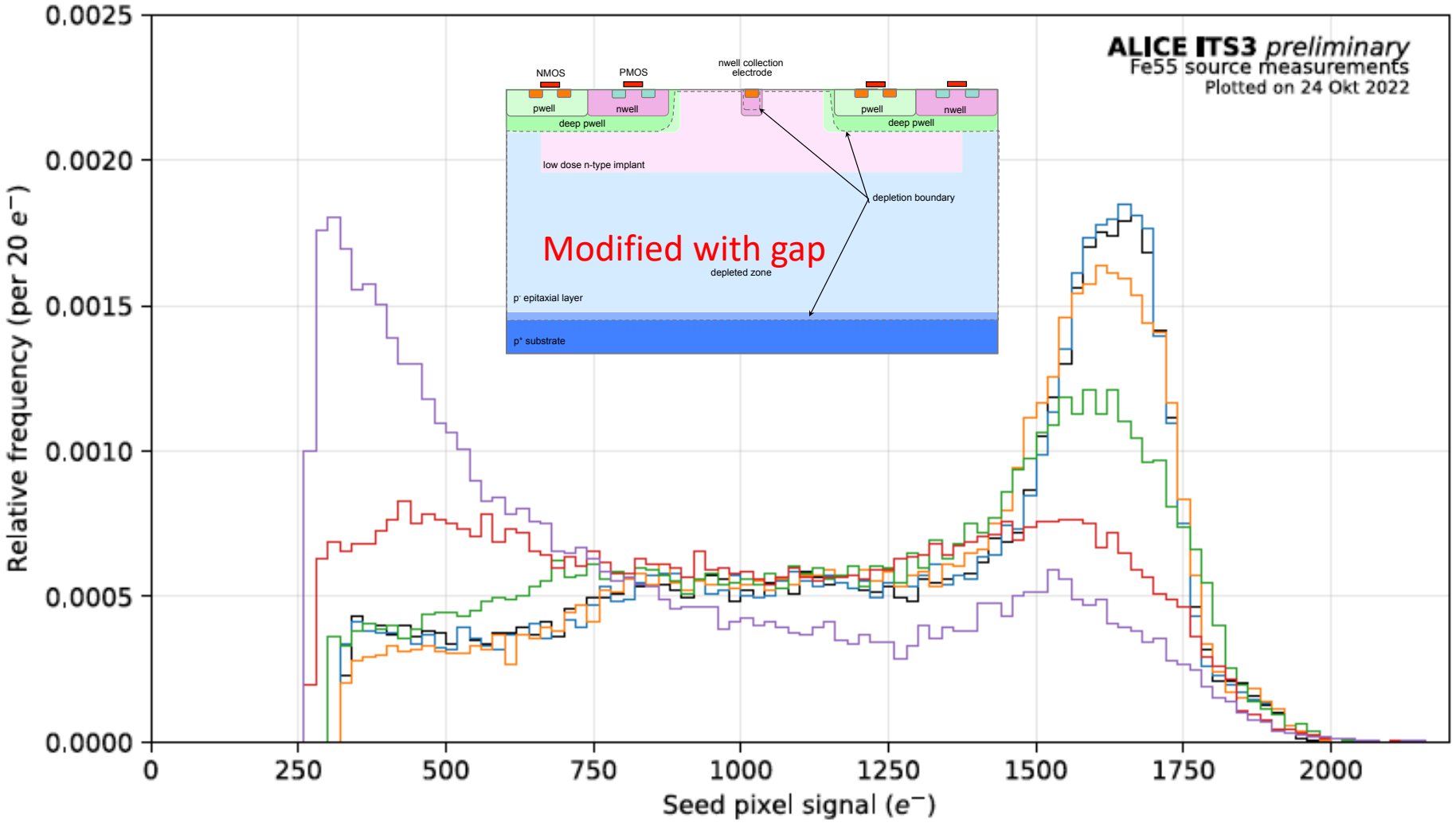
APTS OPAMP



Bong-Hwi, U. Savino et al. ULITIMA 2023

(180nm FASTPIX about 100 ps with time walk and cluster size correction, J. Braach et al. doi:10.48550/arXiv.2306.05938)

Irradiation results: exploring paths to higher fluences (I. Sanna et al.)

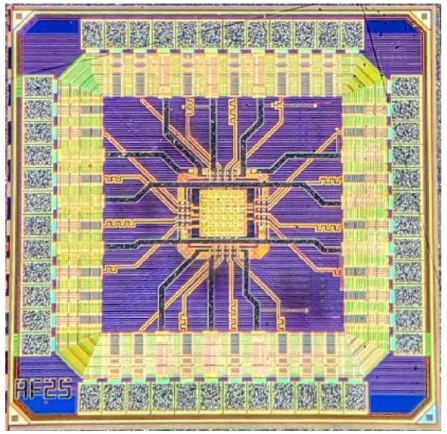


APTS SF
pitch: 15 µm
type: modified with gap
split: 4
$V_{sub} = V_{pwell} = -1.2\,V$
$I_{reset} = 250\,pA$
$I_{biasn} = 5\,\mu A$
$I_{biasp} = 0{,}5\,\mu A$
$I_{bias4} = 150\,\mu A$
$I_{bias3} = 200\,\mu A$
$V_{reset} = 500\,mV$
temperature = 14 °C

Not irradiated
1e13
1e14
1e15
2e15
1e16

DPTS still efficient at RT

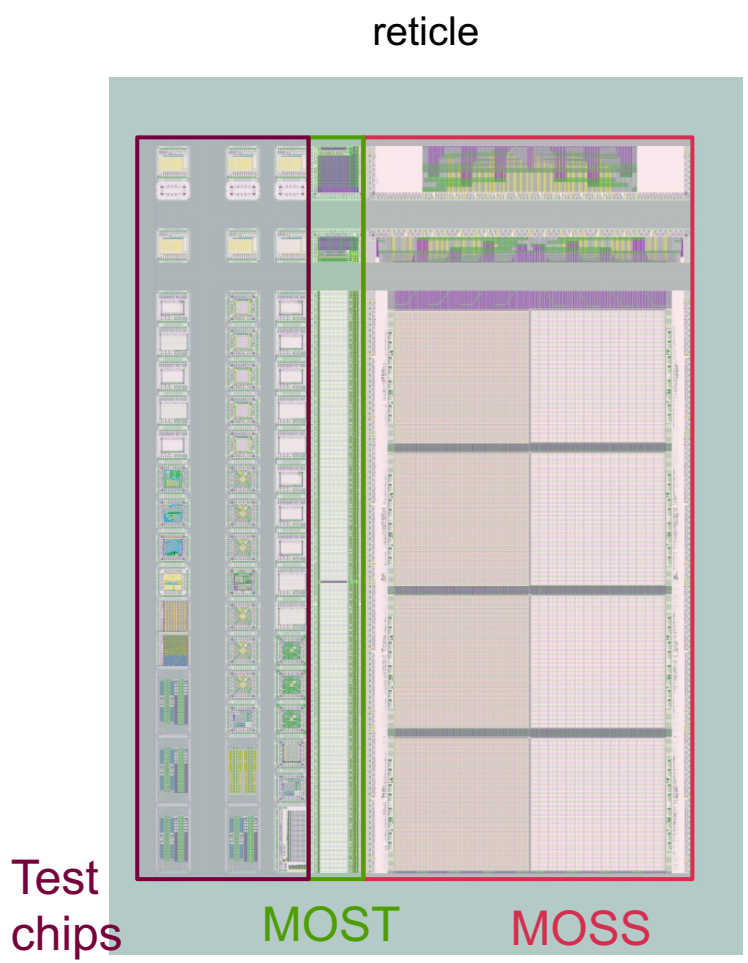
APTS SF

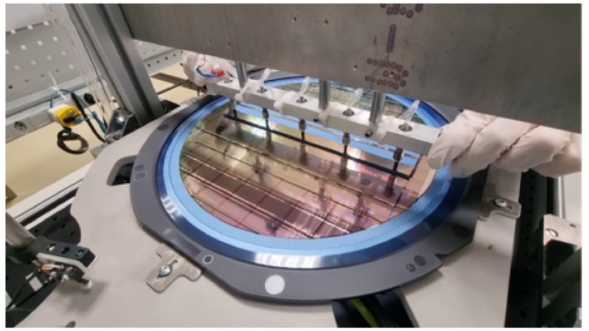


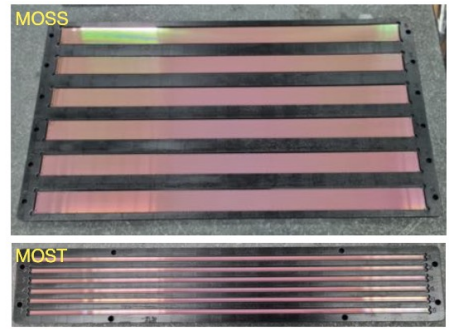
10^{16} n_{eq}/cm^2 will need cooling (needed for 10^{15} for 180 nm)

ER1 submission

- Two stitched sensor chips, 6 of each per wafer, digital on top design
  - MOSS chip (1.4 x 26 cm)
    - Conservative layout (DFM rules), Alpide-like readout scheme and 1/20 power segmentation
  - MOST chip (0.25 x 26 cm)
    - High local density with high granularity of power gating to mitigate faults, async hit driven readout
- 51 chiplets for prototyping blocks and pixel chips
  - PLL, pixel prototypes, fast serial links, SEU test chips, …
  - IPHC, NIKHEF, STFC, DESY, SLAC, INFN, CERN…
- Learn stitching methodology, wafer assembly and automated signoff (P.. Leitao et al.)
- Learn about yield, design for manufacturing (DFM) and defects masking
- Study power schemes, leakage, spread, noise and speed
  - Practical application: Alice ITS3 upgrade (see R. Ricci's presentation)
- Technology and support development
  - New metal stack: new I/Os, PDK, DDK, DRC rules
  - Custom DRC and LVS rule check, custom DFM standard library
  - Legal framework, nda …







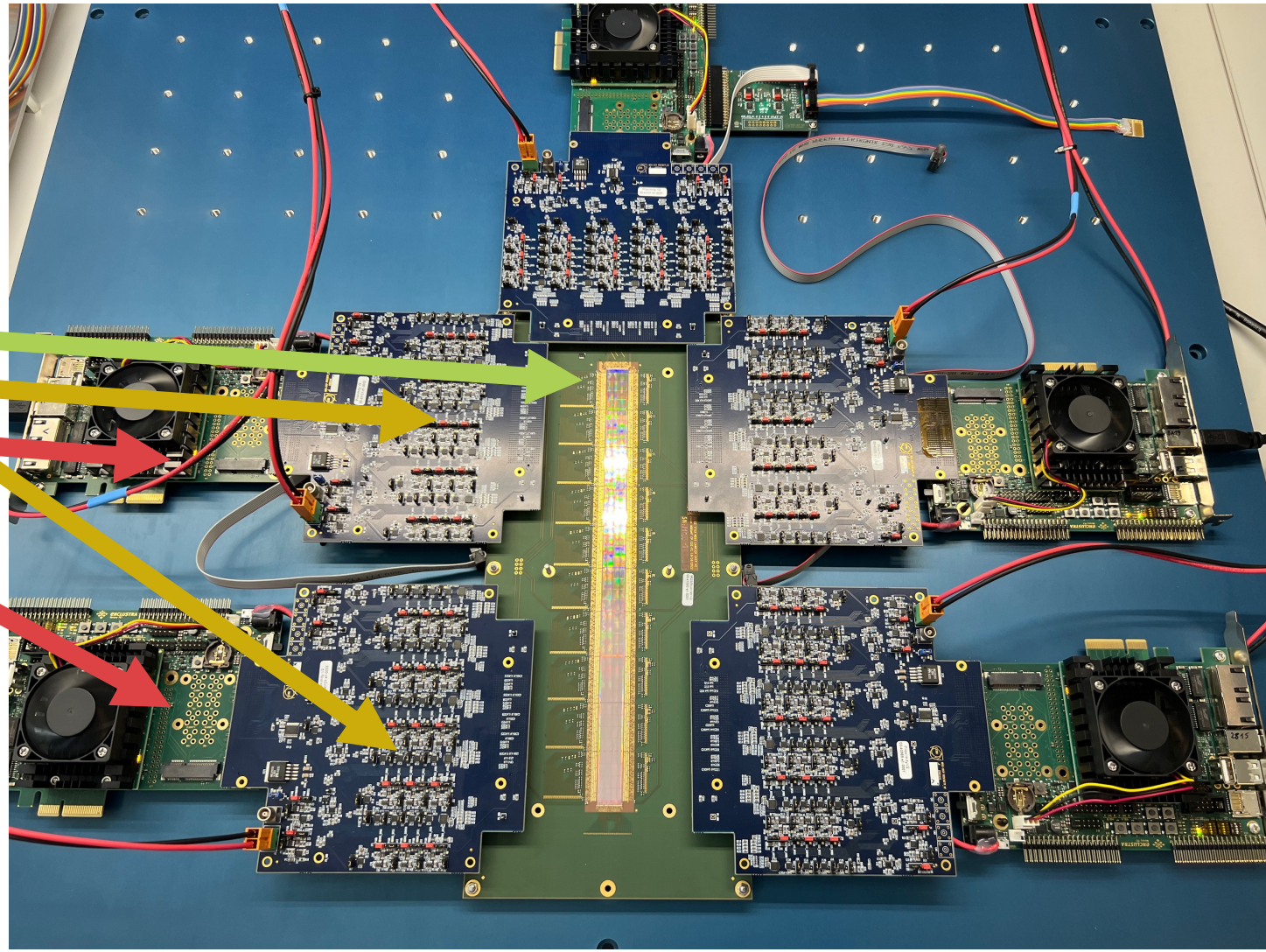
ER1 (MOSS) test system

Gregor Eberwein, Valerio Sarritzu, Antoine Junique, Magnus Mager …

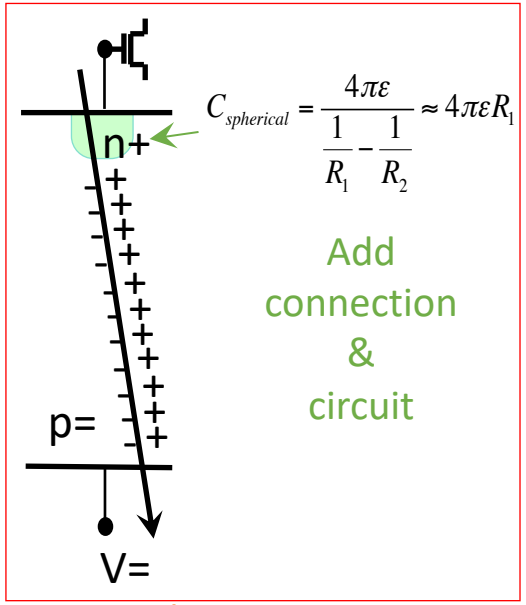
Based on:

- Carrier card (passive)
- 5x proximity card (active, custom made)
- 5x FPGA card (commercial)

- First successful contact in May
- First operation in beam in August
  (D. Colella TIPP2023)



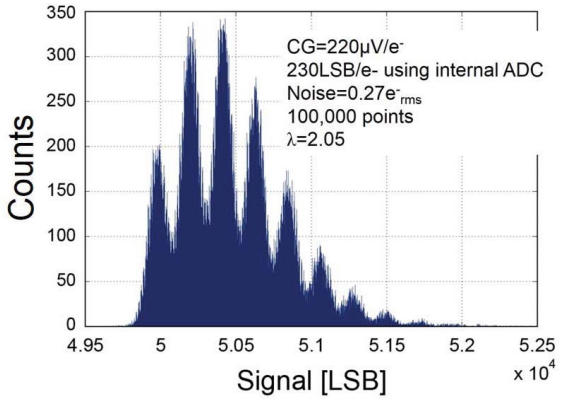
Analog power consumption ~ $(Q/C)^{-2}$ (NIM A 731 (2013) 125)



$$C_{spherical} = \frac{4\pi\varepsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\varepsilon R_1$$

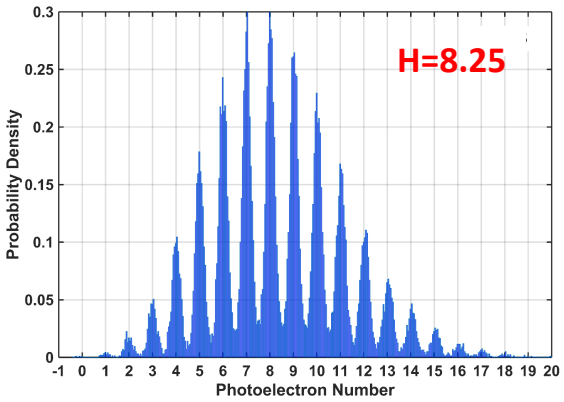
Add connection & circuit

M.W. Seo and S. Kawahito EDL 2015



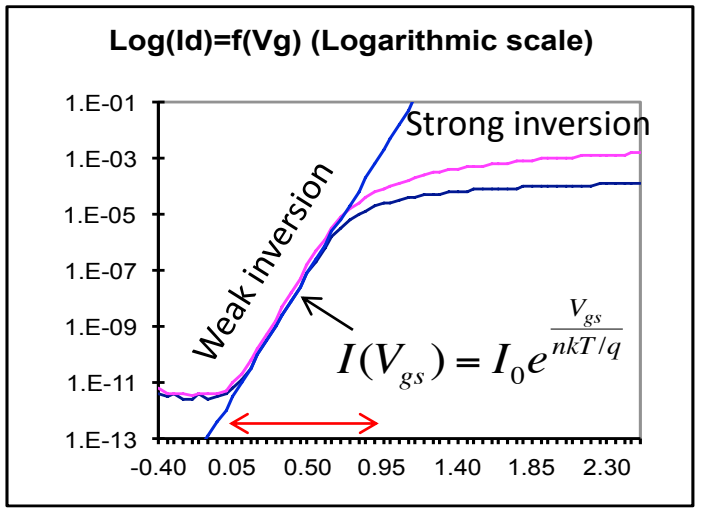
220 μV/e⁻ in 0.11 μm, C=0.73 fF

Ma, Masoodian, Wang, Fossum 2017



350 μV/e⁻ in 45 nm, C=0.46 fF

Non-linearity in weak inversion



- Q/C several 10's of mV in 180 nm
- "Conventional" approach
  - ITS3 estimate ~ 10-15 nW front end for about 10 mW/cm² (ALPIDE in 180nm ~ 40 nW), 5x area reduction
  - Increase power and speed for better timing, μW for < 1 ns F. Piro
- Reduce capacitance further, using:
  - tricks from imaging technology, at present not yet explored
    - now very conventional nwell collection electrode…
    - Still need to extract signal charge from underneath the readout circuit !
  - deeper submicron: 2500 e- to switch inverter in 65 nm, 850 e- in 28 nm, 100 e- in 5 nm A. Marchioro 2019 CERN EP seminar
- Holy Grail: For Q/C > 400 mV, analog power consumption goes to zero. … or gain layers like LGADs see below !

Power consumption and voltage drops

Energy to transfer 1 bit to the periphery (assume line toggle, not step):

1 cm line at 1.8 V = CV^2 = 2 pF x $(1.8\ V)^2$ = **6.5 pJ** Lower VDD in deep submicron = 2 pF x $(1\ V)^2$ = **2 pJ**

Caveat: 2pF/cm can increase depending on line load…

- Digital power density proportional to activity level (hit densities…) and column height
- Voltage drops proportional to the square of the column height and power density
  - For constant power density (eg analog) voltage drops proportional to the square of the column height
  - For digital voltage drops in full CMOS proportional to the third power of the column height
  - Significant challenge for stitched devices.

Off-detector transmission:

ISSCC 2013 / SESSION 2 / ULTRA-HIGH-SPEE

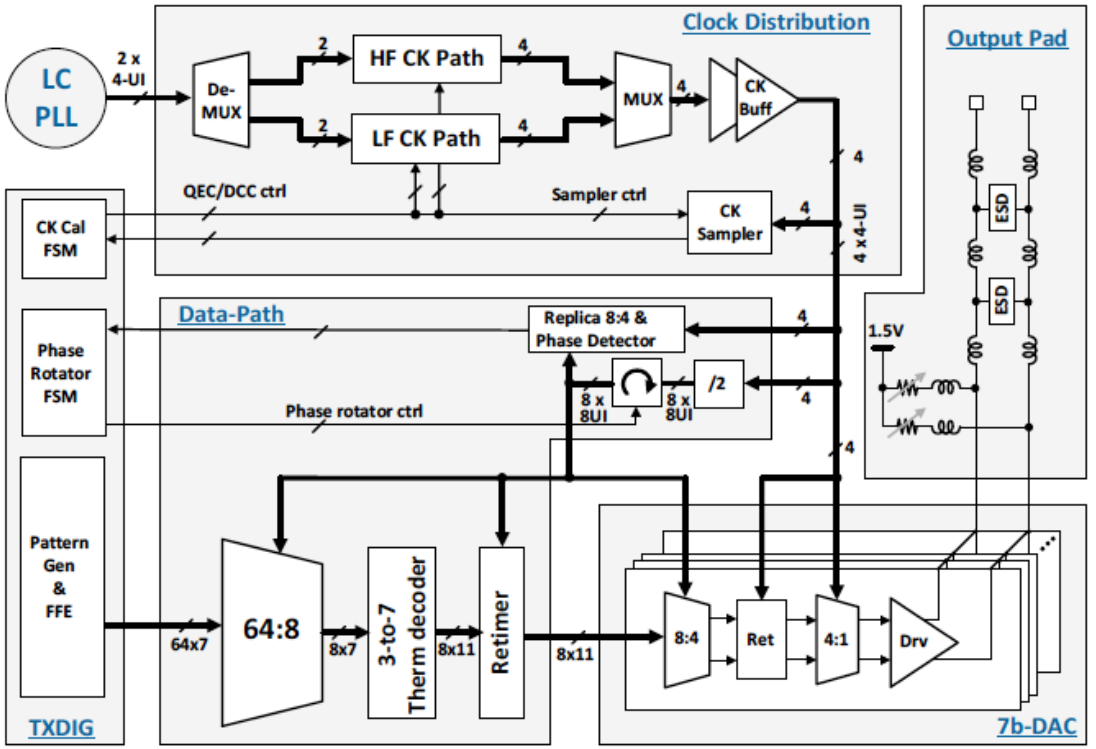
2.6 A 32-to-48Gb/s Serializing Transmitter Using Multiphase Sampling in 65nm CMOS

Amr Amin Hafez, Ming-Shuan Chen, Chih-Kong Ken Yang

University of California, Los Angeles, CA

Block	Power (mW)	Fraction (%)
VCO	26.6	30.2
Divider Chain	18	20.5
Buffer/PFD/CP	2	2.3
Predriver/Driver	26.4	30
Serializer	15	17
Total	88	100

INTEL, ISSCC2021, 224Gbps, PAM-4, 1.7 pJ/bit, 10 nm technology



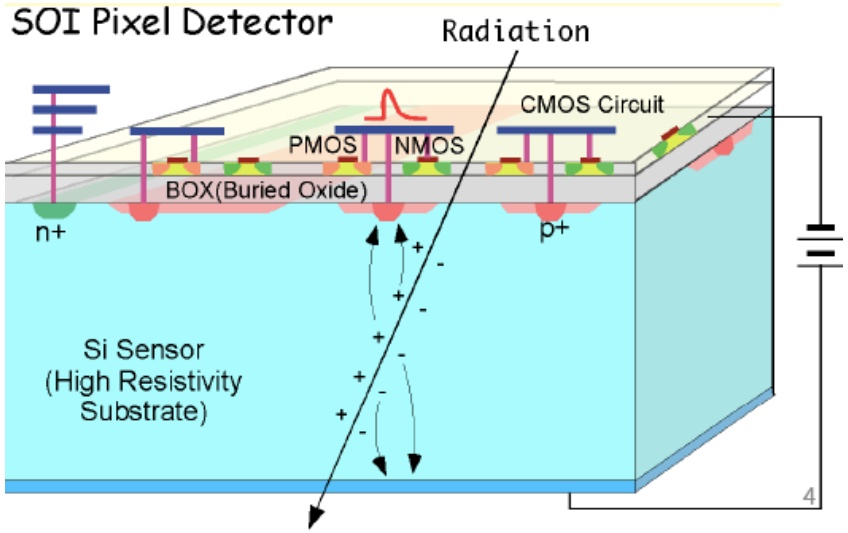
State of the art: a few mW/Gbps, already earlier but also now at much higher bandwidths

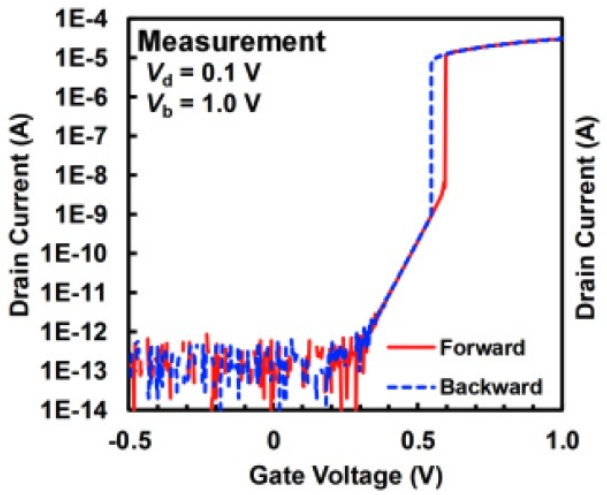
Significant circuit complexity

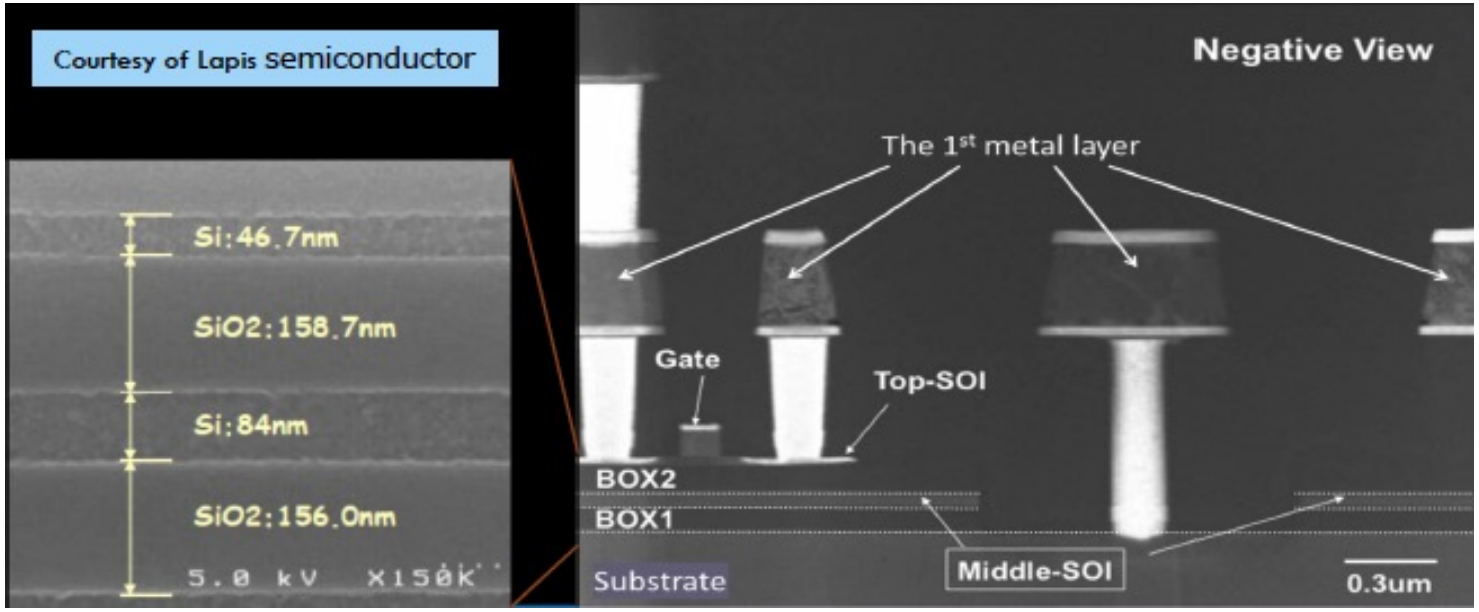
For HEP important penalty for SEU robustness due to triplication/larger devices…

Important: data concentration, physical volume for material budget, and technology

SOI development in Japan





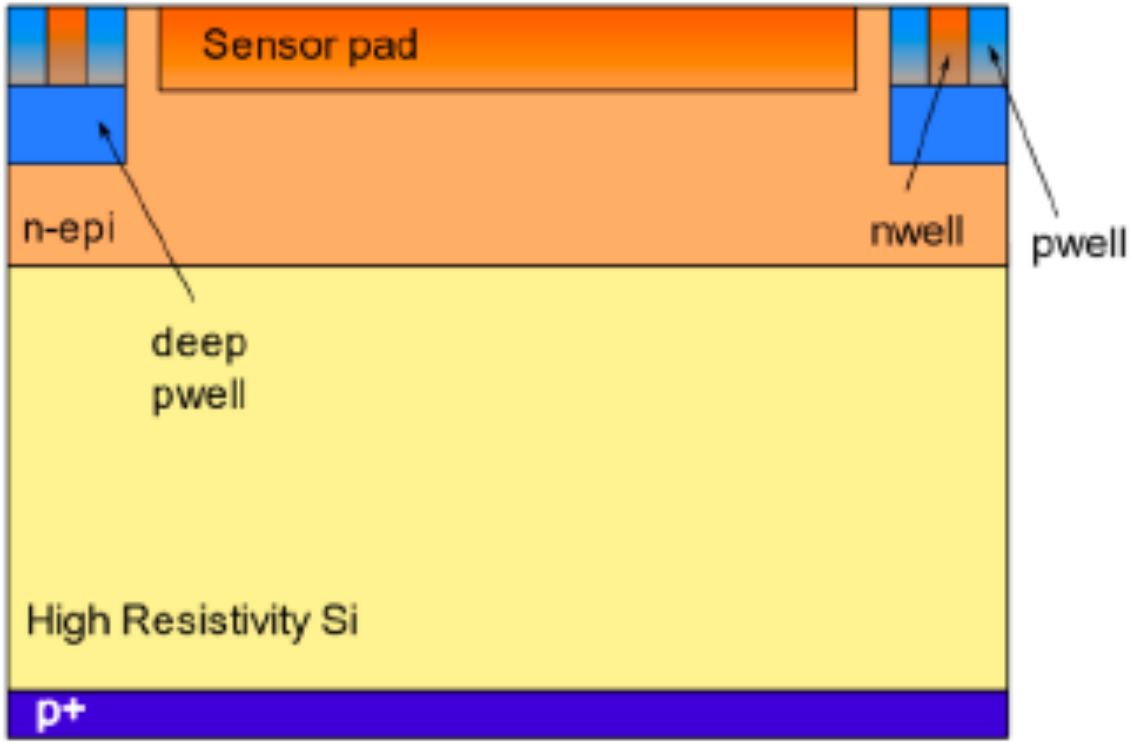


- Fully depleted 0.15 and 0.2 µm SOI technologies, impressive technology development
- Large user base, more than 20 MPWs so far in addition to dedicated runs
- Some freedom on sensor material
- BOX causes reduced radiation tolerance, several measures for improvement, like double box, see bottom left
- Also research on
  - steep slope transistors doi:10.1109/SISPAD.2019.8870519
  - pinned diodes doi:10.3390/s18010027
  - …
- Funded by Japan MEXT KAKENHI Grant-in-Aid for Scientific Research on Innovative Areas 25109001

Courtesy Y. Arai

Technology also used in presentation by Mizuki Uenomachi

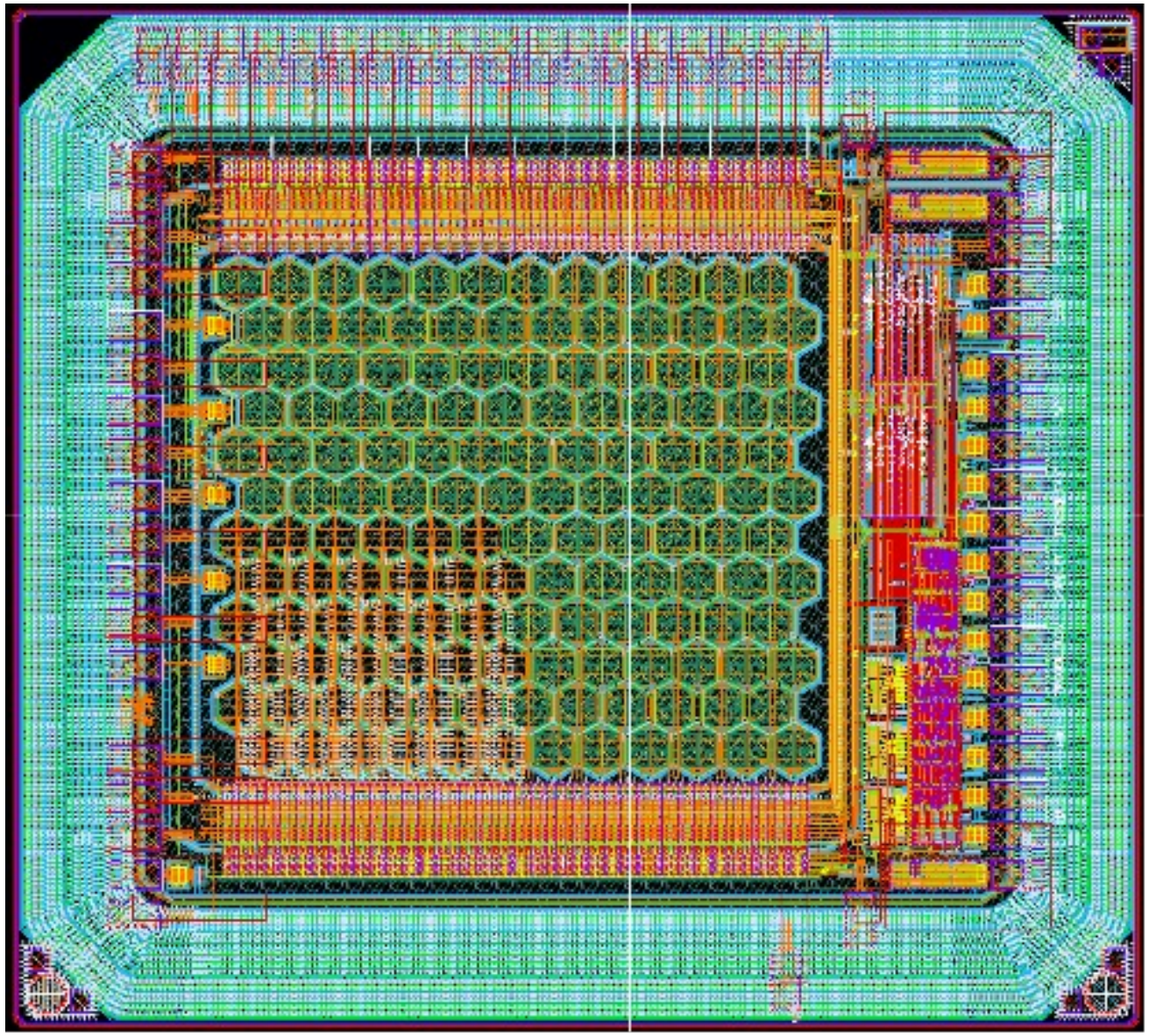
ARCADIA Sensor: LF 110 nm



L. Pancheri 2022
IEEE Transactions on Electron Devices
Vol. 67, No. 6, June 2020

- Depleted MAPS
- Developed in a collaboration between INFN and LFoundry
- 110 nm CMOS, 6 metal layers
- Adding gain layer (gain 10-20) to reach 20 ps resolution
- Prototypes received in January 2023
  - Pixel size: 250 x 100 μm^2
  - Diode area : 220 x 70 μm^2
  - Sensor capacitance: 127 fF
  - Electronics size: 280 x 8 μm^2
  - Active thickness: 50 μm^2
- Test beam campaign ongoing, results in Q4 2023

MONOLITH: SiGe BiCMOS development



- Heterojunction Bipolar Transistor (HBT) gives cut-off frequencies otherwise only reached in more advanced CMOS technologies
- Large collection electrode hexagonal pixel arrangement
- On latest prototype
- Full efficiency
- ~ 20 ps time resolution without gain layer
- Radiation tolerance 10^{16} n_{eq}/cm^2, also for the HBT !
- New prototypes expected this month
- See next presentation and the presention by D. Ferrere

Courtesy G. Iacobucci

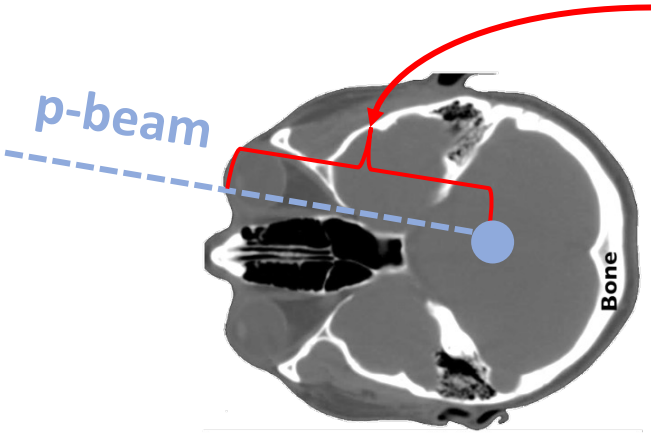
Other developments

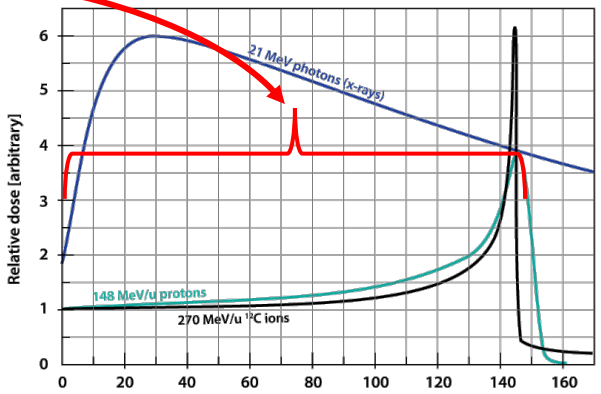
- CITIUS: a 17400 frames/s x-ray imaging detector (stacked, stitched sensor) PIXEL2022
- MIMOSIS for CBM
- MAPS for BELLE2 (see presentation this session)
- …

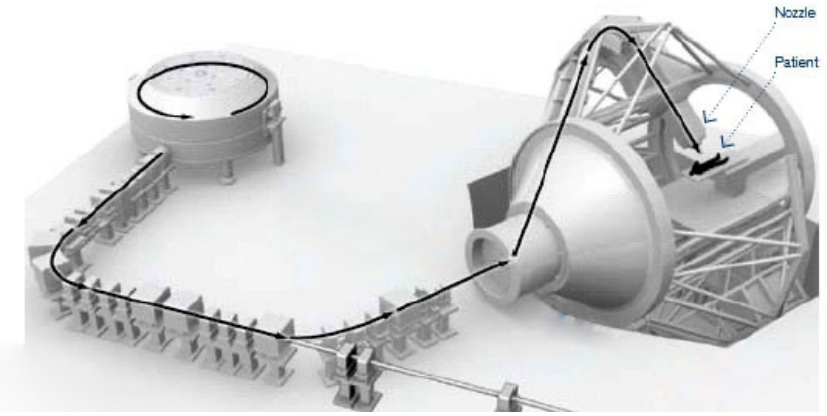
- See also the many presentations at this conference !

From medical imaging to medical tracking: Proton therapy and proton CT

Energy tuning proton beam better than 0.5 % requires proton CT rather than X-ray CT (too poor tissue density resolution)

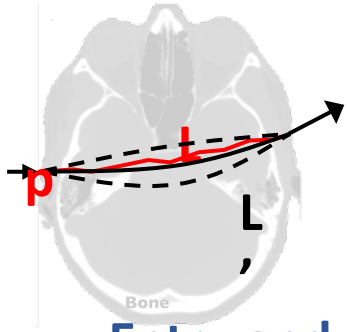






courtesy of P.Giubilato

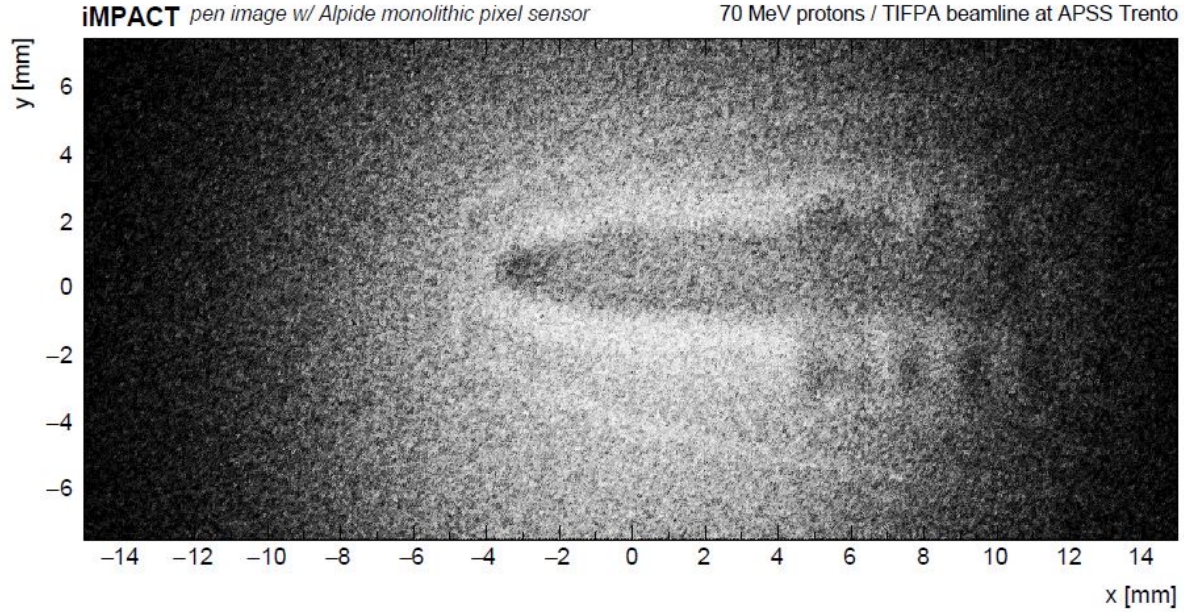
Proton true trajectory



Energy measurement

Entry and exit points + angle

Most Likely Path calculation



Demonstration with ALPIDE chip

Need at least 10^9 proton tracks (entry and exit + most likely path) and 10s of minutes with state of the art detectors.

Gaining time requires detectors which do not yet exist

Concluding remarks

After years of R&D monolithic sensors for HEP move to CMOS MAPS in mainstream CMOS technology, but requirements for HEP are not completely identical to those for visible light imaging, and some technology flexibility can still be beneficial.

Circuit radiation tolerance as for standard CMOS, which naturally evolved towards significant tolerance with some caveats.

Sensor radiation tolerance, precision timing and improved efficiency can be obtained for small collection electrodes from optimization for fast charge collection using techniques based on general principles applicable to different technologies. Large collection electrode sensors provide extreme radiation tolerance and more uniform sensor timing but exhibit large input capacitance.

Decreasing technology feature size or special imaging sensor features or gain layers can increase the voltage excursion on a small collection electrode and ultimately reduce analog front end power to zero and allow precision timing at lower power.

Hybrid vs Monolithic distinction is becoming more vague: 2D integration combined with stitching will bring us a long way, but 3D through wafer-stacking could help for the most challenging applications and is becoming more and more readily available.

Feasibility studies on stitched devices will determine the size of the sensors we will design in the future and whether and to what extent we can profit from unbeatable wafer-scale integration. (production volume is in the outer layers, we need to be prepared for volume test/acceptance/monitoring)

Concluding remarks

A Monolithic Active Pixel Sensor or MAPS is a complex circuit with extra constraints: sensor bias, coupling into the sensor, …

- The increasing complexity of the sensors and the chips we design require evolution towards digital-on-top design techniques with increasing verification effort (cfr F. Faccio and A. Rivetti's presentations).
- Need team of expert chip designers, complemented with device/TCAD/Monte Carlo experts for sensor optimization and simulation. It takes years to train people for this activity and our community, also at CERN, struggles to preserve critical mass and know-how for this activity.
- New developments take very significant design and measurement effort (eg 65 nm qualification) requiring federation/concentration of resources in the HEP community.

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc, illustrated by the interest in chips like ALPIDE and successful developments like Medipix/Timepix (See M. Campbell's presentation this morning) but also by many talks at this conference !

MAPS are one of the few areas where production volume even within HEP would not be negligible, but where our community can have an impact not only on the quality of its own measurements, but also on society in general, and which we should try to exploit to enable access to the most advanced technologies.

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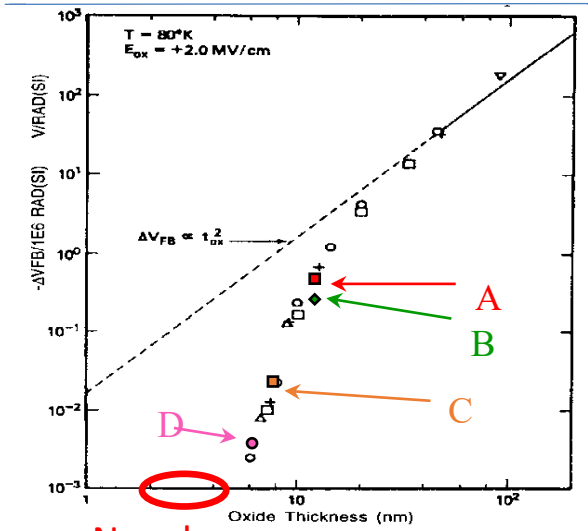
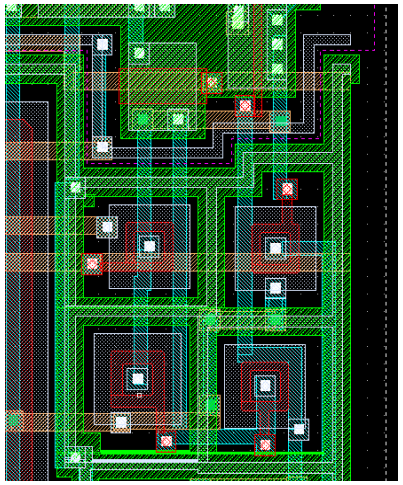
THANK YOU !

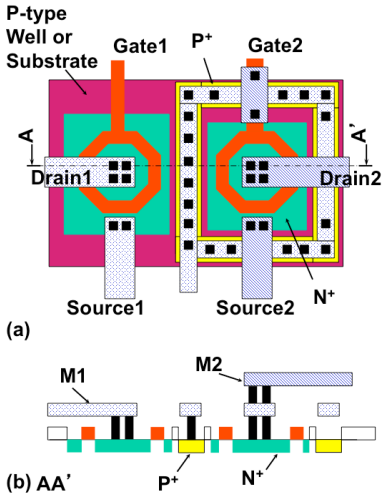
Circuit radiation tolerance: like standard CMOS



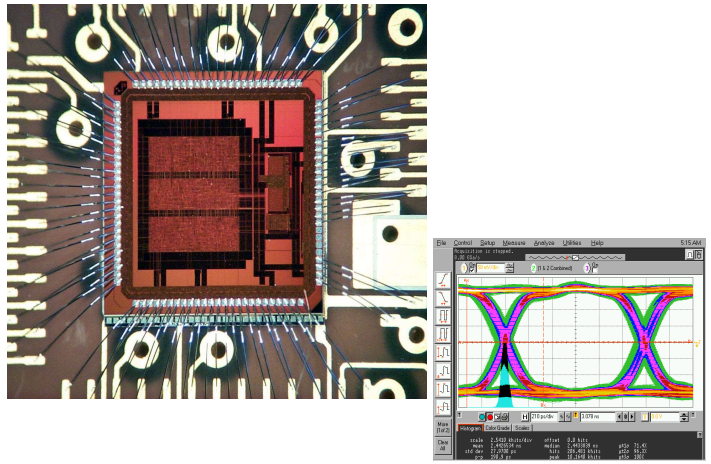
Now here

After N.S. Saks et al, IEEE TNS, Vol. NS-31 (1984) 1249





G. Anelli et al., IEEE TNS-46 (6) (1999) 1690



P. Moreira et al.
http://proj-gol.web.cern.ch/proj-gol/

Total ionizing dose:

- Intrinsic transistor has become more and more radiation tolerant due to thinner gate oxide
- In LHC enclosed NMOS transistors and guard rings in 0.25 µm CMOS to avoid large leakage current
- In deeper submicron enclosed geometry usually no longer necessary for leakage, but for small dimensions parasitic effects dominate e.g. from spacers, new gate dielectrics, **requires extensive measurement campaigns**

F. Faccio et al. IEEE TNS-65 (1) 164, 2018

Single event effects:

- Single Event Upset : triple redundancy with majority voting (now special scripts S. Kulis)
- Latch-up not observed so far in LHC, but observed on MAPs at STAR, and in new technologies => **need attention in the design**

Key achievement after MLR1: TPSCo 65 nm qualified for HEP

- Chain of sensor with process modifications, analog front end, and digital readout fully efficient in test beam validating process modifications and pixel designs.
- Pixel pitch

  DPTS 15 µm pixel pitch, stitched devices in ER1 18 µm and 22.5 µm (180 nm: ALPIDE ~ 28 µm)

  Sensor variant with gap conserves efficiency at larger pixel pitches.

- Radiation tolerance

  NIEL: DPTS 10^{15} n_{eq}/cm^2 at room temperature, 10^{16} n_{eq}/cm^2 will need cooling (needed for 10^{15} for 180 nm)

  TID: transistors in line with other 65 nm CMOS technologies, leads to tested tolerance beyond 100 Mrad for several circuits (ringoscillators, VCO, DAC, bandgap, etc)

  SEU: cross-sections in line with other 65 nm CMOS technologies

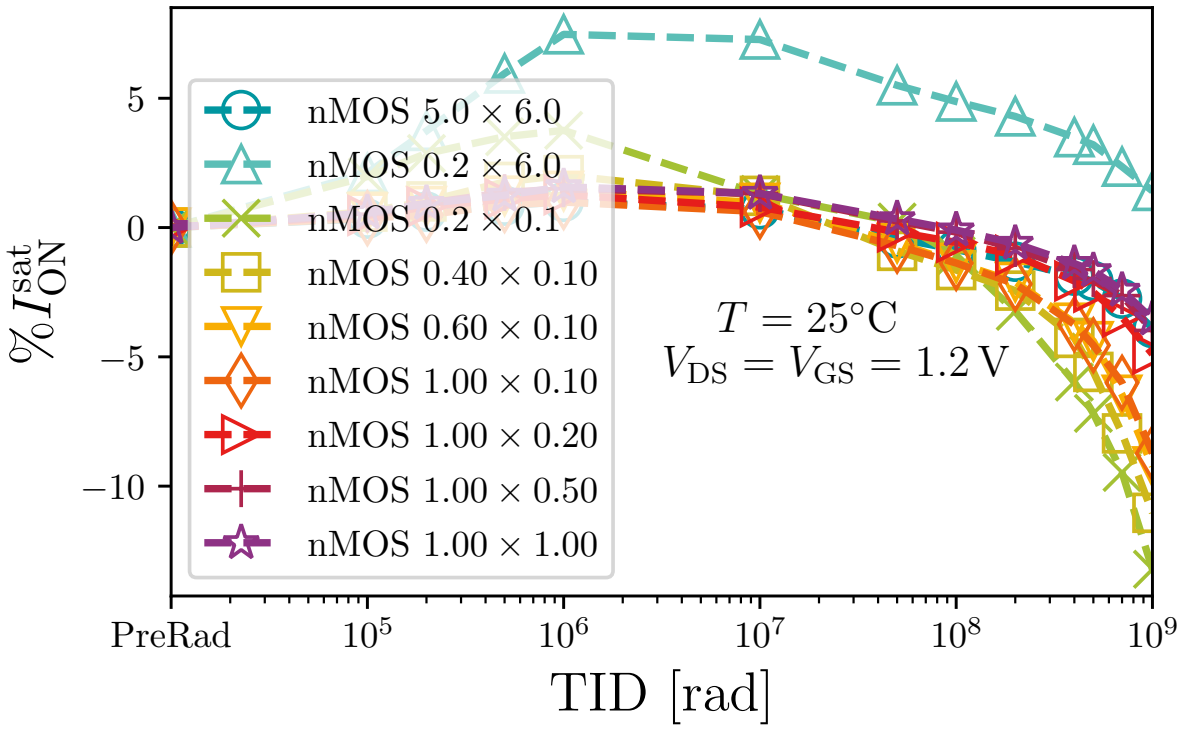
- Timing (only established really for the sensor now);

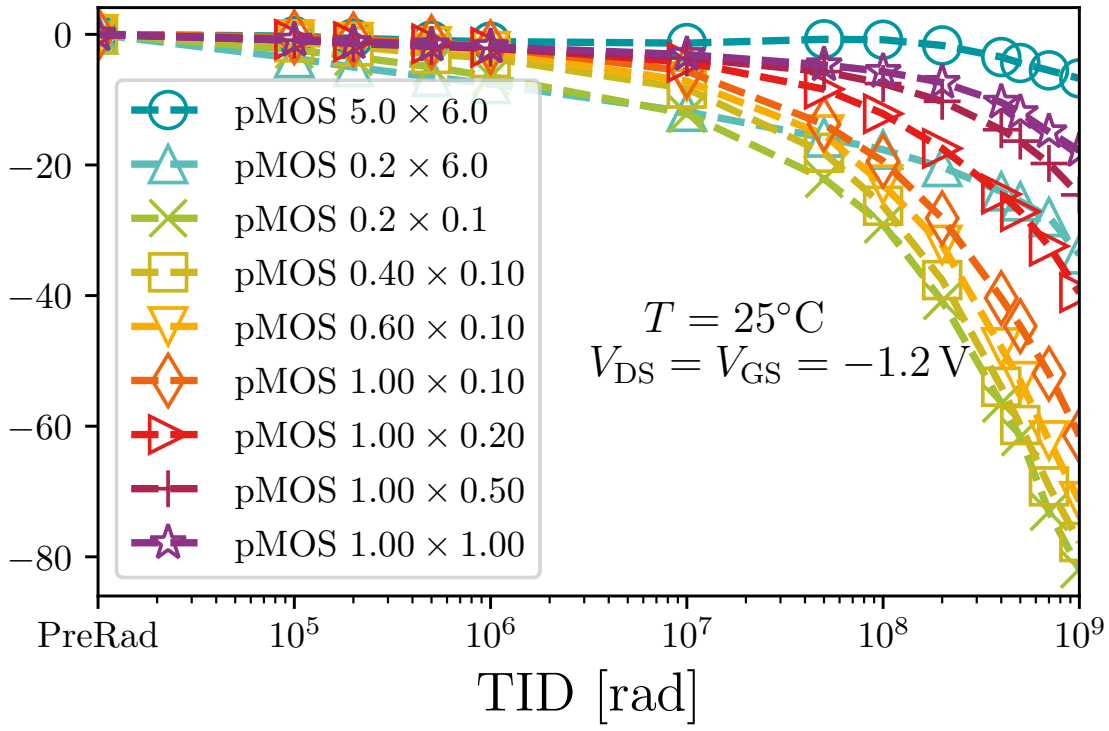
  APTS_OA ~ 80 ps requires further study, no timewalk correction yet etc (180 nm: FASTPIX ~ 100 ps) see backup

- Many features in the technology still unexplored: special imaging devices, wafer stacking, ….

EP R&D Open day 2023, WP1.2 Summary:
https://indico.cern.ch/event/1233482/contributions/5264293/attachments/2596131/4482445/EP_RandD_Days_WP1.2_2023_02_20.pdf
Proceedings on process optimization: https://pos.sissa.it/420/083
Article on DPTS chip (under review at NIMA): https://doi.org/10.48550/arXiv.2212.08621

Transistor radiation tolerance

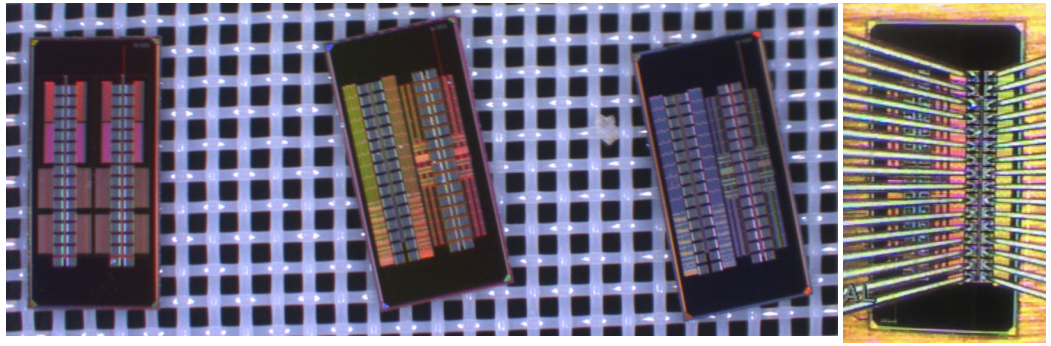




In line with other 65 nm technologies, no showstoppers.

Small size PMOS transistors degrade significantly after several hundred Mrad.

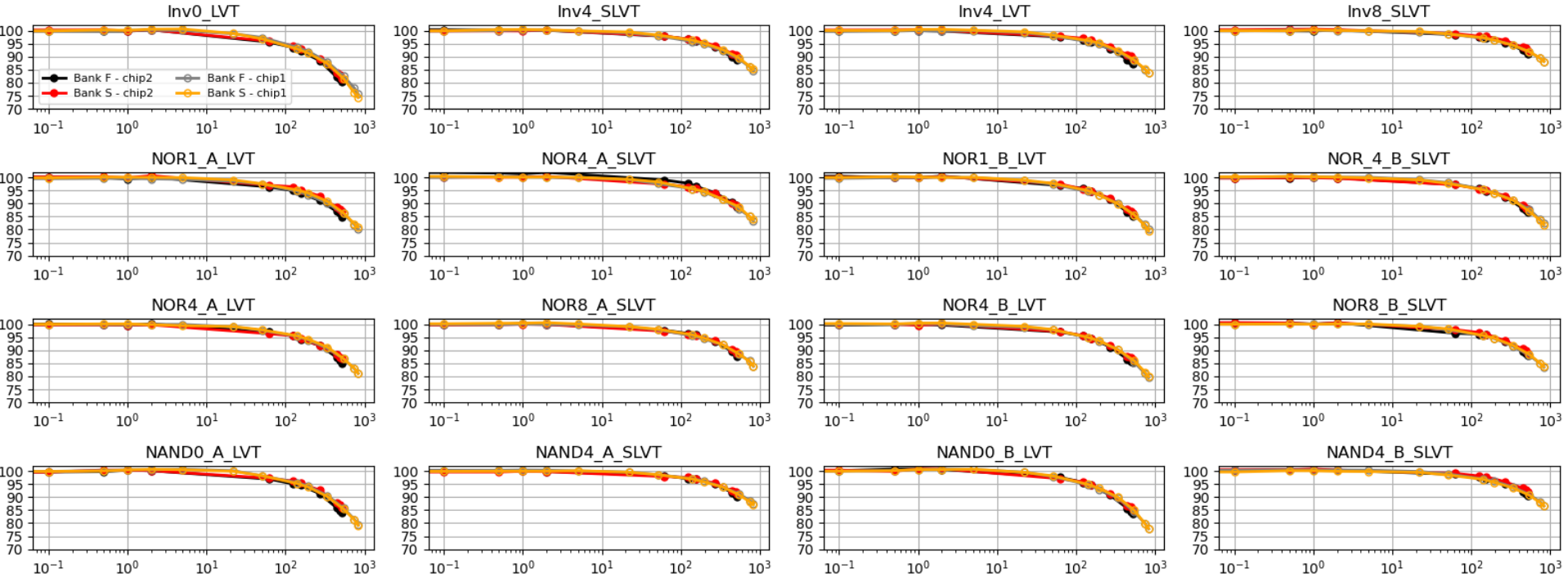
Caveat: modeling of transistors with significant reverse bias

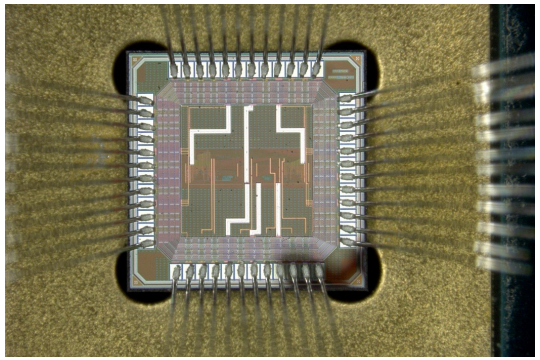


A. Dorda Martin et al. “Measurements of total ionizing dose effects in TPSCo 65 nm and influence of NMOS bulk bias”. doi: 10.1088/1748-0221/18/02/C02036

Ringoscillator test chip

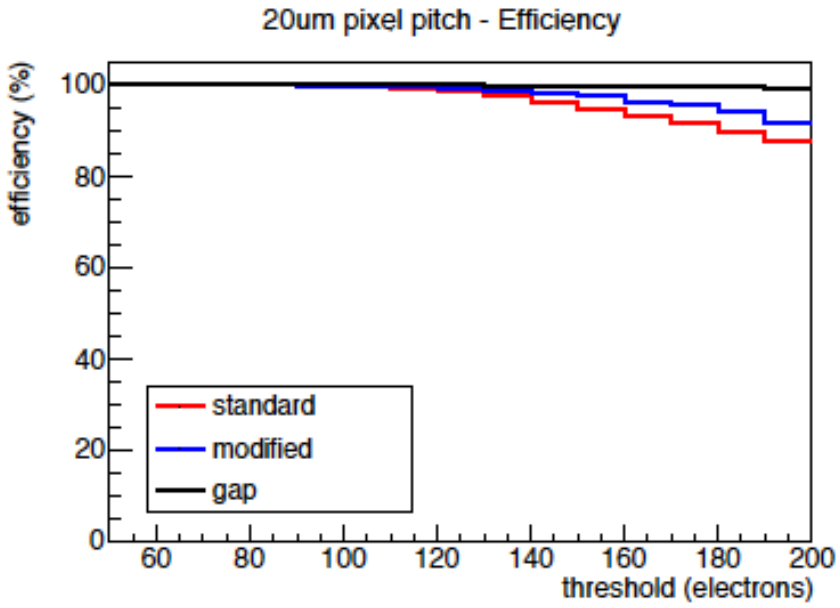
CPPM: Pierre Barrillon, Marlon Barbero, Denis Fougeron, Alexandre Habib and Patrick Pangaud (TWEPP 2022)

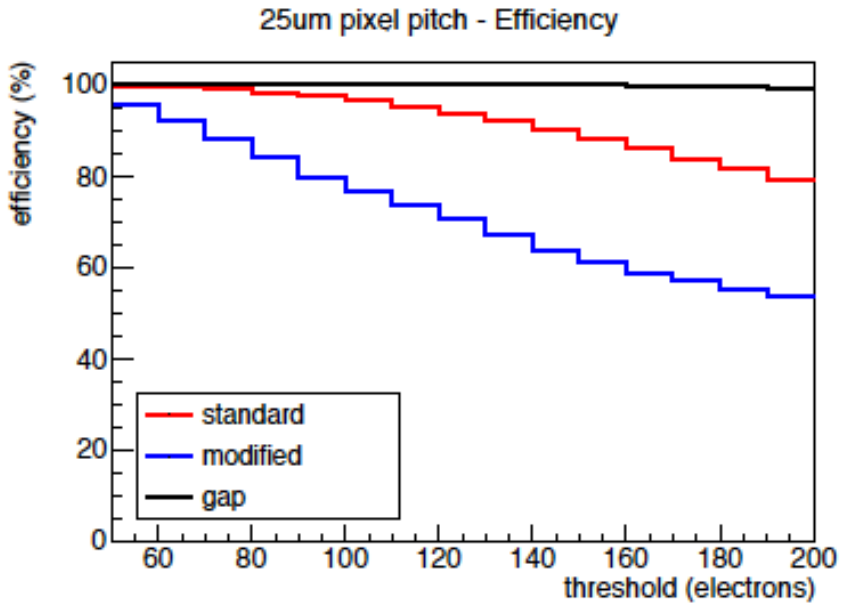


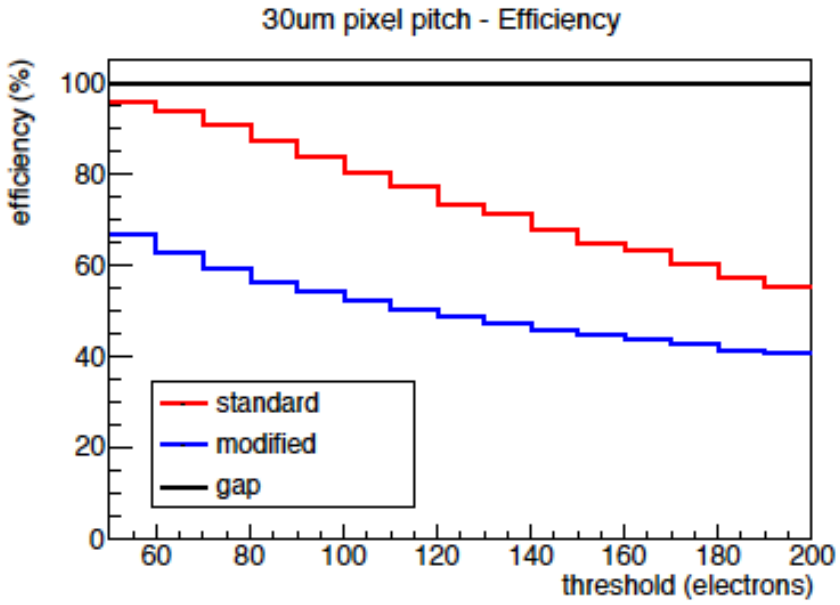


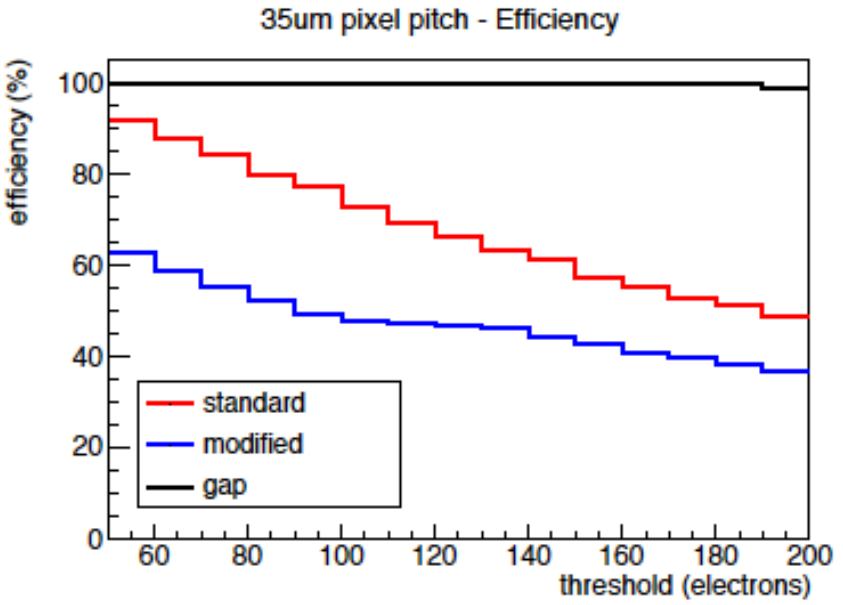
- CPPM contributed to MLR1 with a Ring Oscillator test chip to characterize the standard cells of the TJ 65 nm technology.
- The chip contains 48 ring oscillator based on different standard cells.
- 2 banks of 24 Rows each with the purpose of testing two approaches while irradiating:
  - Functional: the oscillation is enabled
  - Static: the oscillation is disabled
- Oscillation frequency drops by 12-25 % after 830 Mrad. Degradation more pronounced for smaller cells.
- Also several analog designs radiation tolerant up to several 100 Mrad, eg DACs (IPHC) , VCO, bandgap (NIKHEF)…

Different pixel flavors at larger pixel pitches









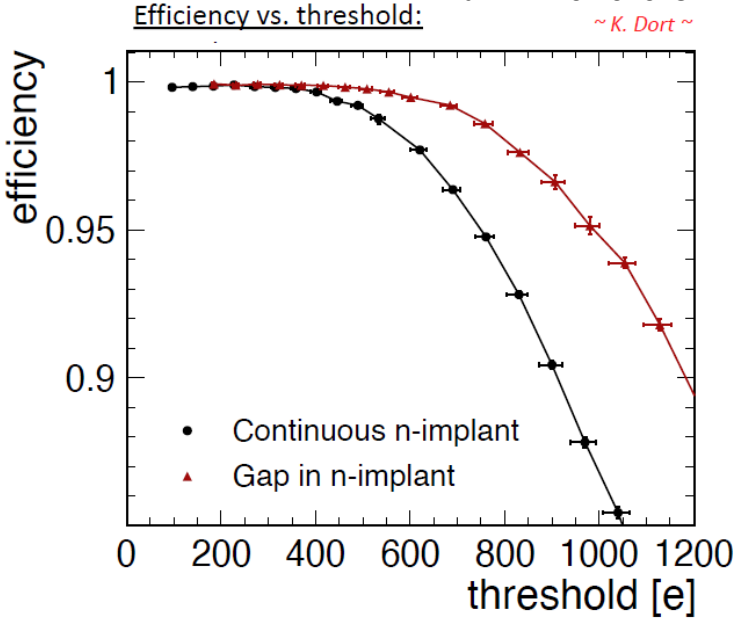
Simulations by J. Hasenbichler for MIPS

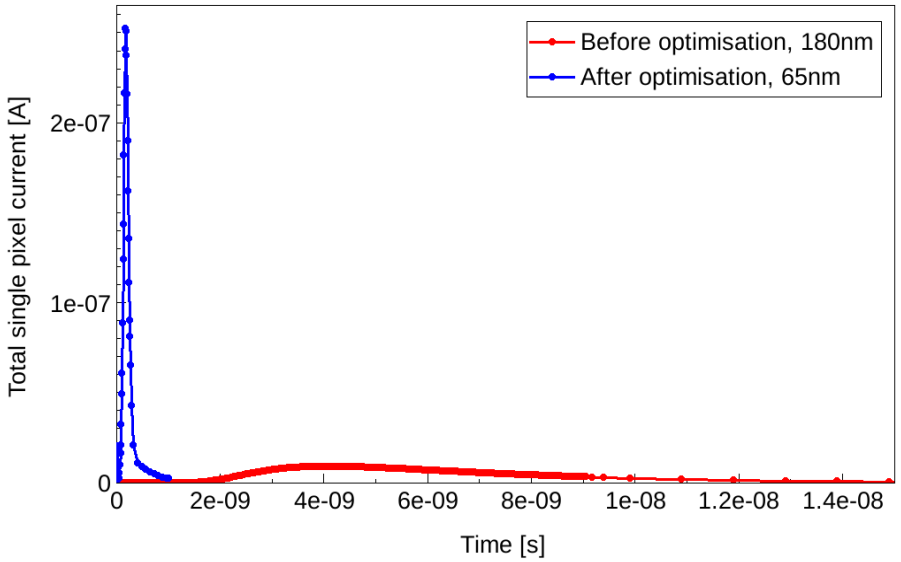
Charge sharing reduces the signal in a single pixel and reduces efficiency especially for larger thresholds.

Only the gap concentrates charge sufficiently to remain efficient for large pixel pitches

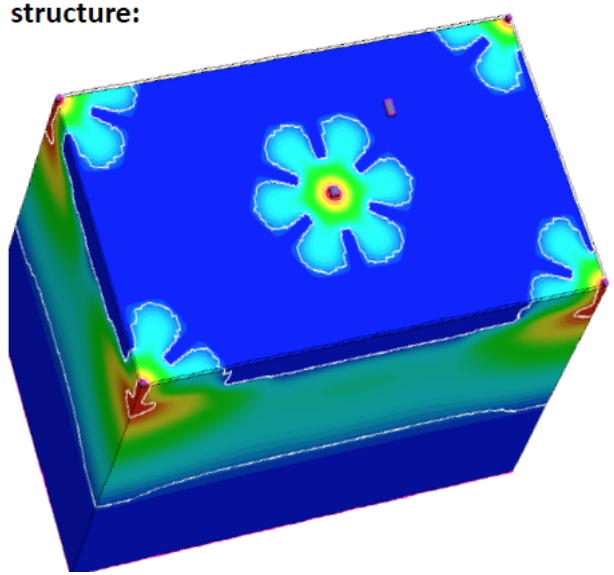
Process optimizations for small collection electrode

arXiv:2102.04025





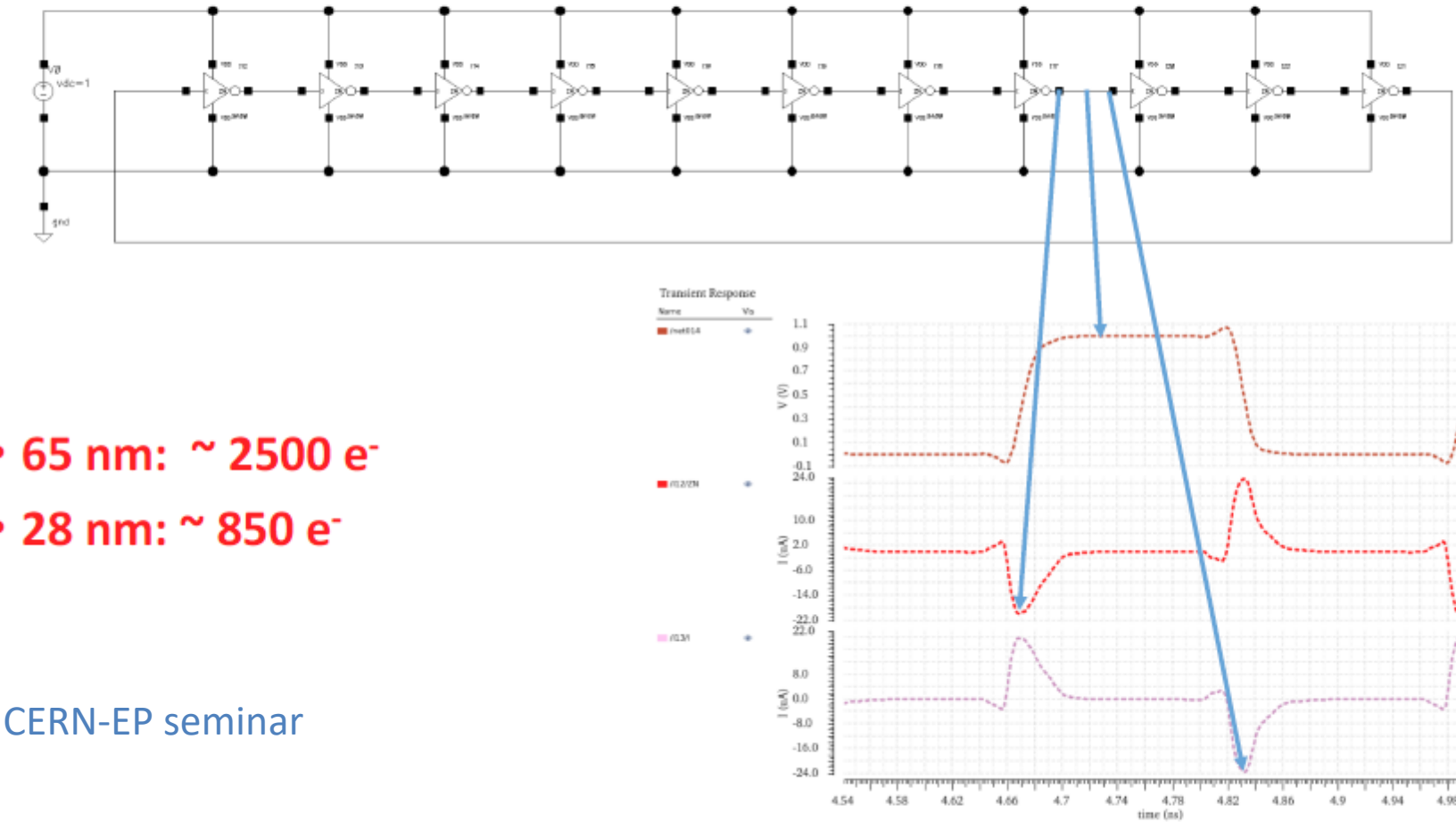
Example of complex 3D TCAD structure:



- Efficiency improvement is not only simulated but also measured, even before irradiation (see top left: efficient operating window is almost doubled)
- The optimization over different pixel pitches and flavors, and technologies has improved the timing by several orders of magnitude. Simulations of even more complex structures bring peak-to-peak variations in the order of 50 ps at the moment
- These techniques have now been applied to several chips, and technologies and are generally applicable.

See M. Muenker's CERN EP detector seminar

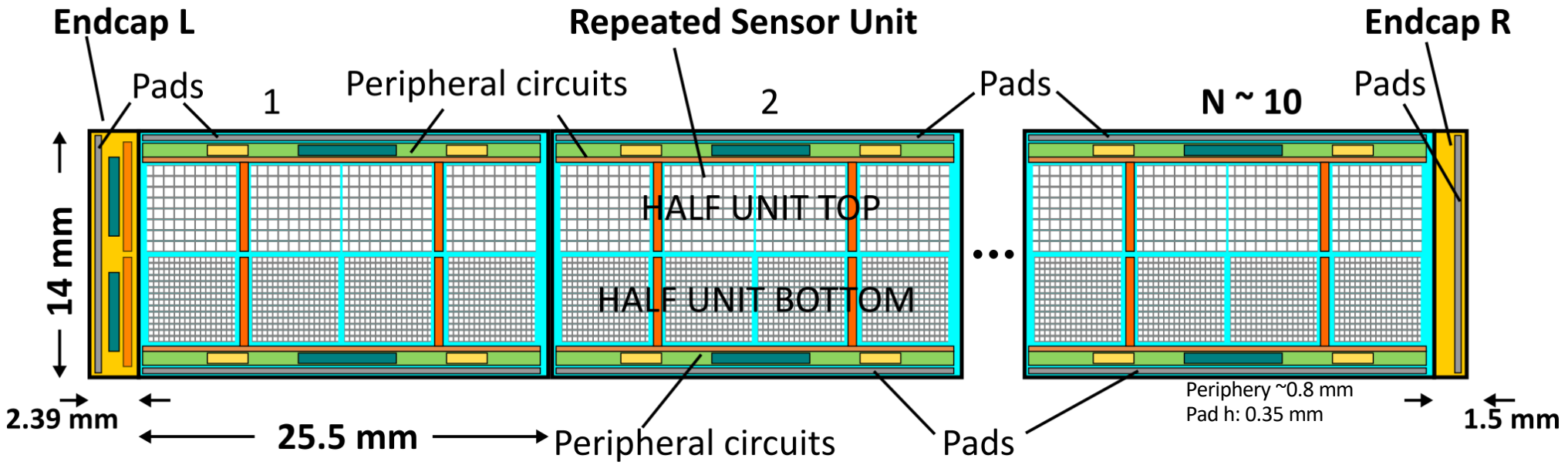
How many electrons are needed to switch a logic gate ?



- **65 nm: ~ 2500 e⁻**
- **28 nm: ~ 850 e⁻**

A. Marchioro, 2019 CERN-EP seminar

MOSS Monolithic Stitched Sensor Prototype

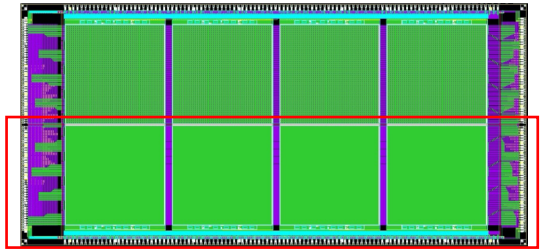


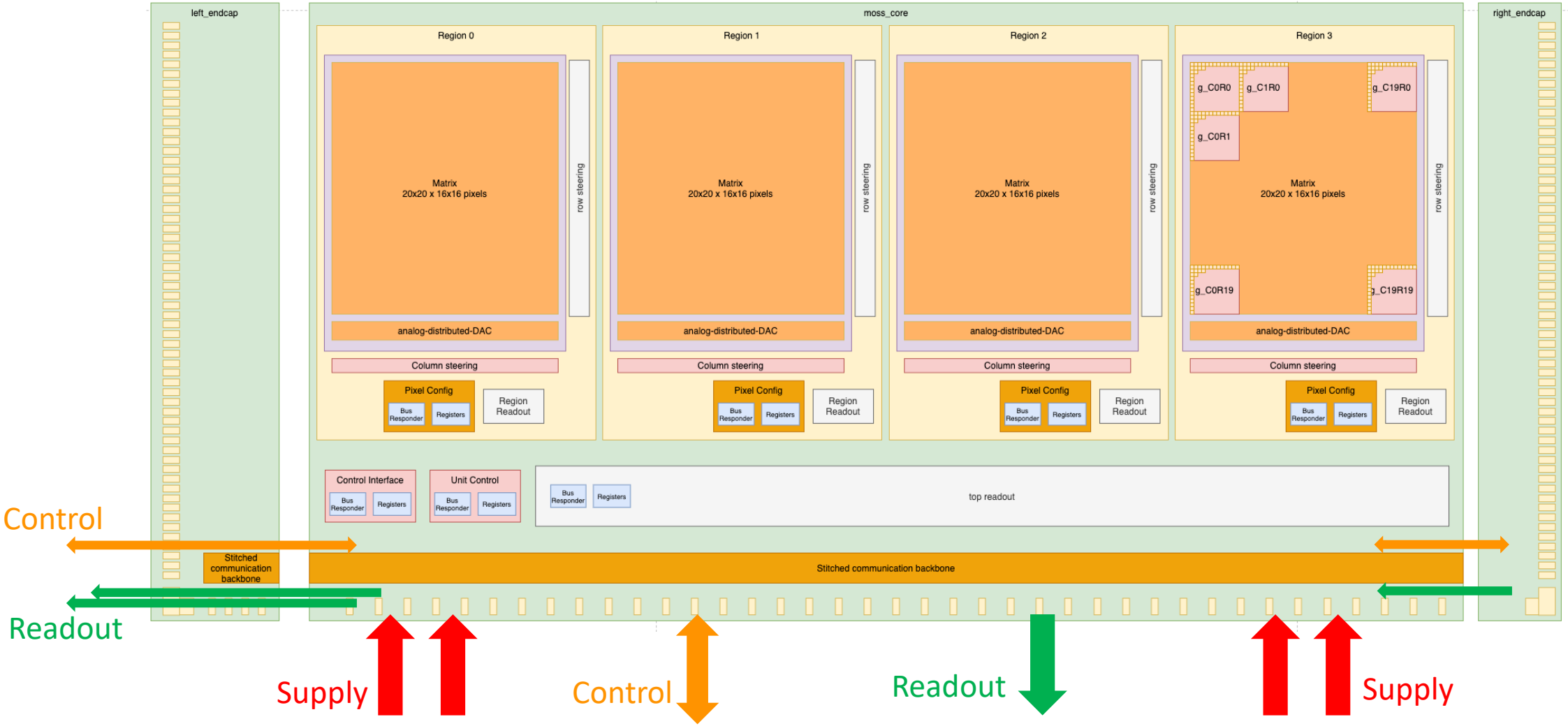
Primary Goals
Learn Stitching technique to make a particle detector
Interconnect power and signals on wafer scale chip
Learn about yield and DFM
Study power, leakage, spread, noise, speed

Repeated units abutting on short edges

- Repeated Sensor Unit, Endcap Left, Endcap Right
- Functionally independent
- Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

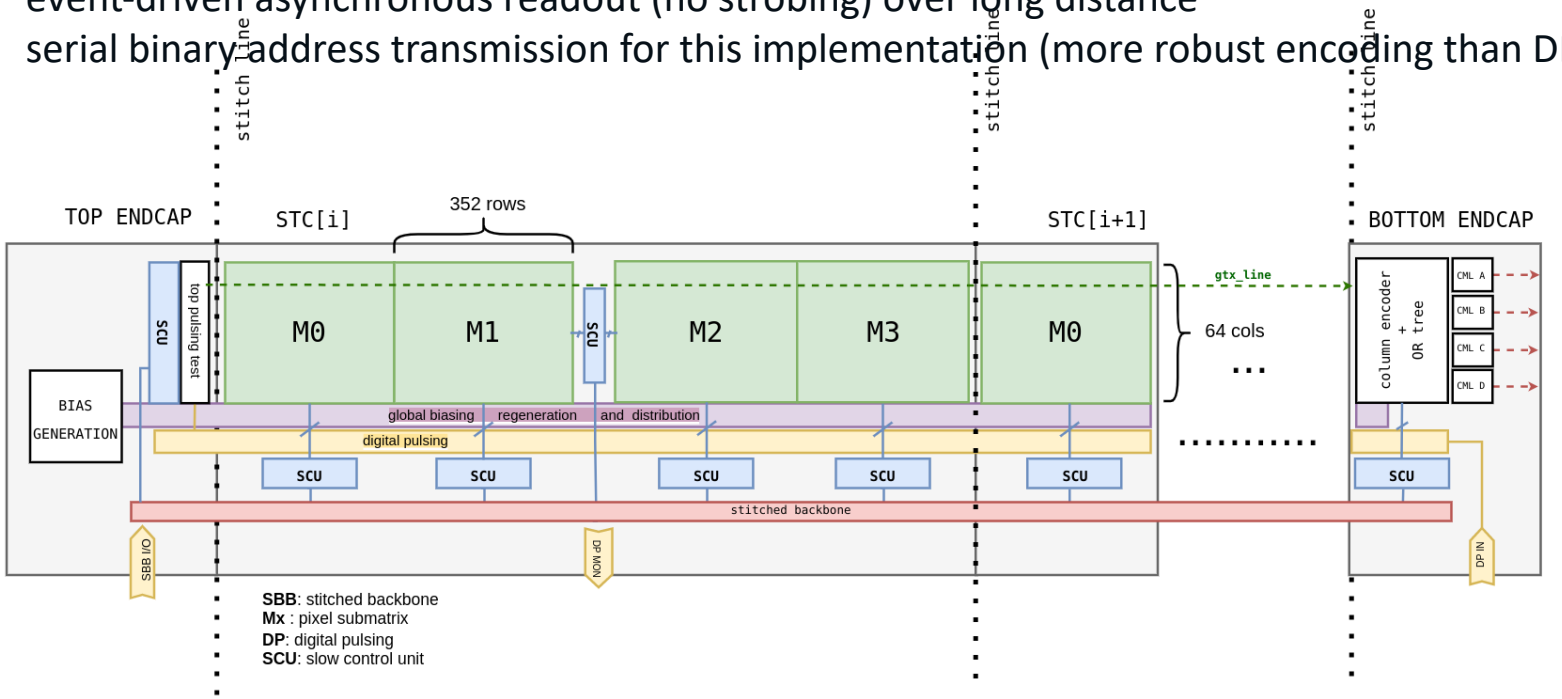
MOSS - Half Unit

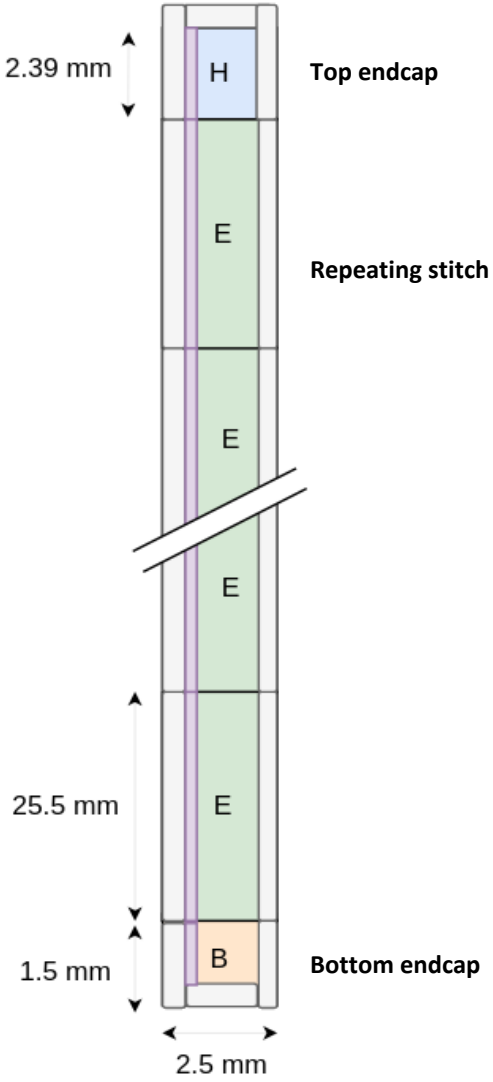




MOST Chip

- Investigate **yield** when local density is preserved
  - Global power domains over full chip (Digital/Analog)
  - Higher granularity in power gating in case of a defect of
    - analog (rows of 4 pixels)
    - digital (half columns)
  - PWELL tied to ground
    - reverse sensor biasing achieved by higher power supply
- Immediate transfer of hit data to the periphery (bottom endcap, 4 CML outputs)
  - event-driven asynchronous readout (no strobing) over long distance
  - serial binary address transmission for this implementation (more robust encoding than DPTS)





MOST Chip: more detail

~ 90k pixels per stitch