Results and perspectives on sensors and electronics for high-resolution 4D-tracking

PSD13: Position Sensitive Fast Timing Detectors Session

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INFN Torino

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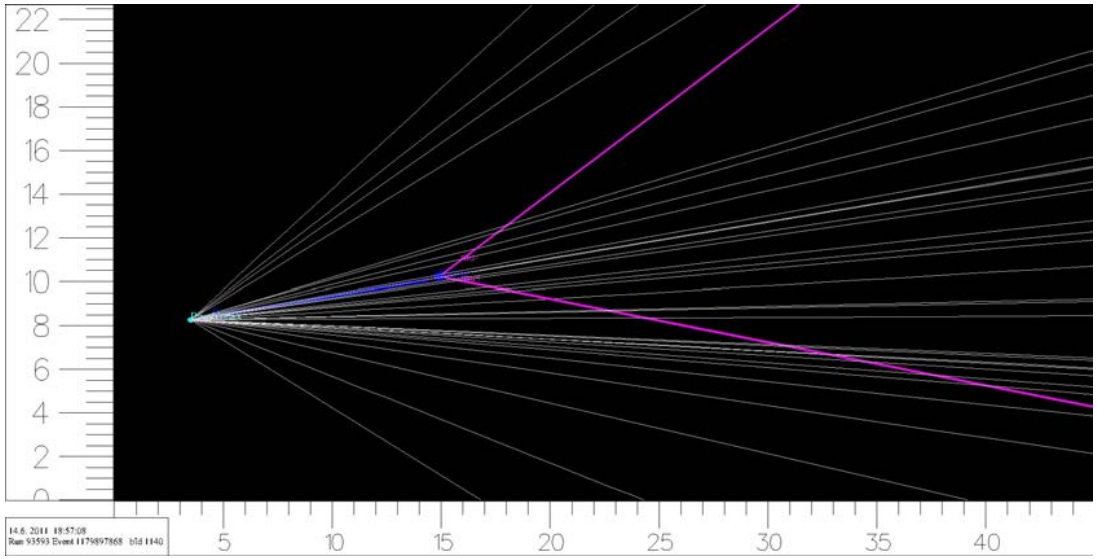
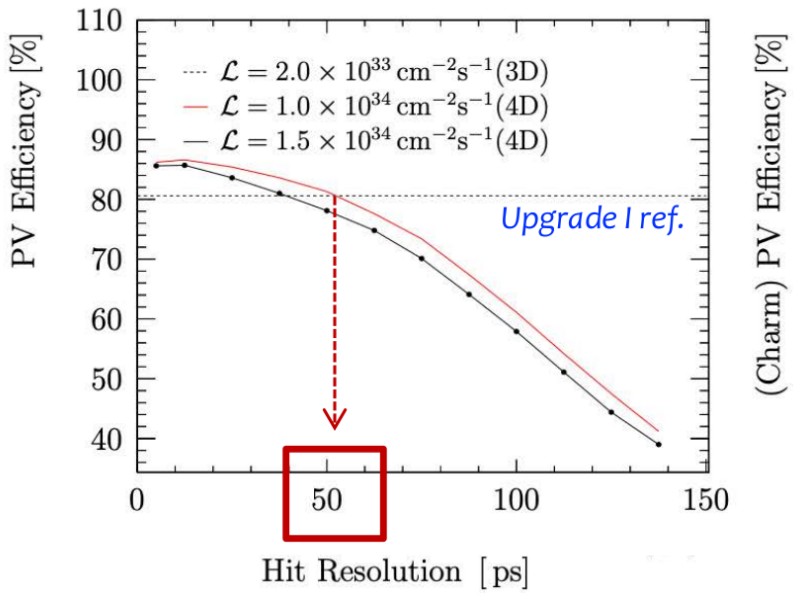
4D Tracking: Context



B_{0S} **meson decaying into a** μ^+ **and** μ^- **pair**



- 4D tracking: adding the time information at pixel level to conventional tracking.
- Helps to mitigate pile-up.
- Resolves merged tracks $\rightarrow$ avoiding bad primary vertex reconstruction $\rightarrow$ increase in reconstruction efficiency.

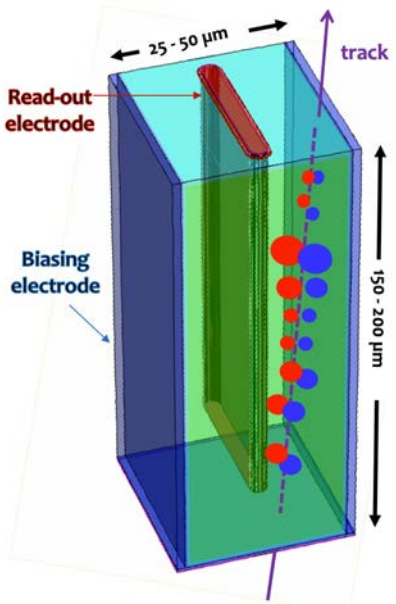
Plot from: Considerations for the VELO detector at the LHCb Upgrade II – CERN-LHCb-2022-001

- Spatial resolution: $\sim 10\,\mu m$ rms.
- Timing resolution: $<50\,ps$ rms $\rightarrow$ comprising all contributions:

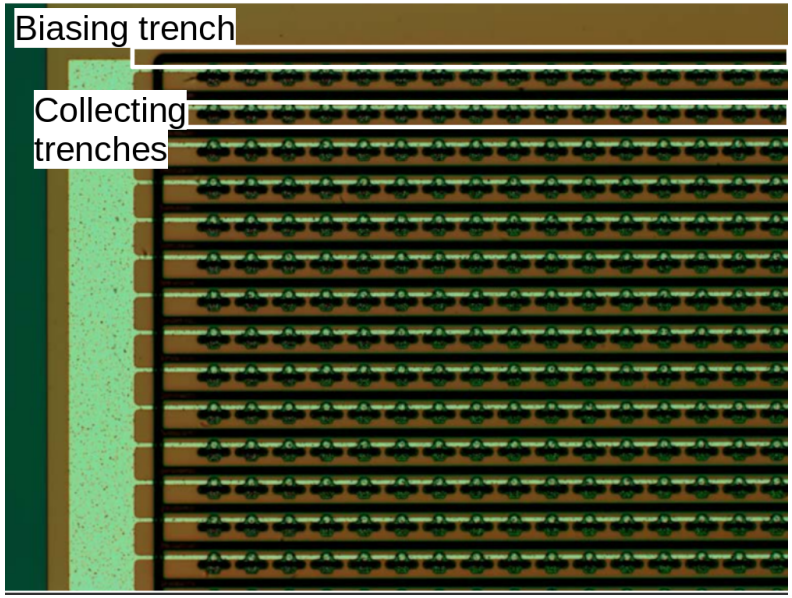
$$\sigma_t = \sqrt{\sigma_{sens}^2 + \sigma_{afe}^2 + \sigma_{tdc}^2 + \sigma_{clk}^2 + \sigma_{corr}^2}$$

- Radiation hardness to: high fluences $10^{16}\ \frac{MeV n_{eq}}{cm^2}$ to $10^{17}\ \frac{MeV n_{eq}}{cm^2}$, TID $> 1\,Grad$.
- Detection efficiency $> 99\,\%$.
- Material budget $< 0.5\,\%$ radiation length per layer.
- Power budget of $1.5\ \frac{W}{cm^2}$ ($\sim 25\,\mu W$ with a $50\,\mu m$ pitch).
- Data band-width $\sim 100\ \frac{Gbps}{cm^2}$.

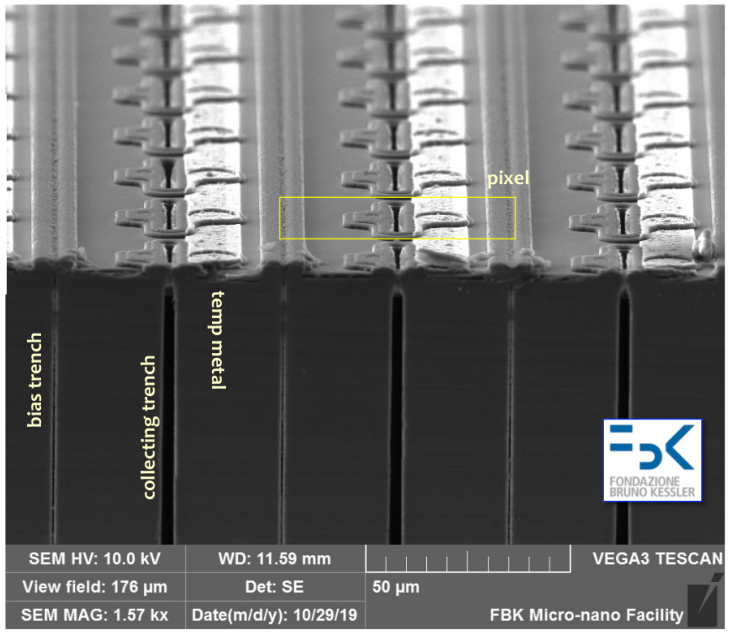
Outline



3D pixel layout



matrix photo: top view



matrix photo: section

- 3D Sensor: the sensitive area is the whole bulk → more charge, lower inter-electrode distance.
- Geometry: 55 µm × 55 µm × 150 µm pixel with segmented trench shaped collecting electrode and continuous biasing electrode → very uniform electrical field.
- Manufactured by FBK using deep-reactive-ion-etching.

TimeSPOT
TIME and SPace real-time Operating Tracker

TimeSPOT project by INFN

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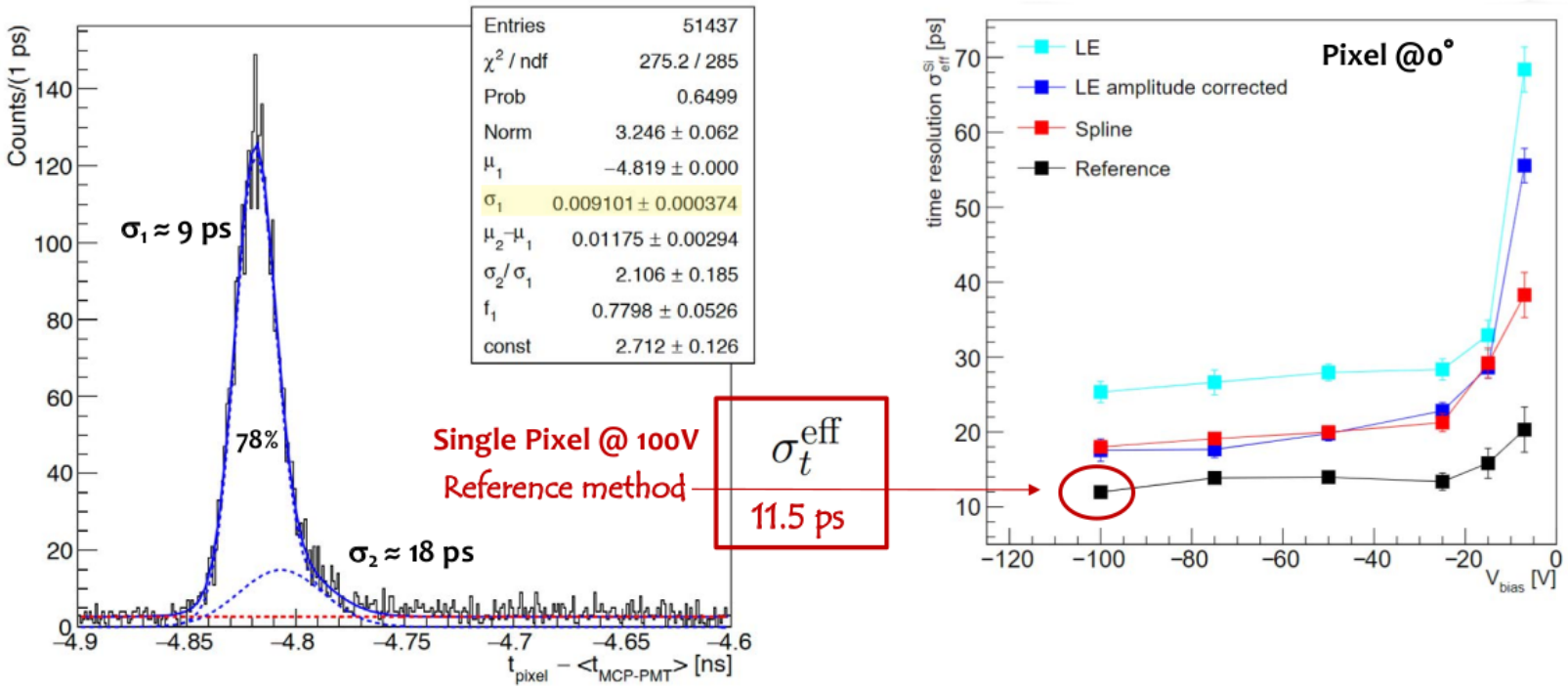
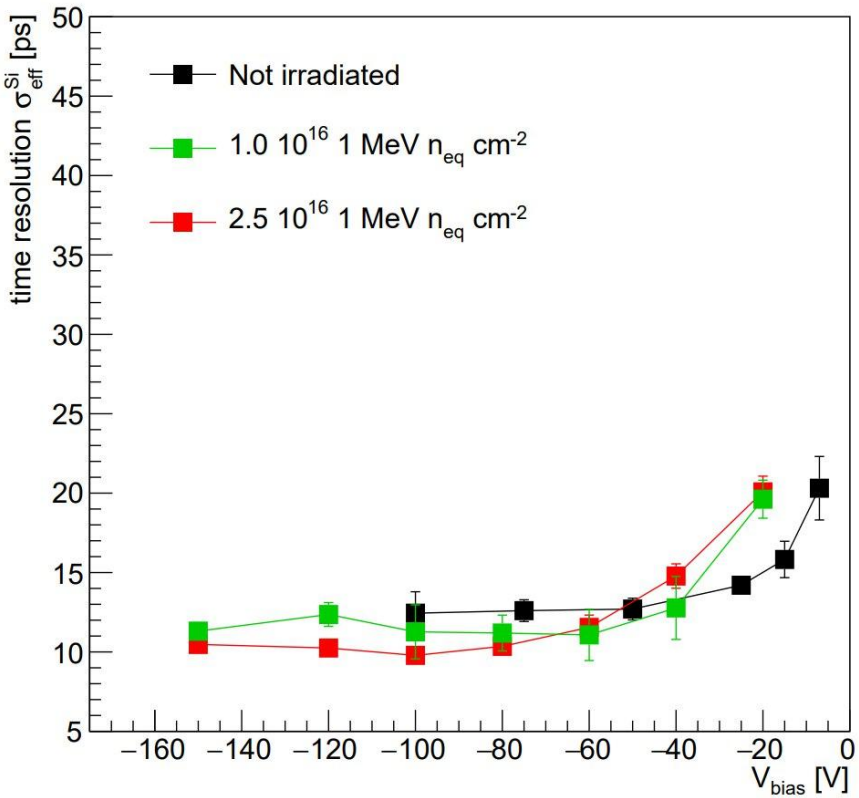
Intrinsic Timing Resolution



Left: histogram of the measured arrival time, right: time resolution vs bias voltage. Taken from [1].

- The intrinsic timing resolution has been evaluated with a test-beam → real particles response with unknown track position and angle → the effect of its field dis-uniformity is also accounted.
- The signals have been processed with a fast discrete electronic → the contribution of its time-walk have been compensated analytically with various CFD approaches.

[1] Borgato F, Brundu D, Cardini A, Cossu GM, Dalla Betta GF, Garau M, La Delfa L, Lai A, Lampis A, Loi A, Obertino MM, Simi G and Vecchi S (2023) Charged-particle timing with 10 ps accuracy using TimeSPOT 3D trench-type silicon pixels. Front. Phys. 11:1117575. doi: 10.3389/fphy.2023.1117575

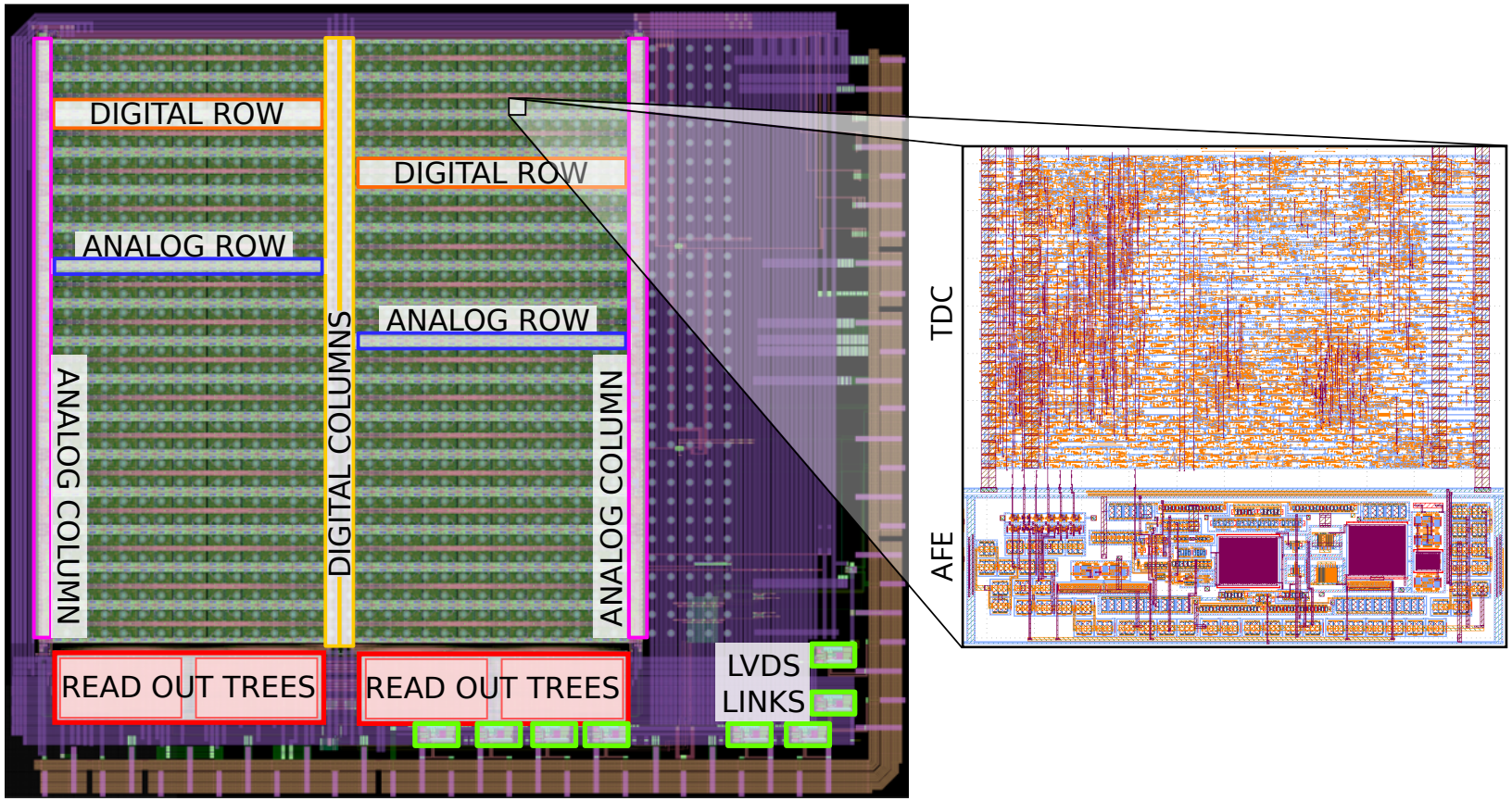


Time resolution vs bias voltage pre and post irradiation, taken from [2]

- The test beam measurement has been also repeated after irradiating the sensors to $2.5 \times 10^{15}\,\mathrm{MeV}\,\frac{n_{eq}}{cm^2}$.
- Comparable performance as pre-irradiation.

[2] Innovative silicon pixel sensors for a 4D Vertex Locator detector for the LHCb high luminosity upgrade, Andrea Lampis, PhD Thesis, https://hdl.handle.net/11584/359379

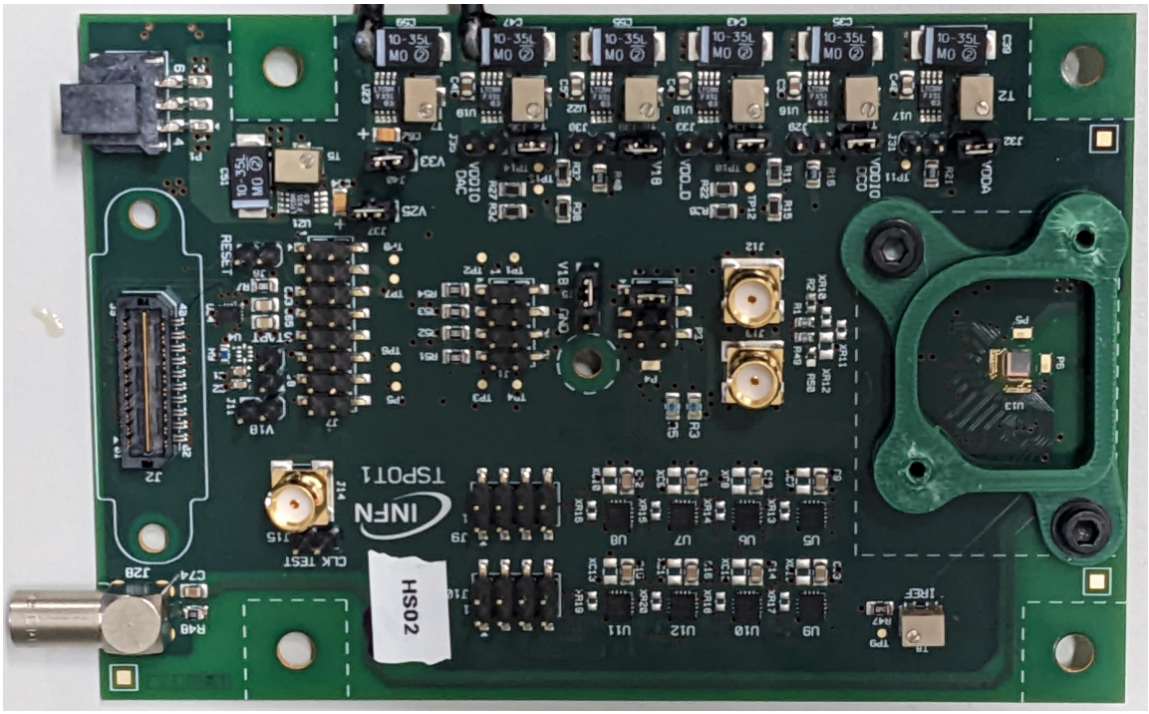
Outline



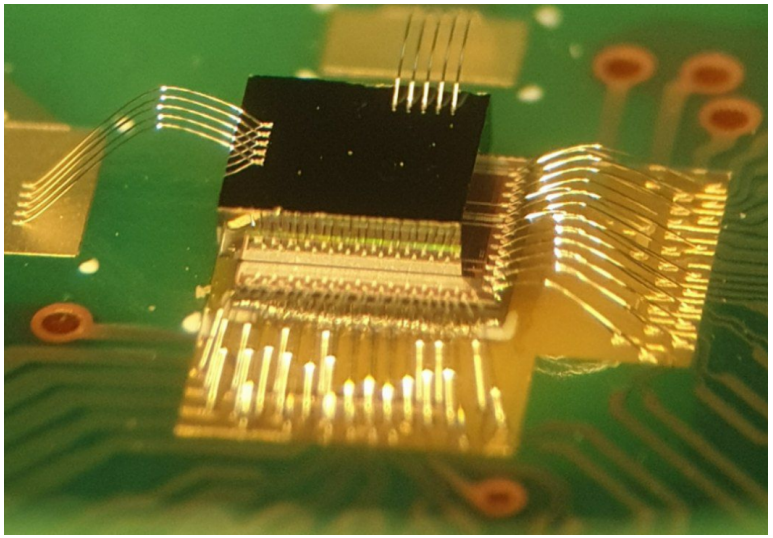
Timespot1 ASIC layout and pixel detail.

- 32×32 timing pixel front-end ASIC developed in 2020 in using a commercial 28 nm CMOS technology.
- 55 µm × 55 µm pixel pitch featuring one Time to Digital Converter (TDC) per pixel → both TA and ToT measurements.

TimeSPOT project by INFN



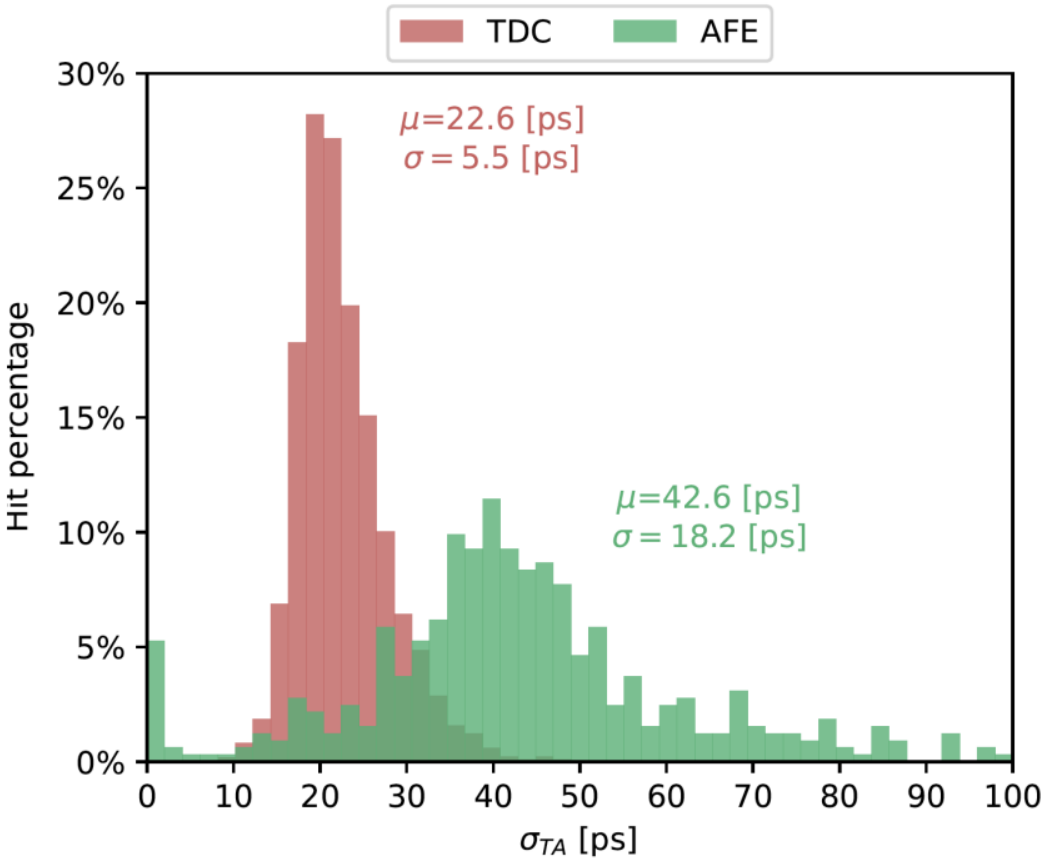
TSPOT1 board: Timespot1 inside the box on the right.



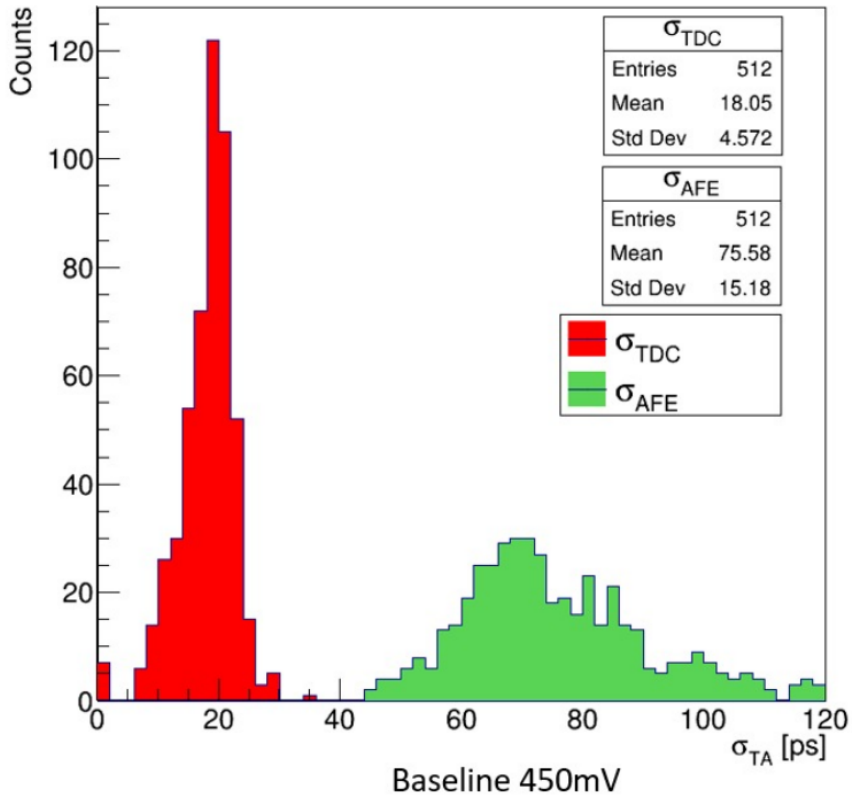
Timespot1 Hybrid: Sensor on top, ASIC below with wire bonded connection to TSPOT1.

- The ASIC has been integrated in the TSPOT1, board designed for both electrical self-tests and particle measurements.
- An hybrid prototype has been assembled by IZM via bump-bonding with the TimeSPOT sensor.

Electrical Self-test: Timing Resolution



Time resolution without sensor.



Time resolution of the hybrid.

- A large channel non-uniformity is present due to an issue with the dynamic channel equalization method → the timing performance have been limited to achieve a better uniformity.
- The hybrid Timespot1 is able to achieve an average time resolution of 75 ps with a per-channel power consumption of $\sim 40\,\mu W$ per channel ($1.32\,\frac{W}{cm^2}$).

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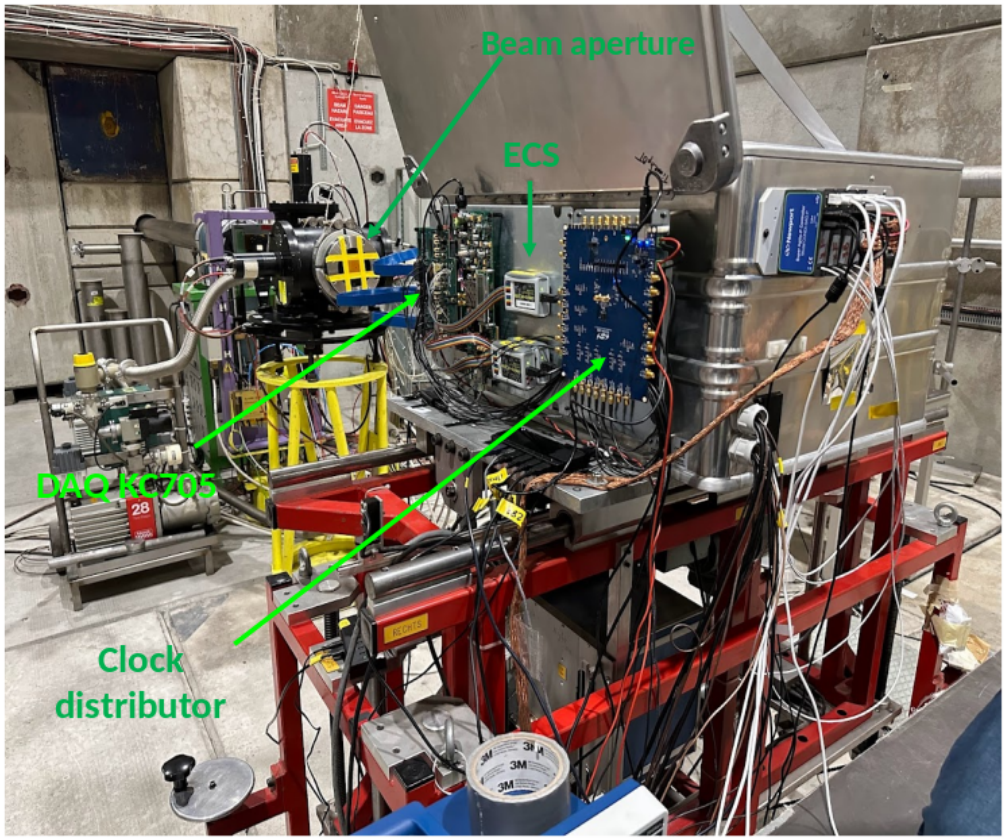
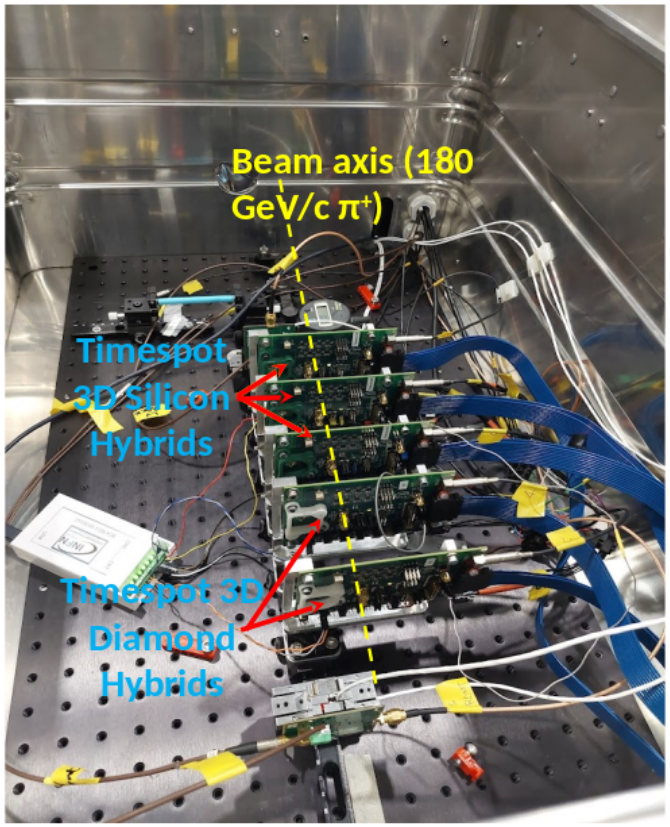
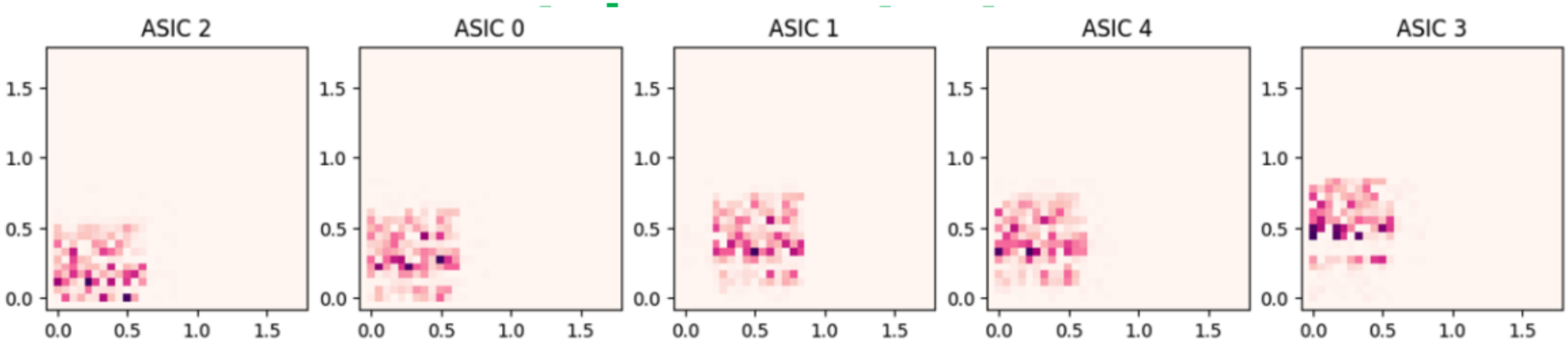
Test Beam Setup





- A 5 stations tracker demonstrator was tested in a test-beam at SPS in May 2023.

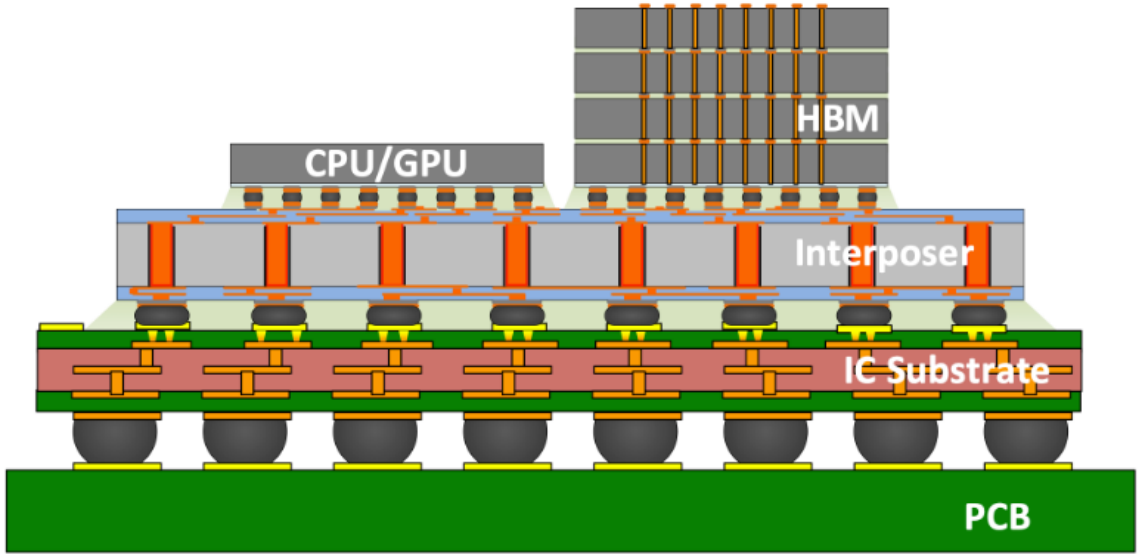


- An issue has been found during the tests: the sensor exhibits an unexpected large leakage current $\rightarrow$ no bias voltage could be applied.
- The leakage is located near some dummy structures inserted for mechanical strength.
- The track can be reconstructed, but the time resolution is affected $\rightarrow$ measured time resolution: 200 ps (As expected by repicating the conditions with a laser setup).

Outline

INFN Ground-up iNITiative for µElectronics developments

- Develop a 4D tracking system suitable for high-luminosity environments → integrated system composed hybrid 28 nm pixel front-end ASIC, and a readout ASIC for high-bandwidth optical data transmission.
- A national initiative funded by INFN. 14 INFN institutes, 70 people (physicist and engineers), 20 FTE, P.I. Adriano Lai (INFN Cagliari).
- Challenges:
  - Obtain reliably sub 50 ps rms time resolution per pixel → heavy consequences on power consumption and data throughput.
  - Delivering power to the pixels in a large scale matrix.
  - Distributing data from the matrix to the read-out.
- Method → leveraging innovative 3D integration technologies → use the TimeSPOT developments as the basis for the building blocks of the system.

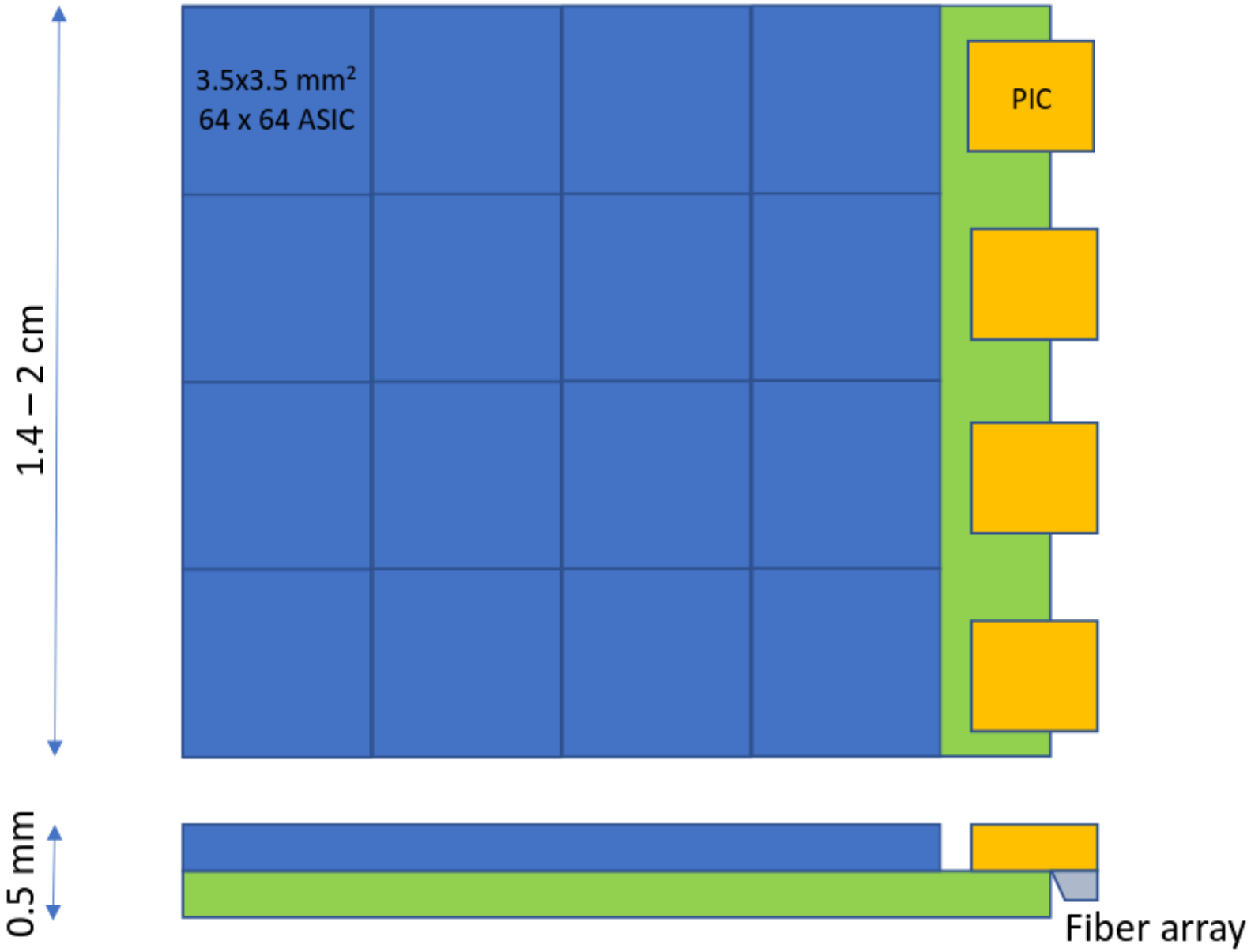


Example of 3D integration, taken from [3]

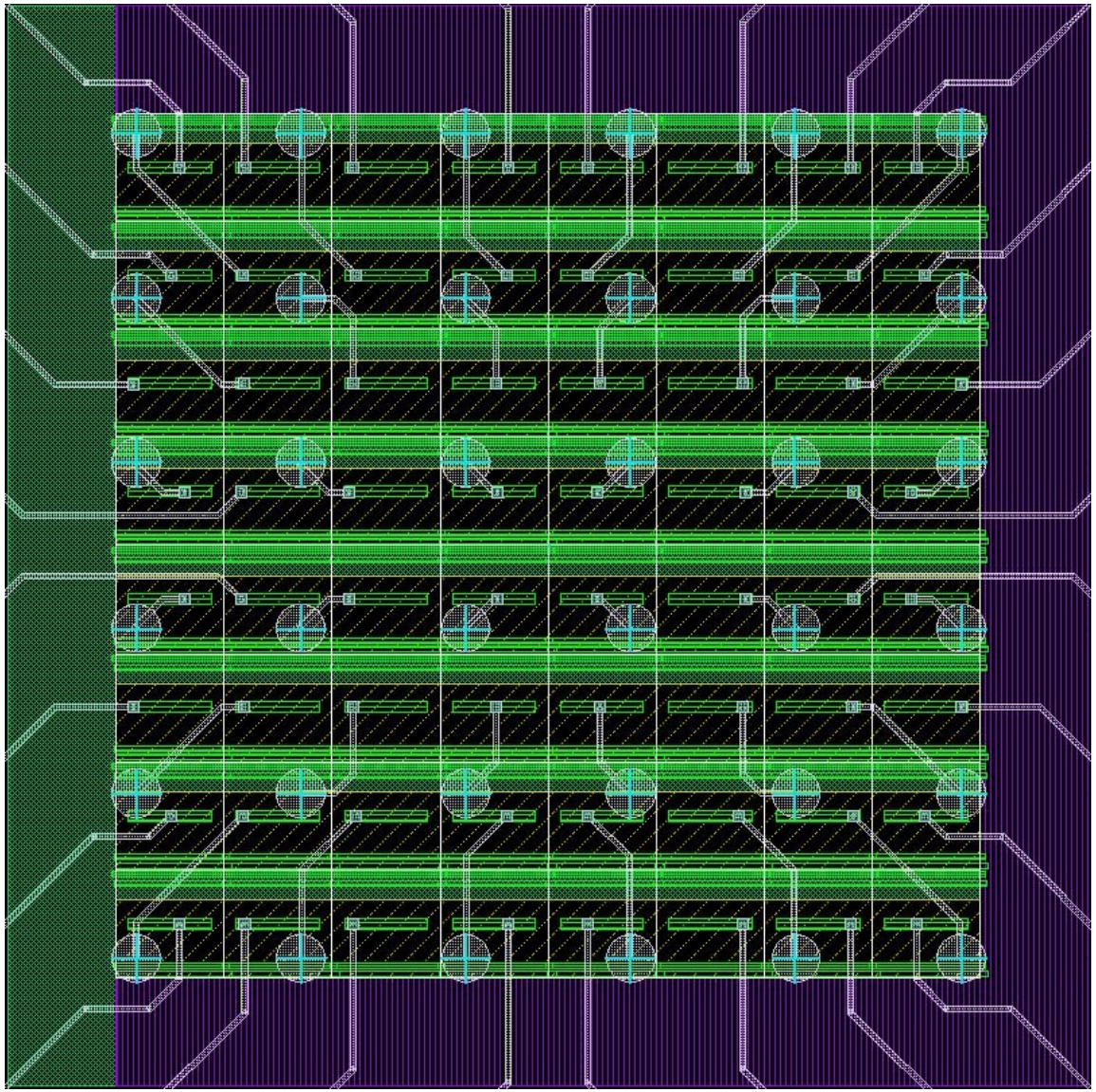
- 3D Integration: enables the vertical interconnection of different active layers → requires Through Silicon Vias (TSV).
- Enables the "Tiling" of the active area with front-end ASICs → no inactive area due to wire-bonding.
- Thinned layers → reduce the material budget compared to a PCB-based integration.
- The front-end ASIC can be accessed across the whole silicon area → more local power and data lines.
- Each layer can be designed around a specific task (e.g. pixel front-end, data merging, clock distribution etc.).

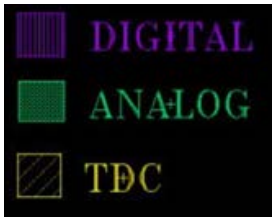
[3] T. Fritzsch, IZM, talk given at Pixel2022 workshop

System Integration Example



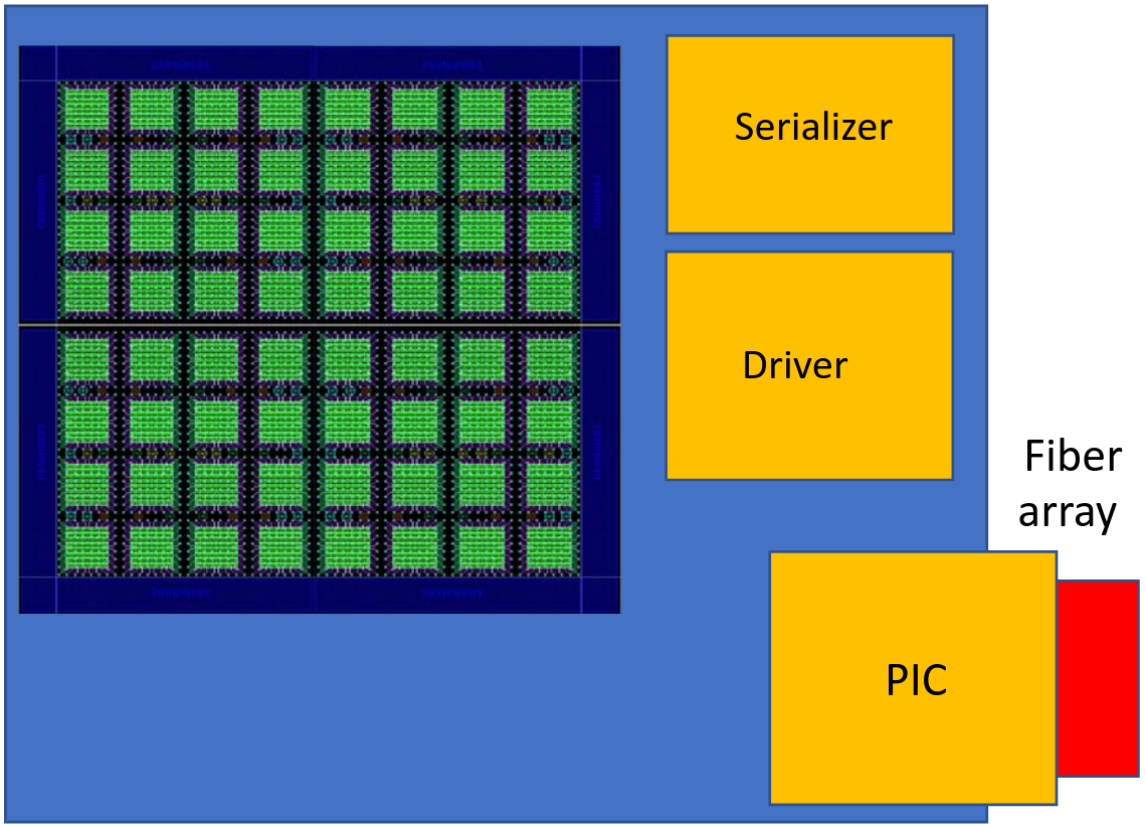
Repetition unit & Reduced Pitch





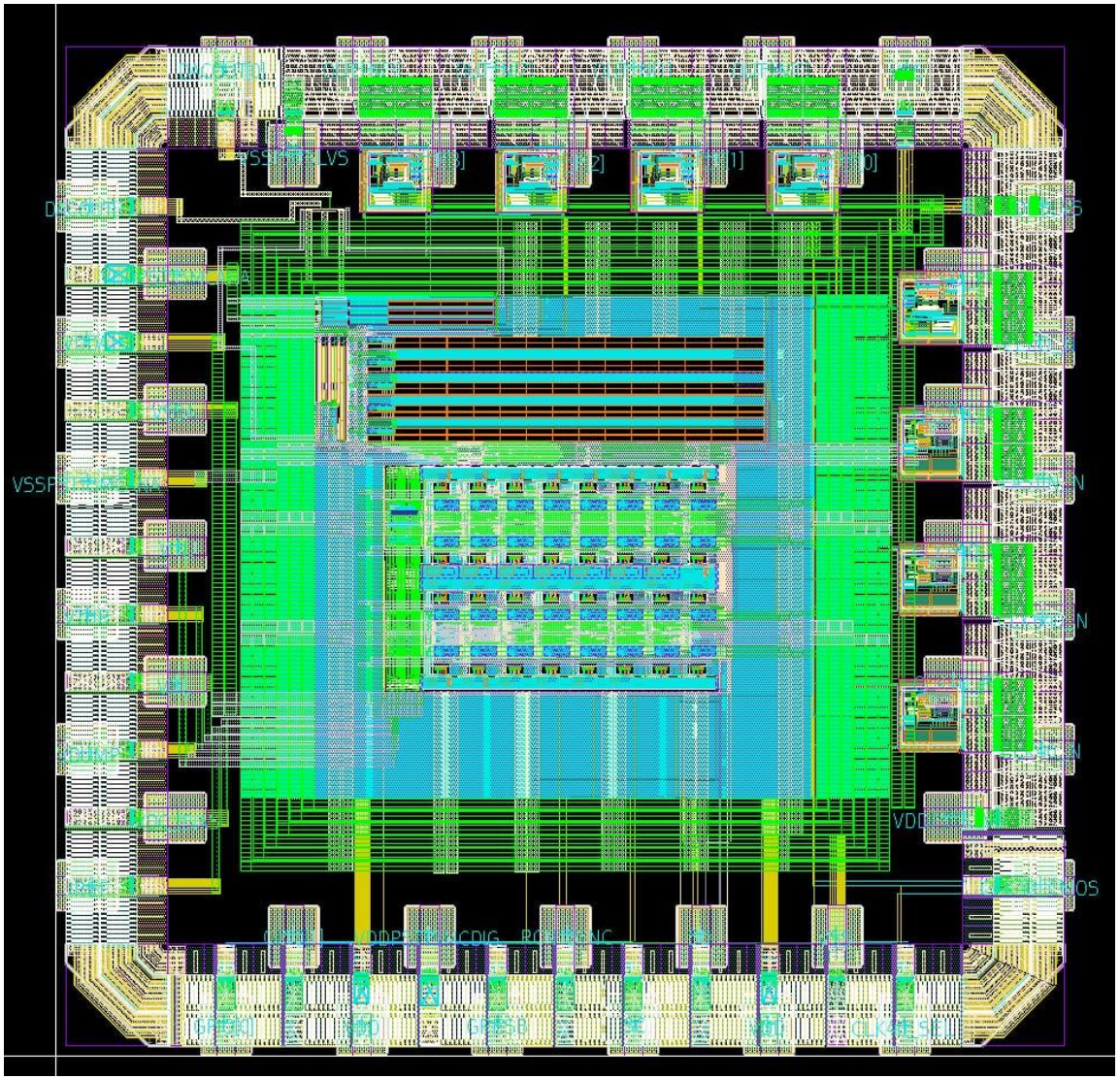
- No inactive area → the ASIC pixel have a reduced pitch compared to the Sensor (36 µm instead of 45 µm).
- An individual 8×8 block is built as a repetition unit → the spare area at the contour is used to place the service electronics and TSVs.
- The Sensor connection must be redistributed using the top metal layer.
- The complete matrix is built using multiple units.

First Matrix Prototype: Fractalic64



- First ASIC, Fractalic64, will be submitted next year:
  - 64×64 pixels matrix.
  - It features an additional periphery for preliminary test with conventional wire-bond integration (dark blue area).
  - The ASIC can also be integrated with TSV.
- It will be first assembled with a regular PCB.
- Photonic Integrated Circuit (PIC) for optical data output.

Test Chip: IGNITE0



Layout of the IGNITE0 ASIC.

- A first test chip, IGNITE0, has been submitted in July to test the individual components of Fractalic64 ($1\,\text{mm} \times 1\,\text{mm}$).
- It contains: various flavors of the Analog Front-End(AFE), the TDC, a DAC for the global voltages setting and a compact low-noise PLL.
- The AFE and TDC are organized in a slightly altered version of a half 8×8 repetition unit (in order to insert circuits for internal node testing).
- The ASIC will be ready to be tested in November.

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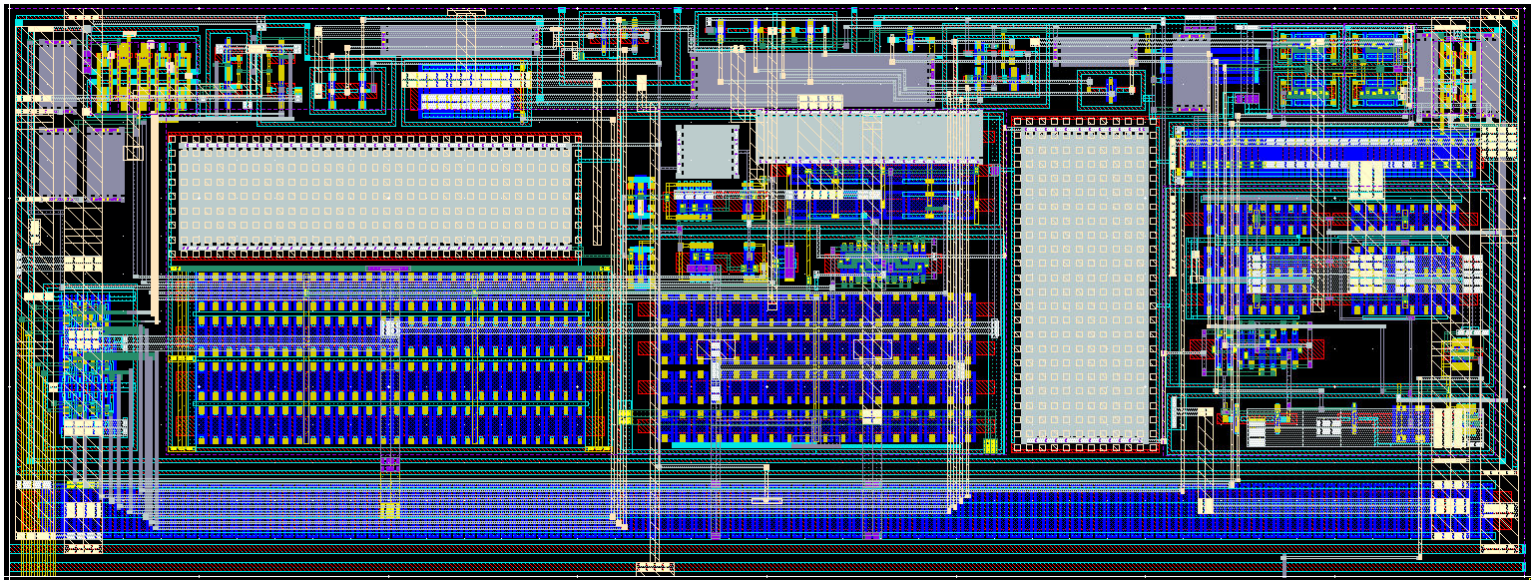
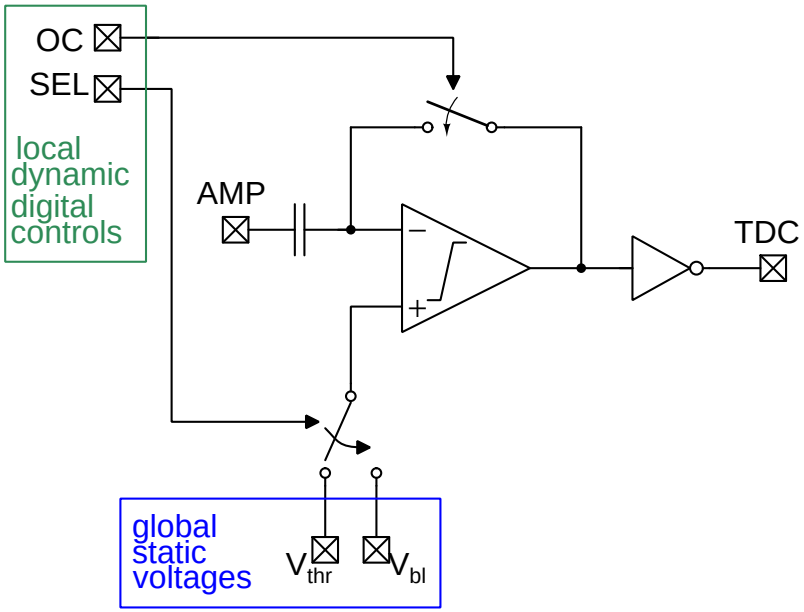


Layout of one of the proposed AFE

- Area: 36 µm × 13.5 µm.
- Different flavors (all geometrically and electrically compatible):
  - Preamplifier: two Charge Sensitive Amplifier (CSA), and one fast trans-impedance.
  - Discriminator: one with discrete time Offset Compensation (OC), one with a fine-tune DAC and one with a direct buffer (to be coupled with the fast preamplifier).
- Programmable power: 3.6 µW → 16.2 µW , nominal 10.8 µW per channel.
- Simulated jitter performance 35 ps → 15 ps, nominal 20 ps

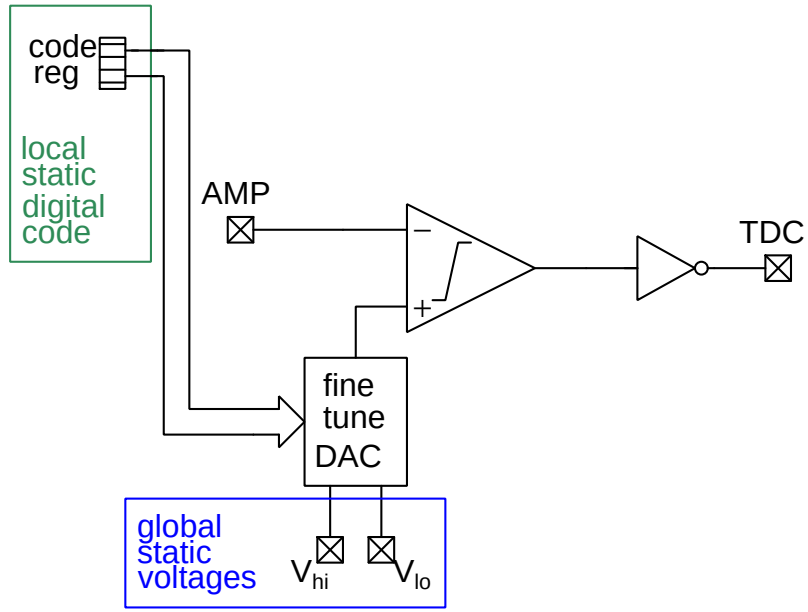
Discriminator: channel equalization



- The circuit autocorrect its offset while saving the desired baseline on a capacitor.

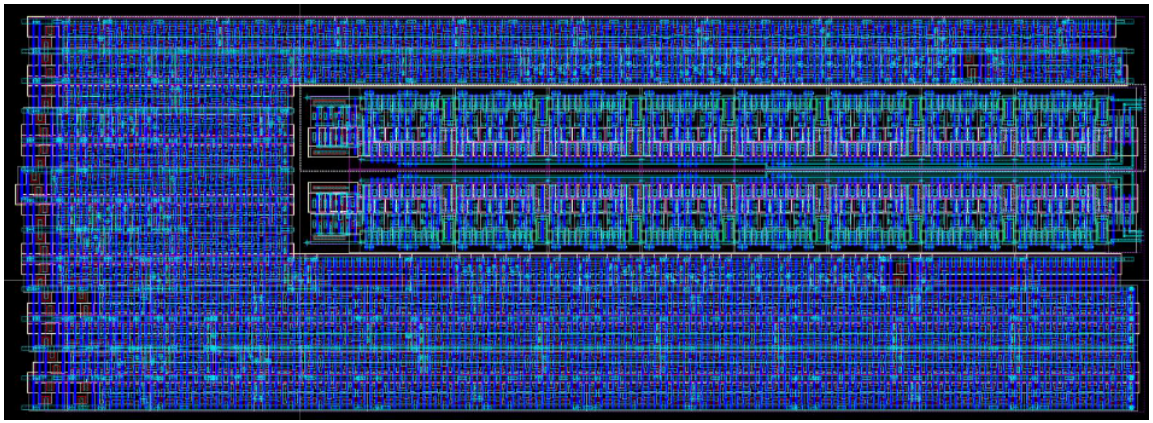
+ Requires two global voltages.
+ Works with local digital controls.
+ Self calibrating.

– The procedure must be strobed.
– Increases the jitter by a factor $\sqrt{2}$.
– The parassitcs of the capacitor loads the preamplifier.



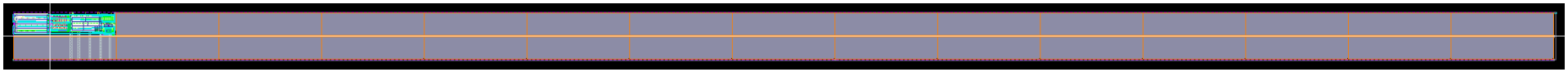
- The threshold is calibrated for each channel in order to compensate the offset.

+ Requires: two global voltages, local digital code.
– Requires registers to save the calibration.
– Requires a calibration procedure with error measurement.
+ The calibration i static.
+ No added component to the jitter.
+ No additional loading to the preamplifier.

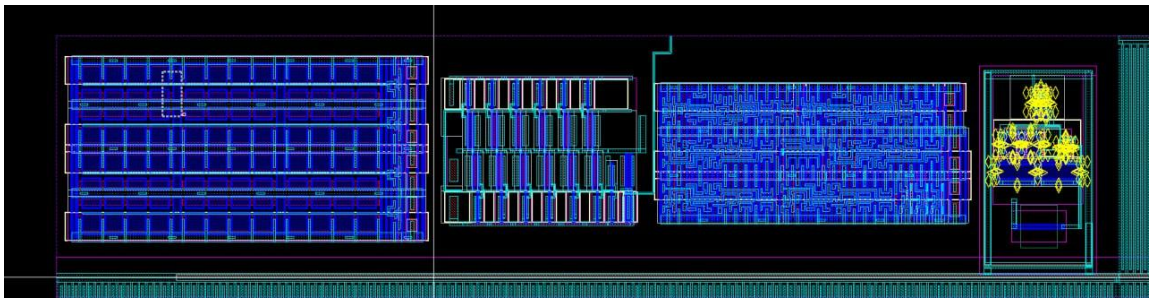


Layout of the TDC

- Area: 27.9 µm × 7.2 µm.
- Vernier based, custom designed DCOs for improved jitter performance and area utilization.
- Utilization of clock gating and high-voltage-threshold transistor to limit power when inactive.
- Power Consumption: static 1.25 µW, dynamic 2.2 µW at 300 kHz
- Time of Arrival (TA): LSB 30 ps, resolution 15 ps, max conversion time 35 ns.
- Time over Threshold (ToT): LSB 0.45 ns (resolution 0.13 ns) with double edge counting.



Layout of the PLL core + filter.



Layout of the PLL core.

- The PLL (Phased Locked Loop) has been designed in order to provide an internal reference clock with a static phase in respect to an external one.
- It can integrate the jitter on multiple edges of the input clock in order to produce a low-jitter reference.
- Based on a starved DCO $\rightarrow$ three starving schemes: static, DAC and external.
- Core area: $30\,\mu m \times 6\,\mu m \rightarrow$ with filter $433\,\mu m \times 15.6\,\mu m \rightarrow$ optimized for integration in the periphery.
- Lock frequency 40 MHz , power consumption 50 µW, jitter filtering from 14 ps (input) to 1.9 ps (output).

- The development of ASICs for the IGNITE project has begun.
- Pixel Electronics power consumption: 14 µW per channel $\rightarrow$ power density 0.875 $\frac{W}{cm^2}$ $\rightarrow$ inside the power-budget (service electronics contributions must also be added).
- Expected time resolution (from simulation):

$$\sigma_t = \sqrt{\sigma_{sens}^2 + \sigma_{afe}^2 + \sigma_{tdc}^2 + \sigma_{clk}^2}$$
$$= \sqrt{11^2 + 20^2 + 15^2 + 1.9^2} = 27.4ps$$

- Performance and operation of the single blocks will be evaluated in November in the IGNITE0 test chip.
- The first 64×64 matrix prototype, Fractalic64, will be submitted next year.