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Radiation-Hardened-by-Design FPGA-Based Systems for Operation in Neutron Radiation Environments

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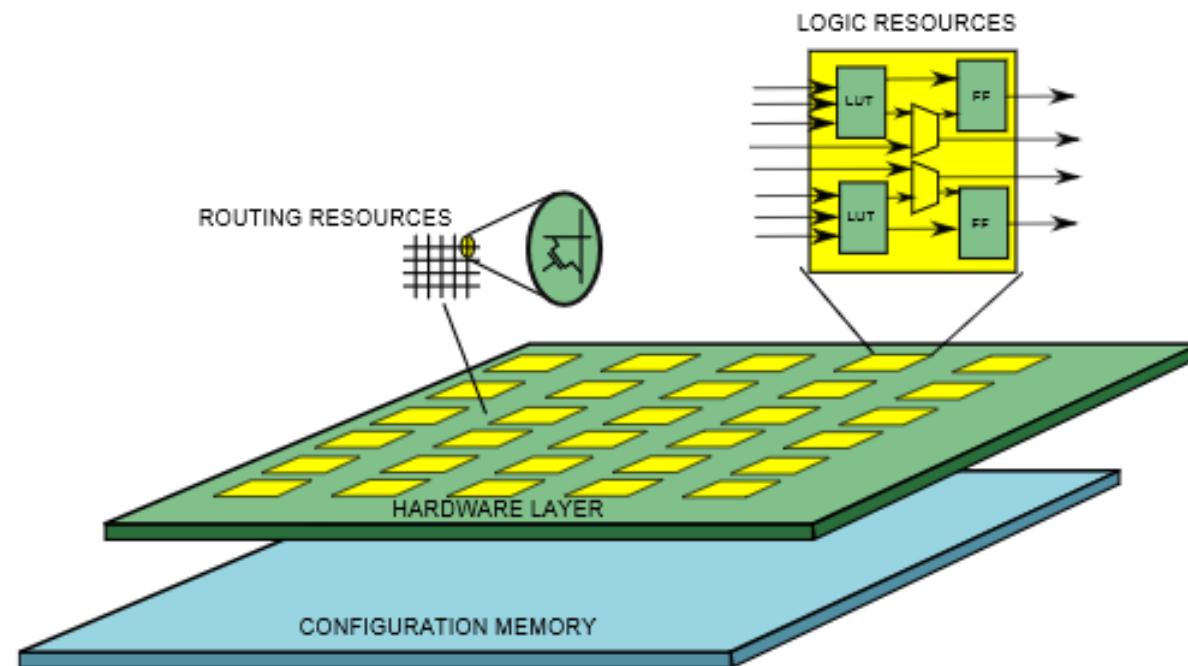
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FPGAs in Neutron Fields

- SRAM FPGAs offer large and flexible real-time processing resources
- Neutrons might generate single-event upsets (SEUs) via secondary ionization
- Upsets in the configuration RAM (CRAM) may break the implemented logic
- Reliability depends on architecture, configuration, and interfaces
- Specific example to showcase general RHBD techniques in FPGAs:
 - a design that measures its own SEUs to operate as a sensor



Configuration memory size
up to few 100 Mb

An FPGA as Sensor and Readout



- SRAMs used as hadron fluence sensors at LHC [1] and in proton therapy [2,3]
- Hadrons with energy > few MeV and thermal neutrons may indirectly induce SEUs in SRAMs

hadron fluence

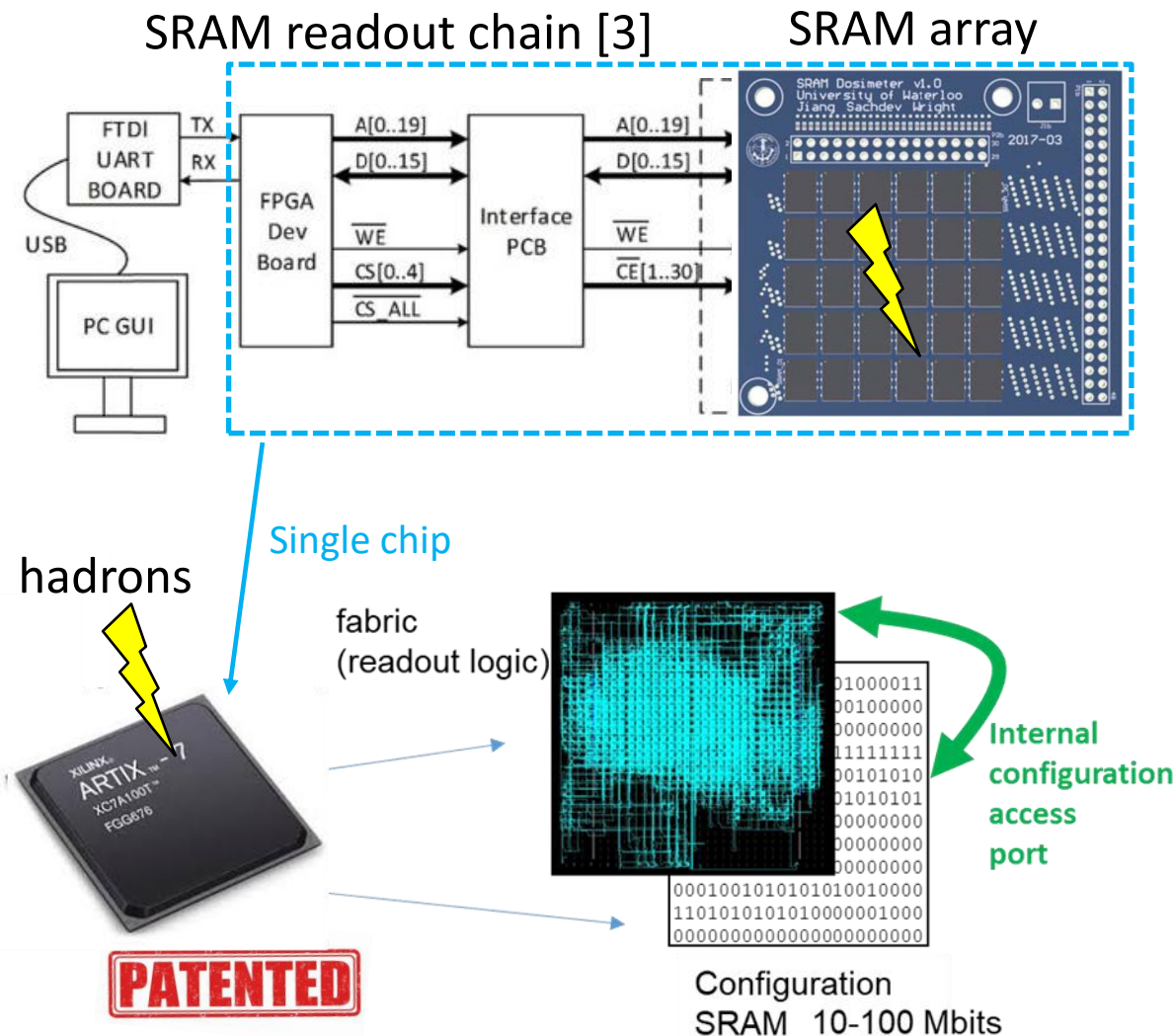
cross section per bit

$$\Phi = \frac{N_{upsets}}{\sigma_{bit} N_{bits}}$$

upset count

memory size

- $\sigma_{bit} = \sigma_{bit}(\text{device}, V_{DD}, \text{hadron}, E)$
- Classic solutions: SRAM + readout device
- **Own work** [4,5]: sensor embedded in a SRAM-based FPGA
 - CRAM as sensitive element + fabric programmed as readout



[1] doi: 10.1109/TNS.2014.2365042

[4] doi: 10.1109/TNS.2023.3265740

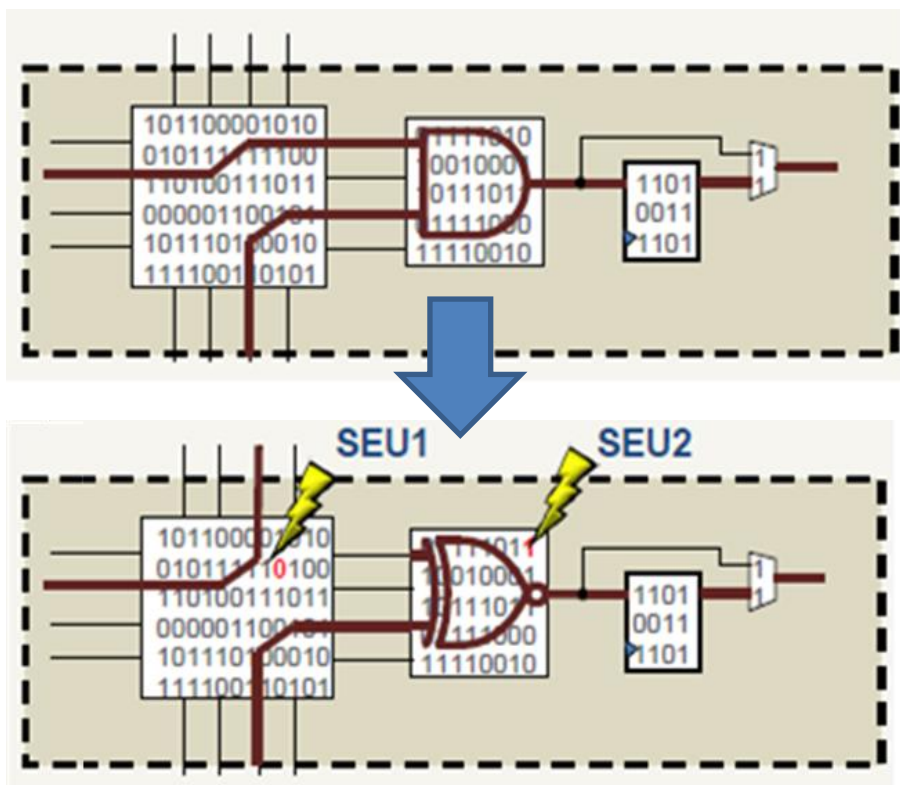
[2] doi: 10.1016/j.radmeas.2019.01.001

[5] tinyurl.com/yxcymnd7

[3] doi: 10.1109/TNS.2018.2884148

Upsets Vs Configuration

- Challenge: upsets (*what we want to measure*) may disrupt the readout logic (*our transducer*)



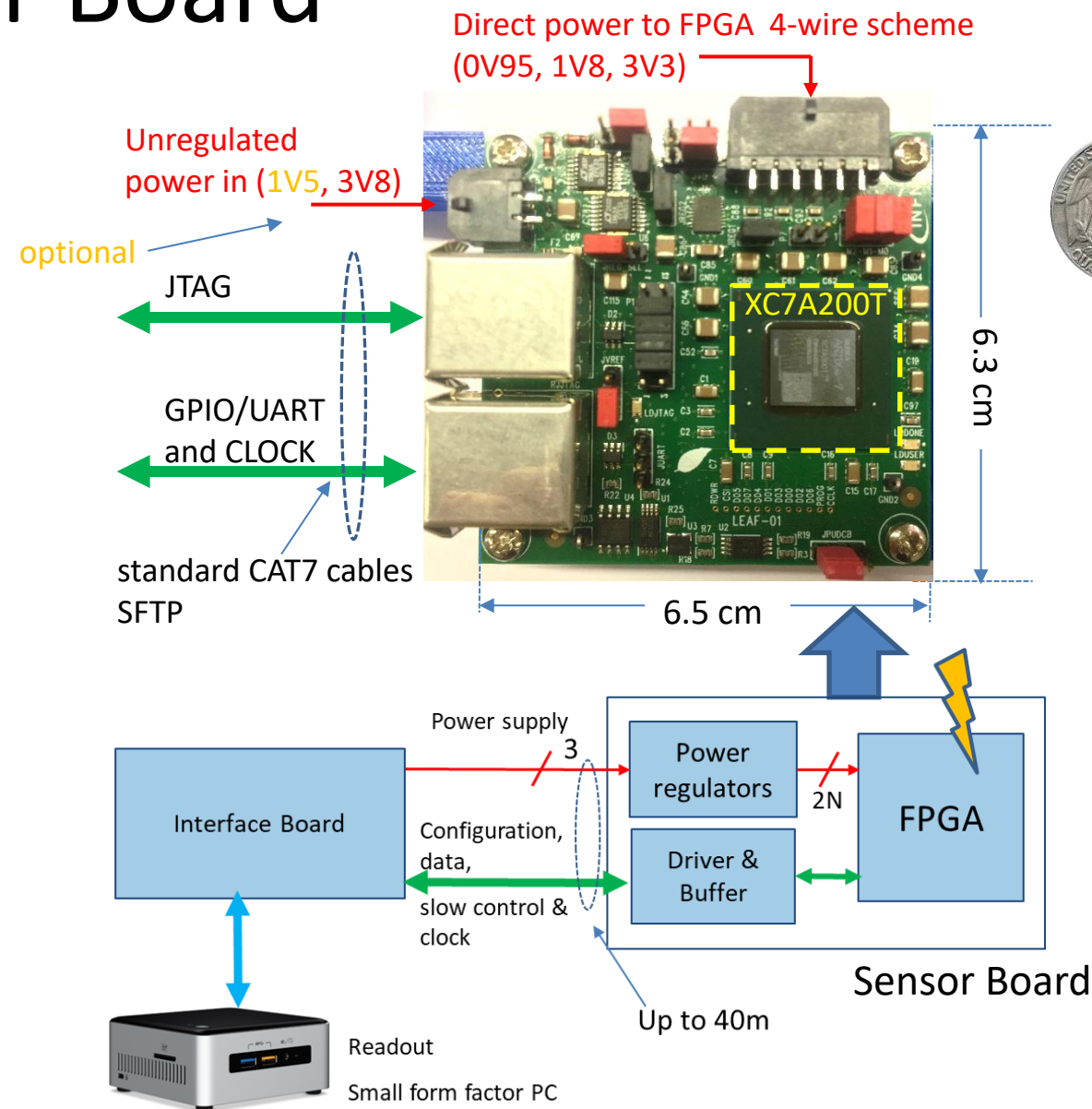
- Readout logic main features
 - detect and correct upsets in CRAM => self-correct functionality
 - self-contained (no external memories for reference bitstream)
 - provide details about upsets (timestamp, memory address, bit offset, polarity)
- Radiation Hardening By Design

Radiation Hardening By Design

- Key idea: minimize single point of failures
- Hardening Levels
 - Logic: triple modular redundancy and majority voting
 - Configuration: redundant frames and access ports (JTAG/ICAP)
 - Implementation: placement and routing directives
 - Printed circuit board: redundant tracks and alternative clock sources

Sensor Board

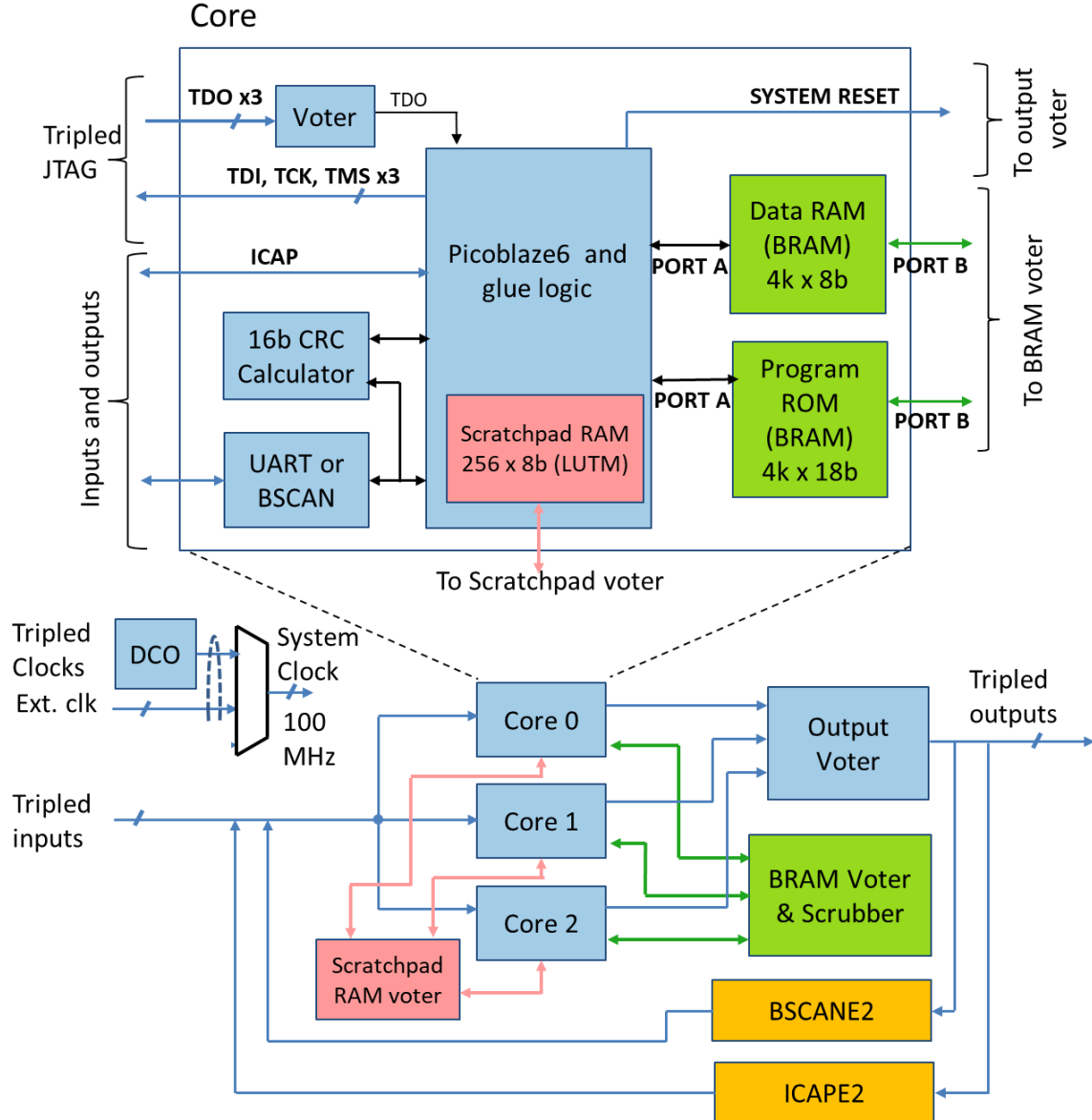
- Compact PCB
 - Only COTS components, radiation tolerance studies in [1,2]
 - Low power consumption (~ 0.7 W)
- AMD Artix-7 FPGA (200T)
 - 28 nm CMOS
 - 59 Mb CRAM + 18 Mb BRAM
 - Sensitive to fast hadrons (protons/neutrons) and thermal neutrons



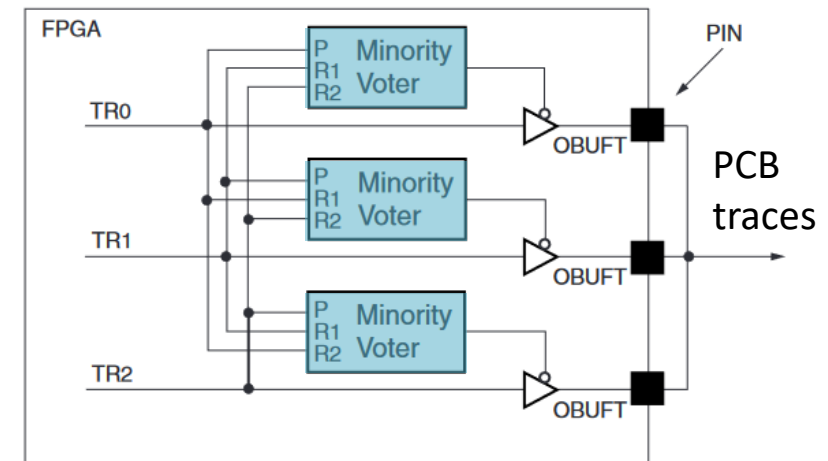
[1] T. Higuchi et al., 2012, doi: 10.1088/1748-0221/7/02/C02022

[2] Y. Yu Nakazawa et al., 2020, doi: 10.1016/j.nima.2019.163247

Redundant Readout Logic



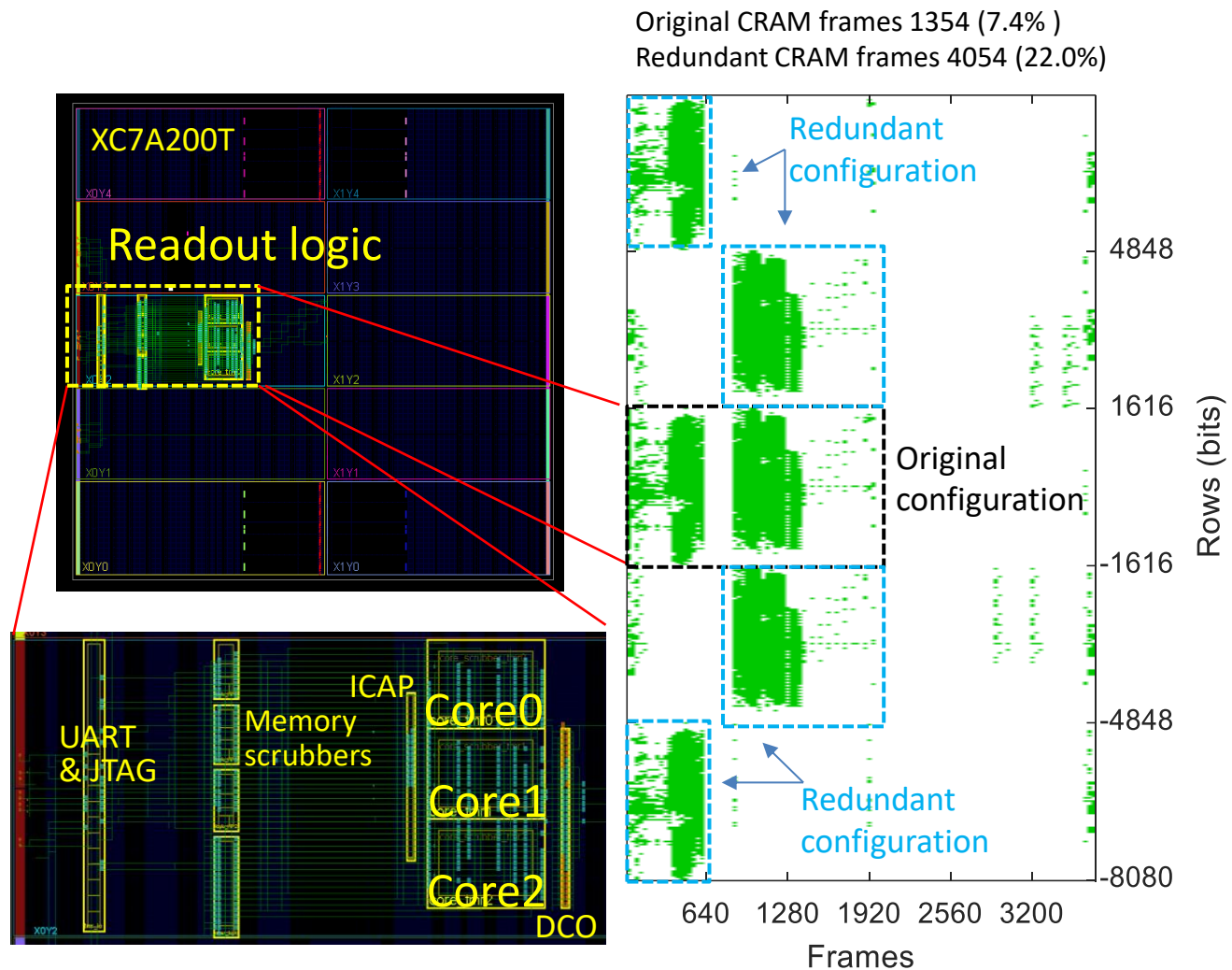
- Triple modular redundancy, triple IOs
- Two configuration access ports: on-the-fly switch between ICAP and JTAG
- Dual clock source



Redundant Layout and Configuration

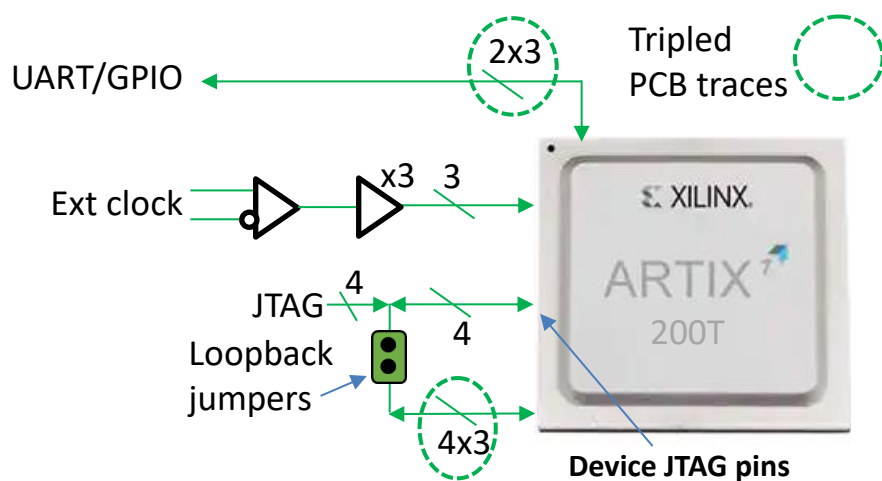
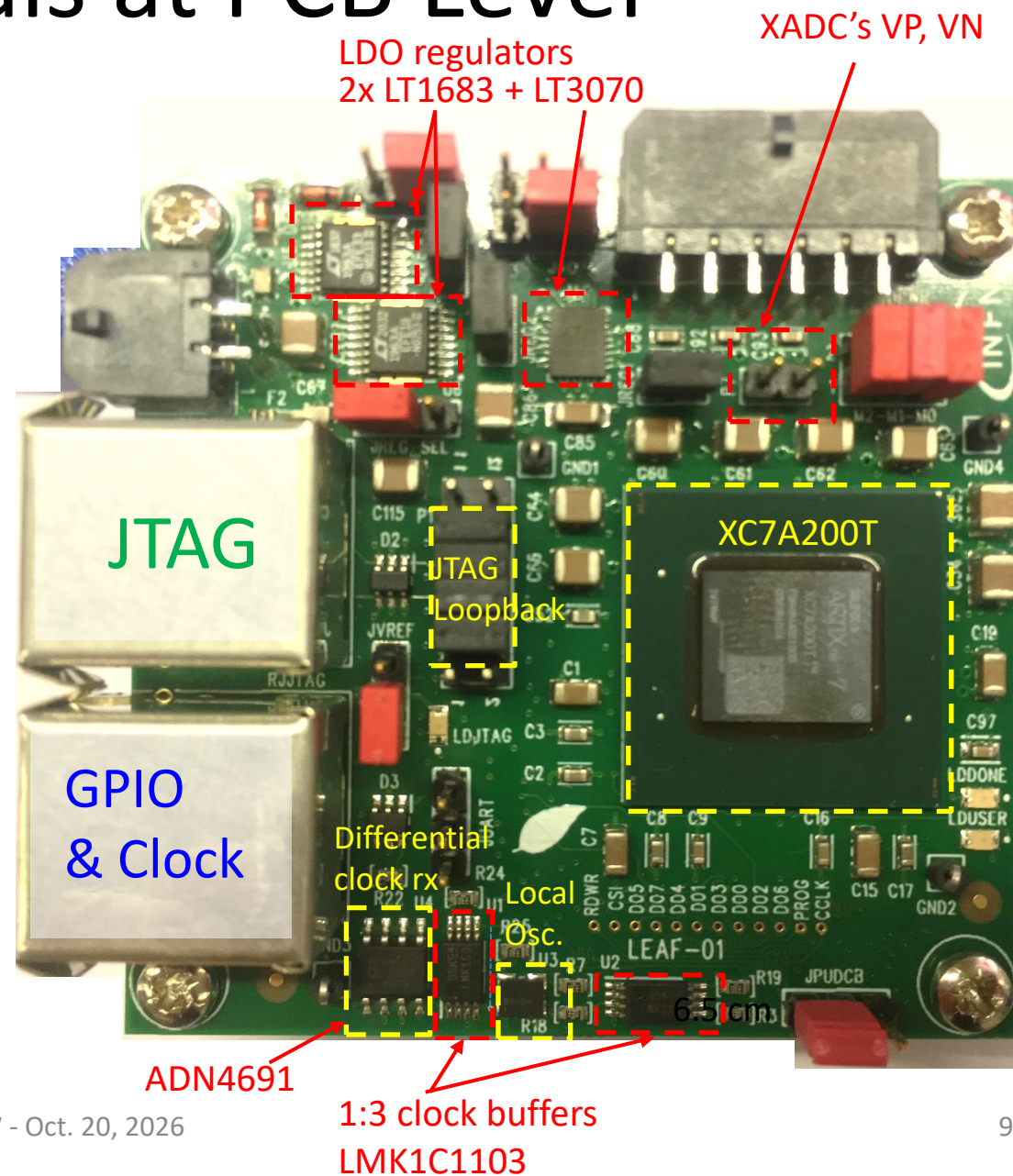
- Redundant modules placed and routed in distinct areas “pblocks”
- Two redundant copies of each original configuration frame
- Readout logic enforces consistency among original and redundant frames (majority voting)
- Full CRAM scan time: 1.5s

Logic Resources	Used	Available	%
Slices: FFs	1813	267600	0.7
Slices: LUTs	2174	133800	1.6
Slices: overall	823	33450	2.5
BRAM 36k	9	365	2.5
BUFG	4	32	12.5
BSCAN	1	4	25.0
ICAP	1	2	50.0



Redundant Signals at PCB Level

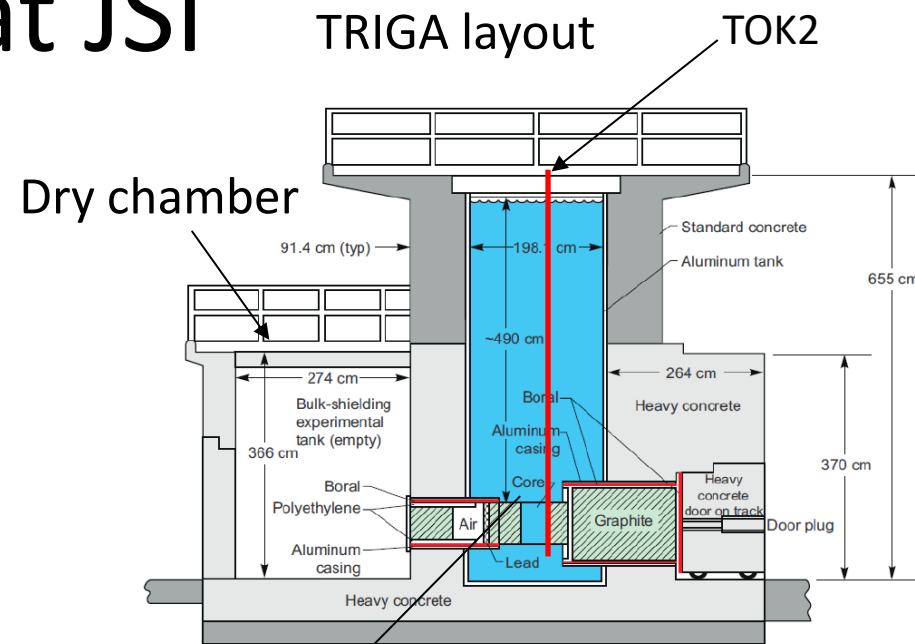
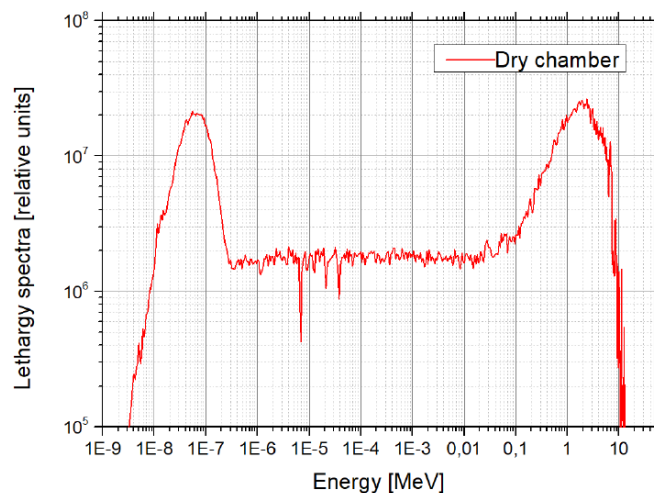
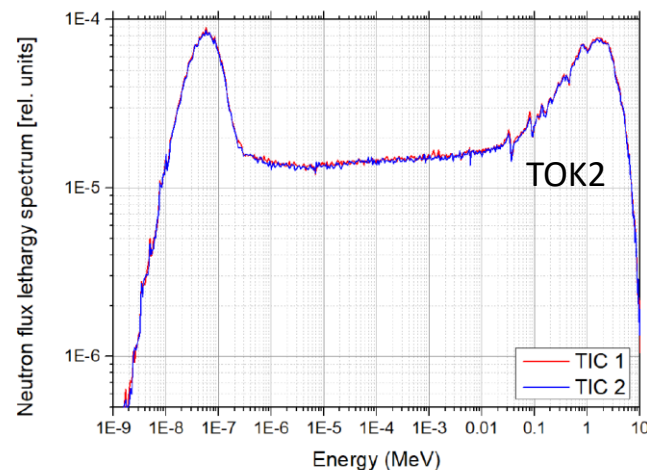
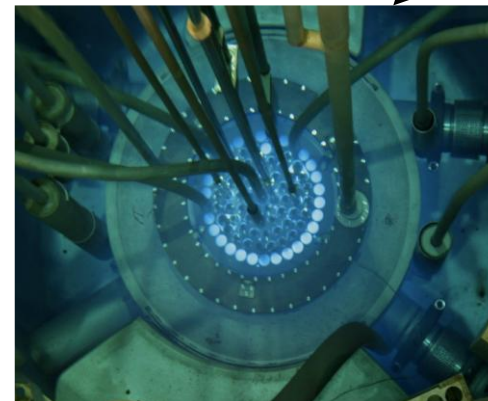
- Tripled traces for all signals
 - clock, UART, GPIO, SelectMAP
- JTAG self-scrubbing (loopback)



[1] R. Giordano *et al.*, Dec. 2015, doi: 10.1109/TNS.2015.2497539

TRIGA Reactor at JSI

- Irradiation tests at the TRIGA reactor of Jožef Stefan Institute (Ljubljana, Slovenia)
 - MARK II 250 kW water-cooled, research reactor from General Atomics
- Dry chamber (large samples, 60cm x 60cm)
 - flux @ full power $8.3 \cdot 10^7$ thermal $n \cdot cm^{-2} \cdot s^{-1}$ (1.7 fast n)
 - Fission plate to harden spectrum (fast n $9.5 \cdot 10^7 cm^{-2} \cdot s^{-1}$)
- TOK2 triangular channel (small samples, 5cm diam.)
 - flux @ full power $3.5 \cdot 10^{12} n_{eq} \cdot cm^{-2} \cdot s^{-1}$

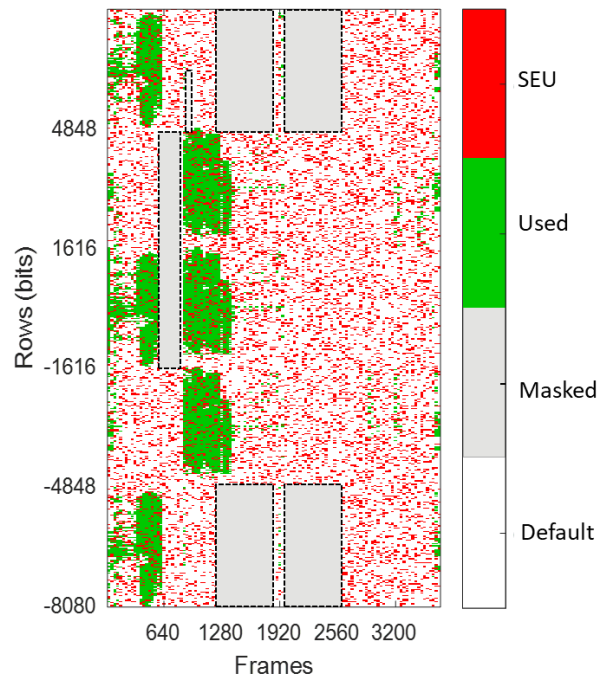


Dry Chamber Test: Readout Logic

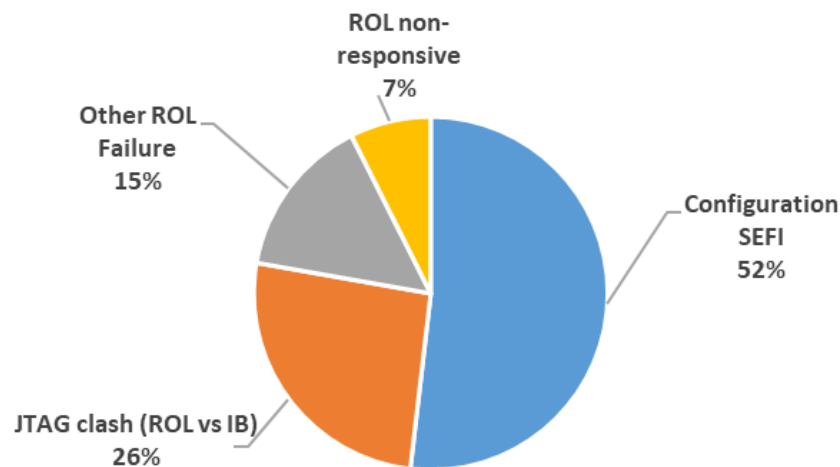
	Parameter	Without fission plate	With fission plate	Overall
Test conditions	Time (s)	$3.20 \cdot 10^4$	$3.04 \cdot 10^4$	$6.24 \cdot 10^5$
	Number of runs	16	22	38
	Thermal $n \phi$ (cm^{-2})	$2.8 \cdot 10^{12}$	$2.4 \cdot 10^{12}$	$5.3 \cdot 10^{12}$
CRAM Upsets	Average SEU Rate (Hz)	6.04	5.78	-
	Total N_{upsets}	$2.0 \cdot 10^5$	$1.7 \cdot 10^5$	$3.7 \cdot 10^5$
	σN_{bits} (cm^{-2})	$6.9 \cdot 10^{-8}$	$7.0 \cdot 10^{-8}$	$6.9 \cdot 10^{-8}$
ROL Failures	N_{fail}			27
	σ_{fail} (cm^{-2})			$5.1 \cdot 10^{-12}$
	Fluence between failures (cm^{-2})			$2.0 \cdot 10^{11}$
	Upsets between failures			$1.4 \cdot 10^4$

- Readout failure cross section
 - $5.1 \cdot 10^{-12} \text{ cm}^2$
- Average detected upsets between failures
 - $1.4 \cdot 10^4$
- Readout failures recovered by power cycling and reconfiguration
- SEUs mainly follow thermal-neutron fluence

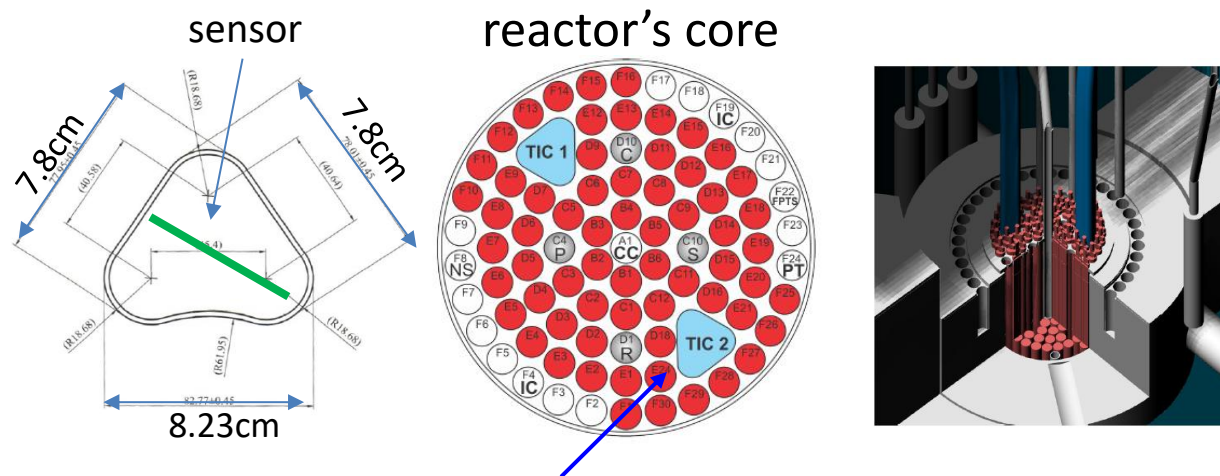
Configuration view



Readout Logic Failure Modes

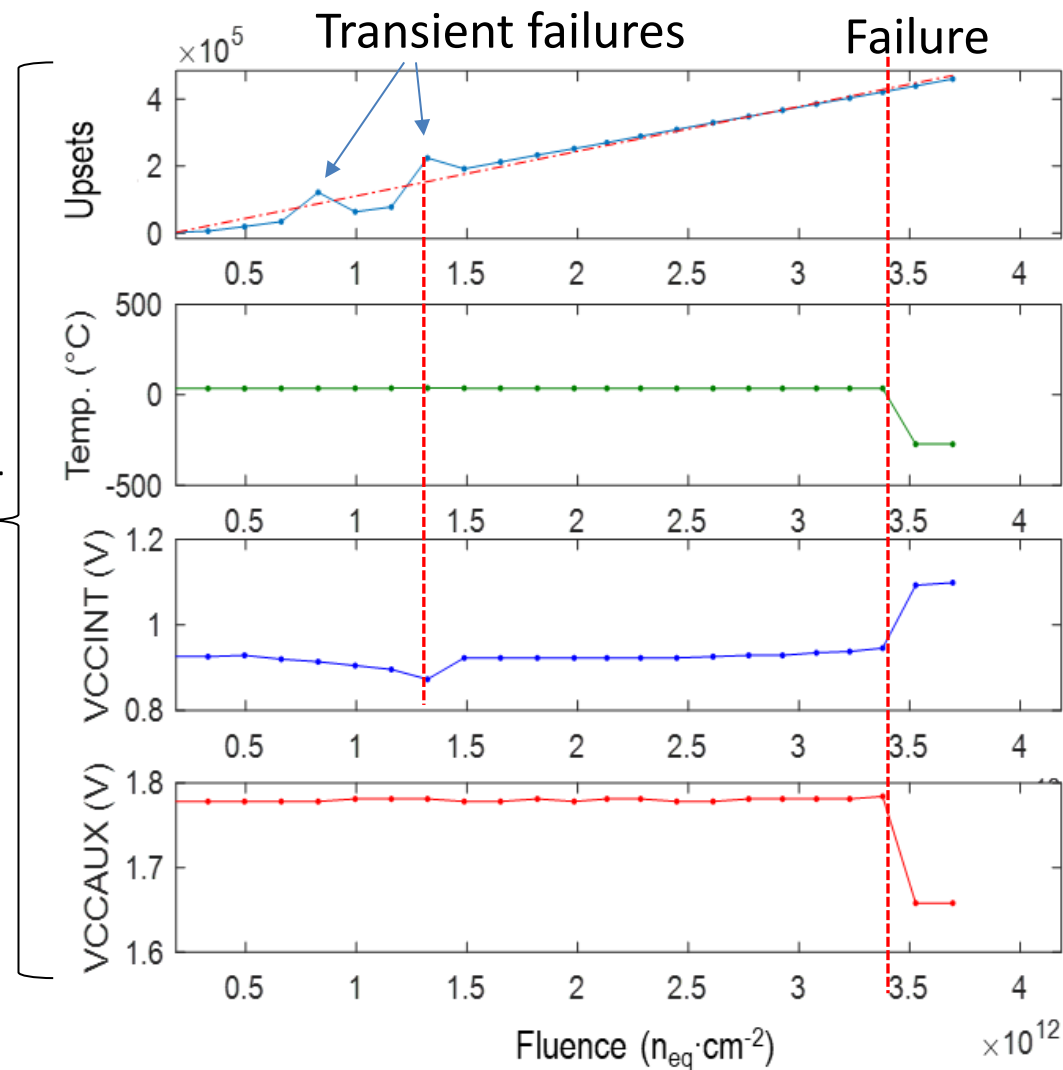


High-Flux Test



- TOK2 channel
 - Flux: $6.6 \cdot 10^9 \text{ n}_{\text{eq}} \text{ cm}^{-2} \text{ s}^{-1}$
 - Readout logic disabled, readback via JTAG
- Persistent temperature and voltage read failure at $3.4 \cdot 10^{12} \text{ n}_{\text{eq}} \text{ cm}^{-2}$
 - Tracked down to voltage regulator failure
- Recovery after months of room-temperature annealing

iMPACT
- XADC

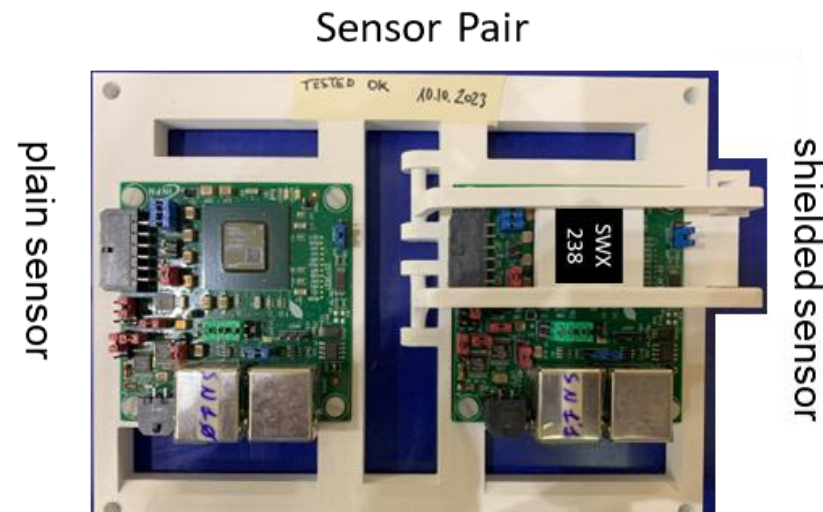


Fast Vs Thermal Neutron Discrimination

Idea



- Sensor Pair:
 - Plain and shielded against thermal neutrons
 - Difference in counts estimates thermal contribution to SEUs



shieldwerx™

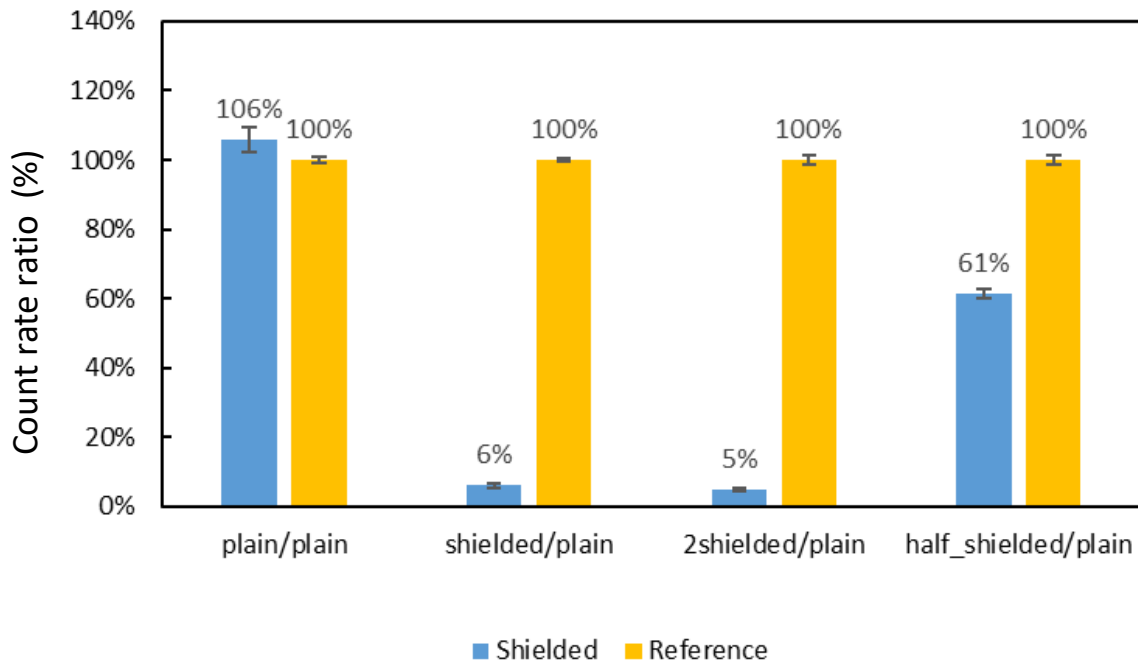


- SWX-238 polymer as thermal neutron shield
 - 27.6% boron in weight
 - 1-layer 1/8" thickness (3.2 mm)
 - Shields 99.75% thermal neutrons
 - Minimal thermalization of fast neutrons

- Simplifying assumptions
 - Same flux on sensors of a pair
 - Plain senses only neutrons (thermal and «fast», i.e., non-thermal)
 - $N_0 = \Phi_t \sigma_t + \Phi_f \sigma_f$
 - Shielded senses fast neutrons only
 - $N_1 = \Phi_f \sigma_f$

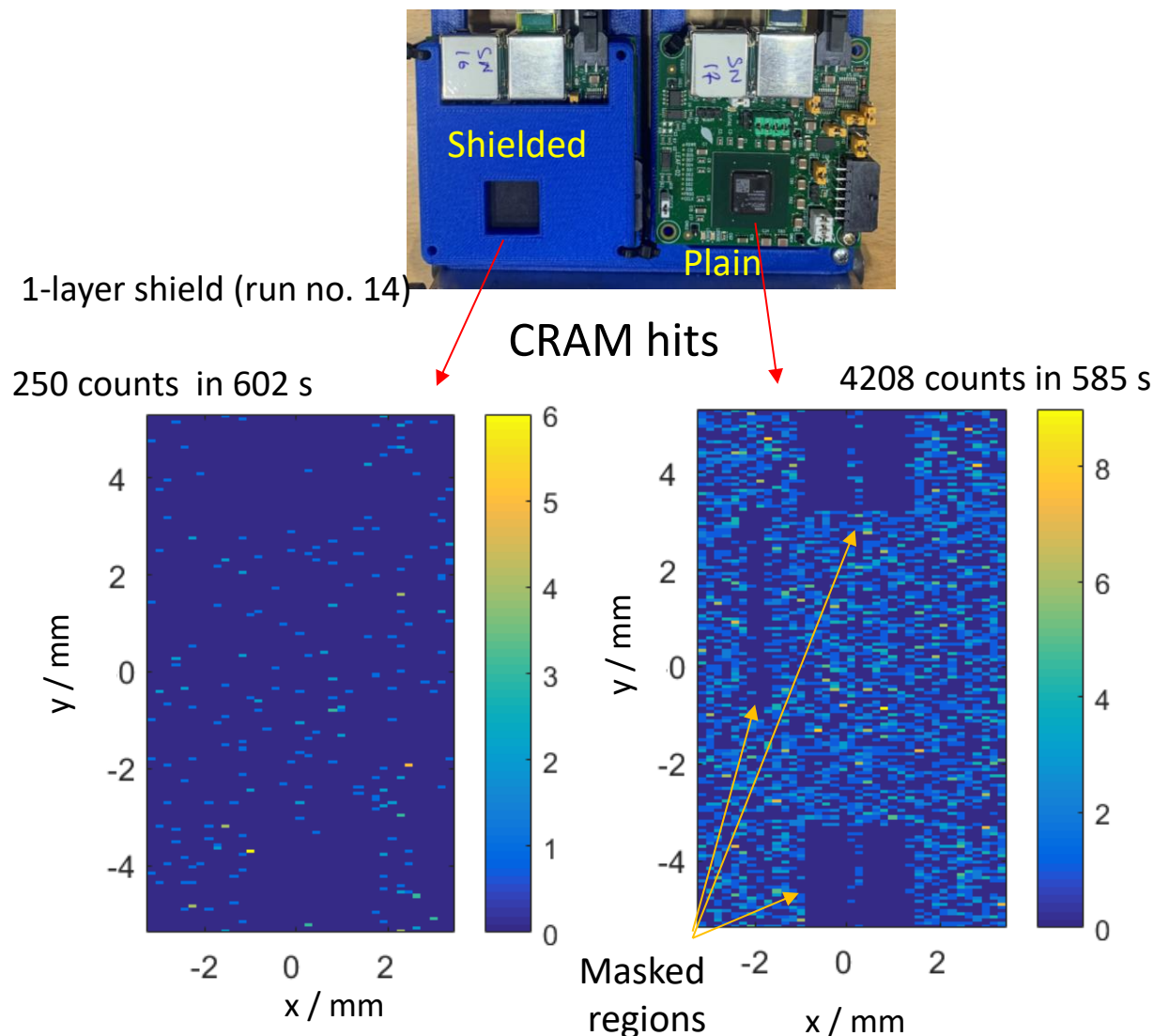
Shielding Effect

Count rate comparison

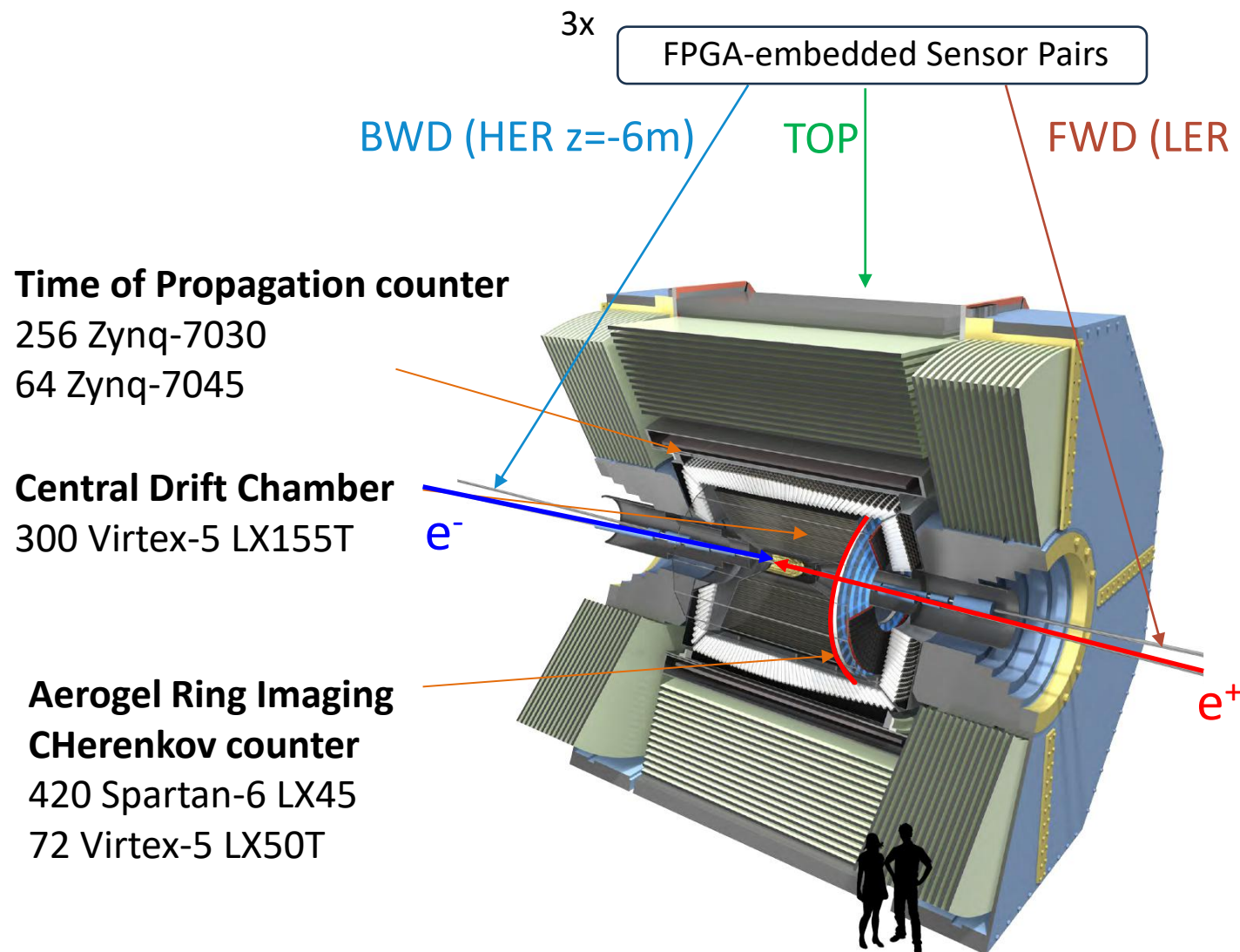


- Tests in TRIGA's dry chamber
- One layer of shield reduces count rate to nearly 6%
- CRAM hit map shows counts in logic pixels [1]
 - 1 pixel = 100 x 100 CRAM cells

[1] doi: 10.1088/1748-0221/19/06/P06043 (more on CRAM-based imaging)

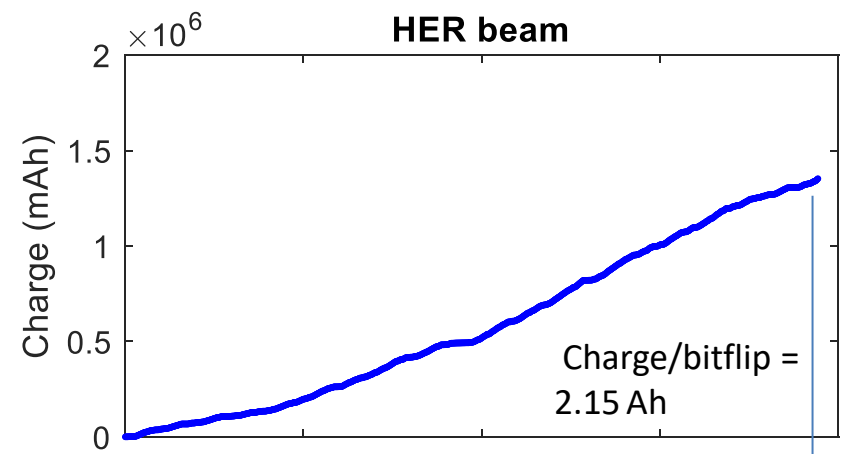
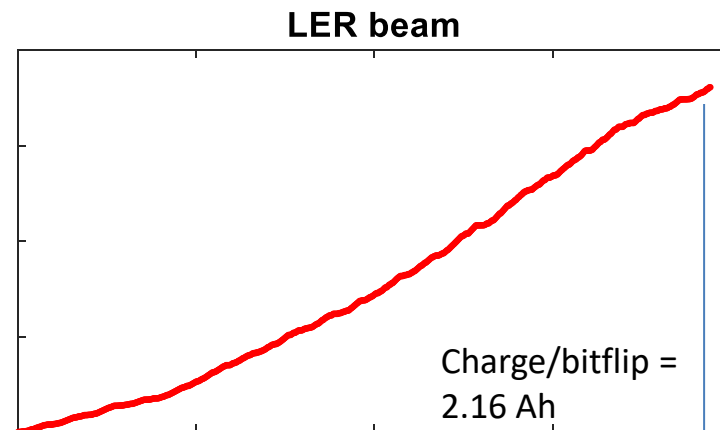
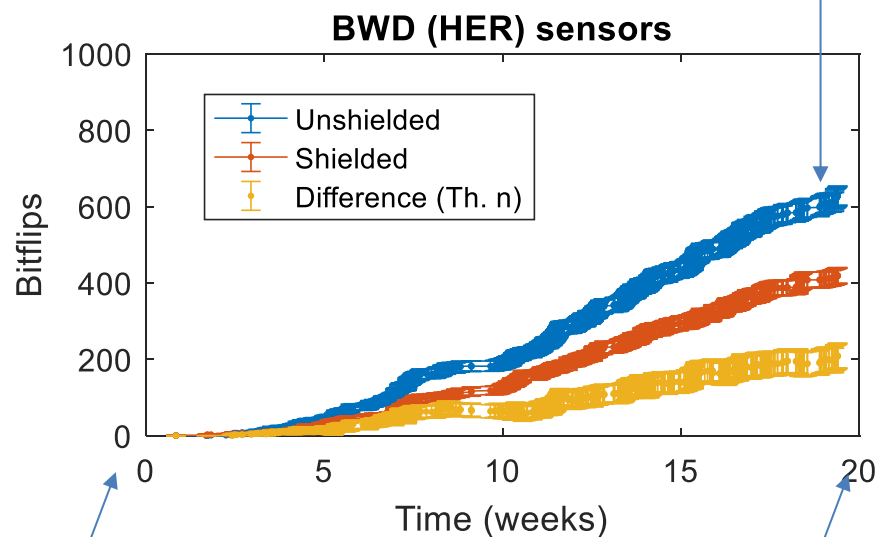
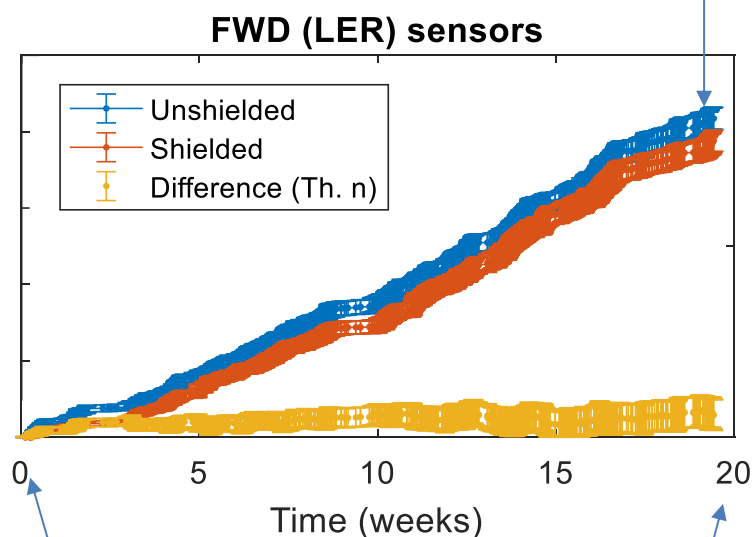


Deployment in Belle II



- Belle II detector @ SuperKEKB e^+e^- collider (Tsukuba, Japan)
- Overall 1100+ SRAM-based FPGAs used on detector
- Beam backgrounds indirectly generate neutrons, which can disrupt data acquisition [1]
- FPGA-embedded sensors monitor neutron-induced upsets

SEU Measurements at Belle II



- Measurements from first half of 2024
- Correlation with integrated beam currents
 - $\rho > 99.57\%$ (correlation coefficient)
- Sensors at different locations show
 - Different trends
 - Different thermal and non-thermal contributions

Feb. 15, 2024

Jun. 30, 2024

Feb. 15, 2024

Jun. 30, 2024

Summary

- RHBD spans logic, physical layout and PCB design
 - Demonstrated concepts can be exported to other applications in neutron fields
 - Application-specific qualification for spectrum, flux and total fluence is required
 - The weaker component limits the complete system
- FPGA's sensitivity to thermal neutrons can be reduced by
 - Shielding with Boron-rich polymers (what we do in Belle II)
 - Switching to other families fabricated with ^{10}B -purified processes